双通道、限流、配电开关

查询样品: TPS2052C, TPS2062C, TPS2062C-2, TPS2066C, TPS2066C-2, TPS2060C, TPS2064C, TPS2064C-2, TPS2002C, TPS2003C

特性

- 双电源开关系列
- **0.5A，1A，1.5A，2A** 的额定电流
- 准确度为 **±20%** 的电流限值容限
- 快速过流响应 **- 2μs**（典型值）
- **70mΩ**（典型值）高侧 **N** 通道金属氧化物半导体场效应晶体管 **(MOSFET)**
- 工作电压范围：**4.5V** 至 **5.5V**
- 去尖峰脉冲故障报告 **(FLTx)**
- 所选的具有 **(TPS20xxC)** 和不具有 **(TPS20xxC-2)** 输出放电的部件
- 反向电流阻断
- 内置软启动
- 与现有的***TI*** *开关系列产品引脚到引脚相对应*
- 环境温度范围：**-40°C** 至 **85°C**

应用范围

- **USB** 端口**/**集线器、笔记本、台式机
- 高清数字电视
- 机顶盒
- 短路保护功能

说明

TPS20xxC 和 TPS20xxC-2 双配电开关系列产品用于诸如 USB 等有可能遇到高电容负载和短路的应用。 这一系列产品为电流介于 0.5A 和 2A 之间的应用提供具有固定电流限值阀值的多种器件。

当输出负载超过电流限值阀值时，TPS20xxC 和 TPS20xxC-2 通过运行在恒定电流模式下来将输出电流限制在安全的水平上。 这就在所有条件下提供了一个可预计的故障电流。 当输出被短接时，快速过载响应时间减轻了主 5V 电源提供稳压电源的负担。 为了大大减少打开和关闭期间的电流冲击，电源开关的上升和下降次数受到控制。

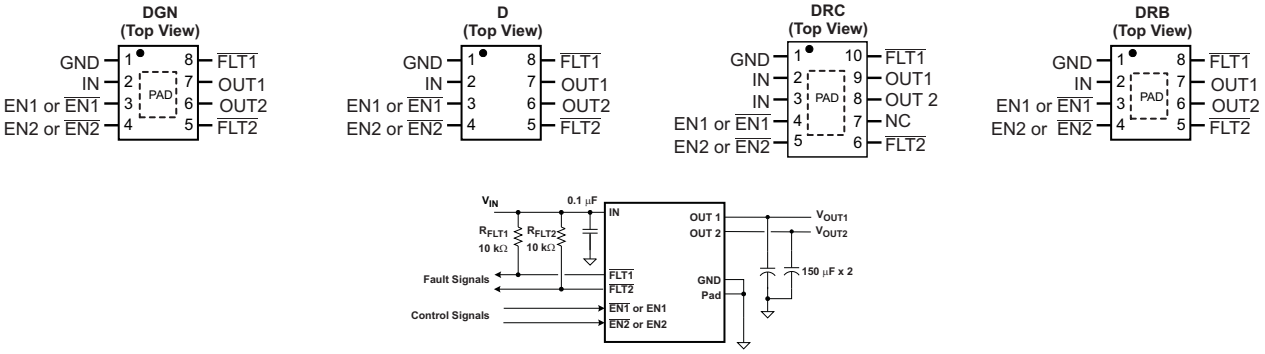

Figure 1. TYPICAL APPLICATION

Table 1. Devices

RATED CURRENT	DEVICES	STATUS			
		MSOP-8 (PowerPad™)	SON -10	SOIC-8	SON-8
0.5 A	TPS2052C	Active	—	—	—
1 A	TPS2062C and 66C	Active and Active	—	Active and Active	—
1 A	TPS2062C-2 and 66C-2	— and Active	—	—	Active and —
1.5 A	TPS2060C and 64C	Active and Active	—	—	—
1.5 A	TPS2064C-2	Active	—	—	—
2 A	TPS2002C and 03C	—	Active and Active	—	—

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEVICE INFORMATION(1)(2)

MAXIMUM OPERATING CURRENT	ENABLE	OUTPUT DISCHARGE	BASE PART NUMBER	PACKAGE DEVICES and MARKING(3)			
				SOIC-8 (D)	MSOP-8 (DGN) PowerPAD™	SON-10 (DRC)	SON-8 (DRB)
0.5	High	Y	TPS2052C	–	PYNI	–	–
1	Low	Y	TPS2062C	2062C	VRBQ	–	–
1	Low	N	TPS2062C-2	–	–	–	PYVI
1	High	Y	TPS2066C	2066C	VRDQ	–	–
1	High	N	TPS2066C-2	–	PYUI	–	–
1.5	Low	Y	TPS2060C	–	VRAQ	–	–
1.5	High	Y	TPS2064C	–	VRCQ	–	–
1.5	High	N	TPS2064C-2	–	PYTI	–	–
2	Low	Y	TPS2002C	–	–	VREQ	–
2	High	Y	TPS2003C	–	–	VRFQ	–

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package code for MSOP-8 is “DGN” and for SON is “DRC”.
(3) “–” indicates the device is not available in this package.

ABSOLUTE MAXIMUM RATINGS(1)(2)

		VALUE		UNIT
		MIN	MAX	
Voltage range on IN, OUTx, ENx or $\overline{ENx}$, $\overline{FLTx}$(3)		–0.3	6	V
Voltage range from IN to OUT		–6	6	V
Maximum junction temperature, T_J		Internally Limited		°C
ESD	Human Body Model		2	kV
	Charged Device Model		500	V
	IEC 61000-4-2, Contact / Air(4)		8 / 15	kV

(1) Absolute maximum ratings apply over recommended junction temperature range.
(2) All voltages are with respect to GND unless otherwise noted.
(3) See INPUT AND OUTPUT CAPACITANCE section.
(4) V_{OUT} was surged on a PCB with input and output bypassing per Figure 1 (except input capacitor was 22 µF) with no device failure.

THERMAL INFORMATION

THERMAL METRIC(1)(2)		D	DGN	DRC	DRB	UNITS
		8 PINS	8 PINS	10 PINS	8-PINS	
θ_{JA}	Junction-to-ambient thermal resistance	129.9	57.2	45.4	50.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	83.5	110.5	58	60.3	
θ_{JB}	Junction-to-board thermal resistance	70.4	60.7	21.1	26.3	
ψ_{JT}	Junction-to-top characterization parameter	36.6	7.8	1.9	2.1	
ψ_{JB}	Junction-to-board characterization parameter	66.9	24	21.3	26.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	14.3	9.1	9.8	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。
(2) 有关该器件的基于印刷电路板 (PCB) 覆铜区的热评估信息， 请参阅TI PCB 热应力 计算。

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RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage, IN		4.5		5.5	V
V_{Enable}	Input voltage, ENx or $\overline{ENx}$		0		5.5	V
I_{OUTx}	Continuous ouput current, OUTx	TPS2052C			0.5	A
		TPS2062C, 62C-2, 66C, and 66C-2			1	A
		TPS2060C, 64Cand 64C-2			1.5	A
		TPS2002C and 03C			2	A
T_J	Operating junction temperature		–40		125	°C
$I_{\overline{FLTx}}$	Sink current into $\overline{FLTx}$		0		5	mA

ELECTRICAL CHARACTERISTICS(1)

$T_J = T_A = 25°C$, $V_{IN} = 5$ V, $V_{ENx} = V_{IN}$ or $V_{\overline{ENx}} = 0$V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	On-resistance	TPS2052C (0.5 A)	DGN		70	84	mΩ
		TPS2052C (0.5 A) $–40°C \le (T_J, T_A) \le 85°C$	DGN		70	95	mΩ
		TPS2062C, 66C, and 66C-2 (1 A)	DGN		70	84	mΩ
		TPS2062C, 66C, and 66C-2 (1 A), $–40°C \le (T_J, T_A) \le 85°C$	DGN		70	95	mΩ
		TPS2062C and 66C (1 A)	D		90	108	mΩ
		TPS2062C and 66C (1 A), $–40°C \le (T_J, T_A) \le 85°C$	D		90	122	mΩ
		TPS2062C-2 (1 A)	DRB		73	87	mΩ
		TPS2062C-2 (1 A) $–40°C \le (T_J, T_A) \le 85°C$	DRB		73	101	mΩ
		TPS2060C, 64C, and 64C-2 (1.5 A)			70	84	mΩ
		TPS2060C, 64C, and 64C-2 (1.5 A), $–40°C \le (T_J, T_A) \le 85°C$			70	95	mΩ
		TPS2002C and 03C (2 A)			70	84	mΩ
		TPS2002C and 03C (2 A), $–40°C \le (T_J, T_A) \le 85°C$			70	95	mΩ
CURRENT LIMIT							
I_{OS}	Current limit, See Figure 7	TPS2052C (0.5 A)		0.75	1	1.25	A
		TPS2062C, 62C-2, 66C, and 66C-2 (1 A)		1.28	1.61	1.94	A
		TPS2060C, 64C, and 64C-2 (1.5 A)		1.83	2.29	2.75	A
		TPS2002C and 03C (2 A)		2.55	3.15	3.77	A
t_{IOS}	Short-circuit response time	V_{IN} = 5 V (see Figure 6), One-half full load → $R_{(SHORT)}$ = 50 mΩ, Measure from application to when current falls below 120% of final value			2		µs
SUPPLY CURRENT							
I_{SD}	Supply current, device disabled	$I_{(OUTx)}$ = 0 mA			0.01	1	µA
I_{S1E}	Supply current, single switch enabled	$I_{(OUTx)}$ = 0 mA			60	75	µA
I_{S2E}	Supply current, both switches enabled	$I_{(OUTx)}$ = 0 mA			100	120	µA
I_{LKG}	Leakage current	V_{OUT} = 0 V, V_{IN} = 5.5 V, disabled, measured I_{VIN}	TPS20xxC-2		0.05	1	µA
	Reverse leakage current	V_{OUT} = 5.5 V, V_{IN} = 0 V, measured I_{OUTx}			0.15	1	µA
OUTPUT DISCHARGE							
R_{PD}	Output pull-down resistance(2)	$V_{IN} = V_{(OUTx)}$ = 5 V, disabled	TPS20xxC	400	470	600	Ω

(1) Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature
(2) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

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ELECTRICAL CHARACTERISTICS

–40°C ≤ (T_J = T_A) ≤ 125°C, 4.5 V ≤ V_{IN} ≤ 5.5 V, V_{ENx} = V_{IN} or $V_{\overline{ENx}}$ = 0 V, I_{OUTx} = 0 A, typical values are at 5 V and 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	On-resistance	TPS2052C (0.5 A)	DGN		70	112	mΩ
		TPS2062C, 66C, and 66C-2 (1 A)	DGN		70	112	
		TPS2062C and 66C (1 A)	D		90	135	
		TPS2062C-2 (1 A)	DRB		73	115	
		TPS2060C, 64C, and 64C-2 (1.5 A)	DGN		70	112	
		TPS2002C and 03C (2 A)	DRC		70	112	
ENABLE INPUT (ENx or $\overline{ENx}$)							
V_{IH}	ENx ($\overline{ENx}$), High-level input voltage	4.5 V ≤ VIN ≤ 5.5 V		2			V
V_{IL}	ENx ($\overline{ENx}$), Low-level input Voltage					0.8	
	Hysteresis	V_{IN} = 5 V			0.14		
	Leakage current	V_{ENx} = 5.5 V or 0 V, $V_{\overline{ENx}}$ = 0 V or 5.5 V		-1	0	1	µA
t_{on}	Turn-on time (2)	V_{IN} = 5 V, C_L = 1 µF, R_L = 100 Ω, ENx ↑ or $\overline{ENx}$ ↓, See Figure 4, Figure 5, and Figure 2					ms
		1 A, 1.5 A, 2 A Rated		1.4	1.9	2.4	
t_{off}	Turn-off time (2)	V_{IN} = 5 V, C_L = 1 µF, R_L = 100 Ω, ENx ↑ or $\overline{EN}$ ↓, See Figure 4, Figure 5, and Figure 2					ms
		1 A, 1.5 A, 2 A Rated		1.95	2.60	3.25	
t_r	Rise time, output (2)	C_L = 1 µF, R_L = 100 Ω, see Figure 3					ms
		1 A, 1.5 A, 2 A Rated		0.58	0.82	1.15	
t_f	Fall time, output (2)	C_L = 1 µF, R_L = 100 Ω, see Figure 3					ms
		1 A, 1.5 A, 2 A Rated		0.33	0.47	0.66	
CURRENT LIMIT							
I_{OS}	Current-limit, See Figure 7	TPS2052C (0.5A)		0.7	1	1.3	A
		TPS2062C, 62C-2, 66C, and 66C-2 (1 A)		1.12	1.61	2.10	
		TPS2060C, 64C, and 64C-2 (1.5 A)		1.72	2.29	2.86	
		TPS2002C and 03C (2 A)		2.35	3.15	3.95	
t_{IOS}	Short-circuit response time	V_{IN} = 5 V (see Figure 6), One-half full load → $R_{(SHORT)}$ = 50 mΩ, measure from application to when current falls below 120% of final value			2		µs
SUPPLY CURRENT							
I_{SD}	Supply current, switch disabled	Standard conditions, $I_{(OUTx)}$ = 0 mA			0.01	10	µA
I_{S1E}	Supply current, single switch enabled	Standard conditions, $I_{(OUTx)}$ = 0 mA				90	
I_{S2E}	Supply current, both switches enabled	Standard conditions, $I_{(OUTx)}$ = 0 mA				150	
I_{LKG}	Leakage current	V_{OUT} = 0 V, V_{IN} = 5.5 V, disabled, measured I_{VIN}	TPS20xxC-2		0.05		
	Reverse leakage current	V_{OUT} = 5.5 V, V_{IN} = 0 V, measured $I_{(OUTx)}$			0.20		
UNDERVOLTAGE LOCKOUT							
UVLO	Low-level input voltage, IN	VIN rising		3.4		4.0	V
	Hysteresis, IN				0.14		V
$\overline{FLTx}$							
	Output low voltage, $\overline{FLTx}$	$I_{\overline{(FLTx)}}$ = 1 mA				0.2	V
	Off-state leakage	$V_{\overline{(FLTx)}}$ = 5.5 V				1	µA
	$\overline{FLTx}$ deglitch (2)	$\overline{FLTx}$ overcurrent assertion and deassertion		7	10	13	ms

(1) Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature
(2) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

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ELECTRICAL CHARACTERISTICS (continued)

–40°C ≤ (T_J = T_A) ≤ 125°C, 4.5 V ≤ V_{IN} ≤ 5.5 V, V_{ENx} = V_{IN} or $V_{\overline{ENx}}$ = 0 V, I_{OUTx} = 0 A, typical values are at 5 V and 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
OUTPUT DISCHARGE						
Output pull-down resistance(3)	V_{IN} = 5 V, V_{OUT} = 5 V, disabled	TPS20xxC	300	470	800	Ω
	V_{IN} = 4 V, V_{OUT} = 5 V, disabled	TPS20xxC	350	560	1200	
THERMAL SHUTDOWN						
Junction thermal shutdown threshold	In current limit		135			°C
	Not in current limit		155			
Hysteresis				20		°C

(3) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

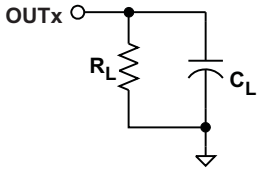

Figure 2. Output Rise / Fall Test Load

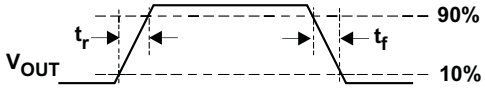

Figure 3. Power-On and Off Timing

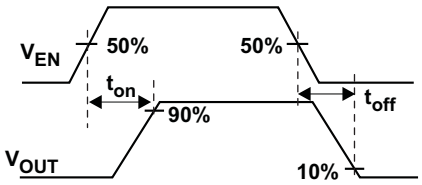

Figure 4. Enable Timing, Active High Enable

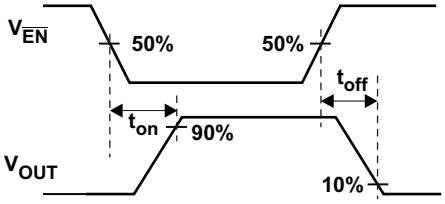

Figure 5. Enable Timing, Active Low Enable

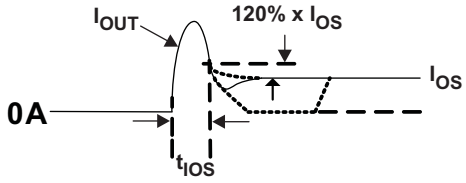

Figure 6. Output Short Circuit Parameters

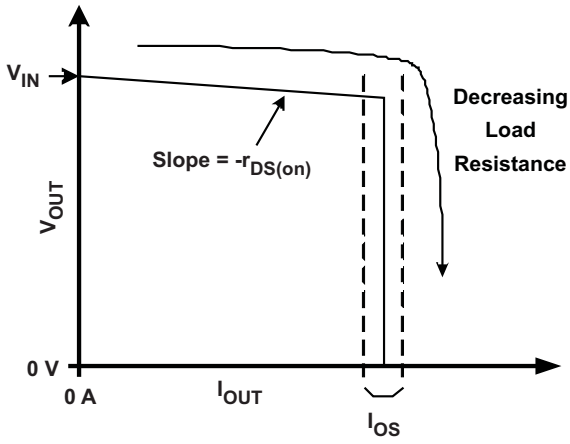

Figure 7. Output Characteristic Showing Current Limit

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FUNCTIONAL BLOCK DIAGRAM

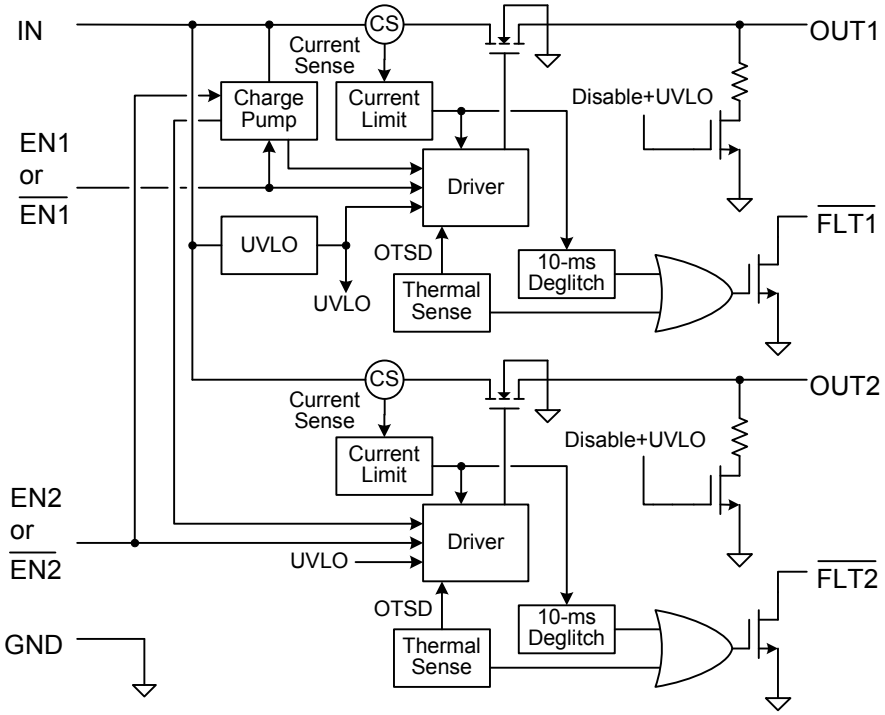

Figure 8. TPS20xxC FUNCTIONAL BLOCK DIAGRAM

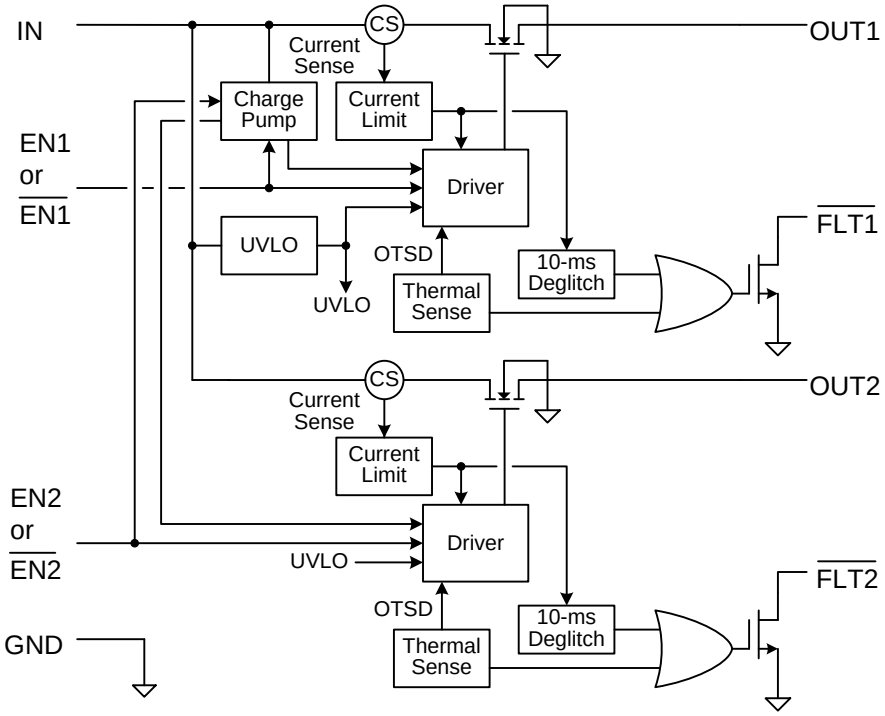

Figure 9. TPS20xxC-2 FUNCTIONAL BLOCK DIAGRAM

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DEVICE INFORMATION

PIN FUNCTIONS – MSOP-8 PACKAGES

NAME	TPS2052C TPS2066C TPS2066C-2 TPS2064C TPS2064C-2	TPS2062C TPS2060C	I/O	DESCRIPTION
GND	1	1	Pwr	Ground connection
IN	2	2	I	Input voltage and power-switch drain; connect a 0.1 µF or greater ceramic capacitor from IN to GND close to the IC
EN1	3	-	I	Enable input channel 1, logic high turns on power switch
$\overline{EN1}$	-	3	I	Enable input channel 1, logic low turns on power switch
EN2	4	-	I	Enable input channel 2, logic high turns on power switch
$\overline{EN2}$	-	4	I	Enable input channel 2, logic low turns on power switch
$\overline{FLT2}$	5	5	O	Active-low open-drain output, asserted during overcurrent, or overtemperature conditions on channel 2
OUT2	6	6	O	Power-switch output channel 2, connected to load
OUT1	7	7	O	Power-switch output channel 1, connected to load
$\overline{FLT1}$	8	8	O	Active-low open-drain output, asserted during over-current, or overtemperature conditions on channel 1
PowerPAD™	PAD	PAD	Pwr	Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect PAD to GND plane as a heatsink.

PIN FUNCTIONS – SOIC-8 PACKAGES

NAME	TPS2066C	TPS2062C	I/O	DESCRIPTION
GND	1	1	Pwr	Ground connection
IN	2	2	I	Input voltage and power-switch drain; connect a 0.1 µF or greater ceramic capacitor from IN to GND close to the IC
EN1	3	-	I	Enable input channel 1, logic high turns on power switch
$\overline{EN1}$	-	3	I	Enable input channel 1, logic low turns on power switch
EN2	4	-	I	Enable input channel 2, logic high turns on power switch
$\overline{EN2}$	-	4	I	Enable input channel 2, logic low turns on power switch
$\overline{FLT2}$	5	5	O	Active-low open-drain output, asserted during overcurrent, or overtemperature conditions on channel 2
OUT2	6	6	O	Power-switch output channel 2, connected to load
OUT1	7	7	O	Power-switch output channel 1, connected to load
$\overline{FLT1}$	8	8	O	Active-low open-drain output, asserted during overcurrent, or overtemperature conditions on channel 1

PIN FUNCTIONS – SON-10 PACKAGES

NAME	TPS2003C	TPS2002C	I/O	DESCRIPTION
GND	1	1	Pwr	Ground connection
IN	2, 3	2, 3	I	Input voltage and power-switch drain; connect a 0.1 µF or greater ceramic capacitor from IN to GND close to the IC
EN1	4	–	I	Enable input channel 1, logic high turns on power switch
$\overline{EN1}$	–	4	I	Enable input channel 1, logic low turns on power switch
EN2	5	–	I	Enable input channel 2, logic high turns on power switch
$\overline{EN2}$	–	5	I	Enable input channel 2, logic low turns on power switch
$\overline{FLT2}$	6	6	O	Active-low open-drain output, asserted during overcurrent, or overtemperature conditions on channel 2
NC	7	7		No connect – leave floating.
OUT2	8	8	O	Power-switch output channel 2, connect to load
OUT1	9	9	O	Power-switch output channel 1, connect to load
$\overline{FLT1}$	10	10	O	Active-low open-drain output, asserted during overcurrent, or overtemperature conditions on channel 1
PowerPAD™	PAD	PAD	Pwr	Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect PAD to GND plane as a heatsink.

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PIN FUNCTIONS – SON-8 PACKAGES

NAME	TPS2062C-2	I/O	DESCRIPTION
GND	1	Pwr	Ground connection
IN	2	I	Input voltage and power-switch drain; connect a 0.1 µF or greater ceramic capacitor from IN to GND close to the IC
$\overline{EN1}$	3	I	Enable input channel 1, logic low turns on power switch
$\overline{EN2}$	4	I	Enable input channel 2, logic low turns on power switch
$\overline{FLT2}$	5	O	Active-low open-drain output, asserted during over-current, or over-temperature conditions on channel 2
OUT2	6	O	Power-switch output channel 2, connect to load
OUT1	7	O	Power-switch output channel 1, connect to load
$\overline{FLT1}$	8	O	Active-low open-drain output, asserted during over-current, or over-temperature conditions on channel 1
PowerPAD™	PAD	Pwr	Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect PAD to GND plane as a heatsink.

TYPICAL CHARACTERISTICS

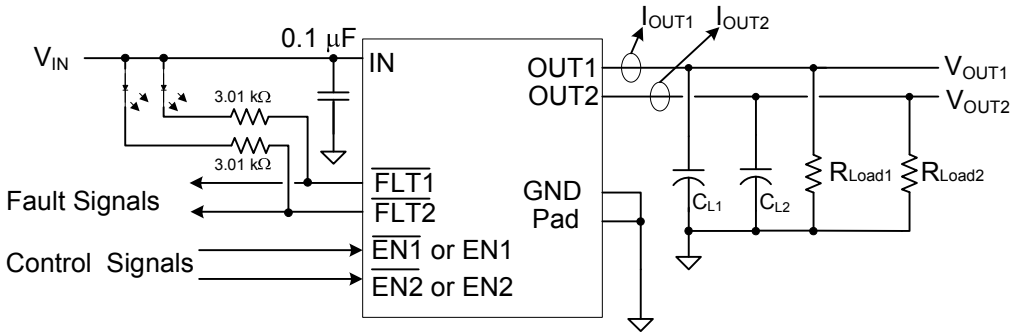

Figure 10. Test Circuit for System Operation in Typical Characteristics Section

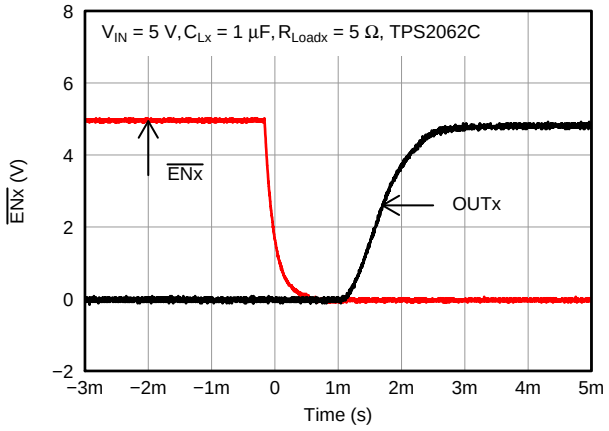

Figure 11. TPS2062C Turn on Delay and Rise Time With 1-µF Load

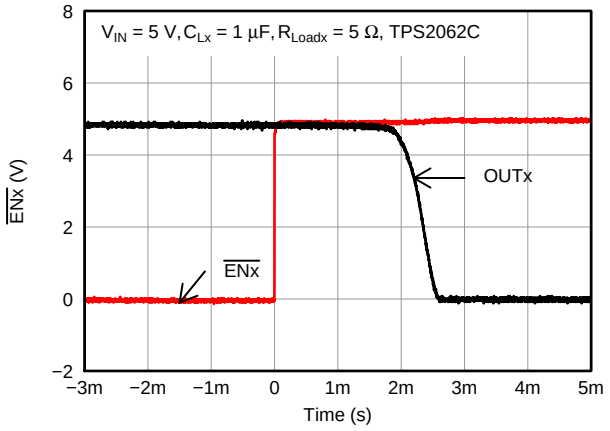

Figure 12. TPS2062C Turn off Delay and Fall Time With 1-µF Load

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TYPICAL CHARACTERISTICS (continued)

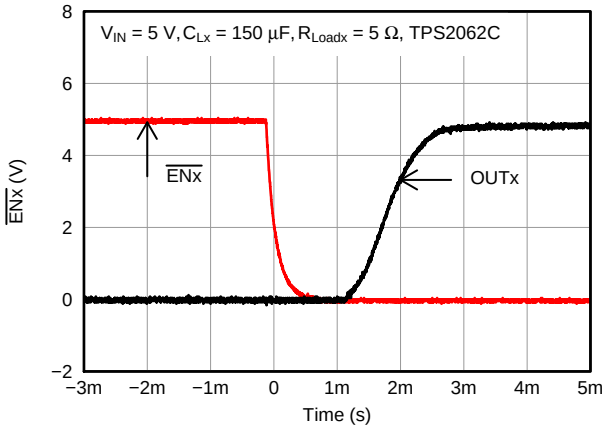

Figure 13. TPS2062C Turn on Delay and Rise Time With 150-µF Load

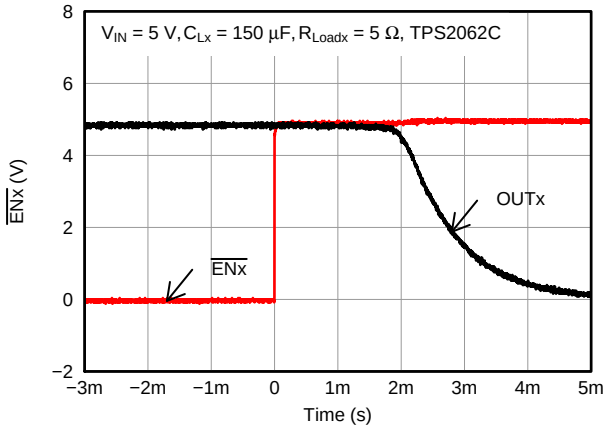

Figure 14. TPS2062C Turn off Delay and Fall Time With 150-µF Load

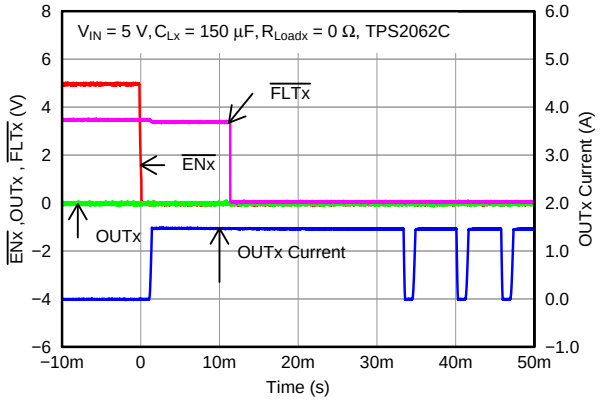

Figure 15. TPS2062C Enable Into Short

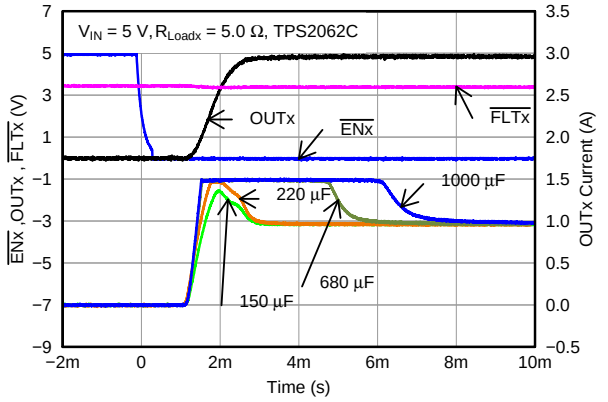

Figure 16. TPS2062C Inrush Current With Different Load Capacitance

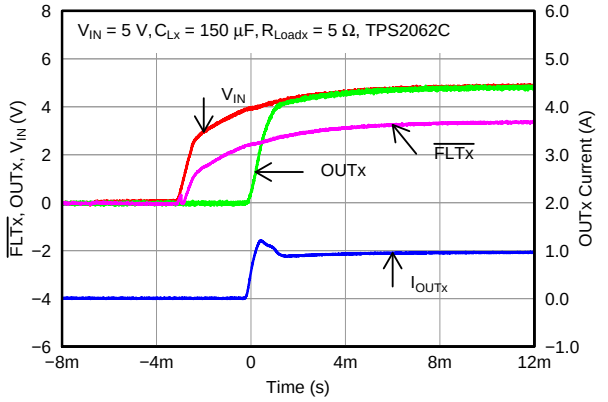

Figure 17. TPS2062C Power Up – Enabled

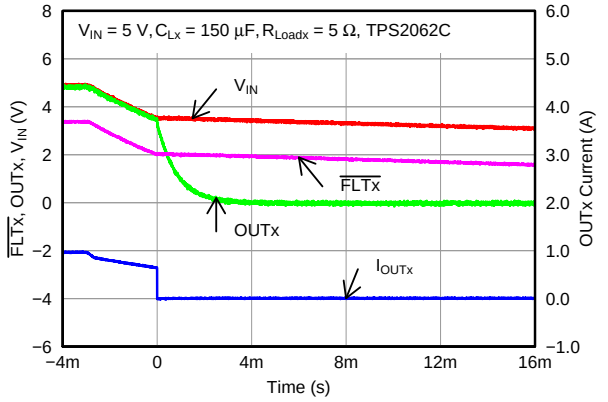

Figure 18. TPS2062C Power Down – Enabled

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TYPICAL CHARACTERISTICS (continued)

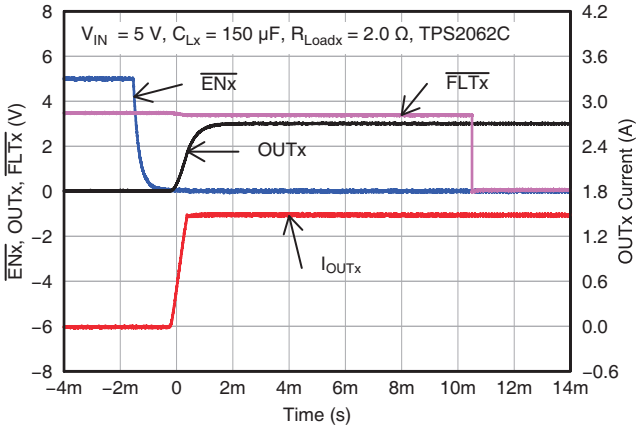

Figure 19. TPS2062C Enable With 2-Ω Load

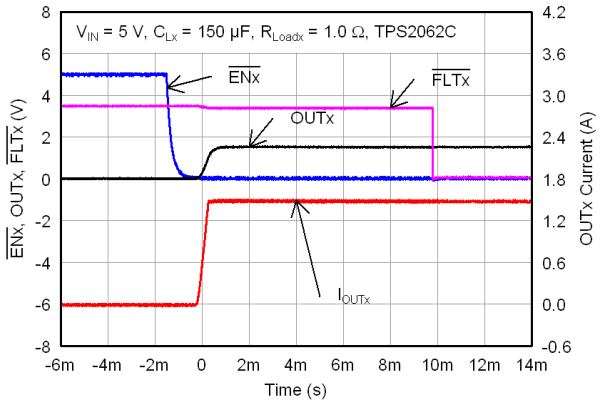

Figure 20. TPS2062C Enable With 1-Ω Load

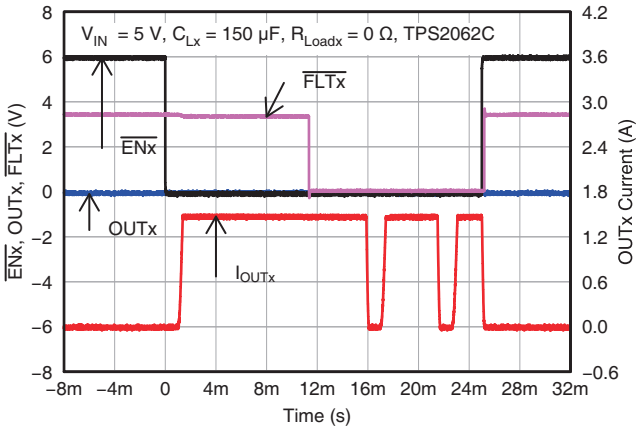

Figure 21. TPS2062C Enable/Disable into Output Short

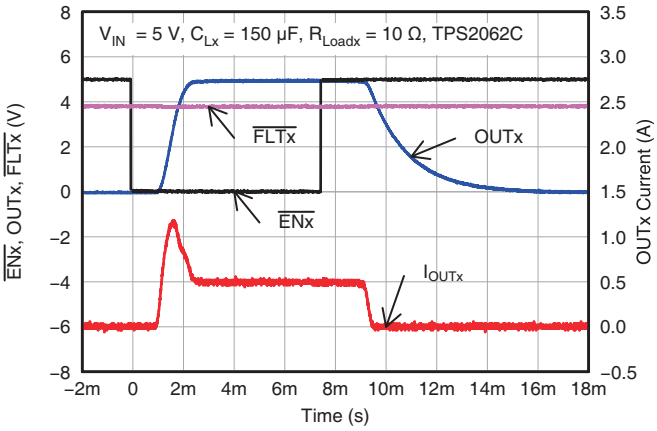

Figure 22. TPS2062C Enable/Disable into 10-Ω Load

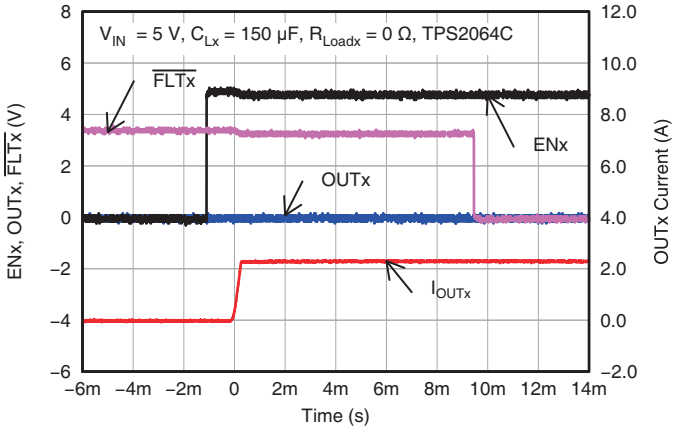

Figure 23. TPS2064C Enable into Short

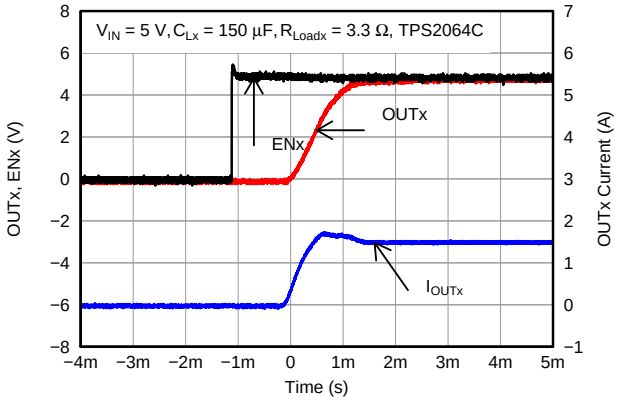

Figure 24. TPS2064C Enable into 3.3 Ω and 150-µF Laod

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TYPICAL CHARACTERISTICS (continued)

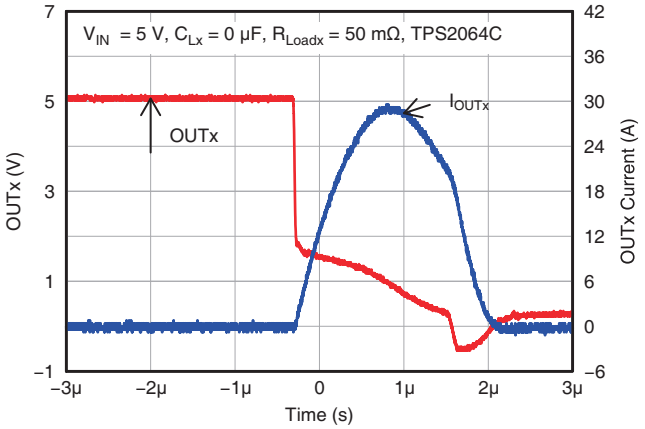

Figure 25. TPS2064C Short Applied

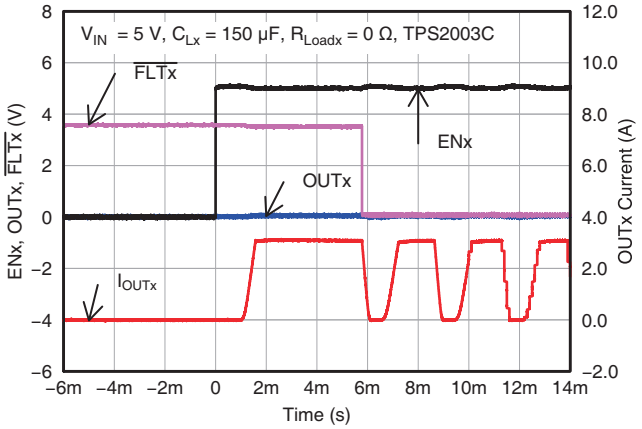

Figure 26. TPS2003C Enable into Short

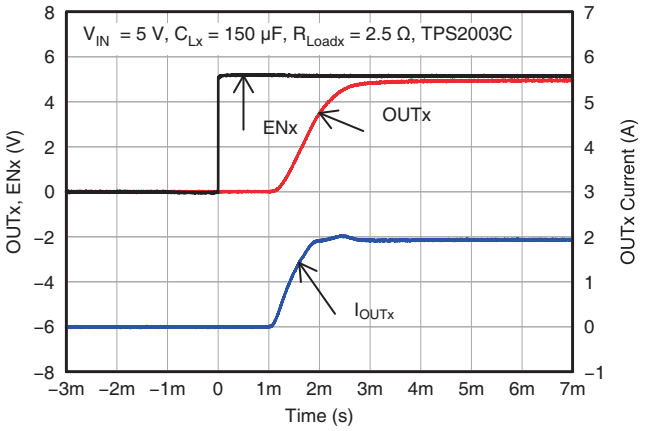

Figure 27. TPS2003C Enable into 2.5 Ω and 150-µF Laod

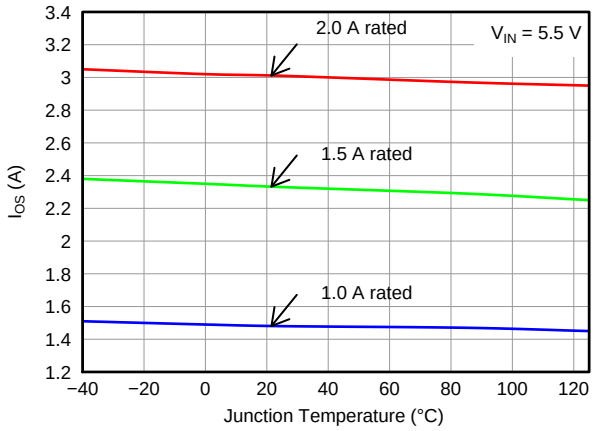

Figure 28. Current Limit (I_{OS}) vs Temperature

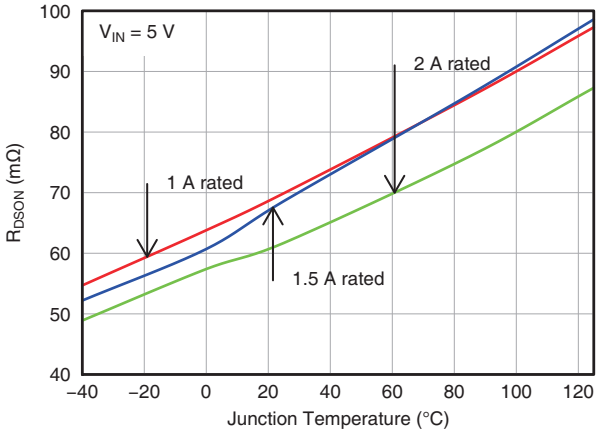

Figure 29. Input - output Resistance ($R_{DS(ON)}$) vs Temperature

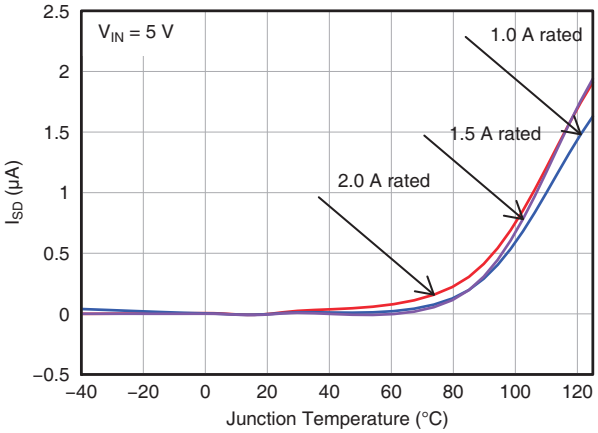

Figure 30. Supply Current (Device Disable) - I_{SD} vs Temperature

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TYPICAL CHARACTERISTICS (continued)

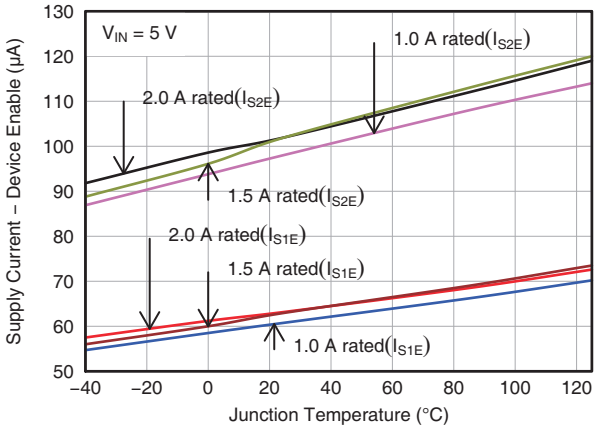

Figure 31. Supply Current (Enable) - I_{SE} vs Temperature

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DETAILED DESCRIPTION

OVERVIEW

The TPS20xxC and TPS20xxC-2 dual are current-limited, power-distribution switches providing between 0.5 A and 2 A of continuous load current in 5-V circuits. These parts use N-channel MOSFETs for low resistance, maintaining output voltage load regulation. They are designed for applications where short circuits or heavy capacitive loads are encountered. Device features include UVLO, ON/OFF control (Enable), reverse blocking when disabled, output discharge when TPS20xxC disabled, overcurrent protection, overtemperature protection, and deglitched fault reporting. They are pin for pin with existing *TI Switch Portfolio*.

UNDERVOLTAGE LOCKOUT (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch when the input voltage is below the UVLO threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage drop from large current surges. $\overline{\text{FLTx}}$ is high impedance when the TPS20xxC and TPS20xxC-2 dual are in UVLO.

ENABLE (ENx or $\overline{\text{ENx}}$)

The logic input of ENx or $\overline{\text{ENx}}$ disables all of the internal circuitry while maintaining the power switch OFF. The supply current of the device can be reduced to less than 1 µA when both switches are disabled. A logic low input on $\overline{\text{ENx}}$ or a logic high input on ENx enables the driver, control circuits, and power switch of corresponding channel.

The ENx or $\overline{\text{ENx}}$ input voltage is compatible with both TTL and CMOS logic levels. The $\overline{\text{FLTx}}$ is immediately cleared and the output discharge circuit is enabled when the device is disabled.

DEGLITCHED FAULT REPORTING

$\overline{\text{FLTx}}$ is an open-drain output that asserts (active low) during an overcurrent or overtemperature condition on each corresponding channel. The $\overline{\text{FLTx}}$ output remains asserted until the fault condition is removed or the channel is disabled. The TPS20xxC and TPS20xxC-2 dual eliminates false $\overline{\text{FLTx}}$ reporting by using internal delay circuitry after entering or leaving an overcurrent condition. The “deglitch” time is typically 10 ms. This ensures that $\overline{\text{FLTx}}$ is not accidentally asserted under overcurrent conditions with a short time, such as starting into a heavy capacitive load. Over temperature conditions are not deglitched. The $\overline{\text{FLTx}}$ pin is high impedance when the device is disabled and in undervoltage lockout (UVLO). The fault circuits are independent so that another channel continues to operate when one channel is in a fault condition.

OVERCURRENT PROTECTION

The TPS20xxC and TPS20xxC-2 dual responds to overloads by limiting each channel output current to the static I_{OS} levels shown in the *Electrical Characteristics* table. When an overload condition is present, the device maintains a constant current (I_{OS}) and reduces the output voltage accordingly, with the output voltage falling to (I_{OS} x R_{SHORT}). Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before voltage is applied to IN. The device senses over-current and immediately switches into a constant-current output. In the second condition, a short or an overload occurs while the device is enabled. At the instant a short -circuit occurs, high currents may flow for several microseconds (t_{IOS}) before the current-limit circuit reacts. The device operates in constant-current mode after the current-limit circuit has responded. In the third condition, the load is increased gradually beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached. The devices are capable of delivering current up to the current-limit threshold without damage. Once the threshold is reached, the device switches into constant-current mode. For all of the above three conditions, the device may begin thermal cycling if the overcurrent condition persists.

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OVERTEMPERATURE PROTECTION

The TPS20xxC and TPS20xxC-2 dual includes per channel overtemperature protection circuitry, which activates at 135°C (min) junction temperature while in current limit. There is an overall thermal shutdown of 155°C (min) junction temperature when the TPS20xxC and TPS20xxC-2 dual are not in current limit. The device remains off until the junction temperature cools 20°C and then restarts. Thermal shutdown may occur during an overload due to the relatively large power dissipation [$(V_{IN} – V_{OUT}) \times I_{OS}$] driving the junction temperature up. The power switch cycles on and off until the fault is removed. This topology allows one channel to continue normal operation even if the other channel is in an over-temperature condition.

SOFTSTART, REVERSE BLOCKING AND DISCHARGE OUTPUT

The power MOSFET driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges on the input supply, and provides built-in soft-start functionality.

The TPS20xxC and TPS20xxC-2 dual power switch will block current from OUT to IN when turned off by the UVLO or disabled.

The TPS20xxC dual includes an output discharge function on each channel. A 470Ω (typ.) discharge resistor will dissipate stored charge and leakage current on OUTx when the device is in UVLO or disabled. However as this circuit is biased from IN, the output discharge will not be active when IN voltage is close to 0 V.

The TPS20xxC-2 does not have this function. The output is be controlled by an external loadings when the device is in ULVO or disabled.

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APPLICATION INFORMATION

INPUT AND OUTPUT CAPACITANCE

Input and output capacitance improves the performance of the device. For all applications, a 0.1 µF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise de-coupling. The actual capacitance should be optimized for the particular application. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce the overshoot voltage from exceeding the absolute maximum voltage of the device during heavy transients.

A 120 µF minimum output capacitance is required when implementing USB standard applications. Typically this uses a 150 µF electrolytic capacitor. If the application does not require 120 µF of output capacitance, a minimum of 10 µF ceramic capacitor on the output is recommended in order to reduce the transient negative voltage on OUTx pin caused by load inductance during a short circuit. The transient negative voltage should be less than 1.5 V for 10 µs.

POWER DISSIPATION AND JUNCTION TEMPERATURE

It is good design practice to estimate power dissipation and maximum expected junction temperature of the TPS20xxC and TPS20xxC-2 dual. The system designer can control choices of package, proximity to other power dissipating devices, and printed circuit board (PCB) design based on these calculations. These have a direct influence on maximum junction temperature. Other factors such as airflow and maximum ambient temperature are often determined by system considerations.

Addition of extra PCB copper area around these devices is recommended to reduce the thermal impedance and maintain the junction temperature as low as practical.

The following procedure requires iteration because power loss is due to the two internal MOSFETs $2 \times I^2 \times r_{DS(on)}$, and $r_{DS(on)}$ is a function of the junction temperature. As an initial estimate, use the $r_{DS(on)}$ at 125°C from the typical characteristics, and the preferred package thermal resistance for the preferred board construction from the thermal parameters section.

$$T_J = T_A + [(2 \times I_{OUT}^2 \times r_{DS(on)} \times \theta_{JA}]$$

Where:

I_{OUT} = rated OUT pin current (A)
$r_{DS(on)}$ = Power switch on-resistance at an assumed T_J (Ω)
T_A = Maximum ambient temperature (°C)
T_J = Maximum junction temperature (°C)
θ_{JA} = Thermal resistance (°C/W)

If the calculated T_J is substantially different from the original assumption, look up a new value of $r_{DS(on)}$ and recalculate.

If the resulting T_J is not less than 125°C, try a PCB construction and/or package with lower θ_{JA}.

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REVISION HISTORY

Changes from Original (October 2011) to Revision A **Page**

- Changed devices TPS2062C and TPS2066C MSOP-8 package From: Preview to Active 1
- Changed the I_{OS} current limit values for TPS2062C and 66C (1 A). 3
- Changed the I_{OS} current limit values for TPS2062C/66C (1 A). 4

Changes from Revision A (March 2012) to Revision B **Page**

- Changed device TPS2060C MSOP-8 package From: Preview To: Active 1

Changes from Revision B (March 2012) to Revision C **Page**

- Changed devices TPS2062C and TPS2066C SOIC-8 package From: Preview To: Active 1
- Changed the TPS2062C and 66C $r_{DS(on)}$ D package TYP value From: 84 to 90 mΩ and added the MAX value 3
- Changed the TPS2062C and 66C $r_{DS(on)}$ D package TYP value From: 84 to 90 mΩ 4

Changes from Revision C (June 2012) to Revision D **Page**

- Changed the Device Information table, Package Devices and Marking columns 2

Changes from Revision D (July 2012) to Revision E **Page**

- Changed devices TPS2002C and TPS2003C SON-10 package From: Preview To: Active 1
- Changed the I_{OS} current limit values for TPS2002C and 03C (2 A). 3
- Corrected Note 2 references in the ELECTRICAL CHARACTERISTICS table 4
- Changed the I_{OS} current limit values for TPS2002C and 03C (2 A). 4

Changes from Revision E (August 2012) to Revision F **Page**

- 将特性从 1A，1.5A，2A 的额定电流改为：0.5A，1A，1.5A，2A 的额定电流 1
- 将特性从：禁用时输出放电改为：所选的具有 (TPS20xxC) 和不具有 (TPS20xxC-2)输出放电的部件 1
- Added DRB pin option 1
- Added TPS2052C, TPS2062C-2, TPS2064C-2, and TPS2066C-2 devices to Table 1 1
- Added TPS2052C, TPS2062C-2, TPS2064C-2, and TPS2066C-2 devices to 2
- Added TPS2052C, TPS2062C-2, TPS2064C-2, and TPS2066C-2 devices to RECOMMENDED OPERATING CONDITIONS table 3
- Added TPS2052C and TPS2066C-2 devices to $r_{DS(on)}$ 3
- Added the TPS2052C and TPS2064C-2 devices to I_{OS} 3
- Added Leakage Current 3
- Added TPS2052C and TPS2066C-2 devices to $r_{DS(on)}$ 4
- Added the TPS2052C and TPS2064C-2 devices to I_{OS} 4
- Added Leakage Current 4
- Added text to the SOFTSTART, REVERSE BLOCKING AND DISCHARGE OUTPUT section 14
- Added last paragraph in the DISCHARGE OUTPUT section 14

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Changes from Revision F (November 2012) to Revision G **Page**

- Changed device TPS2062C-2 SON-8 packages From: Preview To: Active. 1
- Changed devices TPS2066C-2, and TPS2064C-2 MSOP-8 package From: Preview To: Active 1

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2002CDRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VFEQ	Samples
TPS2002CDRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VFEQ	Samples
TPS2003CDRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VRFQ	Samples
TPS2003CDRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VRFQ	Samples
TPS2052CDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYNI	Samples
TPS2052CDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYNI	Samples
TPS2060CDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VRAQ	Samples
TPS2060CDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VRAQ	Samples
TPS2062CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2062C	Samples
TPS2062CDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VRBQ	Samples
TPS2062CDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VRBQ	Samples
TPS2062CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2062C	Samples
TPS2062CDRBR-2	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PYVI	Samples
TPS2062CDRBT-2	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PYVI	Samples
TPS2064CDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VRCQ	Samples
TPS2064CDGN-2	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYTI	Samples
TPS2064CDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VRCQ	Samples
TPS2064CDGNR-2	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYTI	Samples
TPS2065CDBVR-2	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYQI	Samples
TPS2065CDBVT-2	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PYQI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2065CDGN-2	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYRI	Samples
TPS2065CDGNR-2	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYRI	Samples
TPS2066CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2066C	Samples
TPS2066CDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VRDQ	Samples
TPS2066CDGN-2	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYUI	Samples
TPS2066CDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VRDQ	Samples
TPS2066CDGNR-2	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYUI	Samples
TPS2066CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2066C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

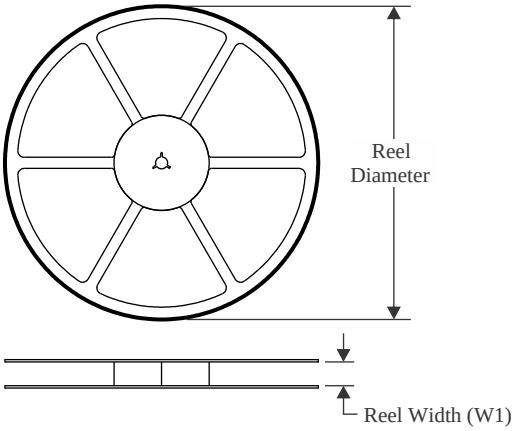
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

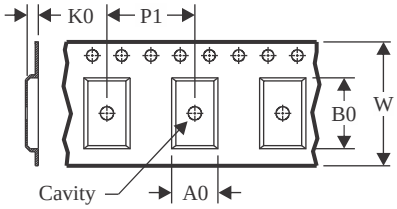
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

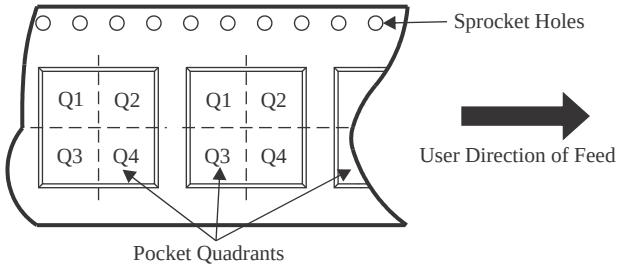


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

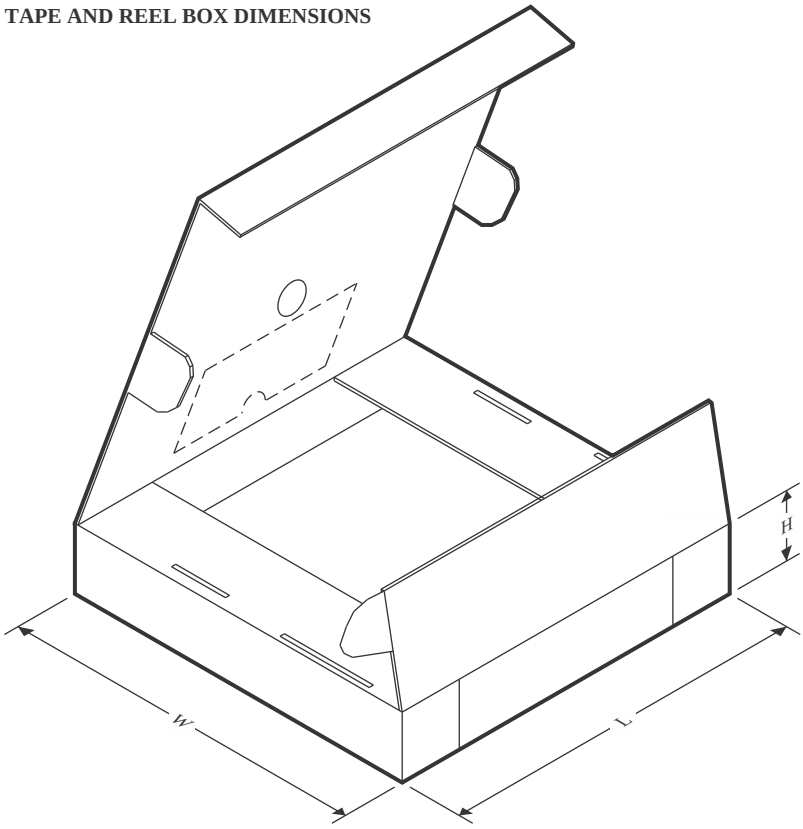


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2002CDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2002CDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2003CDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2003CDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2052CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2060CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2062CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2062CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2062CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2062CDRBR-2	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2062CDRBT-2	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2064CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2064CDGNR-2	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2065CDBVR-2	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2065CDBVT-2	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS2065CDBVT-2	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2065CDGNR-2	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2066CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2066CDGNR-2	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2066CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

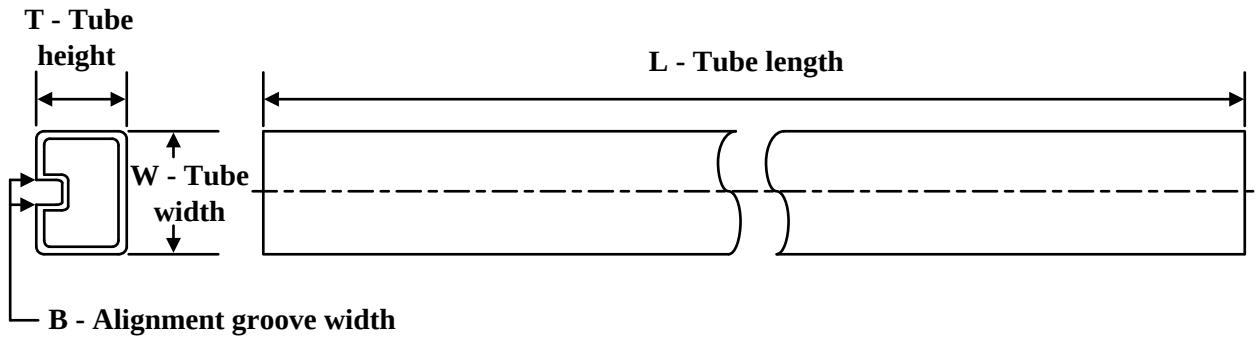


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2002CDRCR	VSON	DRC	10	3000	346.0	346.0	33.0
TPS2002CDRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS2003CDRCR	VSON	DRC	10	3000	346.0	346.0	33.0
TPS2003CDRCT	VSON	DRC	10	250	182.0	182.0	20.0
TPS2052CDGNR	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS2060CDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
TPS2062CDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
TPS2062CDR	SOIC	D	8	2500	356.0	356.0	35.0
TPS2062CDR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2062CDRBR-2	SON	DRB	8	3000	335.0	335.0	25.0
TPS2062CDRBT-2	SON	DRB	8	250	182.0	182.0	20.0
TPS2064CDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
TPS2064CDGNR-2	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS2065CDBVR-2	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2065CDBVT-2	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS2065CDBVT-2	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS2065CDGNR-2	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS2066CDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2066CDGNR-2	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS2066CDR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2052CDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2060CDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2062CD	D	SOIC	8	75	507	8	3940	4.32
TPS2062CDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2064CDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2064CDGN-2	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2065CDGN-2	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2066CD	D	SOIC	8	75	507	8	3940	4.32
TPS2066CDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2066CDGN-2	DGN	HVSSOP	8	80	330	6.55	500	2.88

GENERIC PACKAGE VIEW

DRB 8 VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

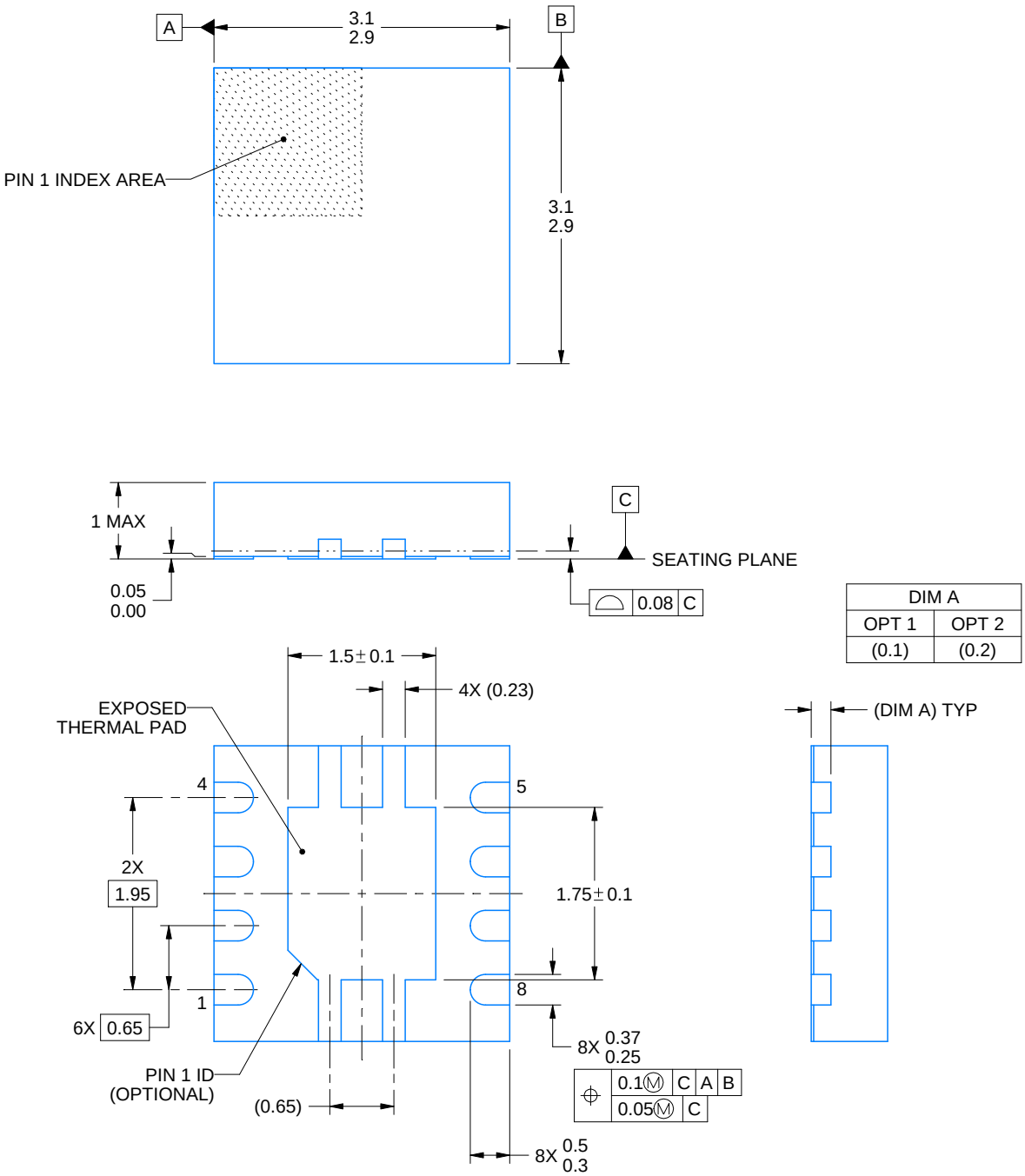
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRB0008A

PACKAGE OUTLINE

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

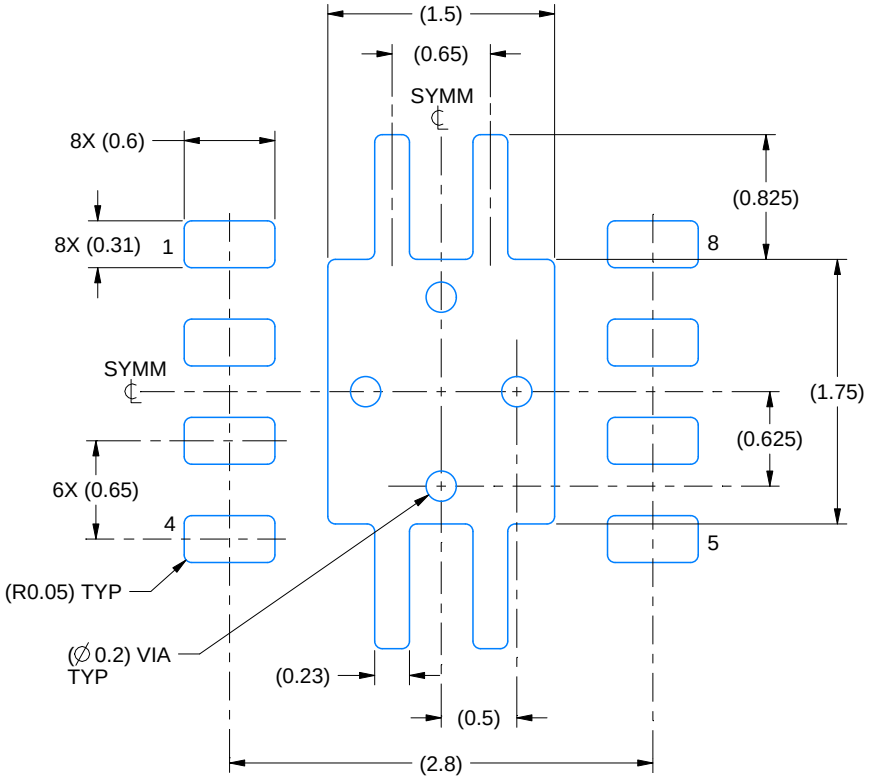
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

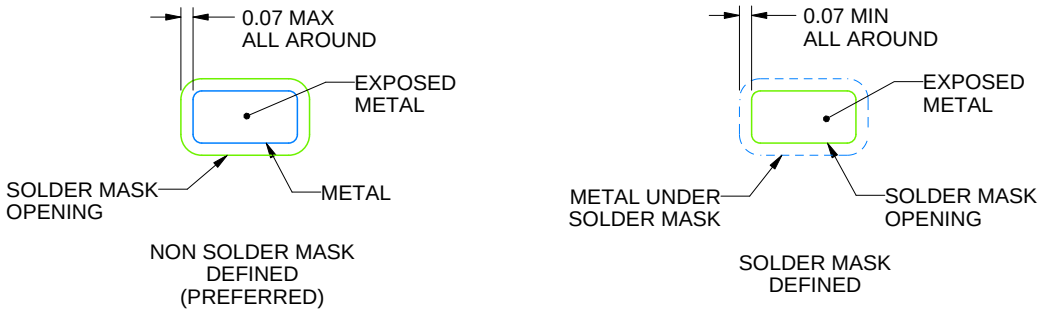
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

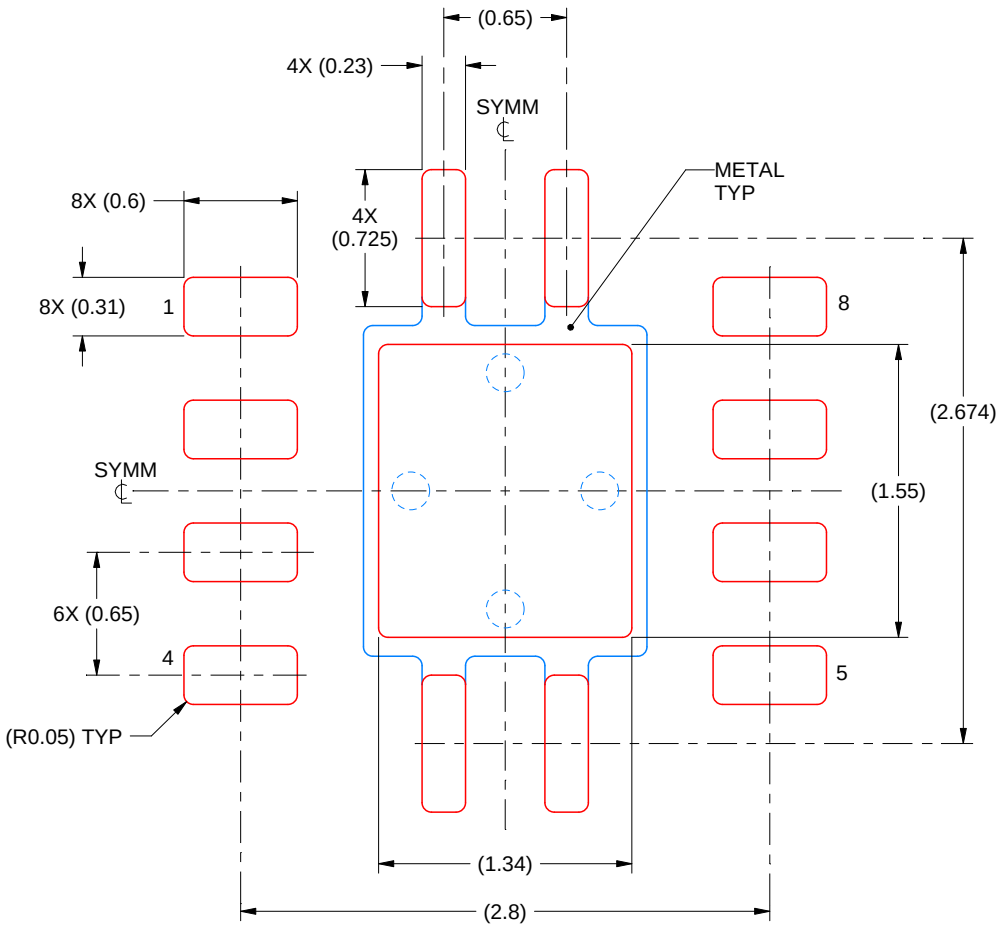


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

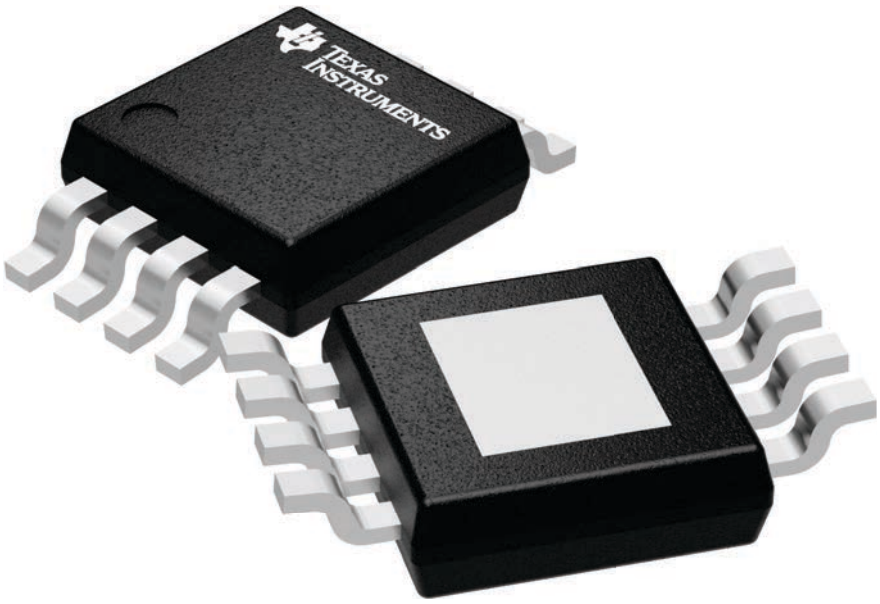
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

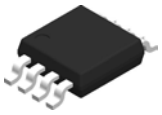
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

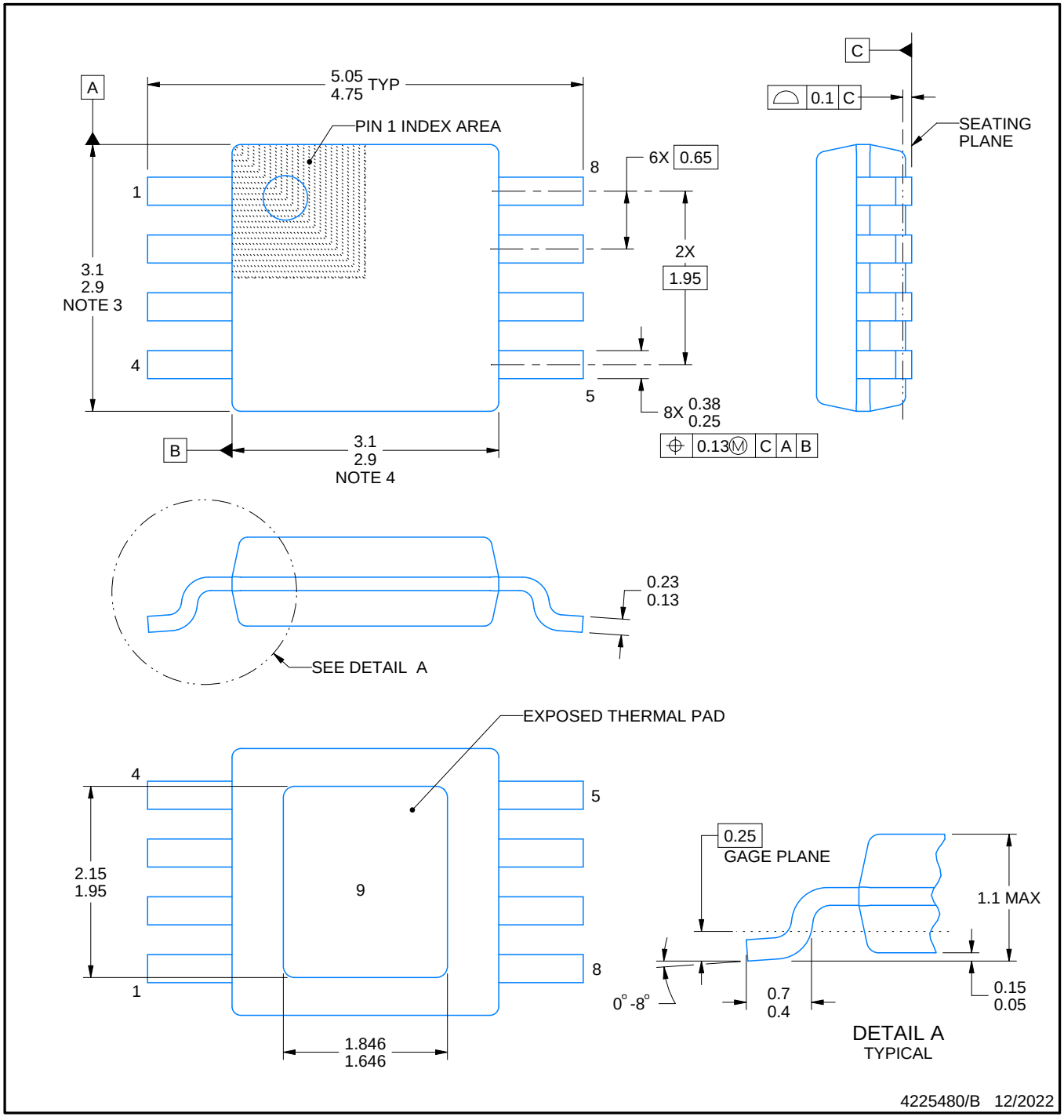
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

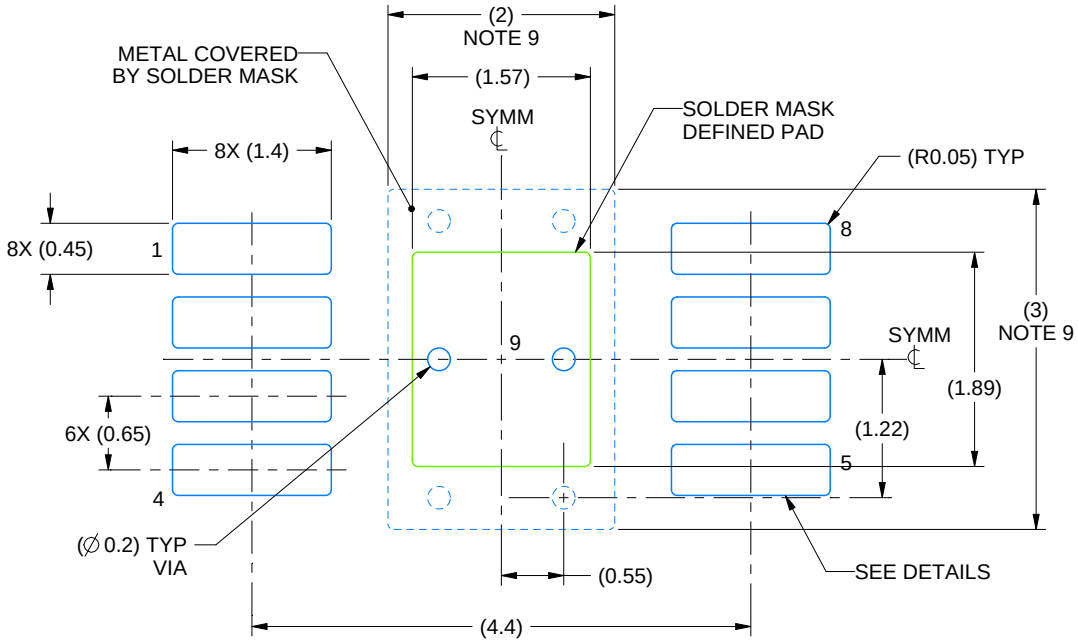
SMALL OUTLINE PACKAGE



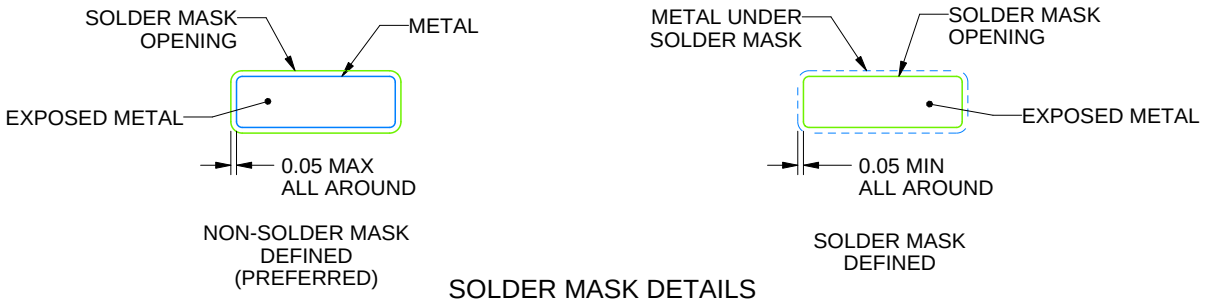
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

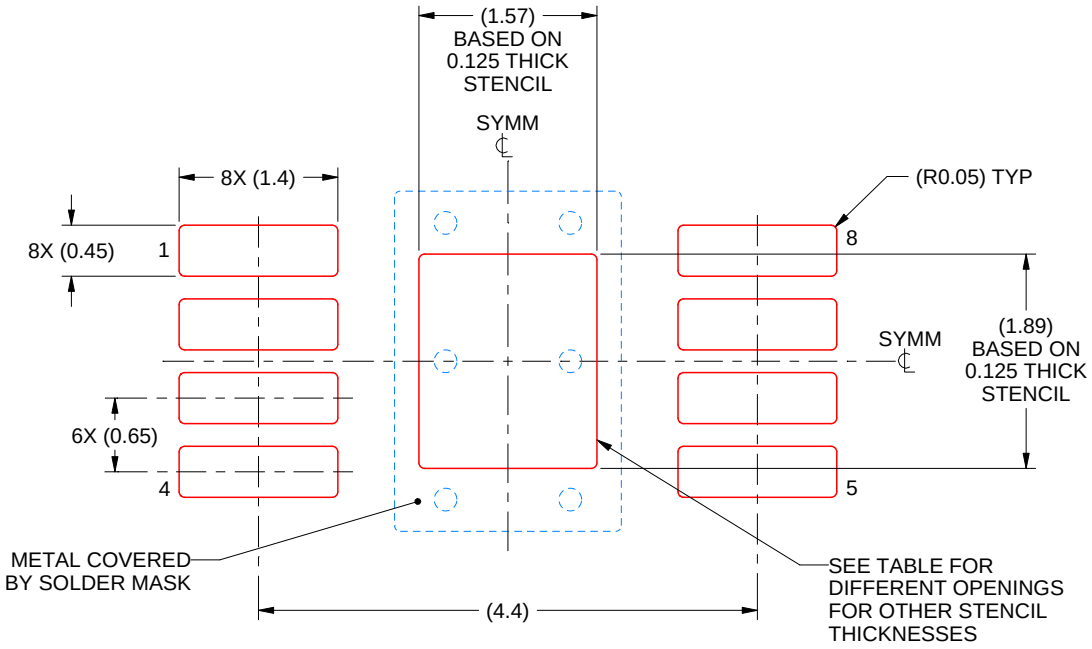


SOLDER MASK DETAILS

4225480/B 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/B 12/2022

NOTES: (continued)

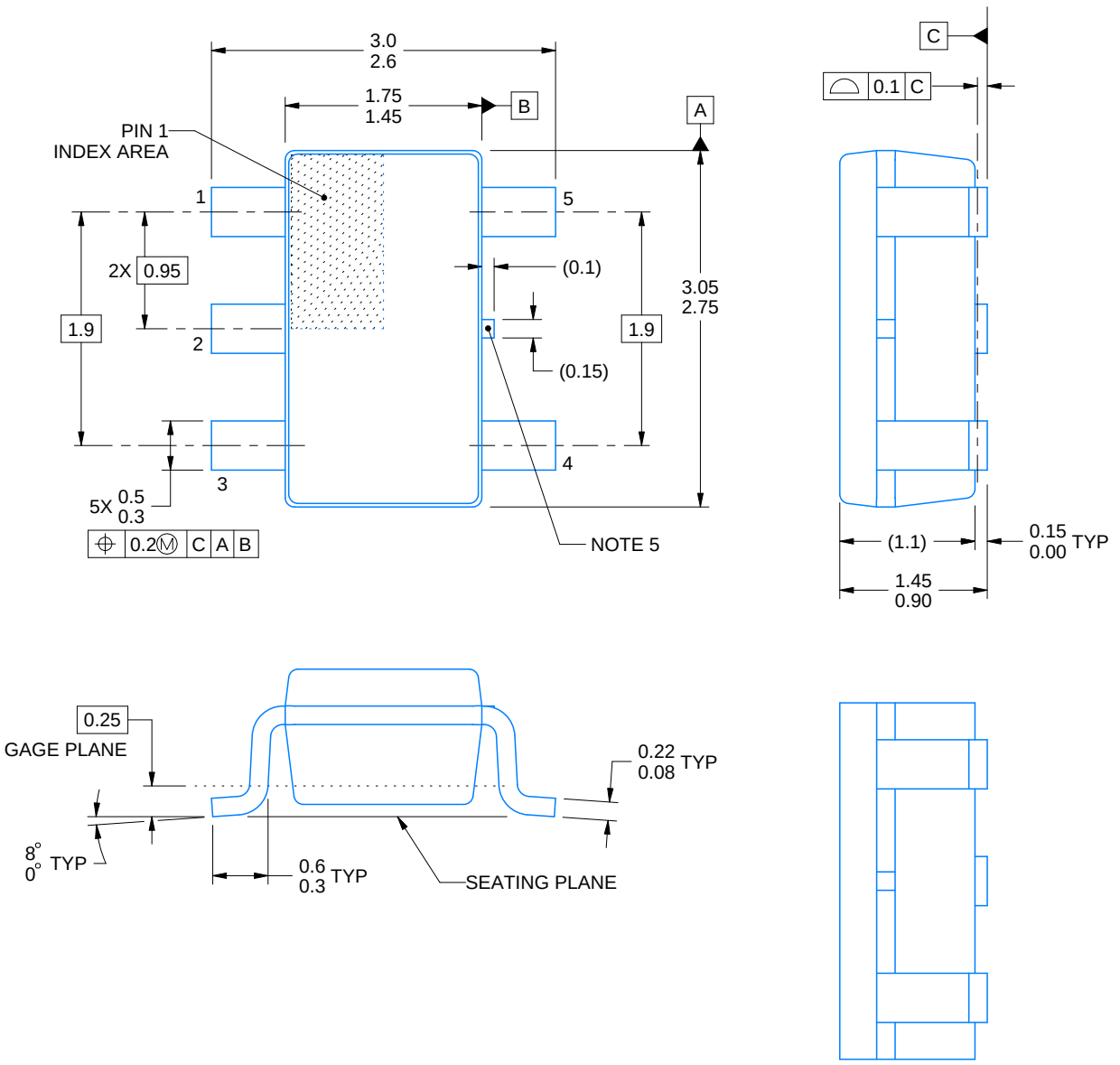
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

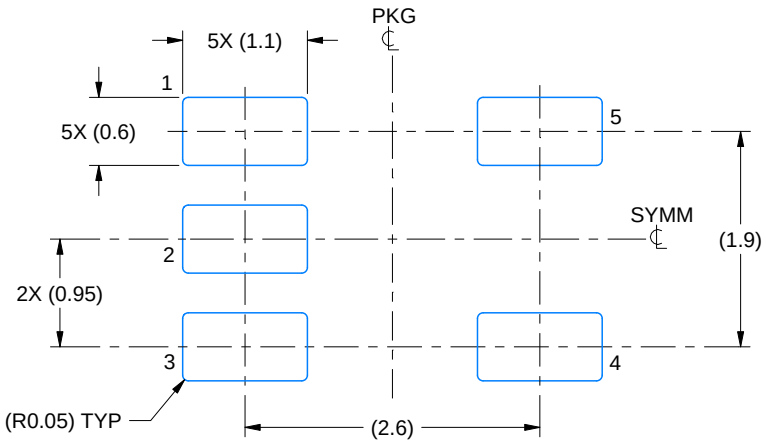


ALTERNATIVE PACKAGE SINGULATION VIEW

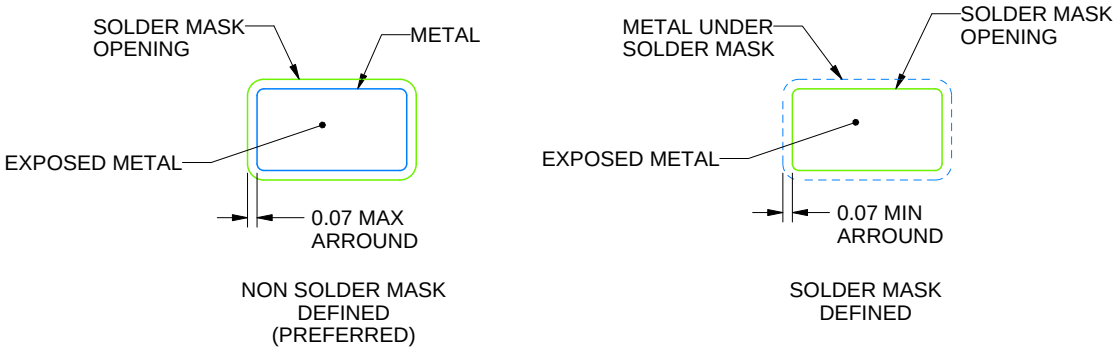
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

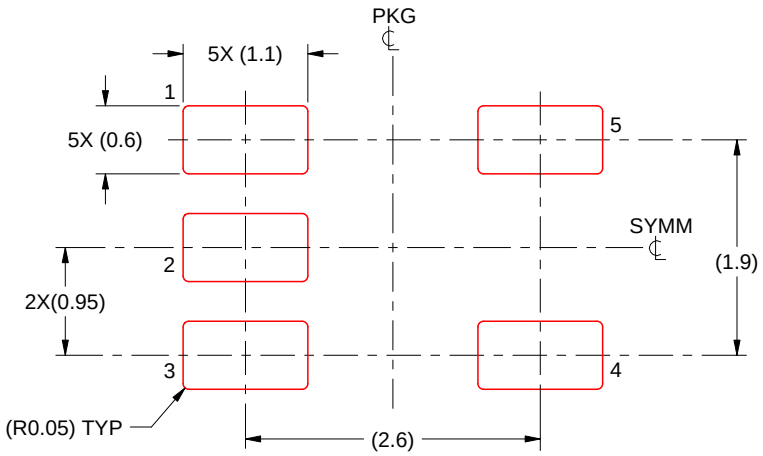


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

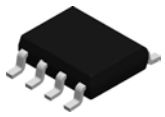


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

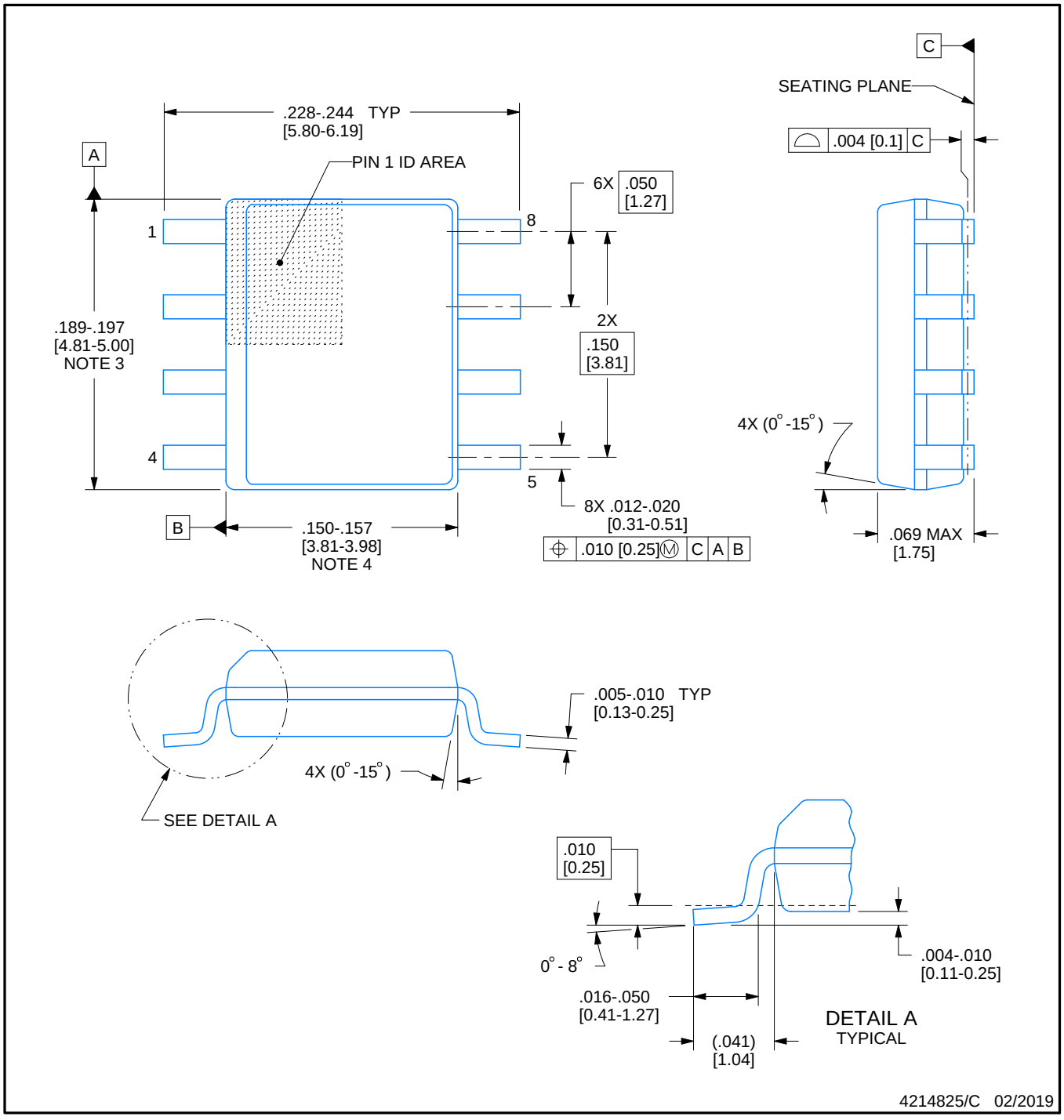


PACKAGE OUTLINE

D0008A

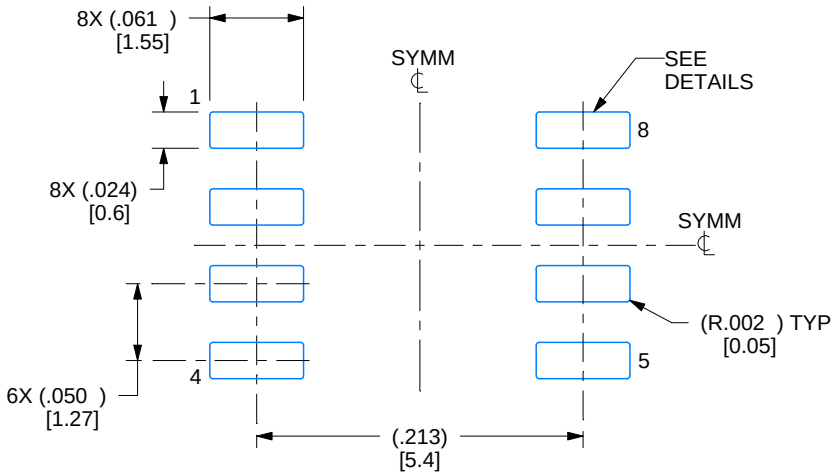
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

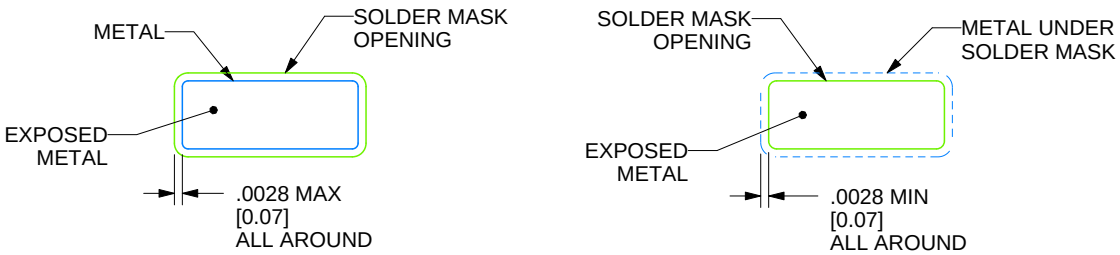


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

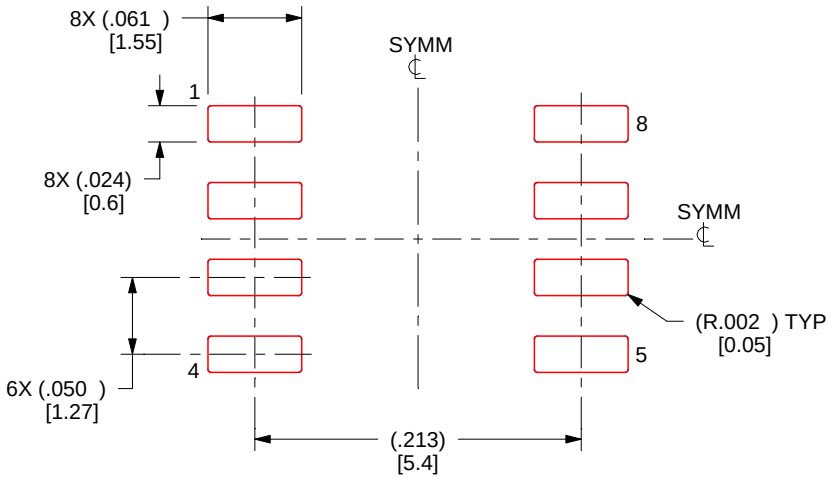
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

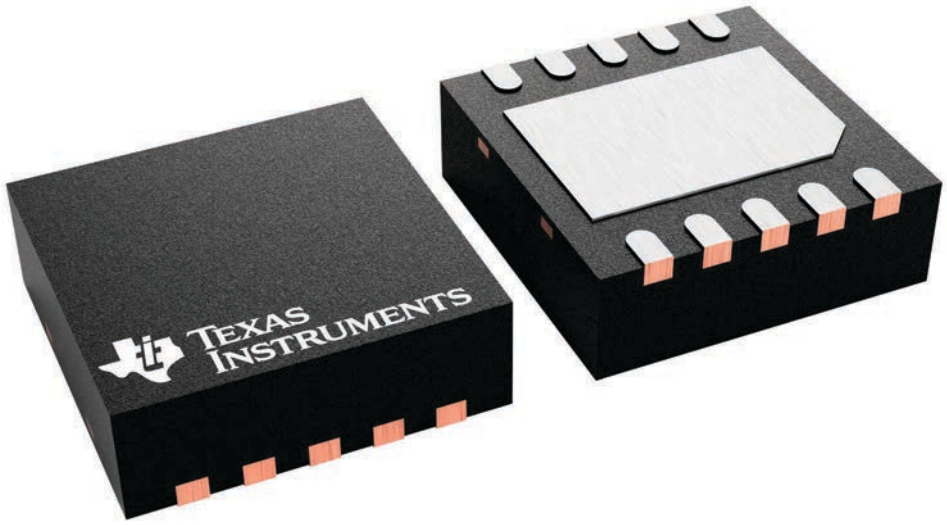
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226193/A

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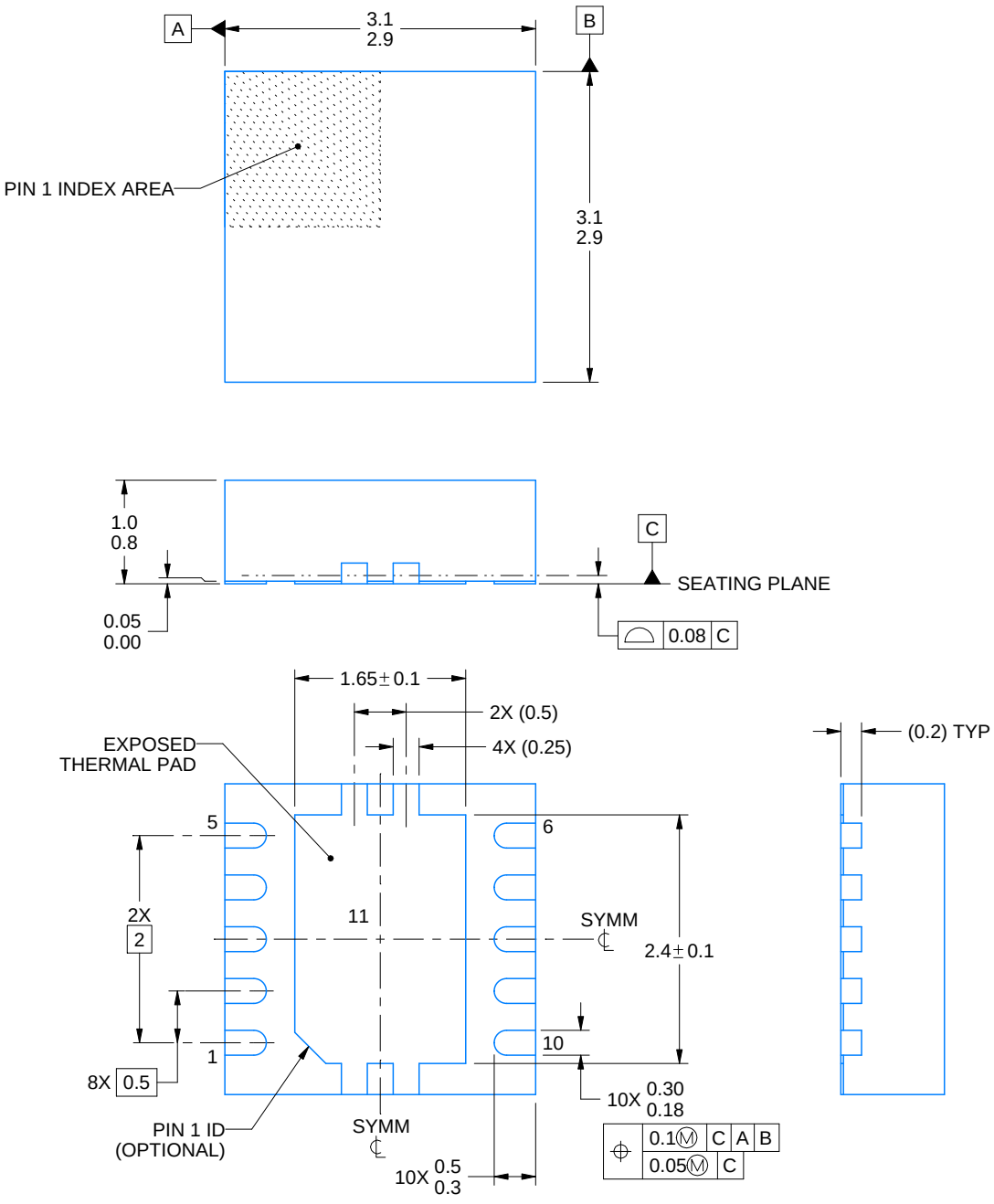
PACKAGE OUTLINE

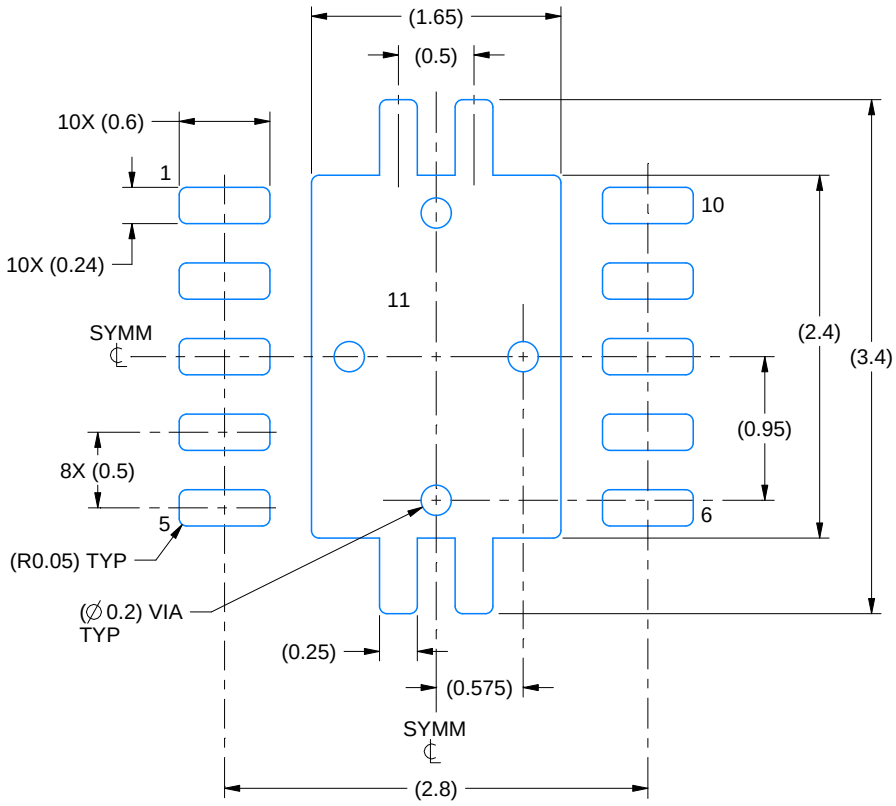
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

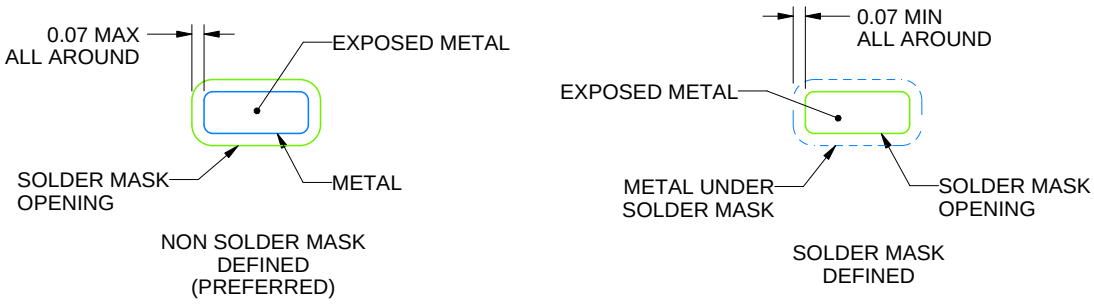


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

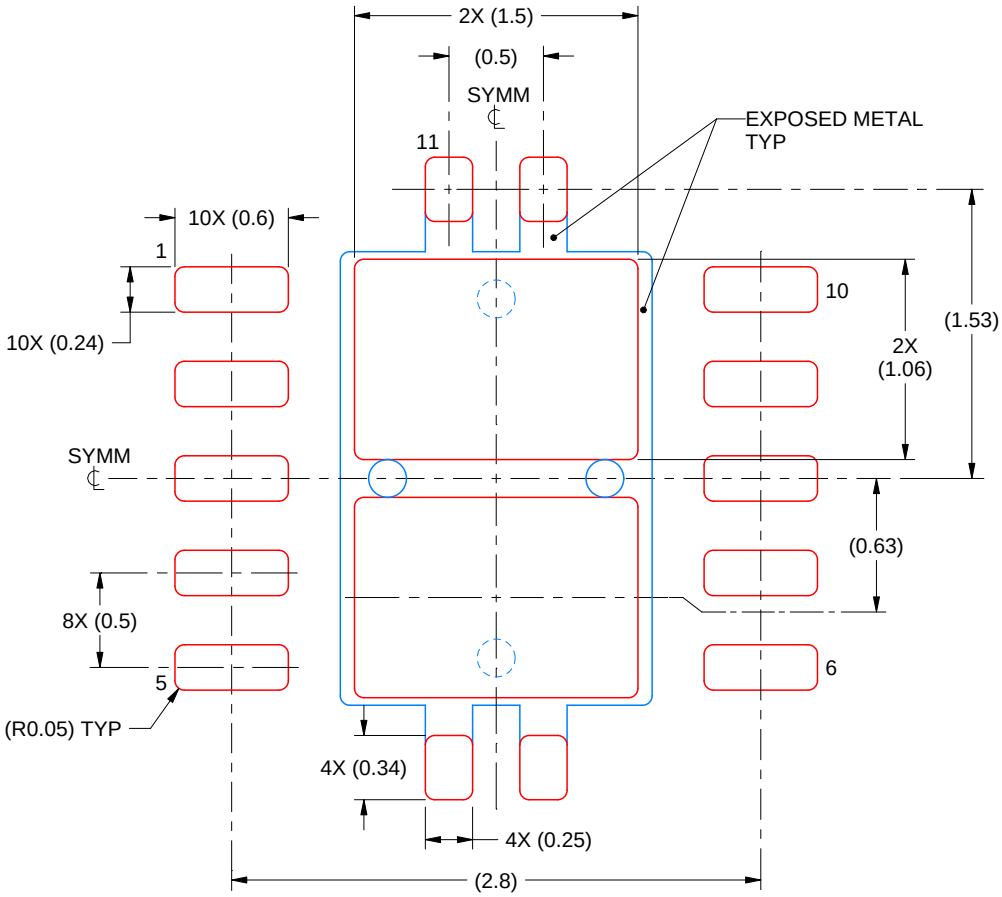


SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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