ADC12010 12-Bit, 10 MSPS, 160 mW A/D Converter with Internal Sample-and-Hold

Check for Samples: ADC12010

FEATURES

- **Internal sample-and-hold**
- **Outputs 2.4V to 5V compatible**
- **Pin compatible with ADC12020, ADC12040, ADC12L063 and ADC12L066**
- **On-chip reference buffer**
- **Power down mode**

APPLICATIONS

- **Image Processing Front End**
- **Instrumentation**
- **PC-Based Data Acquisition**
- **Fax Machines**
- **Wireless Local Loops/Cable Modems**
- **Waveform Digitizers**
- **DSP Front Ends**

KEY SPECIFICATIONS

- **Resolution 12 Bits**
- **Conversion Rate 10 MSPS (min)**
- **DNL ±0.3 LSB (typ)**
- **ENOB (f_{IN} = 10.1 MHz) 11.3 bits (typ)**
- **Supply Voltage +5 / ±5 V / %**
- **Power Consumption, 10 MHz 160 mW (typ)**

DESCRIPTION

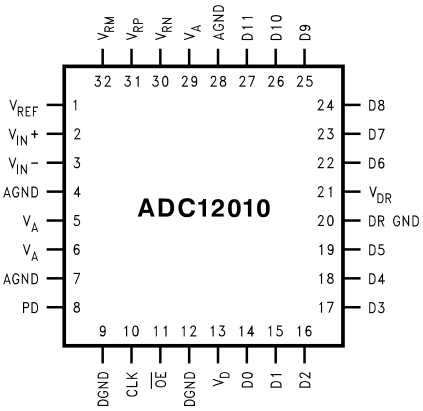
The ADC12010 is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 10 Megasamples per second (MSPS), minimum. This converter uses a differential, pipeline architecture with digital error correction and an on-chip sample-and-hold circuit to minimize die size and power consumption while providing excellent dynamic performance. Operating on a single 5V power supply, this device consumes just 160 mW at 10 MSPS, including the reference current. The Power Down feature reduces power consumption to 25 mW.

The differential inputs provide a full scale input swing equal to $2V_{REF}$ with the possibility of a single-ended input. Full use of the differential input is recommended for optimum performance. For ease of use, the buffered, high impedance, single-ended reference input is converted on-chip to a differential reference for use by the processing circuitry. Output data format is 12-bit offset binary.

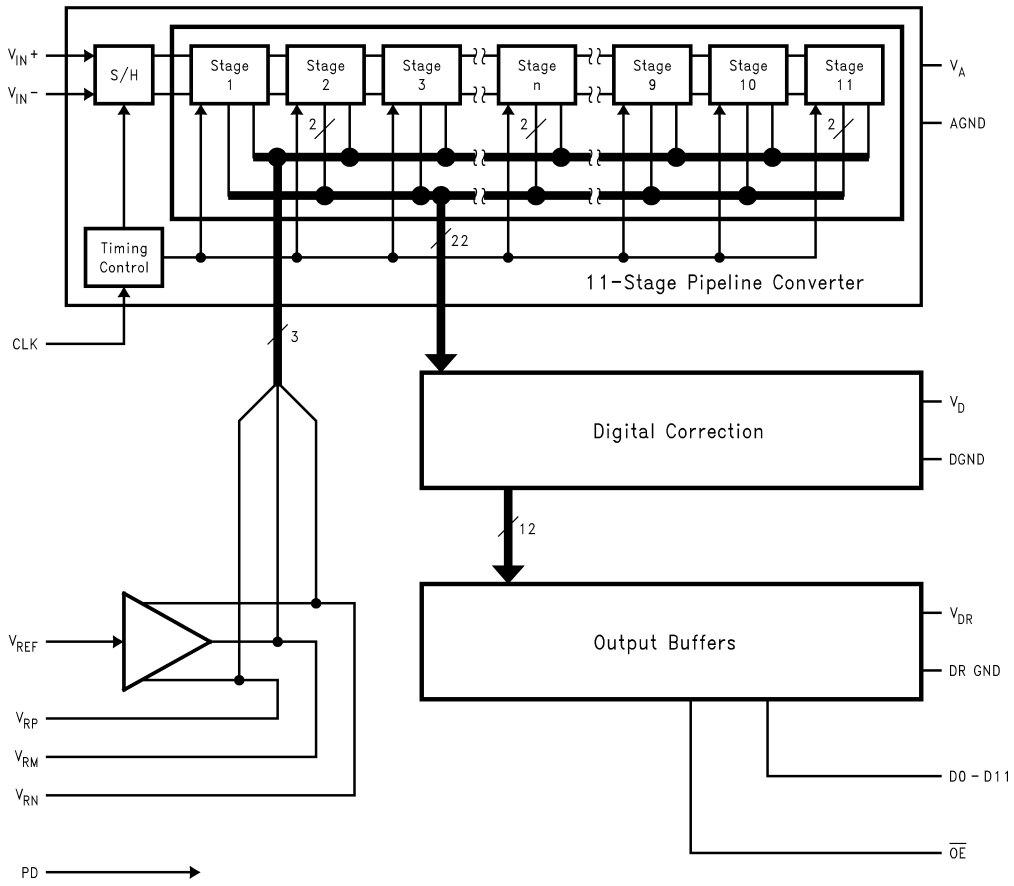
This device is available in the 32-lead LQFP package and will operate over the industrial temperature range of −40°C to +85°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

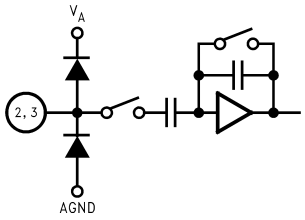
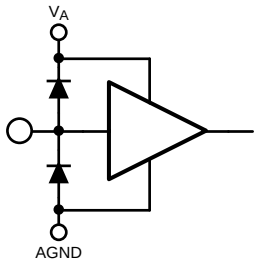
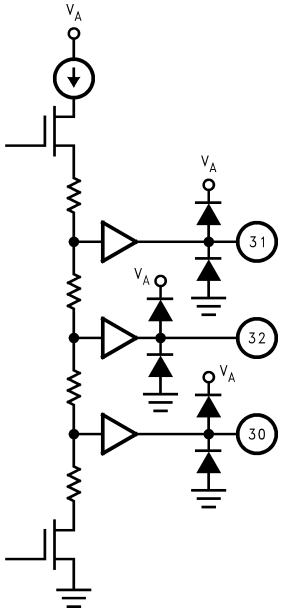
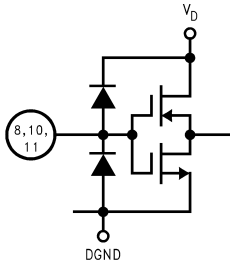
Connection Diagram

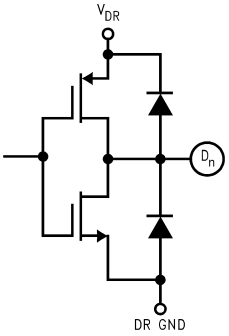


Block Diagram



Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
2	V_{IN}^+		Non-Inverting analog signal Input. With a 2.0V reference voltage, the ground-referenced input signal level is 2.0 V_{P-P} centered on V_{CM}.
3	V_{IN}^-		Inverting analog signal Input. With a 2.0V reference voltage the ground-referenced input signal level is 2.0 V_{P-P} centered on V_{CM}. This pin may be connected to V_{CM} for single-ended operation, but a differential input signal is required for best performance.
1	V_{REF}		Reference input. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. V_{REF} is 2.0V nominal and should be between 1.0V to 2.4V.
31	V_{RP}		These pins are high impedance reference bypass pins. Connect a 0.1 µF capacitor from each of these pins to AGND. DO NOT LOAD these pins.
32	V_{RM}		
30	V_{RN}		
DIGITAL I/O			
10	CLK		Digital clock input. The range of frequencies for this input is 100 kHz to 15 MHz (typical) with ensured performance at 10 MHz. The input is sampled on the rising edge of this input.
11	$\overline{OE}$		$\overline{OE}$ is the output enable pin that, when low, enables the TRI-STATE™ data output pins. When this pin is high, the outputs are in a high impedance state.
8	PD		PD is the Power Down input pin. When high, this input puts the converter into the power down mode. When this pin is low, the converter is in the active mode.

Pin No.	Symbol	Equivalent Circuit	Description
14–19, 22–27	D0–D11		Digital data output pins that make up the 12-bit conversion results. D0 is the LSB, while D11 is the MSB of the offset binary output word. Output levels are TTL/CMOS compatible.
ANALOG POWER			
5, 6, 29	V_A		Positive analog supply pins. These pins should be connected to a quiet +5V voltage source and be bypassed to AGND with 0.1 µF monolithic capacitors located within 1 cm of these power pins, and with a 10 µF capacitor.
4, 7, 28	AGND		The ground return for the analog supply.
DIGITAL POWER			
13	V_D		Positive digital supply pin. This pin should be connected to the same quiet +5V source as is V_A and bypassed to DGND with a 0.1 µF monolithic capacitor in parallel with a 10 µF capacitor, both located within 1 cm of the power pin.
9, 12	DGND		The ground return for the digital supply.
21	V_{DR}		Positive digital supply pin for the ADC12010's output drivers. This pin should be connected to a voltage source of +2.35V to +5V and be bypassed to DR GND with a 0.1 µF monolithic capacitor. If the supply for this pin is different from the supply used for V_A and V_D, it should also be bypassed with a 10 µF tantalum capacitor. V_{DR} should never exceed the voltage on V_D. All bypass capacitors should be located within 1 cm of the supply pin.
20	DR GND		The ground return for the digital supply for the ADC12010's output drivers. This pin should be connected to the system digital ground, but not be connected in close proximity to the ADC12010's DGND or AGND pins. See Section 5 (Layout and Grounding) for more details.

ABSOLUTE MAXIMUM RATINGS (1) (2)

V_A, V_D	6.5V
V_{DR}	≤V_D +0.3V
$\|V_A – V_D\|$	≤ 100 mV
Voltage on Any Input or Output Pin	−0.3V to (V_A or V_D +0.3V)
Input Current at Any Pin (3)	±25 mA
Package Input Current (3)	±50 mA
Package Dissipation at T_A = 25°C	See (4)
ESD Susceptibility	
Human Body Model (5)	2500V
Machine Model (5)	250V
Soldering Temperature, Infrared, 10 sec. (6)	235°C
Storage Temperature	−65°C to +150°C

(1) All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or V_{IN} > V_A), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.
(4) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature, (T_A), and can be calculated using the formula P_DMAX = ($T_J$max - T_A)/θ_{JA}. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
(5) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0Ω.
(6) The 235°C reflow temperature refers to infrared reflow. For Vapor Phase Reflow (VPR), the following Conditions apply: Maintain the temperature at the top of the package body above 183°C for a minimum 60 seconds. The temperature measured on the package body must not exceed 220°C. Only one excursion above 183°C is allowed per reflow cycle.

OPERATING RATINGS (1) (2)

Operating Temperature	−40°C ≤ T_A ≤ +85°C
Supply Voltage (V_A, V_D)	+4.75V to +5.25V
Output Driver Supply (V_{DR})	+2.35V to V_D
V_{REF} Input	1.0V to 2.4V
CLK, PD, $\overline{OE}$	−0.05V to (V_D + 0.05V)
V_{IN} Input	−0V to (V_A − 0.5V)
V_{CM}	1.0V to 4.0V
|AGND–DGND|	≤100mV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.

PACKAGE THERMAL RESISTANCE

Package	θ_{JA}
32-Lead LQFP	79°C / W

CONVERTER ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +5V, V_{DR} = +3.0V, PD = 0V, V_{REF} = +2.0V, f_{CLK} = 10 MHz, t_r = t_f = 3 ns, C_L = 25 pF/pin. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}:** all other limits T_A = T_J = 25°C (1) (2) (3)

Symbol	Parameter	Conditions		Typical (4)	Limits (4)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				**12**	Bits (min)
INL	Integral Non Linearity (5)			±0.5	**±1.5**	LSB (max)
DNL	Differential Non Linearity			±0.3	**±0.9**	LSB (max)
GE	Gain Error			±0.2	**2.9**	%FS (max)
	Offset Error (V_{IN} = V_{IN}−)			−0.1	**1.75**	%FS (max)
	Under Range Output Code			0	**0**	
	Over Range Output Code			4095	**4095**	
DYNAMIC CONVERTER CHARACTERISTICS						
FPBW	Full Power Bandwidth	0 dBFS Input, Output at −3 dB		100		MHz
SNR	Signal-to-Noise Ratio	f_{IN} = 1 MHz, V_{IN} = −0.5 dBFS		70		dB
		f_{IN} = 4.4 MHz, V_{IN} = −0.5 dBFS		70		dB
		f_{IN} = 10.1 MHz, V_{IN} = −0.5 dBFS		70	**66**	dB (min)
SINAD	Signal-to-Noise and Distortion	f_{IN} = 1 MHz, V_{IN} = −0.5 dBFS		70		dB
		f_{IN} = 4.4 MHz, V_{IN} = −0.5 dBFS		70		dB
		f_{IN} = 10.1 MHz, V_{IN} = −0.5 dBFS		69	**66**	dB (min)
ENOB	Effective Number of Bits	f_{IN} = 1 MHz, V_{IN} = −0.5 dBFS		11.4		dB
		f_{IN} = 4.4 MHz, V_{IN} = −0.5 dBFS		11.4		dB
		f_{IN} = 10.1 MHz, V_{IN} = −0.5 dBFS		11.3	**10.7**	dB (min)
THD	Total Harmonic Distortion	f_{IN} = 1 MHz, V_{IN} = −0.5 dBFS		−88		dB
		f_{IN} = 4.4 MHz, V_{IN} = −0.5 dBFS		−86		dB
		f_{IN} = 10.1 MHz, V_{IN} = −0.5 dBFS		−79	**−74**	dB (min)
SFDR	Spurious Free Dynamic Range	f_{IN} = 1 MHz, V_{IN} = −0.5 dBFS		92		dB
		f_{IN} = 4.4 MHz, V_{IN} = −0.5 dBFS		89		dB
		f_{IN} = 10.1 MHz, V_{IN} = −0.5 dBFS		83	**69**	dB (min)
IMD	Intermodulation Distortion	f_{IN} = 4.7 MHz and 4.9 MHz, each = −7 dBFS		−75		dBFS
REFERENCE AND ANALOG INPUT CHARACTERISTICS						
V_{CM}	Common Mode Input Voltage			V_A / 2		V
C_{IN}	V_{IN} Input Capacitance (each pin to GND)	V_{IN} = 2.5 Vdc + 0.7 V_{rms}	(CLK LOW)	8		pF
			(CLK HIGH)	7		pF
V_{REF}	Reference Voltage (6)			2.00	**1.0**	V (min)
					2.4	V (max)
	Reference Input Resistance			100		MΩ(min)

(1) The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per ABSOLUTE MAXIMUM RATINGS (3). However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is 4.75V, the full-scale input voltage must be ≤4.85V to ensure accurate conversions.

(2) To ensure accuracy, it is required that $|V_A–V_D|$ ≤ 100 mV and separate bypass capacitors are used at each power supply pin.

(3) With the test condition for V_{REF} = +2.0V ($4V_{P-P}$ differential input), the 12-bit LSB is 977 µV.

(4) Typical figures are at T_A = T_J = 25°C, and represent most likely parametric norms. Test limits are specified to TI's AOQL (Average Outgoing Quality Level).

(5) Integral Non Linearity is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive and negative full-scale.

(6) Optimum performance will be obtained by keeping the reference input in the 1.8V to 2.2V range. The LM4051CIM3-ADJ (SOT-23 package) is recommended for this application.

DC AND LOGIC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +5V, V_{DR} = +3.0V, PD = 0V, V_{REF} = +2.0V, f_{CLK} = 10 MHz, t_r = t_f = 3 ns, C_L = 25 pF/pin. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}:** all other limits T_A = T_J = 25°C (1) (2) (3)

Symbol	Parameter	Conditions		Typical (4)	Limits (4)	Units (Limits)
CLK, PD, $\overline{OE}$ DIGITAL INPUT CHARACTERISTICS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_D = 5.25V			**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	V_D = 4.75V			**1.0**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 5.0V		10		µA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0V		−10		µA
C_{IN}	Digital Input Capacitance			5		pF
D0–D11 DIGITAL OUTPUT CHARACTERISTICS						
$V_{OUT(1)}$	Logical "1" Output Voltage	I_{OUT} = −0.5 mA	V_{DR} = 2.5V		**2.3**	V (min)
			V_{DR} = 3V		**2.7**	V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	I_{OUT} = 1.6 mA, V_{DR} = 3V			**0.4**	V (max)
I_{OZ}	TRI-STATE Output Current	V_{OUT} = 2.5V or 5V		100		nA
		V_{OUT} = 0V		−100		nA
$+I_{SC}$	Output Short Circuit Source Current	V_{OUT} = 0V		−20		mA (min)
$-I_{SC}$	Output Short Circuit Sink Current	V_{OUT} = V_{DR}		20		mA (min)
POWER SUPPLY CHARACTERISTICS						
I_A	Analog Supply Current	PD Pin = DGND, V_{REF} = 2.0V PD Pin = V_{DR}		30 2.8	**39**	mA (max) mA
I_D	Digital Supply Current	PD Pin = DGND PD Pin = V_{DR}, f_{CLK} = 0		2 2.2	**2.5**	mA (max) mA
I_{DR}	Digital Output Supply Current	PD Pin = DGND, C_L = 0 pF (5) PD Pin = V_{DR}, f_{CLK} = 0		0 0		mA mA
	Total Power Consumption	PD Pin = DGND, C_L = 0 pF (6) PD Pin = V_{DR}, f_{CLK} = 0		160 25	**207**	mW mW
PSRR1+	Power Supply Rejection Ratio	Rejection of Positive Full-Scale Error with V_A = 4.75V vs. 5.25V		69		dBFS
PSRR1−	Power Supply Rejection Ratio	Rejection of Negative Full-Scale Error with V_A = 4.75V vs. 5.25V		51		dBFS
PSRR2	Power Supply Rejection Ratio	Rejection of Power Supply Noise with 10 MHz, 250 mV_{P-P} riding on V_A		48		dBFS

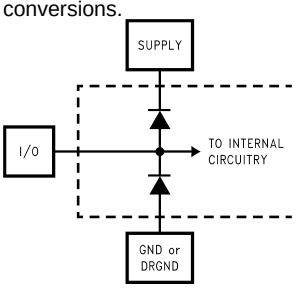
(1) The inputs are protected as shown below. Input voltage magnitudes above V or below GND will not damage this device, provided current is limited per ABSOLUTE MAXIMUM RATINGS (3). However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is 4.75V, the full-scale input voltage must be ≤4.85V to ensure accurate conversions.
(2) To ensure accuracy, it is required that $|V_A–V_D|$ ≤ 100 mV and separate bypass capacitors are used at each power supply pin.
(3) With the test condition for V_{REF} = +2.0V ($4V_{P-PA}$ differential input), the 12-bit LSB is 977 µV.
(4) Typical figures are at T_A = T_J = 25°C, and represent most likely parametric norms. Test limits are specified to TI's AOQL (Average Outgoing Quality Level).
(5) I is the cur$_{DR}$rent consumed by the switching of the output drivers and is primarily determined by load capacitance on the output pins, the supply voltage, V_{DR}, and the rate at which the outputs are switching (which is signal dependent). I_{DR}=V_{DR}(C_0 x f_0 + C_1 x f_1 +....C_{11} x f_{11}) where V_{DR} is the output driver power supply voltage, C_n is total capacitance on the output pin, and f_n is the average frequency at which that pin is toggling.
(6) Excludes I_{DR}. See note 5.

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D = +5V$, $V_{DR} = +3.0V$, PD = 0V, $V_{REF} = +2.0V$, $f_{CLK} = 10$ MHz, $t_r = t_f = 3$ ns, $C_L = 25$ pF/pin. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}:** all other limits $T_A = T_J = 25°C$ (1) (2) (3) (4)

Symbol	Parameter	Conditions	Typical (5)	Limits (5)	Units (Limits)
f_{CLK}[1]	Maximum Clock Frequency		10	**15**	MHz (min)
f_{CLK}[2]	Minimum Clock Frequency		100		kHz
t_{CH}	Clock High Time			**30**	ns (min)
t_{CL}	Clock Low Time			**30**	ns(min)
t_{CONV}	Conversion Latency			**6**	Clock Cycles
t_{OD}	Data Output Delay after Rising CLK Edge	$V_{DR} = 2.5V$	11	**16.8**	ns (max)
		$V_{DR} = 3.0V$	11	**16.8**	ns (max)
t_{AD}	Aperture Delay		1.2		ns
t_{AJ}	Aperture Jitter		2		ps rms
t_{DIS}	Data outputs into TRI-STATE Mode		4		ns
t_{EN}	Data Outputs Active after TRI-STATE		4		ns
t_{PD}	Power Down Mode Exit Cycle	0.1 µF cap on pins 30, 31,32	500		ns

(1) The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per ABSOLUTE MAXIMUM RATINGS (3). However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is 4.75V, the full-scale input voltage must be ≤4.85V to ensure accurate conversions.



(2) To ensure accuracy, it is required that $|V_A – V| \leq 100$ mV and separate bypass capacitors are used at each power supply pin.
(3) With the test condition for $V_{REF} = +2.0V$ ($4V_{P-P}$ differential input), the 12-bit LSB is 977 µV.
(4) Timing specifications are tested at TTL logic levels, $V_{DIL} = 0.4V$ for a falling edge and $V_{IH} = 2.4V$ for a rising edge.
(5) Typical figures are at $T_A = T_J = 25°C$, and represent most likely parametric norms. Test limits are specified to TI's AOQL (Average Outgoing Quality Level).

Specification Definitions

APERTURE DELAY is the time after the rising edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

CLOCK DUTY CYCLE is the ratio of the time during one cycle that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

COMMON MODE VOLTAGE (V_{CM}) is the d.c. potential present at both signal inputs to the ADC.

CONVERSION LATENCY is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It is the difference between the Positive Full Scale Error and the Negative Full Scale Error:

$$\text{Gain Error} = \text{Pos. Full Scale Error} - \text{Neg. Full Scale Error} \quad (1)$$

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dBFS.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC12010 is ensured not to have any missing codes.

NEGATIVE FULL SCALE ERROR is the difference between the actual first code transition and its ideal value of ½ LSB above negative full scale.

OFFSET ERROR is the difference between the two input voltages ($V_{IN}+ - V_{IN}-$) required to cause a transition from code 2047 to 2048.

OUTPUT DELAY is the time delay after the rising edge of the clock before the data update is presented at the output pins.

PIPELINE DELAY (LATENCY) See CONVERSION LATENCY

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. For the ADC12010, PSRR1 is the ratio of the change in Full-Scale Error that results from a change in the dc power supply voltage, expressed in dB. PSRR2 is a measure of how well an a.c. signal riding upon the power supply is rejected at the output.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or dc.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding dc.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dBc, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{f_2^2 + \ldots + f_{10}^2}{f_1^2}} \quad (2)$$

where f_1 is the RMS power of the fundamental (output) frequency and f_2 through f_{10} are the RMS power in the first 9 harmonic frequencies.

Timing Diagram

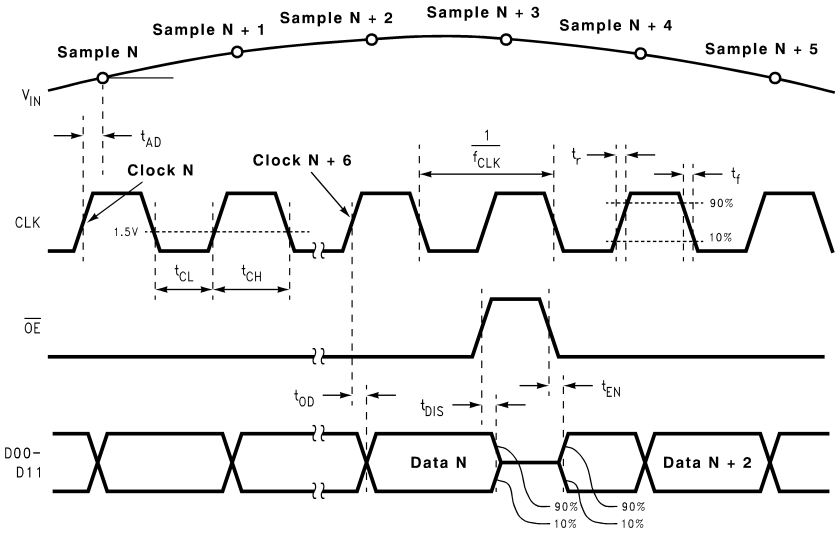


Figure 1. Output Timing

Transfer Characteristic

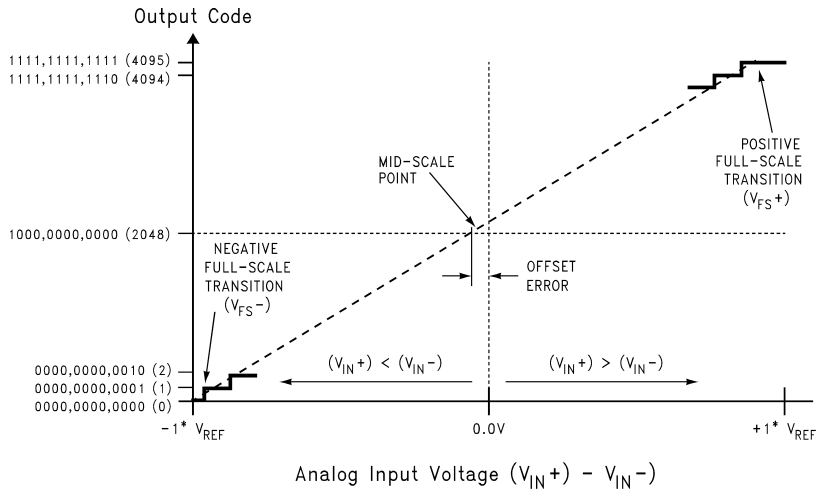


Figure 2. Transfer Characteristic

ADC12010 TYPICAL PERFORMANCE CHARACTERISTICS

$V_A = V_D = 5,0V$, $V_{DR} = 3.0V$, $f_{CLK} = 10$ MHz, $f_{IN} = 10.1$ MHz, $V_{REF} = 2.0V$ unless otherwise stated

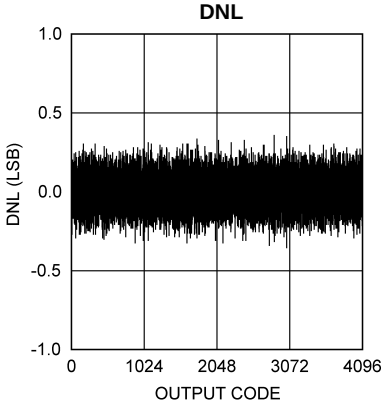


Figure 3.

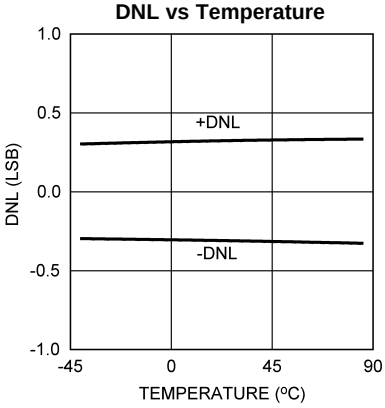


Figure 4.

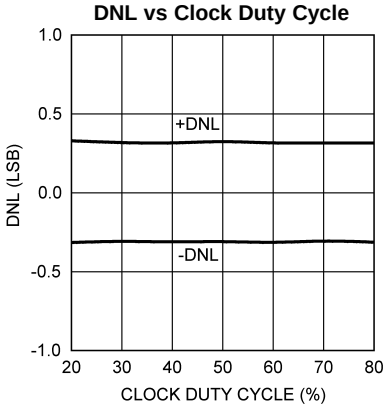


Figure 5.

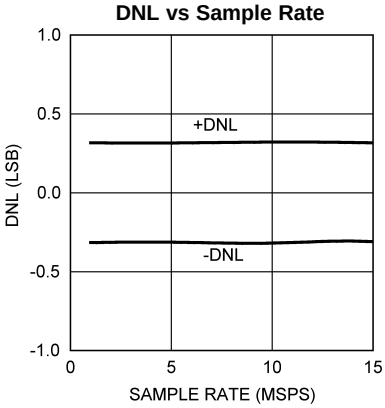


Figure 6.

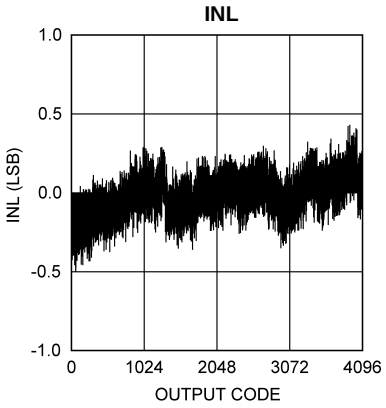


Figure 7.

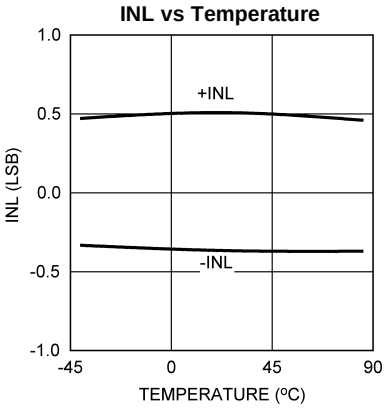


Figure 8.

ADC12010 TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_A = V_D = 5,0V$, $V_{DR} = 3.0V$, $f_{CLK} = 10$ MHz, $f_{IN} = 10.1$ MHz, $V_{REF} = 2.0V$ unless otherwise stated

INL vs Clock Duty Cycle

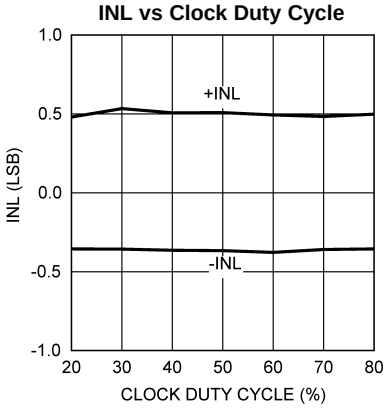


Figure 9.

INL vs Sample Rate

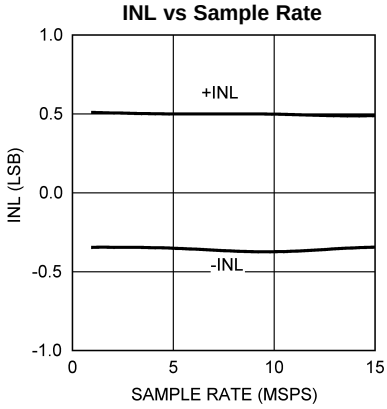


Figure 10.

SNR vs Temperature

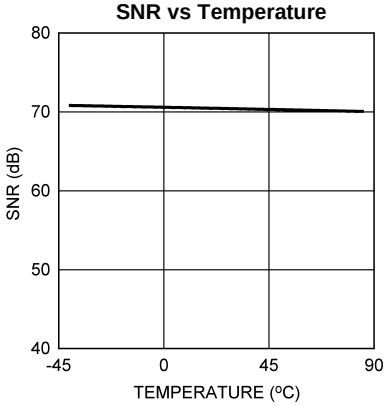


Figure 11.

SNR vs Clock Duty Cycle

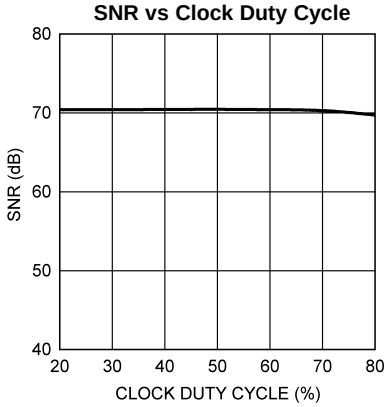


Figure 12.

SNR vs Sample Rate

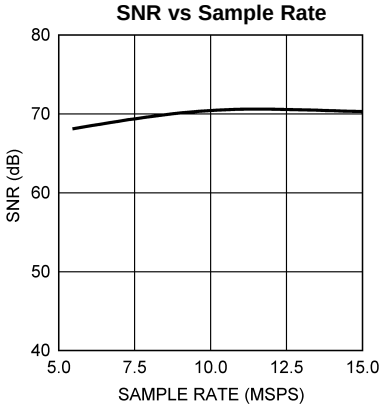


Figure 13.

SNR vs F_{IN}

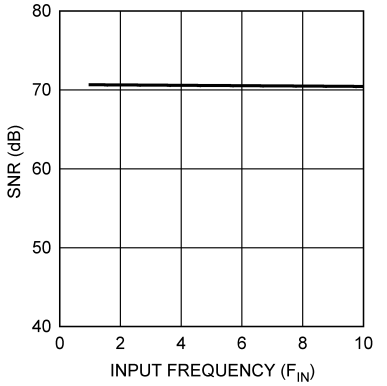


Figure 14.

ADC12010 TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_A = V_D = 5,0V$, $V_{DR} = 3.0V$, $f_{CLK} = 10$ MHz, $f_{IN} = 10.1$ MHz, $V_{REF} = 2.0V$ unless otherwise stated

SNR vs V_{REF}

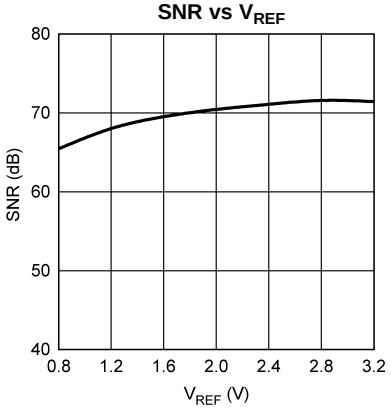


Figure 15.

THD vs Temperature

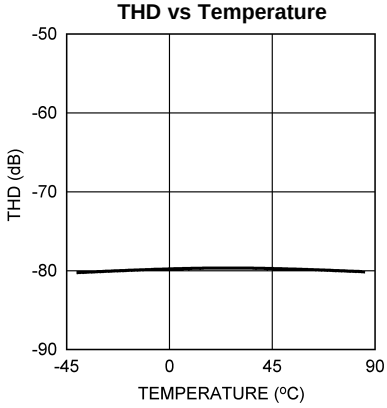


Figure 16.

THD vs Clock Duty Cycle

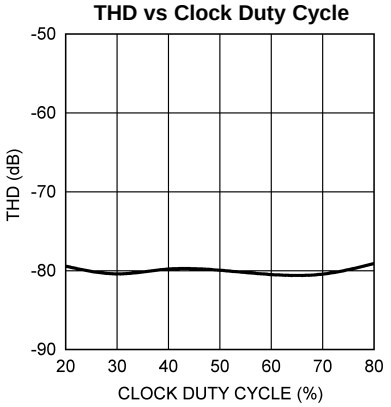


Figure 17.

THD vs Sample Rate

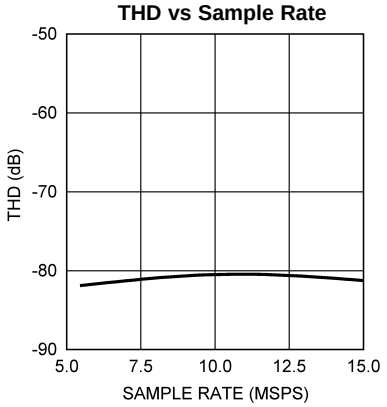


Figure 18.

THD vs F_{IN}

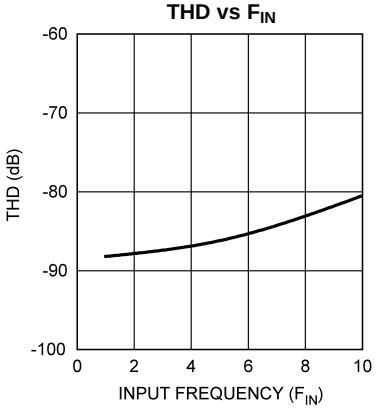


Figure 19.

THD vs V_{REF}

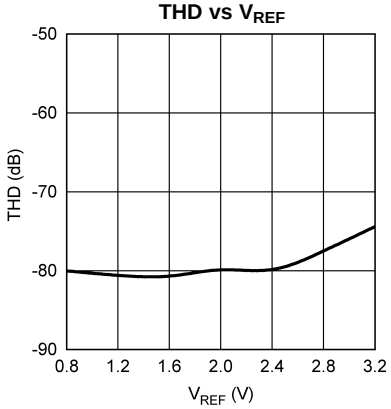


Figure 20.

ADC12010 TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_A = V_D = 5,0V$, $V_{DR} = 3.0V$, $f_{CLK} = 10$ MHz, $f_{IN} = 10.1$ MHz, $V_{REF} = 2.0V$ unless otherwise stated

SINAD vs Temperature

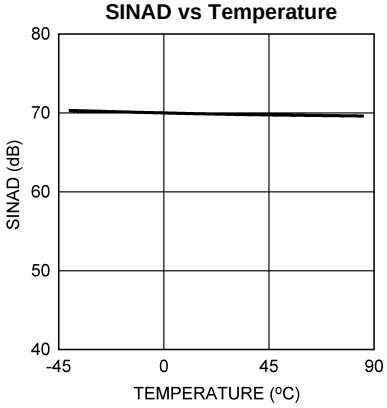


Figure 21.

SINAD vs Clock Duty Cycle

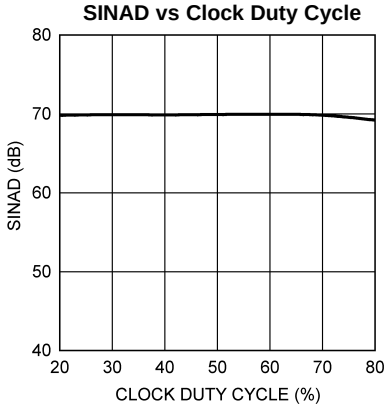


Figure 22.

SINAD vs Sample Rate

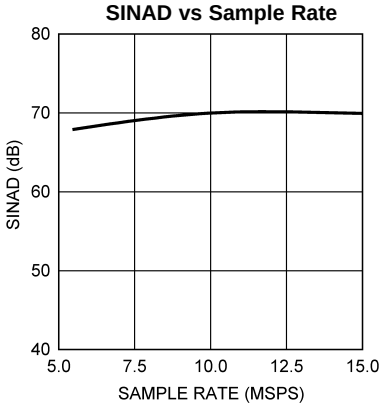


Figure 23.

SINAD vs F_{IN}

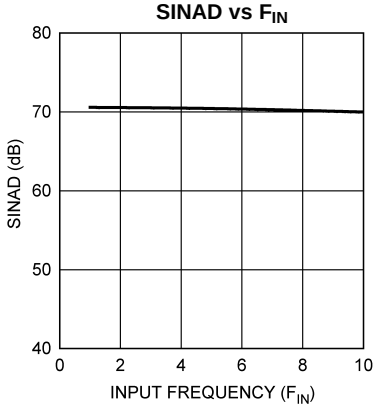


Figure 24.

SINAD vs V_{REF}

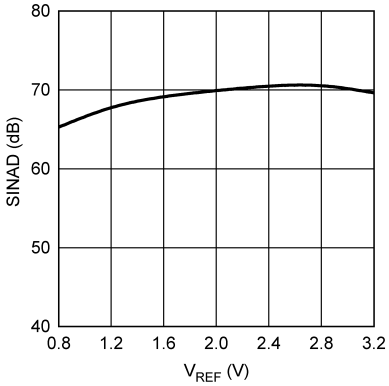


Figure 25.

SFDR vs Temperature

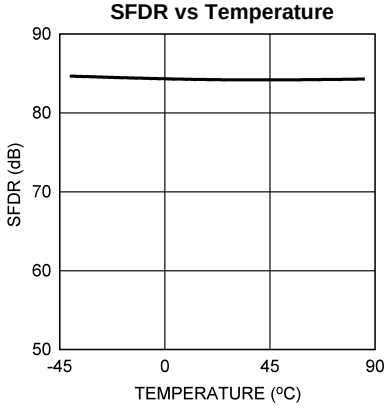


Figure 26.

ADC12010 TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_A = V_D = 5,0V$, $V_{DR} = 3.0V$, $f_{CLK} = 10$ MHz, $f_{IN} = 10.1$ MHz, $V_{REF} = 2.0V$ unless otherwise stated

SFDR vs Clock Duty Cycle

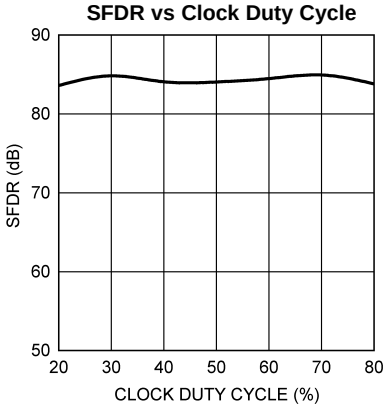


Figure 27.

SFDR vs Sample Rate

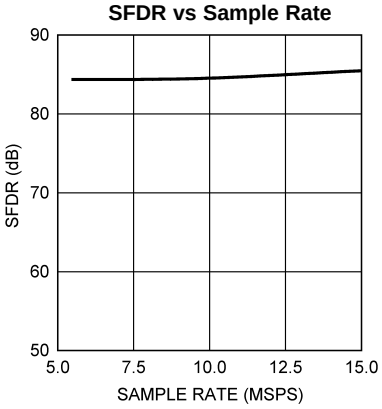


Figure 28.

SFDR vs F_{IN}

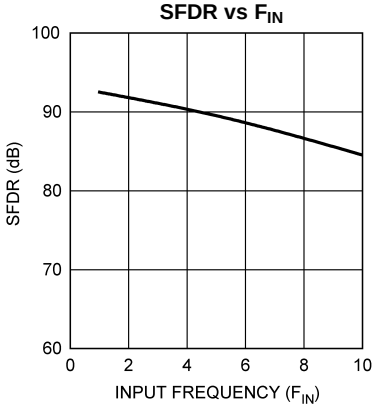


Figure 29.

SFDR vs V_{REF}

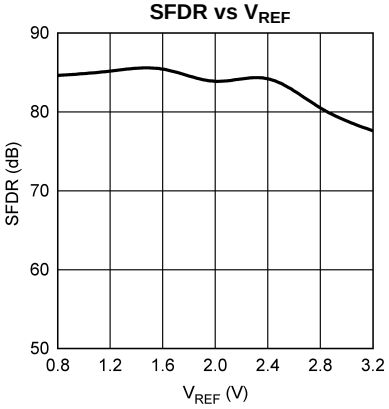


Figure 30.

t_{OD} vs V_{DR}

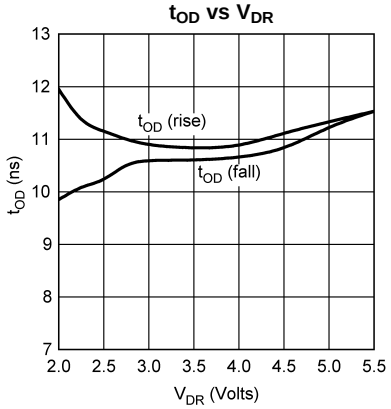


Figure 31.

Spectral Response, 1.1 MHz Input

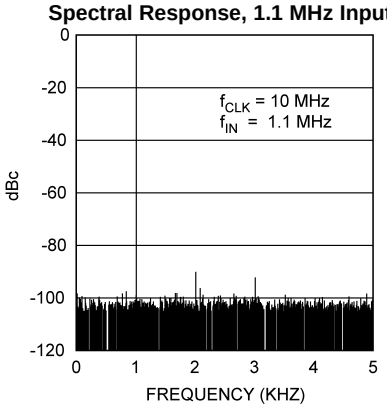


Figure 32.

ADC12010 TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_A = V_D = 5,0V$, $V_{DR} = 3.0V$, $f_{CLK} = 10$ MHz, $f_{IN} = 10.1$ MHz, $V_{REF} = 2.0V$ unless otherwise stated

Spectral Response, 4.4 MHz Input

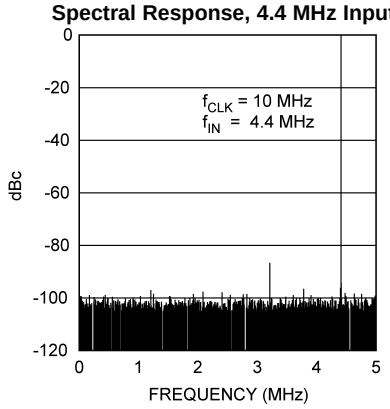


Figure 33.

Spectral Response, 10.1 MHz Input

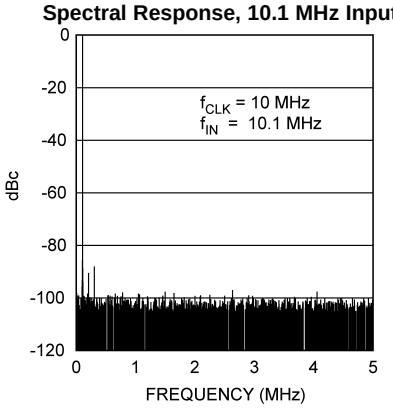


Figure 34.

Functional Description

Operating on a single +5V supply, the ADC12010 uses a pipeline architecture with error correction circuitry to help ensure maximum performance. The differential analog input signal is digitized to 12 bits.

The reference input is buffered to ease the task of driving that pin. The output word rate is the same as the clock frequency. The analog input voltage is acquired at the rising edge of the clock and the digital data for a given sample is delayed by the pipeline for 6 clock cycles.

A logic high on the power down (PD) pin reduces the converter power consumption to 40 mW.

APPLICATION INFORMATION

OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC12010:

- $4.75V \le V_A \le 5.25V$
- $V_D = V_A$
- $2.35V \le V_{DR} \le V_D$
- $100\ kHz \le f_{CLK} \le 15\ MHz$
- $1.0V \le V_{REF} \le 2.4V$
- $1.0V \le V_{CM} \le 4.0V$

Analog Inputs

The ADC12010 has two analog signal inputs, $V_{IN}+$ and $V_{IN}-$. These two pins form a differential input pair. There is one reference input pin, V_{REF}.

Reference Pins

The ADC12010 is designed to operate with a 2.0V reference, but performs well with reference voltages in the range of 1.0V to 2.4V. Lower reference voltages will decrease the signal-to-noise ratio (SNR). Increasing the reference voltage (and the input signal swing) beyond 2.4V will degrade THD for a full-scale input.

It is important that all grounds associated with the reference voltage and the input signal make connection to the ground plane at a single point to minimize the effects of noise currents in the ground path.

The three Reference Bypass Pins (V_{RP}, V_{RM} and V_{RN}) are made available for bypass purposes. These pins should each be bypassed to ground with a 0.1 µF capacitor. Smaller capacitor values will allow faster recovery from the power down mode, but may result in degraded noise performance. DO NOT LOAD these pins.

Signal Inputs

The signal inputs are $V_{IN}+$ and $V_{IN}-$. The input signal, V_{IN}, is defined as

$$V_{IN} = (V_{IN}+) - (V_{IN}-) \quad (3)$$

Figure 35 shows the expected input signal range.

Note that the common mode input voltage range is 1V to 3V with a nominal value of $V_A/2$. The input signals should remain between ground and 4V.

The Peaks of the individual input signals ($V_{IN}+$ and $V_{IN}-$) should each never exceed the voltage described as

$$V_{IN}+,\ V_{IN}- = V_{REF} + V_{CM} \quad (4)$$

to maintain THD and SINAD performance.

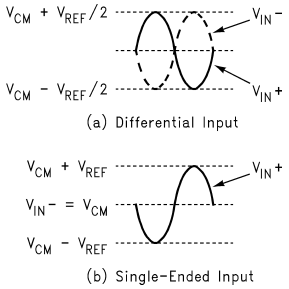


Figure 35. Expected Input Signal Range

The ADC12010 performs best with a differential input with each input centered around V_{CM}. The peak-to-peak voltage swing at both $V_{IN}+$ and $V_{IN}-$ each should not exceed the value of the reference voltage or the output data will be clipped. The two input signals should be exactly 180° out of phase from each other and of the same amplitude. For single frequency inputs, angular errors result in a reduction of the effective full scale input. For a complex waveform, however, angular errors will result in distortion.

For angular deviations of up to 10 degrees from these two signals being 180 out of phase, the full scale error in LSB can be described as approximately

$$E_{FS} = 4096 (1 - \sin (90° + dev)) \quad (5)$$

Where dev is the angular difference, in degrees, between the two signals having a 180° relative phase relationship to each other (see Figure 36). Drive the analog inputs with a source impedance less than 100Ω.

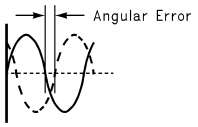


Figure 36. Angular Errors Between the Two Input Signals Will Reduce the Output Level

For differential operation, each analog input signal should have a peak-to-peak voltage equal to the input reference voltage, V_{REF}, and be centered around a common mode voltage, V_{CM}.

Table 1. Input to Output Relationship–Differential Input

V_{IN}+	V_{IN}−	Output
$V_{CM} - V_{REF}/2$	$V_{CM} + V_{REF}/2$	0000 0000 0000
$V_{CM} - V_{REF}/4$	$V_{CM} + V_{REF}/4$	0100 0000 0000
V_{CM}	V_{CM}	1000 0000 0000
$V_{CM} + V_{REF}/4$	$V_{CM} - V_{REF}/4$	1100 0000 0000
$V_{CM} + V_{REF}/2$	$V_{CM} - V_{REF}/2$	1111 1111 1111

Table 2. Input to Output Relationship–Single-Ended Input

V_{IN}^{+}	V_{IN}^{-}	Output
$V_{CM} - V_{REF}$	V_{CM}	0000 0000 0000
$V_{CM} - V_{REF}/2$	V_{CM}	0100 0000 0000
V_{CM}	V_{CM}	1000 0000 0000
$V_{CM} + V_{REF}/2$	V_{CM}	1100 0000 0000
$V_{CM} + V_{REF}$	V_{CM}	1111 1111 1111

Single-Ended Operation

Single-ended performance is lower than with differential input signals. For this reason, single-ended operation is not recommended. However, if single ended-operation is required, and the resulting performance degradation is acceptable, one of the analog inputs should be connected to the d.c. common mode voltage of the driven input. The peak-to-peak differential input signal should be twice the reference voltage to maximize SNR and SINAD performance (Figure 35b). For example, set V_{REF} to 1.0V, bias V_{IN}− to 1.0V and drive V_{IN}+ with a signal range of 0V to 2.0V.

Because very large input signal swings can degrade distortion performance, better performance with a single-ended input can be obtained by reducing the reference voltage when maintaining a full-range output. Table 1 and Table 2 indicate the input to output relationship of the ADC12010.

Driving the Analog Input

The V_{IN}+ and the V_{IN}− inputs of the ADC12010 consist of an analog switch followed by a switched-capacitor amplifier. The capacitance seen at the analog input pins changes with the clock level, appearing as 8 pF when the clock is low, and 7 pF when the clock is high. Although this difference is small, a dynamic capacitance is more difficult to drive than is a fixed capacitance, so choose the driving amplifier carefully. The LMH6550, the LMH6702 and the LMH6628 are good amplifiers for driving the ADC12010.

The internal switching action at the analog inputs causes energy to be output from the input pins. As the driving source tries to compensate for this, it adds noise to the signal. To prevent this, use an RC at each of the inputs, as shown in Figure 38 and Figure 39. These components should be placed close to the ADC because the input pins of the ADC is the most sensitive part of the system and this is the last opportunity to filter the input. The capacitors should be eliminated for undersampling applications.

The LMH6550 and the LMH6552 are excellent devices for driving the ADC12010, especially when single-ended to differential conversion with d.c. coupling is necessary. An example of the use of the LMH6550 to drive the analog input of the ADC12010 is shown in Figure 38.

For high frequency, narrow band applications, a transformer is generally the recommended way to drive the analog inputs, as shown in Figure 39.

Input Common Mode Voltage

The input common mode voltage, V_{CM}, should be in the range of 0.5V to 4.0V and be of a value such that the peak excursions of the analog signal does not go more negative than ground or more positive than 0.5 Volts below the V_A supply voltage. The nominal V_{CM} should generally be equal to $V_{REF}/2$, but V_{RM} can be used as a V_{CM} source as long as V_{CM} need not supply more than 10 µA of current. Figure 38 shows the use of the V_{RM} output to drive the V_{CM} input of the LMH6550. The common mode output voltage of the LMH6550 is equal to the V_{CM} input input voltage.

DIGITAL INPUTS

The digital TTL/CMOS compatible inputs consist of CLK, $\overline{OE}$ and PD.

CLK

The **CLK** signal controls the timing of the sampling process. Drive the clock input with a stable, low jitter clock signal in the range of 100 kHz to 15 MHz with rise and fall times of less than 3ns. The trace carrying the clock signal should be as short as possible and should not cross any other signal line, analog or digital, not even at 90°.

If the **CLK** is interrupted, or its frequency too low, the charge on internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This is what limits the lowest sample rate to 100 ksps.

The duty cycle of the clock signal can affect the performance of the A/D Converter. Because achieving a precise duty cycle is difficult, the ADC12010 is designed to maintain performance over a range of duty cycles. While it is specified and performance is ensured with a 50% clock duty cycle, performance is typically maintained over a clock duty cycle range of 30% to 70%.

The clock line should be terminated at its source in the characteristic impedance of that line. It is highly desirable that the the source driving the ADC **CLK** pin only drive that pin. However, if that source is used to drive other things, each driven pin should be a.c. terminated with a series RC to ground, as shown in Figure 37, such that the resistor value is equal to the characteristic impedance of the clock line and the capacitor value is

$$C \geq \frac{4 \times t_{PR} \times L}{Z_0} \tag{6}$$

where t_{PR} is the signal propagation rate down the clock line, "L" is the line length and Z_O is the characteristic impedance of the clock line. This termination should be as close as possible to the ADC clock pin but beyond it as seen from the clock source. Typical t_{PD} is about 150 ps/inch (60 ps/cm) on FR-4 board material. The units of "L" and t_{PD} should be the same (inches or centimeters).

Take care to maintain a constant clock line impedance throughout the length of the line. Refer to Application Note AN-905 (SNLA035) or AN-1113 (SNLA011) for information on setting and determining characteristic impedance.

The $\overline{OE}$ Input

The $\overline{OE}$ pin, when high, puts the output pins into a high impedance state. When this pin is low the outputs are in the active state. The ADC12010 will continue to convert whether this pin is high or low, but the output can not be read while the $\overline{OE}$ pin is high.

The $\overline{OE}$ pin should NOT be used to multiplex devices together to drive a common bus as this will result in excessive capacitance on the data output pins, reducing SNR and SINAD performance of the converter. See Section 3.0.

PD

The PD pin, when high, holds the ADC12010 in a power-down mode to conserve power when the converter is not being used. The power consumption in this state is 25 mW with a 10 Mhz clock and the output data pins are undefined in this mode. The data in the pipeline is corrupted while in the power down mode.

The Power Down Mode Exit Cycle time is determined by the value of the capacitors on pins 30, 31 and 32. These capacitors loose their charge in the Power Down mode and must be charged by on-chip circuitry before conversions can be accurate.

DATA OUTPUTS

The ADC12010 has 12 TTL/CMOS compatible Data Output pins. Valid offset binary data is present at these outputs while the $\overline{OE}$ and PD pins are low. While the t_{OD} time provides information about output timing, a simple way to capture a valid output is to latch the data on the falling edge of the conversion clock (pin 10).

Be very careful when driving a high capacitance bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_{DR} and DR GND. These large charging current spikes can cause on-chip noise that can couple into the analog circuitry, degrading dynamic performance. Adequate power supply bypassing and careful attention to the ground plane will reduce this problem. Additionally, bus capacitance beyond that specified will cause t_{OD} to increase, making it difficult to properly latch the ADC output data. The result could be an apparent reduction in dynamic performance.

To minimize noise due to output switching, minimize the load currents at the digital outputs. This can be done by connecting buffers (74AC541, for example) between the ADC outputs and any other circuitry. Only one driven input should be connected to each output pin. Additionally, inserting series 100Ω resistors at the digital outputs, close to the ADC pins, will isolate the outputs from trace and other circuit capacitances and limit the output currents, which could otherwise result in performance degradation. See Figure 37.

While the ADC12010 will operate with V_{DR} voltages down to 1.8V, t_{OD} increases with reduced V_{DR}. Be careful of external timing when using reduced V_{DR}.

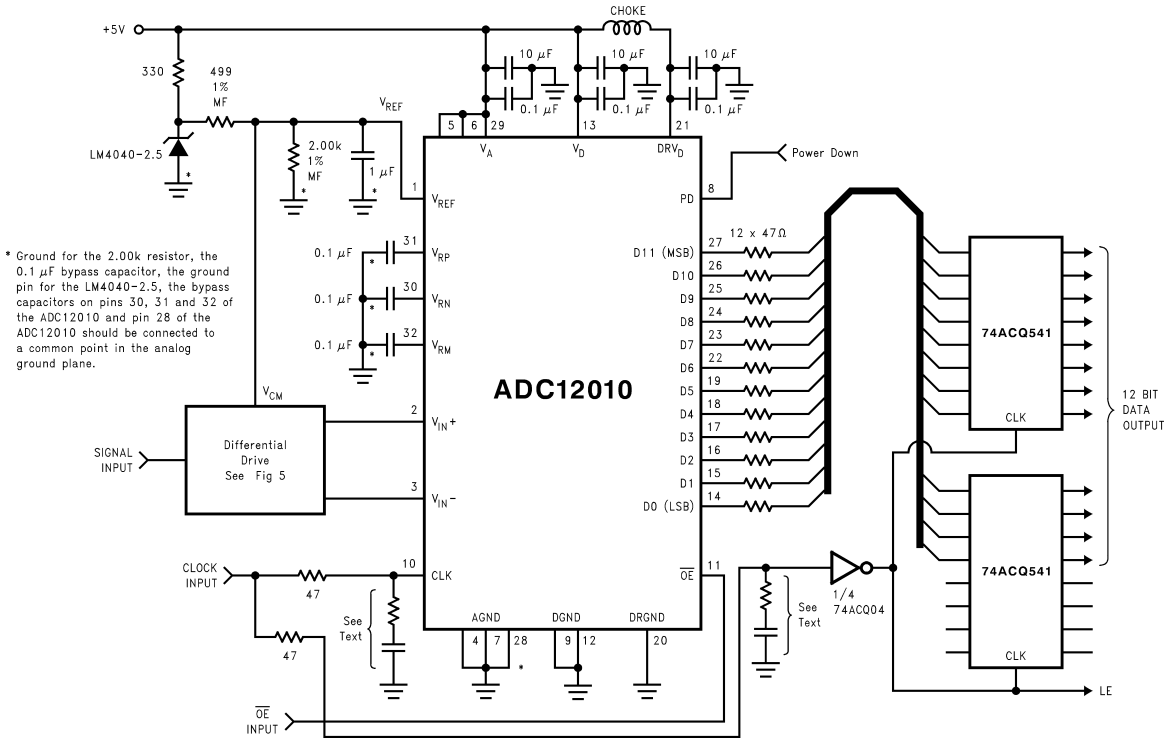


Figure 37. Simple Application Circuit with Single-Ended to Differential Buffer

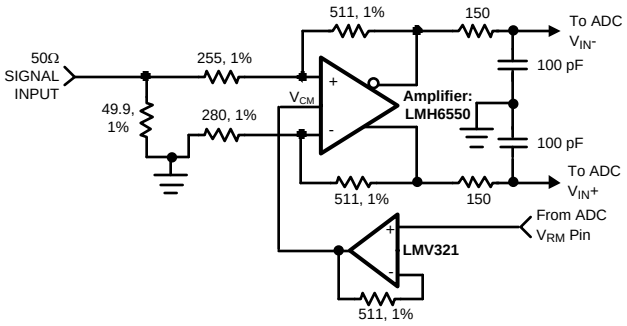


Figure 38. Differential Drive Circuit of Figure 37

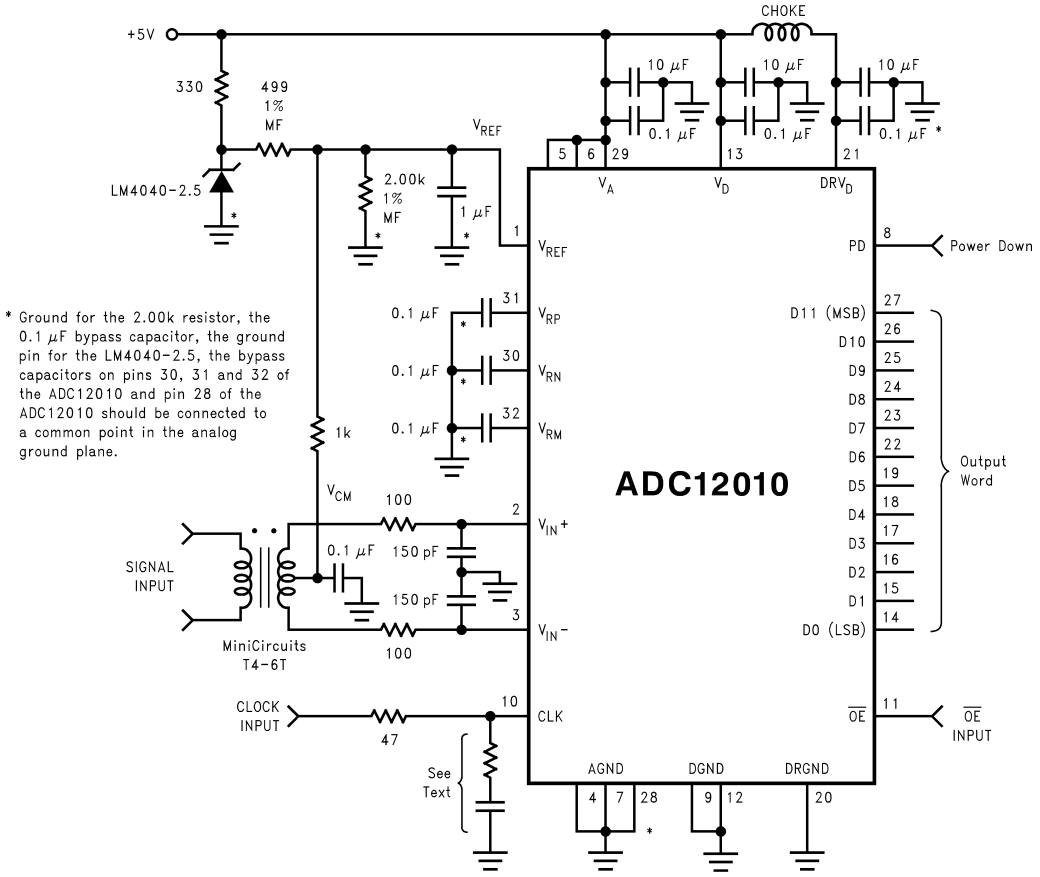


Figure 39. Driving the Signal Inputs with a Transformer

POWER SUPPLY CONSIDERATIONS

The power supply pins should be bypassed with a 10 µF capacitor and with a 0.1 µF ceramic chip capacitor within a centimeter of each power pin. Leadless chip capacitors are preferred because they have low series inductance.

As is the case with all high-speed converters, the ADC12010 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be kept below 100 mV_{P-P}.

No pin should ever have a voltage on it that is in excess of the supply voltages, not even on a transient basis. Be especially careful of this during turn on and turn off of power.

The V_{DR} pin provides power for the output drivers and may be operated from a supply in the range of 2.35V to V_D (nominal 5V). This can simplify interfacing to 3V devices and systems. **DO NOT operate the V_{DR} pin at a voltage higher than V_D.**

LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Maintaining separate analog and digital areas of the board, with the ADC12010 between these areas, is required to achieve specified performance.

The ground return for the data outputs (DR GND) carries the ground current for the output drivers. The output current can exhibit high transients that could add noise to the conversion process. To prevent this from happening, the DR GND pins should NOT be connected to system ground in close proximity to any of the ADC12010's other ground pins.

Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry, and to keep the clock line as short as possible.

Digital circuits create substantial supply and ground current transients. The logic noise thus generated could have significant impact upon system noise performance. The best logic family to use in systems with A/D converters is one which employs non-saturating transistor designs, or has low noise characteristics, such as the 74LS, 74HC(T) and 74AC(T)Q families. The worst noise generators are logic families that draw the largest supply current transients during clock or signal edges, like the 74F and the 74AC(T) families. In high speed circuits, however, it is often necessary to use these higher speed devices. Best performance requires careful attention to PC board layout and to proper signal integrity techniques.

The effects of the noise generated from the ADC output switching can be minimized through the use of 47Ω to 100Ω resistors in series with each data output line. Locate these resistors as close to the ADC output pins as possible.

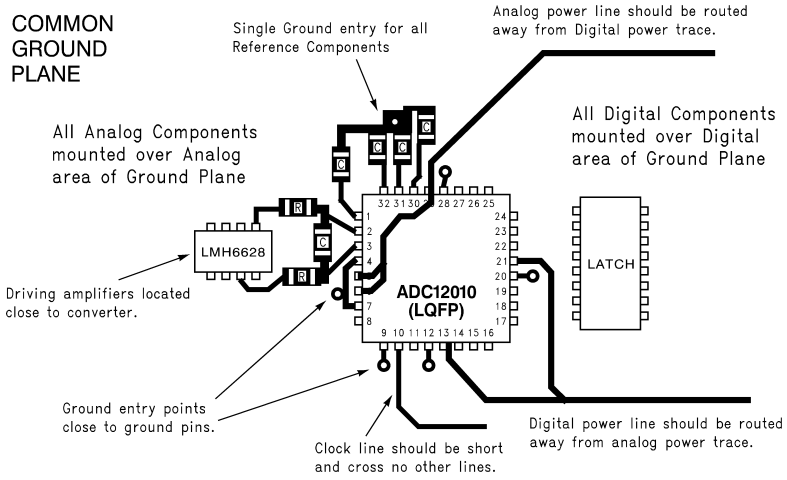


Figure 40. Example of a Suitable Layout

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. To maximize accuracy in high speed, high resolution systems, however, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. Even the generally accepted 90° crossing should be avoided with the clock line as even a little coupling can cause problems at high frequencies. This is because other lines can introduce jitter into the clock line, which can lead to degradation of SNR. Also, the high speed clock can introduce noise into the analog chain.

Best performance at high frequencies and at high resolution is obtained with a straight signal path. That is, the signal path through all components should form a straight line wherever possible.

Be especially careful with the layout of inductors. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors should *not* be placed side by side, even with just a small part of their bodies beside each other.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the analog ground plane.

Figure 40 gives an example of a suitable layout. A single ground plane is recommended with separate analog and digital power planes. The analog and digital power planes should NOT overlap each other. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed over the analog power plane. All digital circuitry and I/O lines should be placed over the digital power plane. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the ground plane at a single point. All ground connections should have a low inductance path to ground..

DYNAMIC PERFORMANCE

To achieve the best dynamic performance, the clock source driving the CLK input must be free of jitter. Isolate the ADC clock from any digital circuitry with buffers, as with the clock tree shown in Figure 41.

As mentioned in LAYOUT AND GROUNDING, it is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal, which can lead to reduced SNR performance, and the clock can introduce noise into other lines. Even lines with 90° crossings have capacitive coupling, so try to avoid even these 90° crossings of the clock line.

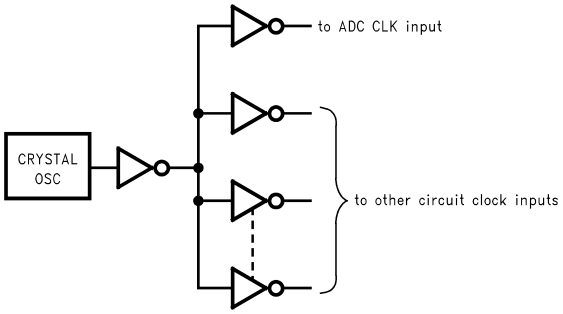


Figure 41. Isolating the ADC Clock from other Circuitry with a Clock Tree

COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 100 mV beyond the supply rails (more than 100 mV below the ground pins or 100 mV above the supply pins). Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital components (e.g., 74F and 74AC devices) to exhibit overshoot or undershoot that goes above the power supply or below ground. A resistor of about 47Ω to 100Ω in series with any offending digital input, close to the signal source, will eliminate the problem.

Do not allow input voltages to exceed the supply voltage, even on a transient basis. Not even during power up or power down.

Be careful not to overdrive the inputs of the ADC12010 with a device that is powered from supplies outside the range of the ADC12010 supply. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_{DR} and DR GND. These large charging current spikes can couple into the analog circuitry, degrading dynamic performance. Adequate bypassing and maintaining separate analog and digital areas on the pc board will reduce this problem.

Additionally, bus capacitance beyond that specified will cause t_{OD} to increase, making it difficult to properly latch the ADC output data. The result could, again, be an apparent reduction in dynamic performance.

The digital data outputs should be buffered (with 74AC541, for example). Dynamic performance can also be improved by adding series resistors at each digital output, close to the ADC12010, which reduces the energy coupled back into the converter output pins by limiting the output current. A reasonable value for these resistors is 100Ω.

Using an inadequate amplifier to drive the analog input. As explained in Signal Inputs, the capacitance seen at the input alternates between 8 pF and 7 pF, depending upon the phase of the clock. This dynamic load is more difficult to drive than is a fixed capacitance.

If the amplifier exhibits overshoot, ringing, or any evidence of instability, even at a very low level, it will degrade performance. A small series resistor and shunt capacitor at each amplifier output (as shown in Figure 38 and Figure 39) will improve performance. The LMH6550 , the LMH6702 and the LMH6628 have been successfully used to drive the analog inputs of the ADC12010.

Also, it is important that the signals at the two inputs have exactly the same amplitude and be exactly 180º out of phase with each other. Board layout, especially equality of the length of the two traces to the input pins, will affect the effective phase between these two signals. Remember that an operational amplifier operated in the non-inverting configuration will exhibit more time delay than will the same device operating in the inverting configuration.

Operating with the reference pins outside of the specified range. As mentioned in Reference Pins, V_{REF} should be in the range of

$$1.0V \leq V_{REF} \leq 2.4V \quad (7)$$

Operating outside of these limits could lead to performance degradation.

Using a clock source with excessive jitter, using excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR and SINAD performance.

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	25

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC12010CIVY/NOPB	Active	Production	LQFP (NEY) | 32	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC12010 CIVY
ADC12010CIVY/NOPB.A	Active	Production	LQFP (NEY) | 32	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC12010 CIVY
ADC12010CIVYX/NOPB	Active	Production	LQFP (NEY) | 32	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC12010 CIVY
ADC12010CIVYX/NOPB.A	Active	Production	LQFP (NEY) | 32	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC12010 CIVY

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

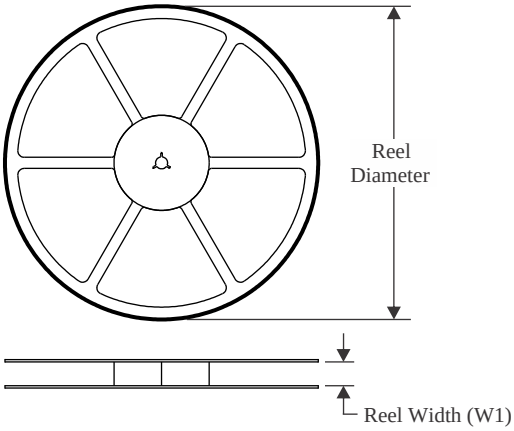
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

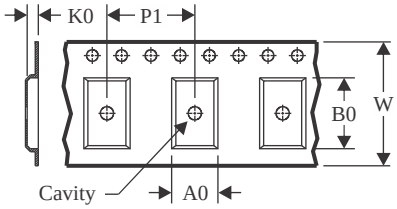
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

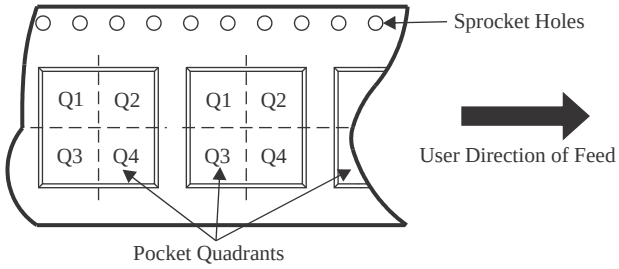


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

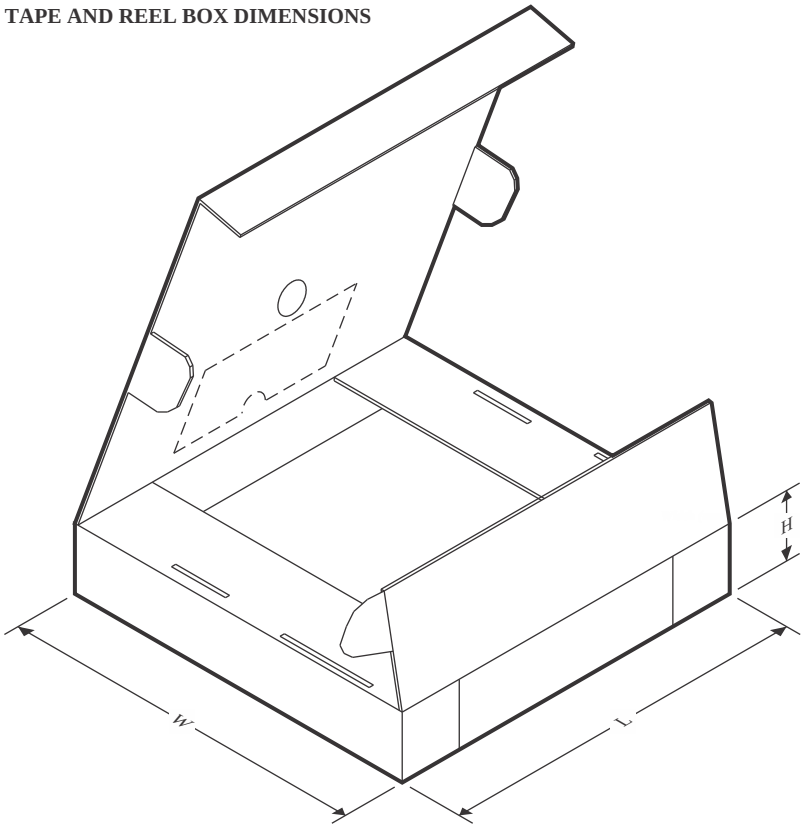
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC12010CIVYX/NOPB	LQFP	NEY	32	1000	330.0	16.4	9.8	9.8	2.0	12.0	16.0	Q2

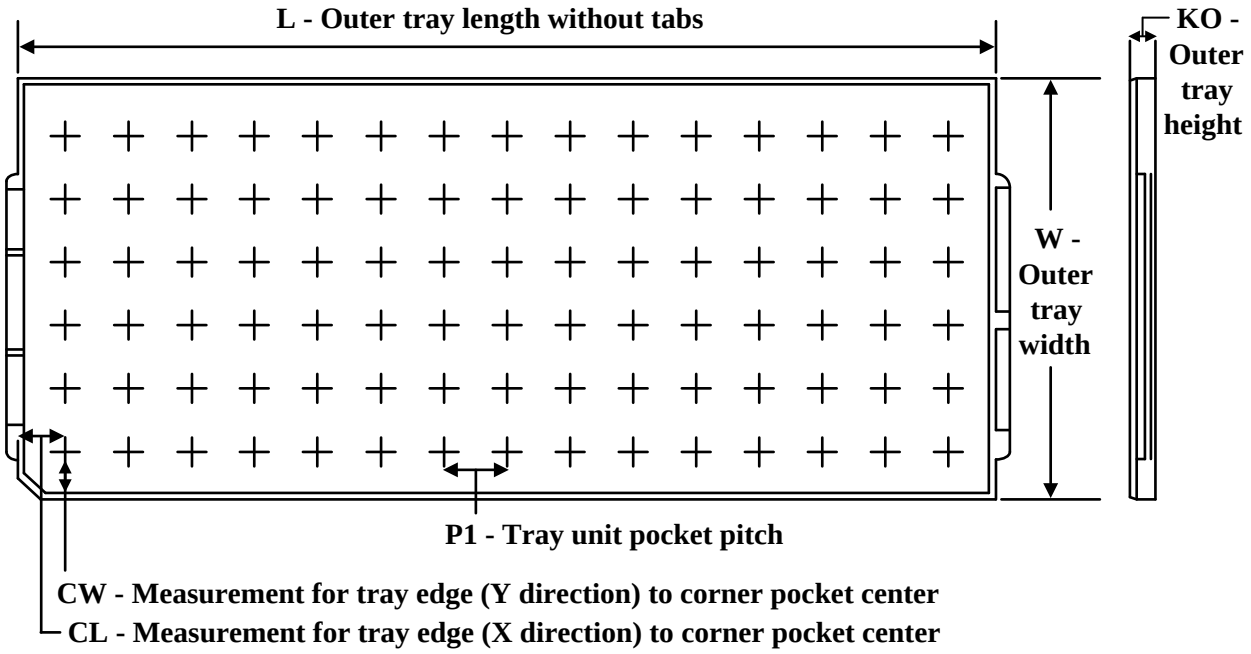
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC12010CIVYX/NOPB	LQFP	NEY	32	1000	356.0	356.0	36.0

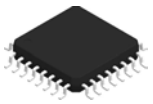
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADC12010CIVY/NOPB	NEY	LQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
ADC12010CIVY/ NOPB.A	NEY	LQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

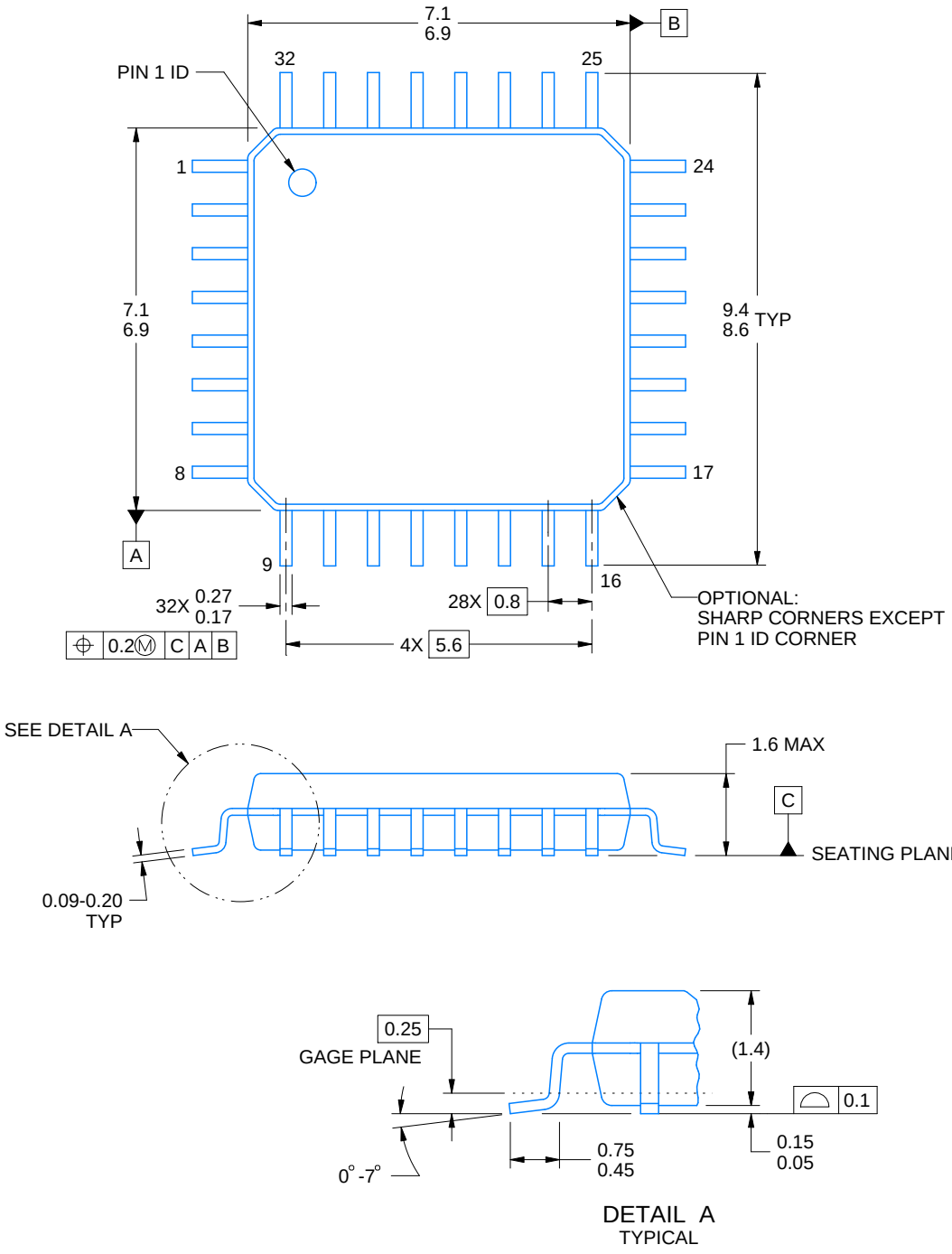


PACKAGE OUTLINE

NEY0032A

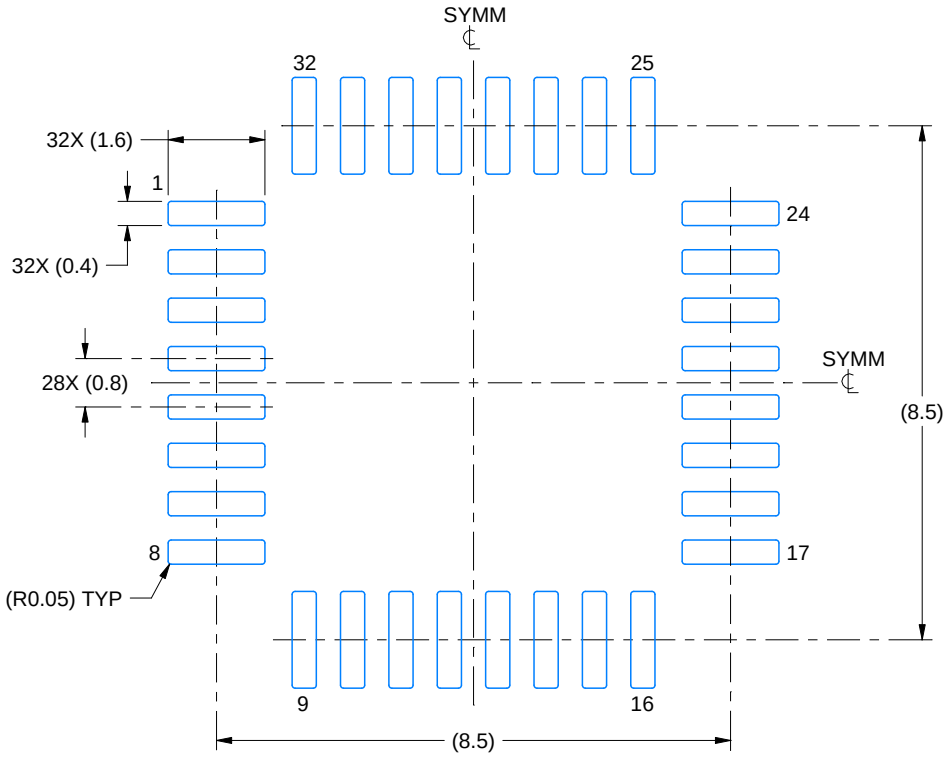
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

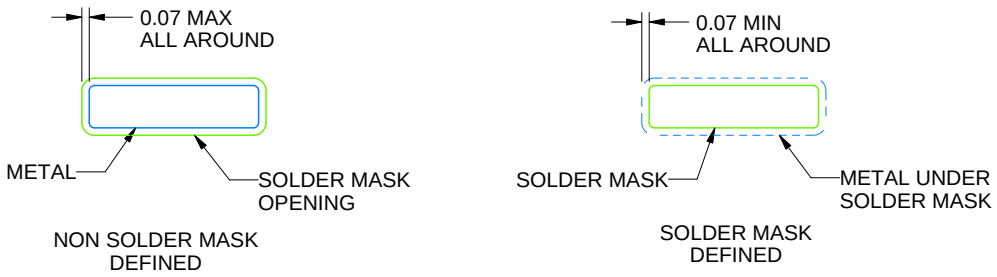


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4219901/A 10/2016

NOTES: (continued)

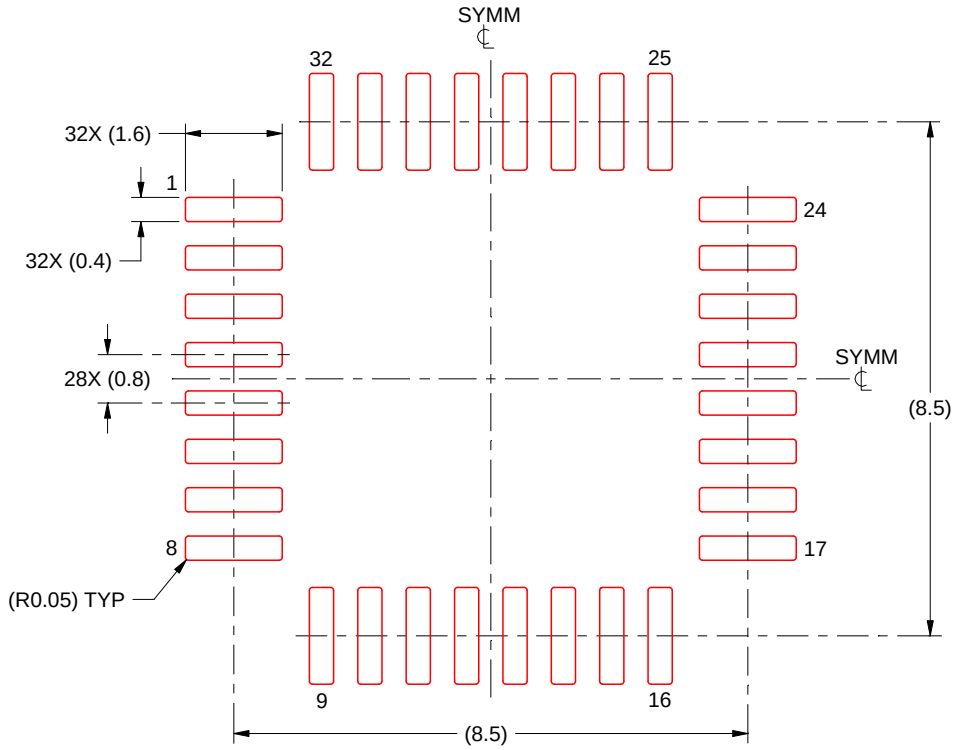
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NEY0032A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
SCALE 8X

4219901/A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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