ADS1118 具有内部基准和温度传感器的兼容 SPI™ 的 16 位模数转换器

1 特性

- 超小型 X2QFN 封装：
  2mm × 1.5mm × 0.4mm
- 宽电源电压范围：2V 至 5.5V
- 低流耗：
  - 连续模式：只有 150μA
  - 单冲模式：汽车断电
- 可编程数据传输速率：
  8SPS 至 860SPS
- 单周期稳定
- 内部低漂移电压基准
- 内部温度传感器：
  在 0°C 至 70°C 范围内误差最大值为 0.5°C
- 内部振荡器
- 内部可编程增益放大器 (PGA)
- 四路单端或两个差分输入

2 应用

- 温度测量：
  - 热电偶测量
  - 冷结点补偿
  - 热敏电阻测量
- 便携式仪表
- 工厂自动化和过程控制

3 说明

ADS1118 是一款精密、低功耗、16 位模数转换器 (ADC)，提供 测量 采用超小型无引线 X2QFN-10 封装或 VSSOP-10 封装的传感器最常见信号所需的所有功能。ADS1118 集成了可编程增益放大器 (PGA)、电压基准、振荡器和高精度温度传感器。这些 功能以及 2V 至 5.5V 的宽电源电压范围，使得 ADS1118 非常适合功率受限和空间受限的传感器测量 应用。

ADS1118 数据转换速率最高可达每秒 860 次采样 (SPS)。PGA 的输入范围为 ±256mV 至 ±6.144V，能够以高分辨率测量大信号和小信号。该器件通过输入多路复用器 (MUX) 测量双路差分输入或四路单端输入。高精度温度传感器用于系统级温度监控或对热电偶进行冷结点补偿。

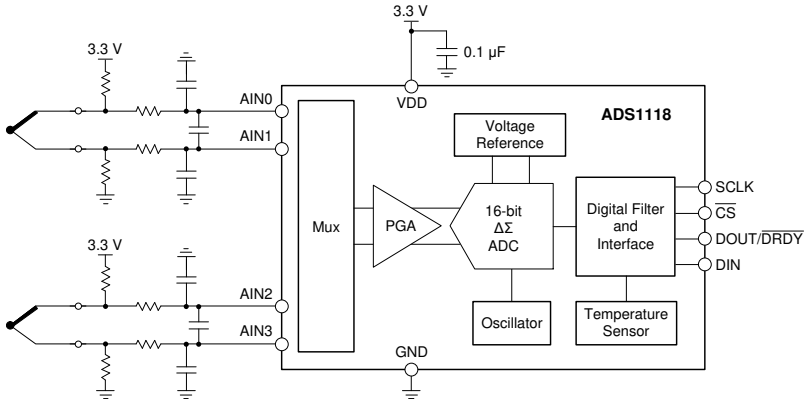
ADS1118 可选择以连续转换模式或单次模式运行。该器件在单次模式下完成一次转换后自动断电。在空闲状态下，单次模式会显著降低流耗。所有数据均通过串行外设接口 (SPI™) 进行传输。ADS1118 的额定工作温度范围为 -40°C 至 +125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ADS1118	X2QFN (10)	1.50mm x 2.00mm
	VSSOP (10)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

K 型热电偶测量
使用集成温度传感器进行冷结点补偿



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (October 2015) to Revision F **Page**

- Changed maximum VDD voltage from 5.5 V to 7 V in the *Absolute Maximum Ratings* table ... 6
- Changed bit description of Config Register bit 0 ... 27

Changes from Revision D (October 2013) to Revision E **Page**

- 已添加 添加了 *ESD 额定值* 表、*特性* *说明* 部分、*噪声性能* 部分、*器件功能模式* 部分、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- 更改了标题、*说明* 部分、*特性* 部分和首页的方框图 ... 1
- Changed title from *Product Family* to *Device Comparison Table* and deleted *Package Designator* column ... 5
- Updated descriptions and changed name of I/O column in *Pin Configurations and Functions* table ... 5
- Changed digital input voltage range and added minimum specification for T_J in *Absolute Maximum Ratings* table ... 6
- Added *Differential input impedance* specification in *Electrical Characteristics* ... 7
- Changed Condition statement in *Timing Requirements: Serial Interface* ... 9
- Moved t_{CSDOD}, t_{DOPD}, and t_{CSDOZ} parameters from *Timing Requirements* to *Switching Characteristics* ... 9
- Moved t_{CSDOD} and t_{CSDOZ} values from MIN column to MAX column. ... 9
- Deleted *Noise vs Input Signal*, *Noise vs Supply Voltage*, and *Noise vs Input Signal* plots ... 10
- Updated *Overview* section and deleted "Gain = 2/3, 1, 2, 4, 8, or 16" from *Functional Block Diagram* ... 17
- Updated *Analog Inputs* section ... 19
- Updated *Full-Scale Range (FSR) and LSB Size* section ... 20
- Updated *Reset and Power Up* section ... 22
- Updated *32-Bit Data Transmission Cycle* section ... 25
- Updated *Register Maps* section ... 26
- Updated *Application Information* section ... 28

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- Updated Figure 48 31
- Deleted *Thermocouple Measurement With Cold Junction Temperature* section, and moved Figure 50 to *Typical Application* section 33

Changes from Revision C (February 2013) to Revision D **Page**

- 已删除 删除了器件图形 1
- Changed bit 1 to NOP0 in Figure 44 26
- Changed NOP bit description in Figure 44: changes bits[2:0] to bits [2:1] and changed NOP to NOP[1:0] 27

Changes from Revision B (August 2012) to Revision C **Page**

- 将文档更改为最新标准 1
- 已更改 更改了“单冲模式”子项目符号（在“低电流消耗” 特性 项目符号中） 1
- 已更改 更改了“内部温度传感器” 特性 项目符号 1
- 已更改 说明 部分中的 VDE 和 CSA 安全相关认证说明 1
- Changed Product Family table 5
- Changed Function column name in Pin Descriptions table 5
- Changed Analog Input, *Full-scale input voltage range* parameter row in *Electrical Characteristics* table 6
- Changed footnotes 1 and 2 in Electrical Characteristics table 6
- Changed conditions for Electrical Characteristics table 7
- Changed System Performance, *Integral nonlinearity* and *Gain Error* test conditions in Electrical Characteristics table 7
- Changed first two Temperature Sensor, *Temperature sensor accuracy* parameter test conditions in Electrical Characteristics table 7
- Changed Power-Supply Requirements, *Supply current* parameter test conditions in *Electrical Characteristics* table 8
- Changed footnote 3 of Timing Requirements: Serial Interface Timing table 9
- Updated Figure 3 10
- Updated Figure 9 10
- Changed title of Figure 11 to Figure 14 10
- Updated Figure 15 and Figure 33 11
- Changed conditions in Figure 21 to Figure 25 12
- Updated Figure 20 13
- Changed comments in Figure 27 to Figure 31 13
- Changed *Overview* section 17
- Updated *Multiplexer* section 18
- Changed *Full-Scale Input* section 20
- Changed *Voltage Reference* section 20
- Changed *Oscillator* section 20
- Added multiplication points to example equations in *Converting from Digital Codes to Temperature* section 21
- Changed *Serial Interface*, *Chip Select*, *Serial Clock*, *Data Input*, and *Data Output and Data Ready* sections 23
- Changed *Data Retrieval* section 24
- Changed *Registers* section 26
- Changed *Aliasing*, *Reset and Power Up*, *Operating Modes*, and *Duty Cycling for Low Power* sections 29
- Updated Figure 50 33

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Changes from Revision A (July 2011) to Revision B **Page**

- Added *(VSSOP)* to titles of Figure 20 to Figure 25 13
- Added Figure 26 to Figure 31..... 14

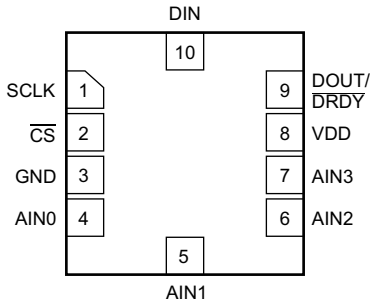
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5 Device Comparison Table

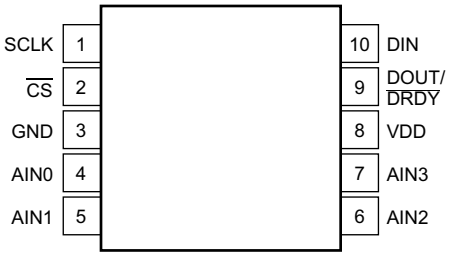
DEVICE	RESOLUTION (Bits)	MAXIMUM SAMPLE RATE (SPS)	INPUT CHANNELS Differential (Single-Ended)	PGA	INTERFACE	SPECIAL FEATURES
ADS1118	16	860	2 (4)	Yes	SPI	Temperature sensor
ADS1018	12	3300	2 (4)	Yes	SPI	Temperature sensor
ADS1115	16	860	2 (4)	Yes	I^2C	Comparator
ADS1114	16	860	1 (1)	Yes	I^2C	Comparator
ADS1113	16	860	1 (1)	No	I^2C	None
ADS1015	12	3300	2 (4)	Yes	I^2C	Comparator
ADS1014	12	3300	1 (1)	Yes	I^2C	Comparator
ADS1013	12	3300	1 (1)	No	I^2C	None

6 Pin Configuration and Functions

RUG Package
10-Pin X2QFN
Top View



DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	SCLK	Digital input	Serial clock input
2	$\overline{CS}$	Digital input	Chip select; active low. Connect to GND if not used.
3	GND	Supply	Ground
4	AIN0	Analog input	Analog input 0. Leave unconnected or tie to VDD if not used.
5	AIN1	Analog input	Analog input 1. Leave unconnected or tie to VDD if not used.
6	AIN2	Analog input	Analog input 2. Leave unconnected or tie to VDD if not used.
7	AIN3	Analog input	Analog input 3. Leave unconnected or tie to VDD if not used.
8	VDD	Supply	Power supply. Connect a 100-nF power supply decoupling capacitor to GND.
9	DOUT/$\overline{DRDY}$	Digital output	Serial data output combined with data ready; active low
10	DIN	Digital input	Serial data input

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7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power-supply voltage	VDD to GND	–0.3	7	V
Analog input voltage	AIN0, AIN1, AIN2, AIN3	GND – 0.3	VDD + 0.3	V
Digital input voltage	DIN, DOUT/$\overline{DRDY}$, SCLK, $\overline{CS}$	GND – 0.3	VDD + 0.3	V
Input current, continuous	Any pin except power supply pins	–10	10	mA
Temperature	Junction, T_J	–40	150	°C
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
VDD	Power supply	VDD to GND	2		5.5	V
ANALOG INPUTS(1)						
FSR	Full-scale input voltage range(2)	$V_{IN} = V_{(AINP)} - V_{(AINN)}$	See Table 3			
$V_{(AINx)}$	Absolute input voltage		GND		VDD	V
DIGITAL INPUTS						
	Input voltage		GND		VDD	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40		125	°C

(1) AINP and AINN denote the selected positive and negative inputs. AINx denotes one of the four available analog inputs.
(2) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V or 5.5 V (whichever is smaller) must be applied to this device.

7.4 Thermal Information

THERMAL METRIC(1)		ADS1118		UNIT
		DGS (VSSOP)	RUG (X2QFN)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	186.8	245.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.5	69.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	108.4	172	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.7	8.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	106.5	170.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

Maximum and minimum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C.
All specifications are at VDD = 3.3 V, data rate = 8 SPS, and full-scale range (FSR) = ±2.048 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Common-mode input impedance	FSR = ±6.144 V(1)		8		MΩ
		FSR = ±4.096 V(1), FSR = ±2.048 V		6		
		FSR = ±1.024 V		3		
		FSR = ±0.512 V, FSR = ±0.256 V		100		
	Differential input impedance	FSR = ±6.144 V(1)		22		MΩ
		FSR = ±4.096 V(1)		15		
		FSR = ±2.048 V		4.9		
		FSR = ±1.024 V		2.4		
		FSR = ±0.512 V, FSR = ±0.256 V		710		kΩ
SYSTEM PERFORMANCE						
	Resolution (No missing codes)			16		Bits
DR	Data rate			8, 16, 32, 64, 128, 250, 475, 860		SPS
	Data rate variation	All data rates	–10%		10%	
	Output noise			See *Noise Performance* section		
INL	Integral nonlinearity	DR = 8 SPS, FSR = ±2.048 V(2)			1	LSB
	Offset error	FSR = ±2.048 V, differential inputs		±0.1	±2	LSB
		FSR = ±2.048 V, single-ended inputs		±0.25		
	Offset drift	FSR = ±2.048 V		0.002		LSB/°C
	Offset power-supply rejection	FSR = ±2.048 V, DC supply variation		0.2		LSB/V
	Offset channel match	Match between any two inputs		0.6		LSB
	Gain error(3)	FSR = ±2.048 V, T_A = 25°C		0.01%	0.15%	
	Gain drift(3)(4)	FSR = ±0.256 V		7		ppm/°C
		FSR = ±2.048 V		5	40	
		FSR = ±6.144 V(1)		5		
	Gain power-supply rejection			10		ppm/V
	Gain match(3)	Match between any two gains		0.01%	0.1%	
	Gain channel match	Match between any two inputs		0.01%	0.1%	
CMRR	Common-mode rejection ratio	At DC, FSR = ±0.256 V		105		dB
		At DC, FSR = ±2.048 V		100		
		At DC, FSR = ±6.144 V(1)		90		
		f_{CM} = 50 Hz, DR = 860 SPS		105		
		f_{CM} = 60 Hz, DR = 860 SPS		105		
TEMPERATURE SENSOR						
	Temperature range		–40		125	°C
	Temperature resolution			0.03125		°C/LSB
	Accuracy	T_A = 0°C to 70°C		0.2	±0.5	°C
		T_A = –40°C to +125°C		0.4	±1	
		vs supply		0.03125	±0.25	°C/V

(1) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V or 5.5 V (whichever is smaller) must be applied to this device.
(2) Best-fit INL; covers 99% of full-scale.
(3) Includes all errors from onboard PGA and voltage reference.
(4) Maximum value specified by characterization.

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Electrical Characteristics (continued)

Maximum and minimum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C.
All specifications are at VDD = 3.3 V, data rate = 8 SPS, and full-scale range (FSR) = ±2.048 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS/OUTPUTS						
V_{IH}	High-level input voltage		0.7 VDD		VDD	V
V_{IL}	Low-level input voltage		GND		0.2 VDD	V
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 VDD			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA	GND		0.2 VDD	V
I_H	Input leakage, high	V_{IH} = 5.5 V	–10		10	µA
I_L	Input leakage, low	V_{IL} = GND	–10		10	µA
POWER SUPPLY						
I_{VDD}	Supply current	Power down, T_A = 25°C		0.5	2	µA
		Power down			5	
		Operating, T_A = 25°C		150	200	
		Operating			300	
P_D	Power dissipation	VDD = 5 V		0.9		mW
		VDD = 3.3 V		0.5		
		VDD = 2 V		0.3		

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7.6 Timing Requirements: Serial Interface

Over operating ambient temperature range and VDD = 2 V to 5.5 V (unless otherwise noted)

		MIN	MAX	UNIT
t_{CSSC}	Delay time, $\overline{CS}$ falling edge to first SCLK rising edge(1)	100		ns
t_{SCCS}	Delay time, final SCLK falling edge to $\overline{CS}$ rising edge	100		ns
t_{CSH}	Pulse duration, $\overline{CS}$ high	200		ns
t_{SCLK}	SCLK period	250		ns
t_{SPWH}	Pulse duration, SCLK high	100		ns
t_{SPWL}	Pulse duration, SCLK low(2)	100		ns
			28	ms
t_{DIST}	Setup time, DIN valid before SCLK falling edge	50		ns
t_{DIHD}	Hold time, DIN valid after SCLK falling edge	50		ns
t_{DOHD}	Hold time, SCLK rising edge to DOUT invalid	0		ns

(1) $\overline{CS}$ can be tied low permanently in case the serial bus is not shared with any other device.
(2) Holding SCLK low longer than 28 ms resets the SPI interface.

7.7 Switching Characteristics: Serial Interface

Over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CSDOD}	Propagation delay time, $\overline{CS}$ falling edge to DOUT driven	DOUT load = 20 pF || 100 kΩ to GND			100	ns
t_{DOPD}	Propagation delay time, SCLK rising edge to valid new DOUT	DOUT load = 20 pF || 100 kΩ to GND	0		50	ns
t_{CSDOZ}	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance	DOUT load = 20 pF || 100 kΩ to GND			100	ns

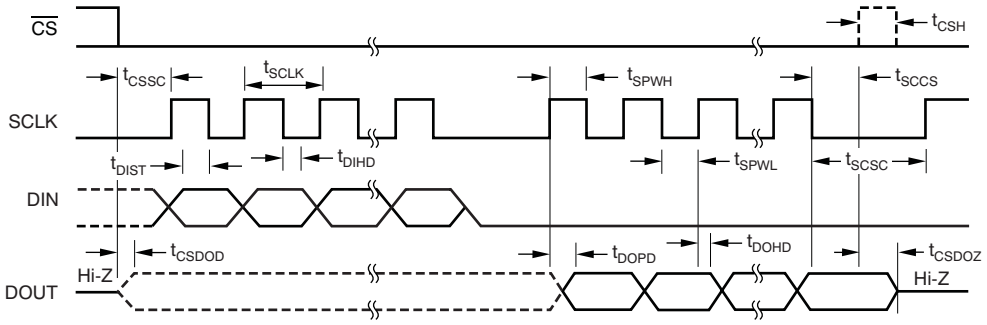
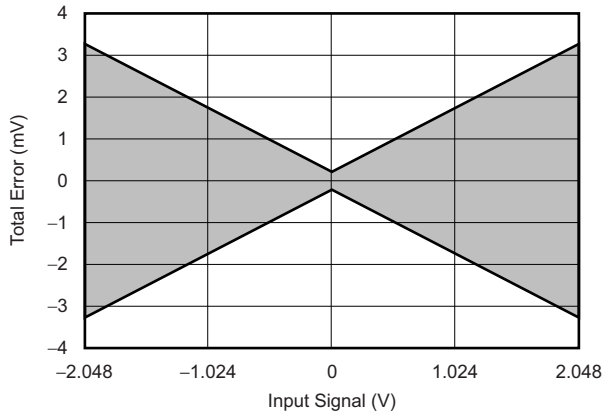


Figure 1. Serial Interface Timing

7.8 Typical Characteristics

At T_A = 25°C, VDD = 3.3 V, FSR = ±2.048 V (unless otherwise noted).



DR = 860 SPS, diff inputs, includes noise, offset and gain error

Figure 2. Total Error vs Input Signal

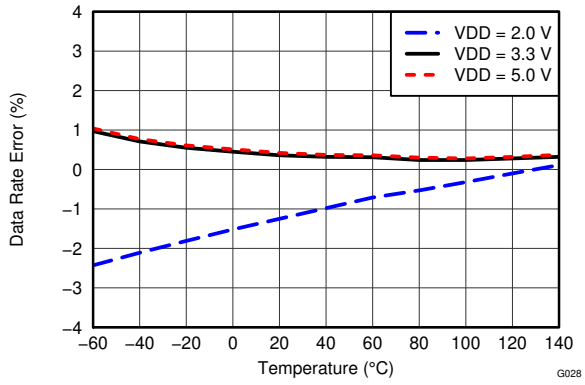


Figure 3. Data Rate vs Temperature

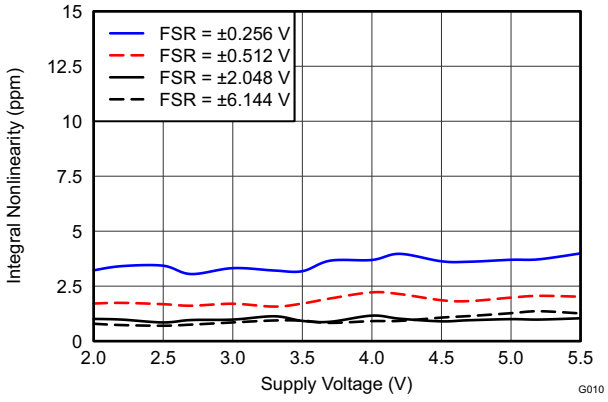
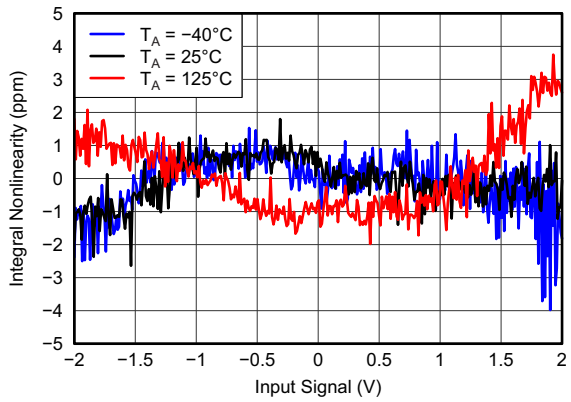
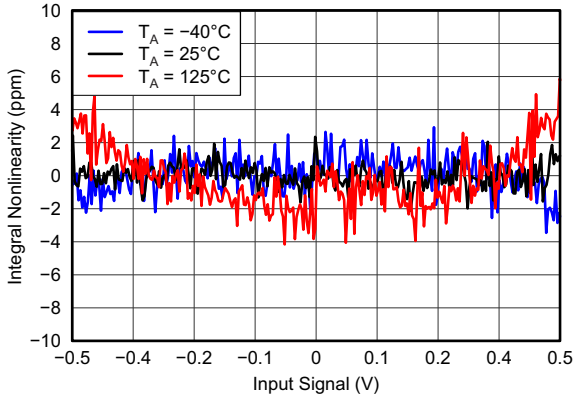


Figure 4. INL vs Supply Voltage



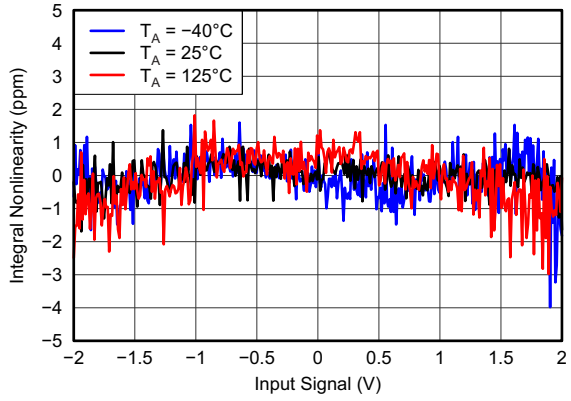
FSR = ±2.048 V, DR = 8 SPS, VDD = 3.3 V, best fit

Figure 5. INL vs Input Signal



FSR = ±0.512 V, DR = 8 SPS, VDD = 3.3 V, best fit

Figure 6. INL vs Input Signal



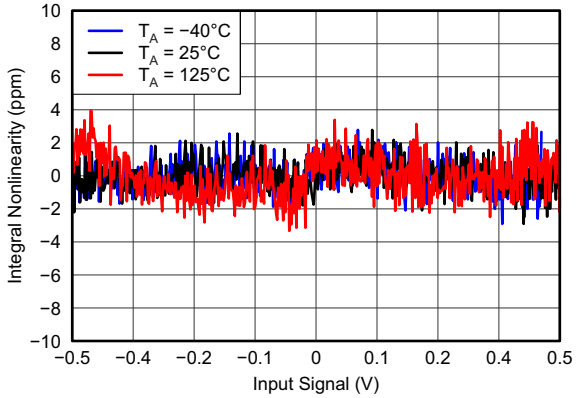
FSR = ±2.048 V, DR = 8 SPS, VDD = 5 V, best fit

Figure 7. INL vs Input Signal

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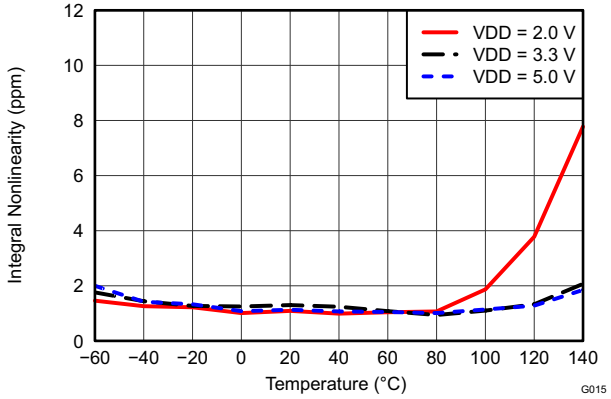
Typical Characteristics (continued)

At T_A = 25°C, VDD = 3.3 V, FSR = ±2.048 V (unless otherwise noted).



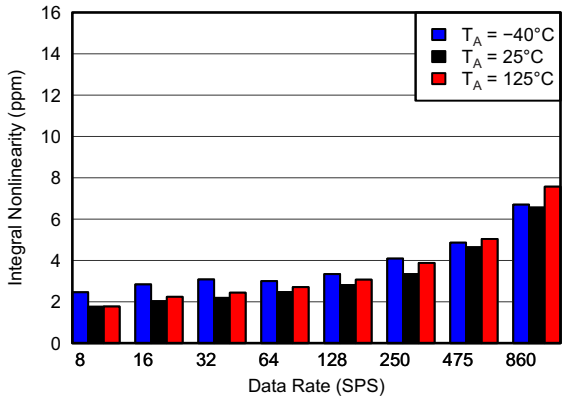
FSR = ±0.512 V, DR = 8 SPS, VDD = 5 V, best fit

Figure 8. INL vs Input Signal



FSR = ±2.048 V, DR = 8 SPS, best fit

Figure 9. INL vs Temperature



FSR = ±2.048 V, best fit

Figure 10. INL vs Data Rate

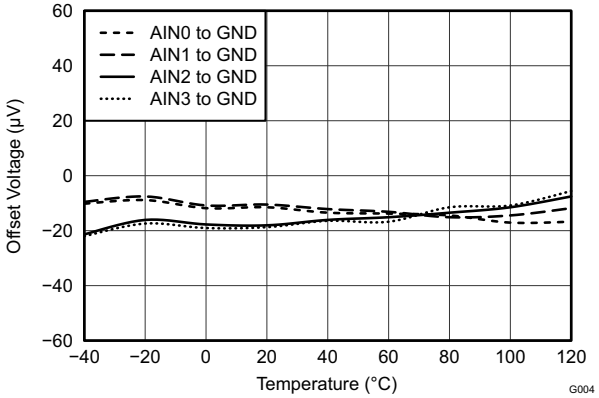


Figure 11. Single-Ended Offset Voltage vs Temperature

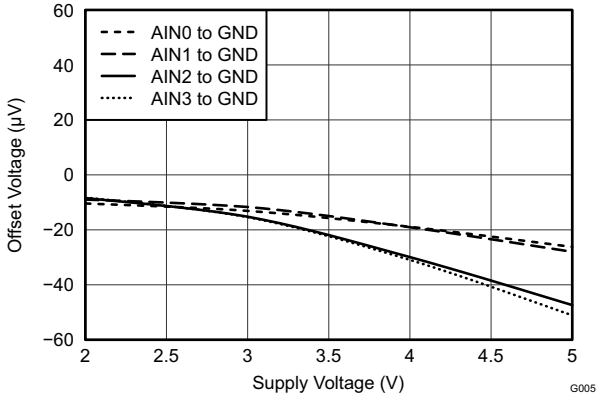


Figure 12. Single-Ended Offset Voltage vs Supply

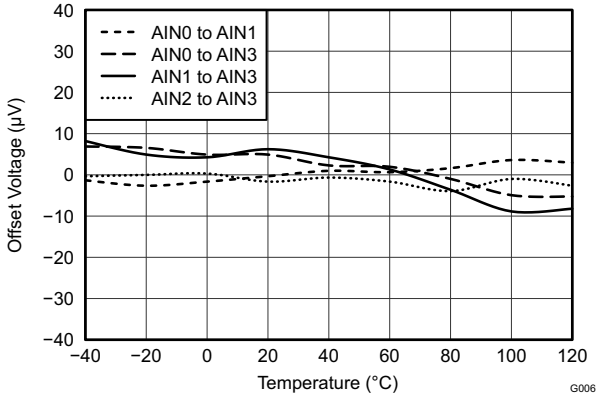


Figure 13. Differential Offset Voltage vs Temperature

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Typical Characteristics (continued)

At T_A = 25°C, VDD = 3.3 V, FSR = ±2.048 V (unless otherwise noted).

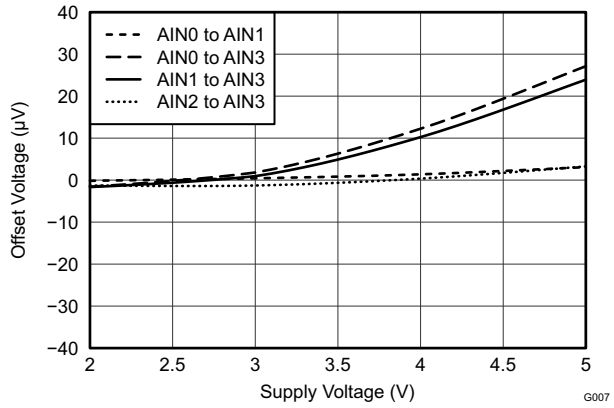
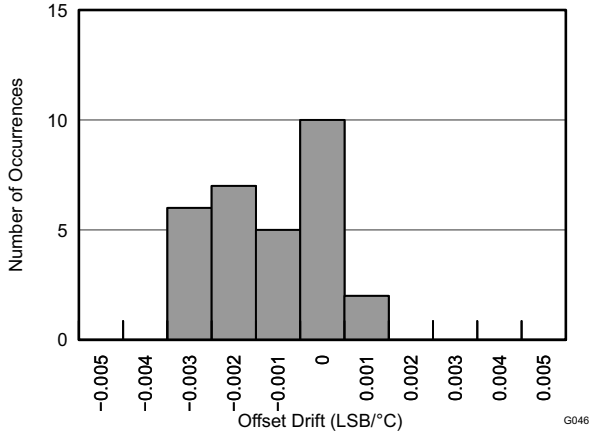
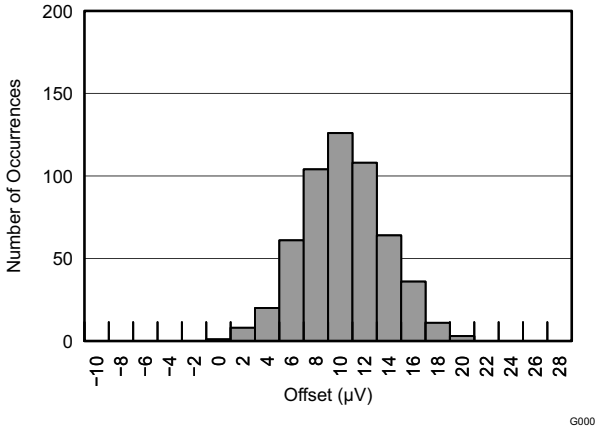


Figure 14. Differential Offset Voltage vs Supply



FSR = ±2.048 V, T_A = –40°C to +125°C, MUX = AIN0 to AIN3,
540 units from 3 production lots

Figure 15. Offset Drift Histogram



FSR = ±2.048 V,
540 units from 3 production lots

Figure 16. Offset Histogram

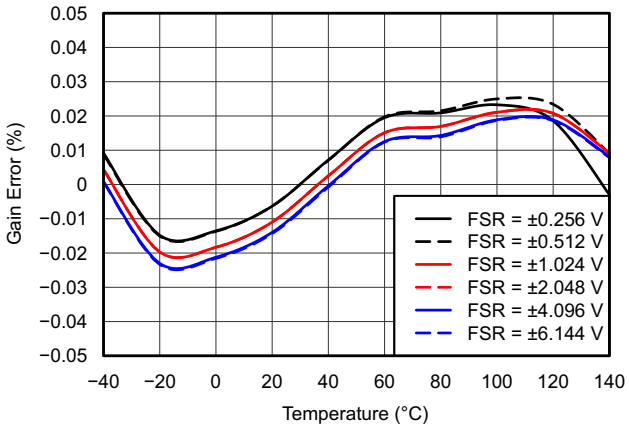


Figure 17. Gain Error vs Temperature

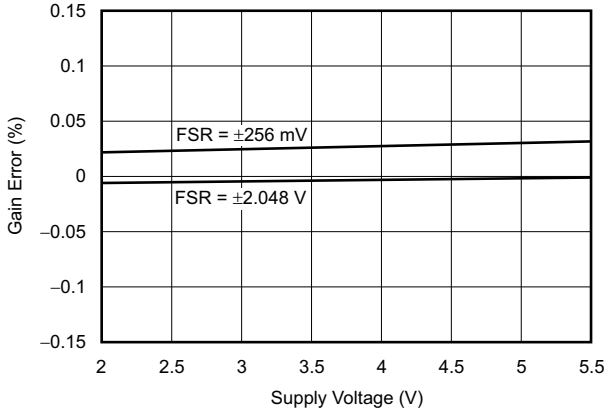
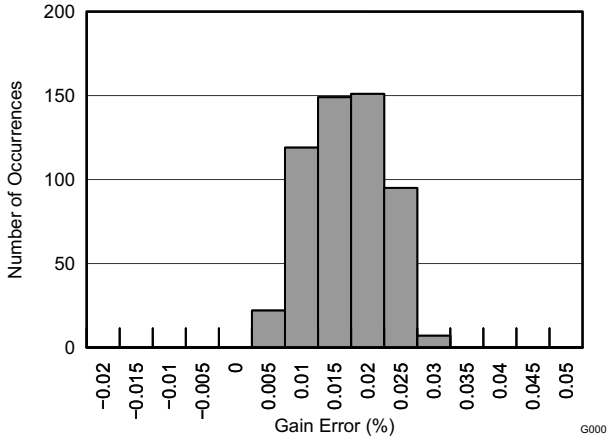


Figure 18. Gain Error vs Supply



FSR = ±2.048 V,
540 units from 3 production lots

Figure 19. Gain Error Histogram

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Typical Characteristics (continued)

At T_A = 25°C, VDD = 3.3 V, FSR = ±2.048 V (unless otherwise noted).

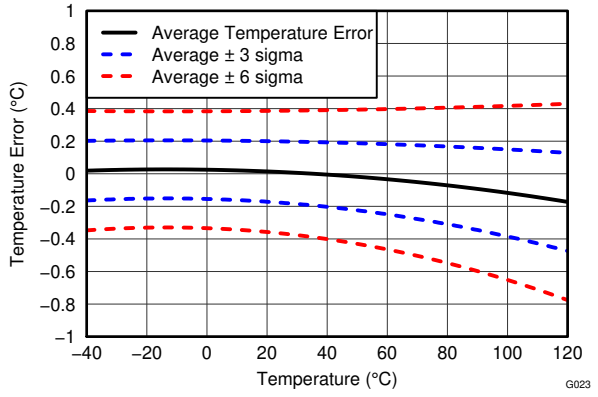
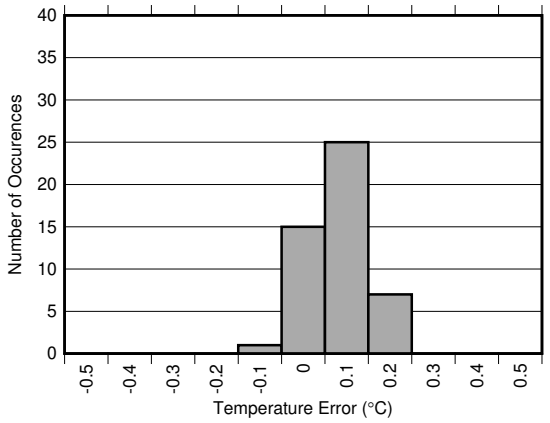
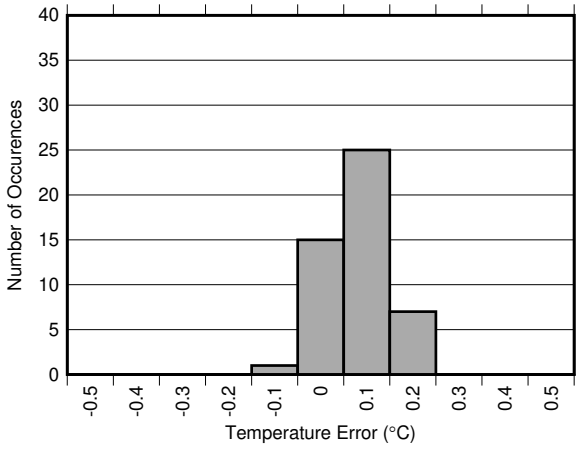


Figure 20. Temperature Sensor Error vs Temp (VSSOP)



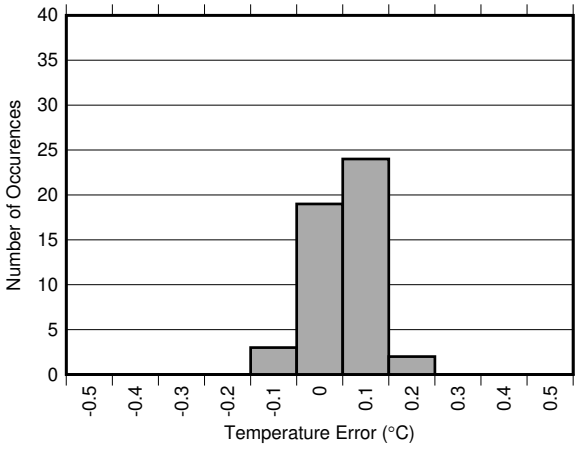
T_A = –40°C, 48 units from 3 production lots

Figure 21. Temperature Sensor Error Histogram (VSSOP)



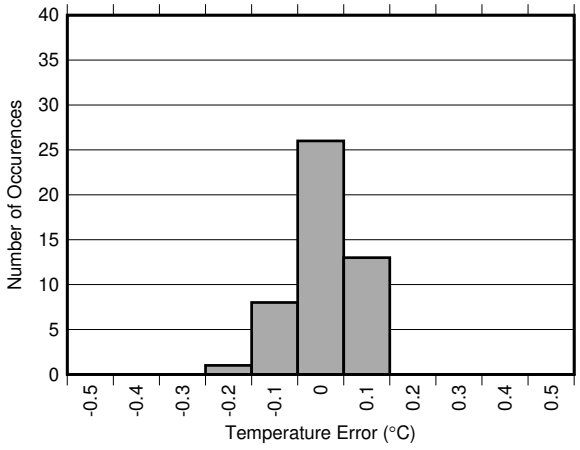
T_A = 0°C, 48 units from 3 production lots

Figure 22. Temperature Sensor Error Histogram (VSSOP)



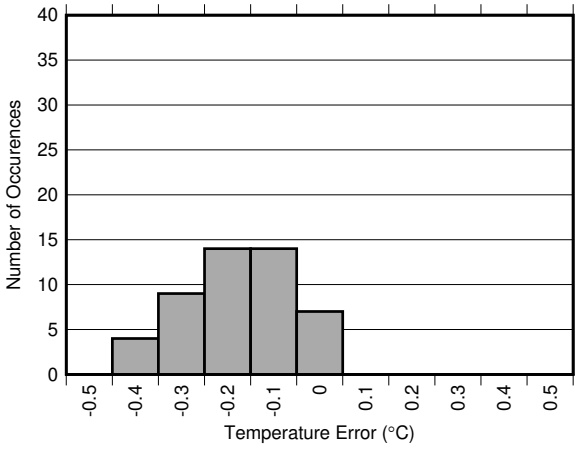
T_A = 25°C, 48 units from 3 production lots

Figure 23. Temperature Sensor Error Histogram (VSSOP)



T_A = 70°C, 48 units from 3 production lots

Figure 24. Temperature Sensor Error Histogram (VSSOP)



T_A = 125°C, 48 units from 3 production lots

Figure 25. Temperature Sensor Error Histogram (VSSOP)

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Typical Characteristics (continued)

At T_A = 25°C, VDD = 3.3 V, FSR = ±2.048 V (unless otherwise noted).

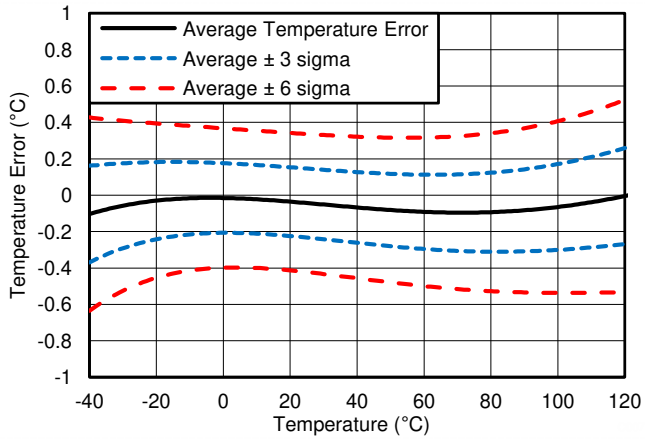
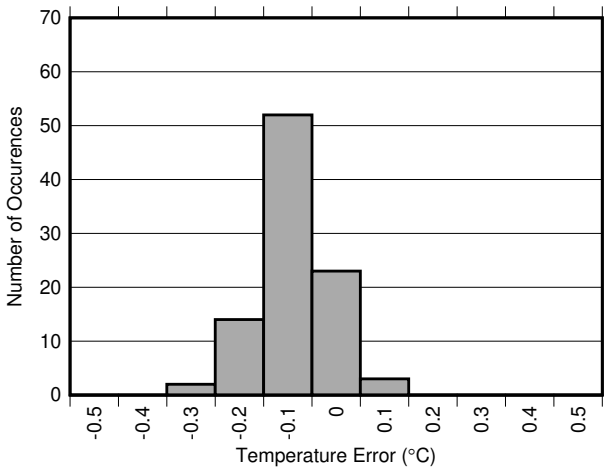
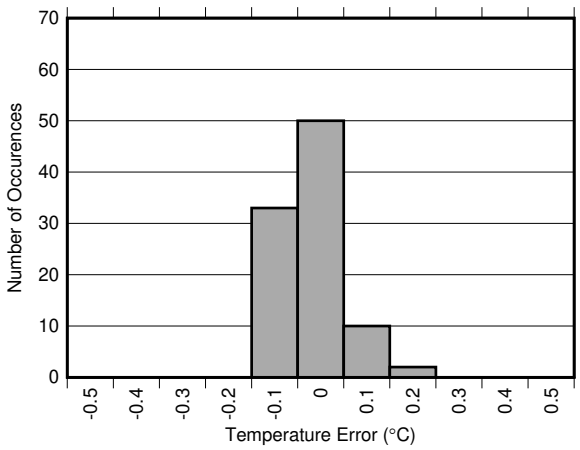


Figure 26. Temperature Sensor Error vs Temp (X2QFN)



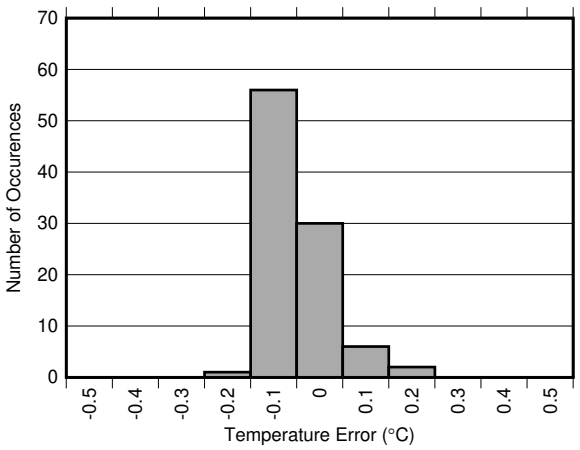
T_A = –40°C, 94 units from production

Figure 27. Temperature Sensor Error Histogram (X2QFN)



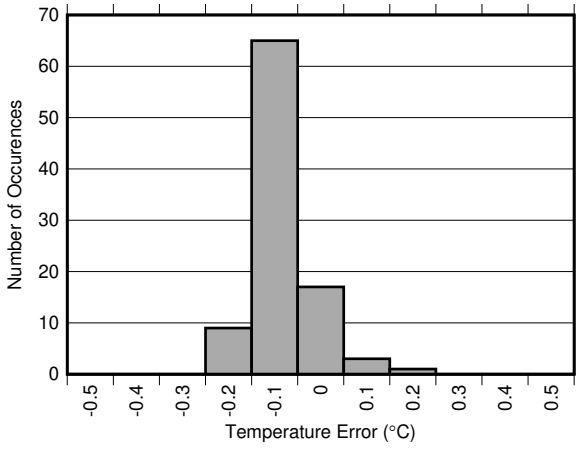
T_A = 0°C, 94 units from production

Figure 28. Temperature Sensor Error Histogram (X2QFN)



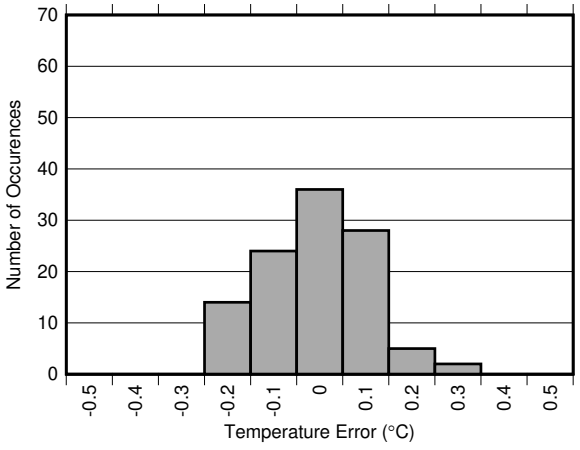
T_A = 25°C, 94 units from production

Figure 29. Temperature Sensor Error Histogram (X2QFN)



T_A = 70°C, 94 units from production

Figure 30. Temperature Sensor Error Histogram (X2QFN)



T_A = 125°C, 94 units from production

Figure 31. Temperature Sensor Error Histogram (X2QFN)

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Typical Characteristics (continued)

At T_A = 25°C, VDD = 3.3 V, FSR = ±2.048 V (unless otherwise noted).

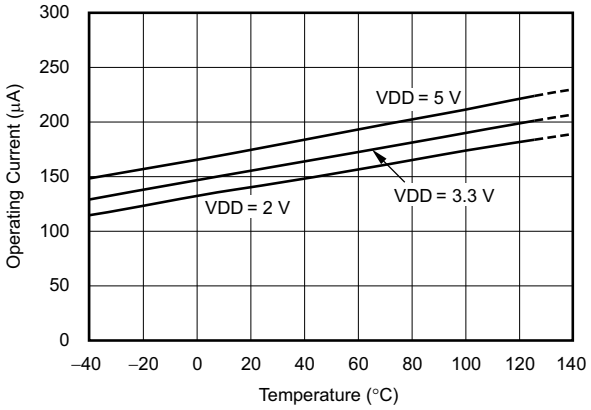


Figure 32. Operating Current vs Temperature

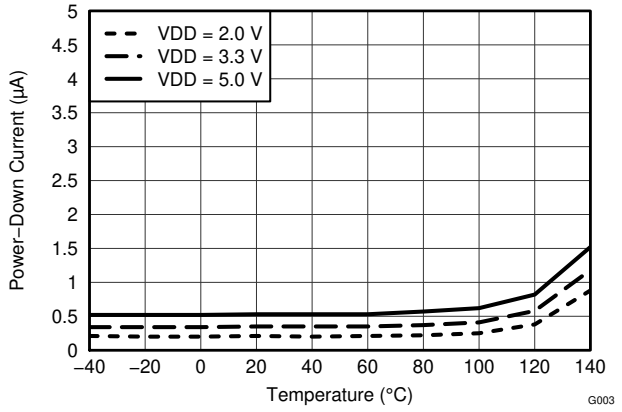


Figure 33. Power-Down Current vs Temperature

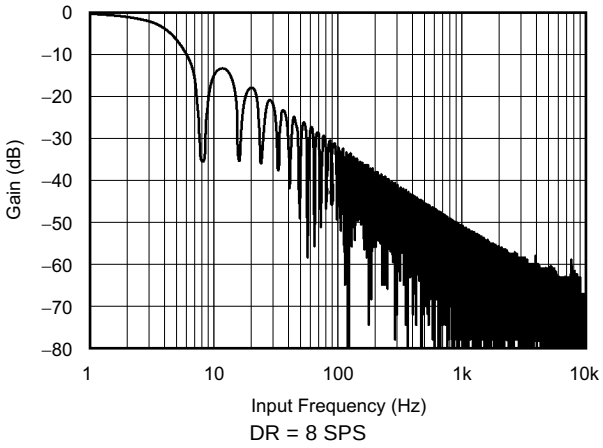


Figure 34. Digital Filter Frequency Response

8 Parameter Measurement Information

8.1 Noise Performance

Delta-sigma (ΔΣ) analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal of a ΔΣ ADC is sampled at a high frequency (modulator frequency) and subsequently filtered and decimated in the digital domain to yield a conversion result at the respective output data rate. The ratio between modulator frequency and output data rate is called *oversampling ratio* (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, the input-referred noise drops when reducing the output data rate because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, which is particularly useful when measuring low-level signals.

Table 1 and Table 2 summarize the device noise performance. Data are representative of typical noise performance at T_A = 25°C with the inputs shorted together externally. Table 1 show the input-referred noise in units of μV_{RMS} for the conditions shown. Note that μV_{PP} values are shown in parenthesis. Table 2 shows the corresponding data in effective number of bits (ENOB) calculated from μV_{RMS} values using Equation 1. The noise-free bits calculated from peak-to-peak noise values using Equation 2 are shown in parenthesis.

$$ENOB = \ln (FSR / V_{RMS\text{-}Noise}) / \ln(2) \quad (1)$$

$$\text{Noise-Free Bits} = \ln (FSR / V_{PP\text{-}Noise}) / \ln(2) \quad (2)$$

Table 1. Noise in μV_{RMS} (μV_{PP}) at VDD = 3.3 V

DATA RATE (SPS)	FSR (Full-Scale Range)					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
8	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
16	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
32	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
64	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
128	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (12.35)
250	187.5 (252.09)	125 (148.28)	62.5 (84.03)	31.25 (39.54)	15.62 (16.06)	7.81 (18.53)
475	187.5 (266.92)	125 (227.38)	62.5 (79.08)	31.25 (56.84)	15.62 (32.13)	7.81 (25.95)
860	187.5 (430.06)	125 (266.93)	62.5 (118.63)	31.25 (64.26)	15.62 (40.78)	7.81 (35.83)

Table 2. ENOB from RMS Noise (Noise-Free Bits from Peak-to-Peak Noise) at VDD = 3.3 V

DATA RATE (SPS)	FSR (Full-Scale Range)					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
8	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
16	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
32	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
64	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
128	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.33)
250	16 (15.57)	16 (15.75)	16 (15.57)	16 (15.66)	16 (15.96)	16 (14.75)
475	16 (15.49)	16 (15.13)	16 (15.66)	16 (15.13)	16 (14.95)	16 (14.26)
860	16 (14.8)	16 (14.9)	16 (15.07)	16 (14.95)	16 (14.61)	16 (13.8)

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9 Detailed Description

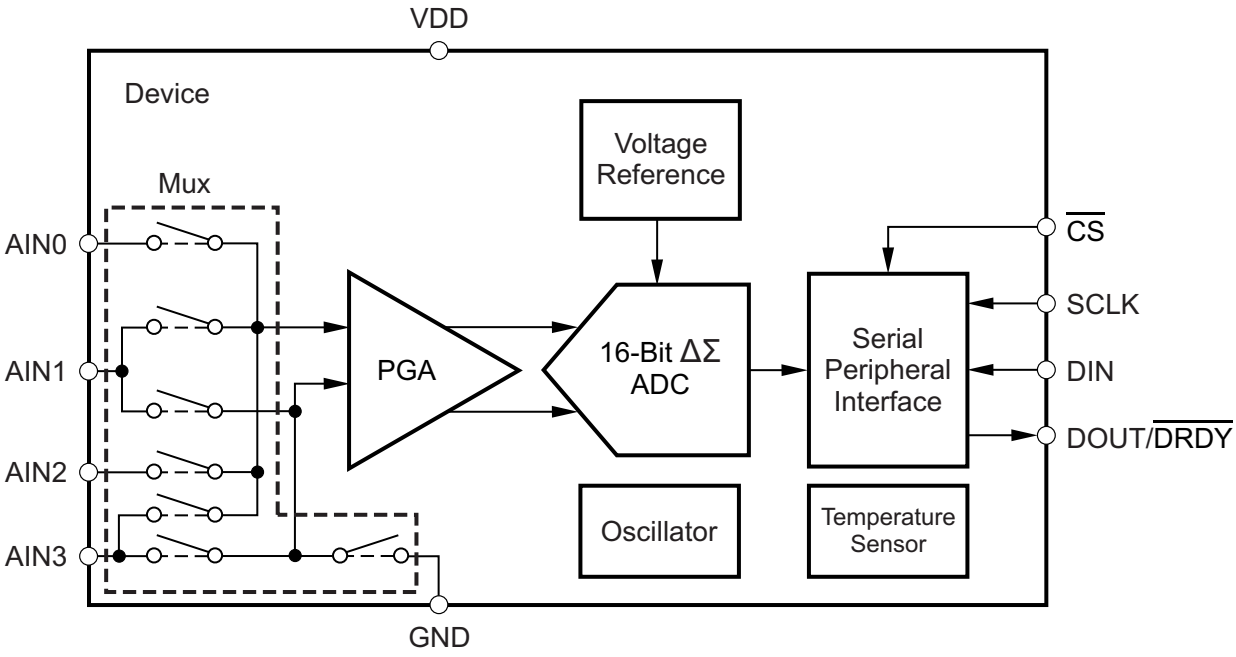
9.1 Overview

The ADS1118 is a very small, low-power, 16-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC). The ADS1118 consists of a ΔΣ ADC core with adjustable gain, an internal voltage reference, a clock oscillator, and an SPI. This device is also a highly linear and accurate temperature sensor. All of these features are intended to reduce required external circuitry and improve performance. *Functional Block Diagram* shows the ADS1118 functional block diagram.

The ADS1118 ADC core measures a differential signal, V_{IN}, that is the difference of $V_{(AINP)}$ and $V_{(AINN)}$. The converter core consists of a differential, switched-capacitor ΔΣ modulator followed by a digital filter. This architecture results in a very strong attenuation in any common-mode signals. Input signals are compared to the internal voltage reference. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage.

The ADS1118 has two available conversion modes: single-shot mode and continuous conversion mode. In single-shot mode, the ADC performs one conversion of the input signal upon request and stores the value to an internal conversion register. The device then enters a power-down state. This mode is intended to provide significant power savings in systems that require only periodic conversions or when there are long idle periods between conversions. In continuous conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recently completed conversion.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Multiplexer

The ADS1118 contains an input multiplexer (mux), as shown in Figure 35. Either four single-ended or two differential signals can be measured. Additionally, AIN0, AIN1, and AIN2 can be measured differentially to AIN3. The multiplexer is configured by bits MUX[2:0] in the Config register. When single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer.

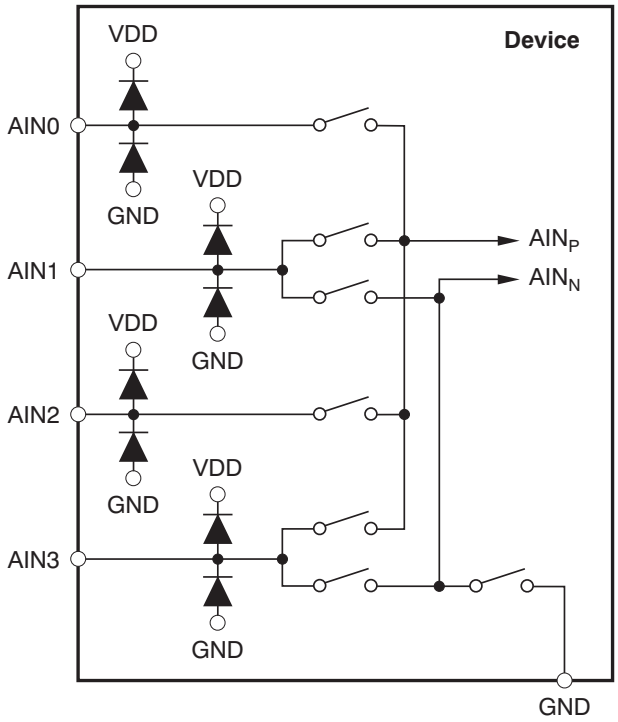


Figure 35. Input Multiplexer

When measuring single-ended inputs, the device does not output negative codes. These negative codes indicate negative differential signals; that is, $(V_{(AINP)} – V_{(AINN)}) < 0$. Electrostatic discharge (ESD) diodes to VDD and GND protect the ADS1118 inputs. To prevent the ESD diodes from turning on, keep the absolute voltage on any input within the range given in Equation 3:

$$GND – 0.3\ V < V_{(AINx)} < VDD + 0.3\ V \quad (3)$$

If the voltages on the input pins can possibly violate these conditions, use external Schottky diodes and series resistors to limit the input current to safe values (see the *Absolute Maximum Ratings* table).

Also, overdriving one unused input on the ADS1118 may affect conversions currently taking place on other input pins. If overdriving unused inputs is possible, clamp the signal with external Schottky diodes.

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Feature Description (continued)

9.3.2 Analog Inputs

The ADS1118 uses a switched-capacitor input stage where capacitors are continuously charged and then discharged to measure the voltage between AIN_P and AIN_N. This frequency at which the input signal is sampled is called the sampling frequency or the modulator frequency ($f_{(MOD)}$). ADS1118 has a 1 MHz internal oscillator which is further divided by a factor of 4 to generate the modulator frequency at 250 kHz. The capacitors used in this input stage are small, and to external circuitry, the average loading appears resistive. This structure is shown in Figure 36. The resistance is set by the capacitor values and the rate at which they are switched. Figure 37 shows the setting of the switches illustrated in Figure 36. During the sampling phase, switches S_1 are closed. This event charges C_{A1} to $V_{(AINP)}$, C_{A2} to $V_{(AINN)}$, and C_B to ($V_{(AINP)}$ – $V_{(AINN)}$). During the discharge phase, S_1 is first opened and then S_2 is closed. Both C_{A1} and C_{A2} then discharge to approximately 0.7 V and C_B discharges to 0 V. This charging draws a very small transient current from the source driving the ADS1118 analog inputs. The average value of this current can be used to calculate the effective impedance (Z_{eff}), where $Z_{eff} = V_{IN} / I_{AVERAGE}$.

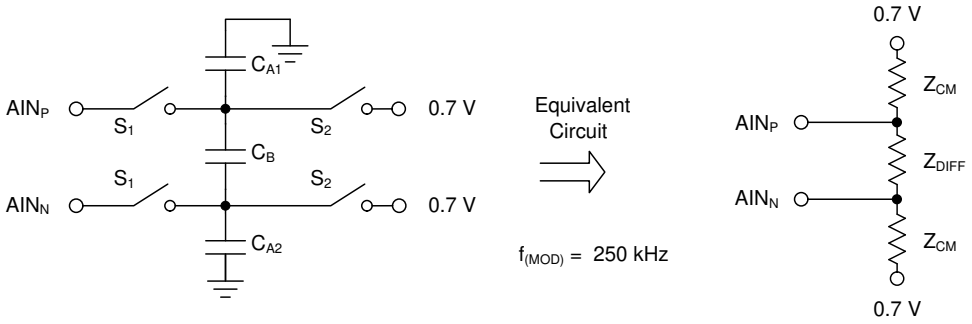


Figure 36. Simplified Analog Input Circuit

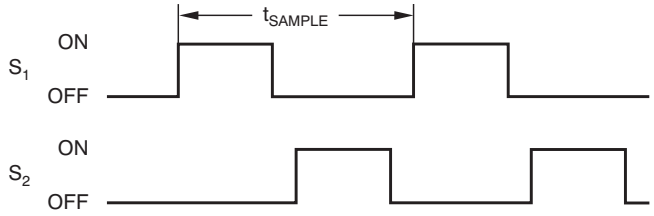


Figure 37. S_1 and S_2 Switch Timing

The common-mode input impedance is measured by applying a common-mode signal to the shorted AIN_P and AIN_N inputs and measuring the average current consumed by each pin. The common-mode input impedance changes depending on the full-scale range, but is approximately 6 MΩ for the default full-scale range. In Figure 36, the common-mode input impedance is Z_{CM}.

The differential input impedance is measured by applying a differential signal to AIN_P and AIN_N inputs where one input is held at 0.7 V. The current that flows through the pin connected to 0.7 V is the differential current and scales with the full-scale range. In Figure 36, the differential input impedance is Z_{DIFF}.

Make sure to consider the typical value of the input impedance. Unless the input source has a low impedance, the ADS1118 input impedance may affect the measurement accuracy. For sources with high-output impedance, buffering may be necessary. Active buffers introduce noise, and also introduce offset and gain errors. Consider all of these factors in high-accuracy applications.

The clock oscillator frequency drifts slightly with temperature; therefore, the input impedances also drift. For most applications, this input impedance drift is negligible, and can be ignored.

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Feature Description (continued)

9.3.3 Full-Scale Range (FSR) and LSB Size

A programmable gain amplifier (PGA) is implemented before the ADS1118 ΔΣ core. The full-scale range is configured by three bits (PGA[2:0]) in the Config Register and can be set to ±6.144 V, ±4.096 V, ±2.048 V, ±1.024 V, ±0.512 V, ±0.256 V. Table 3 shows the FSR together with the corresponding LSB size. LSB size is calculated from full-scale voltage by the formula shown in Equation 4. However, analog input voltages may never exceed the analog input voltage limits given in the *Electrical Characteristics*. If a supply voltage of VDD greater than 4 V is used, the ±6.144 V full-scale range allows input voltages to extend up to the supply. Note though that in this case, or whenever the supply voltage is less than the full-scale range (for example, VDD = 3.3 V and full-scale range = ±4.096 V), a full-scale ADC output code cannot be obtained. This inability means that some dynamic range is lost.

$$LSB = FSR / 2^{16} \quad (4)$$

Table 3. Full-Scale Range and Corresponding LSB Size

FSR	LSB SIZE
±6.144 V(1)	187.5 μV
±4.096 V(1)	125 μV
±2.048 V	62.5 μV
±1.024 V	31.25 μV
±0.512 V	15.625 μV
±0.256 V	7.8125 μV

(1) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V must be applied to this device.

9.3.4 Voltage Reference

The ADS1118 has an integrated voltage reference. An external reference cannot be used with this device. Errors associated with the initial voltage reference accuracy and the reference drift with temperature are included in the gain error and gain drift specifications in the *Electrical Characteristics*.

9.3.5 Oscillator

The ADS1118 has an integrated oscillator running at 1 MHz. No external clock is required to operate the device. Note that the internal oscillator drifts over temperature and time. The output data rate will scale proportional with the oscillator frequency.

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9.3.6 Temperature Sensor

The ADS1118 offers an integrated precision temperature sensor. The temperature sensor mode is enabled by setting bit TS_MODE = 1 in the Config Register. Temperature data are represented as a 14-bit result that is left-justified within the 16-bit conversion result. Data are output starting with the most significant byte (MSB). When reading the two data bytes, the first 14 bits are used to indicate the temperature measurement result. One 14-bit LSB equals 0.03125°C. Negative numbers are represented in binary twos complement format, as shown in Table 4.

Table 4. 14-Bit Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	01 0000 0000 0000	1000
127.96875	00 1111 1111 1111	0FFF
100	00 1100 1000 0000	0C80
75	00 1001 0110 0000	0960
50	00 0110 0100 0000	0640
25	00 0011 0010 0000	0320
0.25	00 0000 0000 1000	0008
0.03125	00 0000 0000 0001	0001
0	00 0000 0000 0000	0000
–0.25	11 1111 1111 1000	3FF8
–25	11 1100 1110 0000	3CE0
–40	11 1011 0000 0000	3B00

9.3.6.1 Converting from Temperature to Digital Codes

For positive temperatures:

Twos complement is not performed on positive numbers. Therefore, simply convert the number to binary code in a 14-bit, left justified format with the MSB = 0 to denote the positive sign.

Example: 50°C / (0.03125°C/count) = 1600 = 0640h = 00 0110 0100 0000

For negative temperatures:

Generate the twos complement of a negative number by complementing the absolute binary number and adding 1. Then denote the negative sign with the MSB = 1.

Example: |–25°C| / (0.03125°C/count) = 800 = 0320h = 00 0011 0010 0000

Twos complement format: 11 1100 1101 1111 + 1 = 11 1100 1110 0000

9.3.6.2 Converting from Digital Codes to Temperature

To convert from digital codes to temperature, first check whether the MSB is a 0 or a 1. If the MSB is a 0, simply multiply the decimal code by 0.03125°C to obtain the result. If the MSB = 1, subtract 1 from the result and complement all of the bits. Then multiply the result by –0.03125°C.

Example: The device reads back 0960h: 0960h has an MSB = 0.

0960h × 0.03125°C = 2400 × 0.03125°C = 75°C

Example: The device reads back 3CE0h: 3CE0h has an MSB = 1.

Subtract 1 and complement the result: 3CE0h → 0320h

0320h × (–0.03125°C) = 800 × (–0.03125°C) = –25°C

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9.4 Device Functional Modes

9.4.1 Reset and Power Up

When the ADS1118 powers up, a reset is performed. As part of the reset process, the ADS1118 sets all of its bits in the Config Register to the respective default settings. By default, the ADS1118 enters a power-down state at start-up. The device interface and digital blocks are active, but no data conversions are performed. The initial power-down state of the ADS1118 is intended to relieve systems with tight power-supply requirements from encountering a surge during power up.

9.4.2 Operating Modes

The ADS1118 operates in one of two modes: continuous-conversion or single-shot. The MODE bit in the Config register selects the respective operating mode.

9.4.2.1 Single-Shot Mode and Power-Down

When the MODE bit in the Config register is set to 1, the ADS1118 enters a power-down state, and operates in single-shot mode. This power-down state is the default state for the ADS1118 when power is first applied. Although powered down, the device still responds to commands. The ADS1118 remains in this power-down state until a 1 is written to the single-shot (SS) bit in the Config register. When the SS bit is asserted, the device powers up, resets the SS bit to 0, and starts a single conversion. When conversion data are ready for retrieval, the device powers down again. Writing a 1 to the SS bit while a conversion is ongoing has no effect. To switch to continuous-conversion mode, write a 0 to the MODE bit in the Config register.

9.4.2.2 Continuous-Conversion Mode

In continuous-conversion mode (MODE bit set to 0), the ADS1118 continuously performs conversions. When a conversion completes, the ADS1118 places the result in the Conversion register and immediately begins another conversion. To switch to single-shot mode, write a 1 to the MODE bit in the Config register, or reset the device.

9.4.3 Duty Cycling for Low Power

The noise performance of a $\Delta\Sigma$ ADC generally improves when lowering the output data rate because more samples of the internal modulator can be averaged to yield one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates may not be required. For these applications, the ADS1118 supports duty cycling that can yield significant power savings by periodically requesting high data rate readings at an effectively lower data rate. For example, an ADS1118 in power-down state with a data rate set to 860 SPS can be operated by a microcontroller that instructs a single-shot conversion every 125 ms (8 SPS). Because a conversion at 860 SPS only requires approximately 1.2 ms, the ADS1118 enters power-down state for the remaining 123.8 ms. In this configuration, the ADS1118 consumes approximately 1/100th the power that is otherwise consumed in continuous conversion mode. The duty cycling rate is completely arbitrary and is defined by the master controller. The ADS1118 offers lower data rates that do not implement duty cycling and also offers improved noise performance if required.

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9.5 Programming

9.5.1 Serial Interface

The SPI-compatible serial interface consists of either four signals (CS, SCLK, DIN, and DOUT/DRDY), or three signals (in which case CS may be tied low). The interface is used to read conversion data, read and write registers, and control device operation.

9.5.2 Chip Select (CS)

The chip select pin (CS) selects the ADS1118 for SPI communication. This feature is useful when multiple devices share the same serial bus. Keep CS low for the duration of the serial communication. When CS is taken high, the serial interface is reset, SCLK is ignored, and DOUT/DRDY enters a high-impedance state. In this state, DOUT/DRDY cannot provide data-ready indication. In situations where multiple devices are present and DOUT/DRDY must be monitored, lower CS periodically. At this point, the DOUT/DRDY pin either immediately goes high to indicate that no new data are available, or immediately goes low to indicate that new data are present in the Conversion register and are available for transfer. New data can be transferred at any time without concern of data corruption. When a transmission starts, the current result is locked into the output shift register and does not change until the communication completes. This system avoids any possibility of data corruption.

9.5.3 Serial Clock (SCLK)

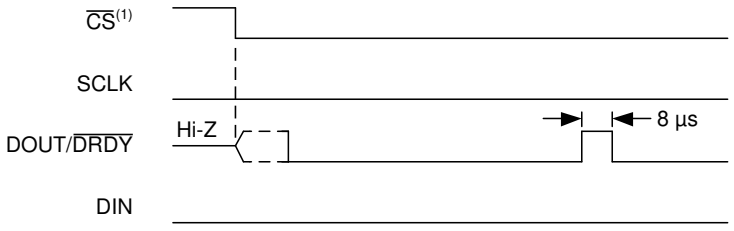
The serial clock (SCLK) features a Schmitt-triggered input and is used to clock data on the DIN and DOUT/DRDY pins into and out of the ADS1118. Even though the input has hysteresis, TI recommends keeping SCLK as clean as possible to prevent glitches from accidentally shifting the data. If SCLK is held low for 28 ms, the serial interface resets and the next SCLK pulse starts a new communication cycle. This time-out feature can be used to recover communication when a serial interface transmission is interrupted. When the serial interface is idle, hold SCLK low.

9.5.4 Data Input (DIN)

The data input pin (DIN) is used along with SCLK to send data to the ADS1118. The device latches data on DIN on the SCLK falling edge. The ADS1118 never drives the DIN pin.

9.5.5 Data Output and Data Ready (DOUT/DRDY)

The data output and data ready pin (DOUT/DRDY) is used with SCLK to read conversion and register data from the ADS1118. Data on DOUT/DRDY are shifted out on the SCLK rising edge. DOUT/DRDY is also used to indicate that a conversion is complete and new data are available. This pin transitions low when new data are ready for retrieval. DOUT/DRDY is also able to trigger a microcontroller to start reading data from the ADS1118. In continuous-conversion mode, DOUT/DRDY transitions high again 8 µs before the next data ready signal (DOUT/DRDY low) if no data are retrieved from the device. This transition is shown in Figure 38. Complete the data transfer before DOUT/DRDY returns high.



(1) CS may be held low. If CS is low, DOUT/DRDY asserts low indicating new data are available.

Figure 38. DOUT/DRDY Behavior Without Data Retrieval in Continuous Conversion Mode

When CS is high, DOUT/DRDY is configured by default with a weak internal pullup resistor. This feature reduces the risk of DOUT/DRDY floating near midsupply and causing leakage current in the master device. To disable this pullup resistor and place the device into a high-impedance state, set the PULL_UP_EN bit to 0 in the Config Register.

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Programming (continued)

9.5.6 Data Format

The ADS1118 provides 16 bits of data in binary twos complement format. A positive full-scale input produces an output code of 7FFFh and a negative full-scale input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. Table 5 summarizes the ideal output codes for different input signals. Figure 39 shows code transitions versus input voltage.

Table 5. Input Signal versus Ideal Output Code

INPUT SIGNAL, V_{IN} (AIN_P – AIN_N)	IDEAL OUTPUT CODE(1)
≥ +FS $(2^{15} – 1)/2^{15}$	7FFFh
+FS/2^{15}	0001h
0	0
–FS/2^{15}	FFFFh
≤ –FS	8000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

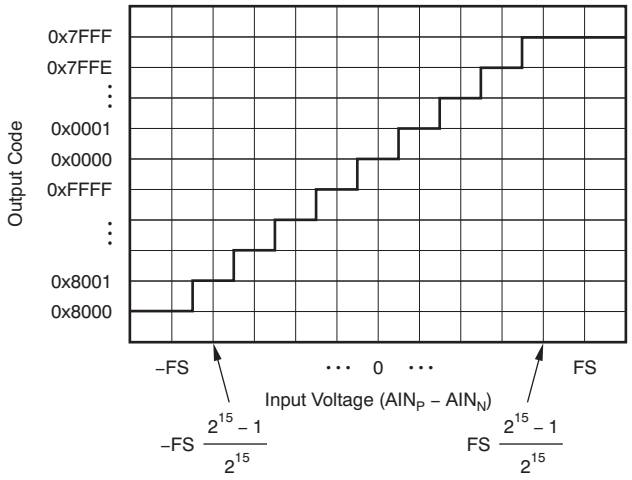


Figure 39. ADS1118 Code Transition Diagram

9.5.7 Data Retrieval

Data is written to and read from the ADS1118 in the same manner for both single-shot and continuous conversion modes, without having to issue any commands. The operating mode for the ADS1118 is selected by the MODE bit in the Config register.

Set the MODE bit to 0 to put the device in continuous-conversion mode. In continuous-conversion mode, the device is constantly starting new conversions even when $\overline{CS}$ is high.

Set the MODE bit to 1 for single-shot mode. In single-shot mode, a new conversion only starts by writing a 1 to the SS bit.

The conversion data are always buffered, and retain the current data until replaced by new conversion data. Therefore, data can be read at any time without concern of data corruption. When DOUT/$\overline{DRDY}$ asserts low, indicating that new conversion data are ready, the conversion data are read by shifting the data out on DOUT/$\overline{DRDY}$. The MSB of the data (bit 15) on DOUT/$\overline{DRDY}$ is clocked out on the first SCLK rising edge. At the same time that the conversion result is clocked out of DOUT/$\overline{DRDY}$, new Config register data are latched on DIN on the SCLK falling edge.

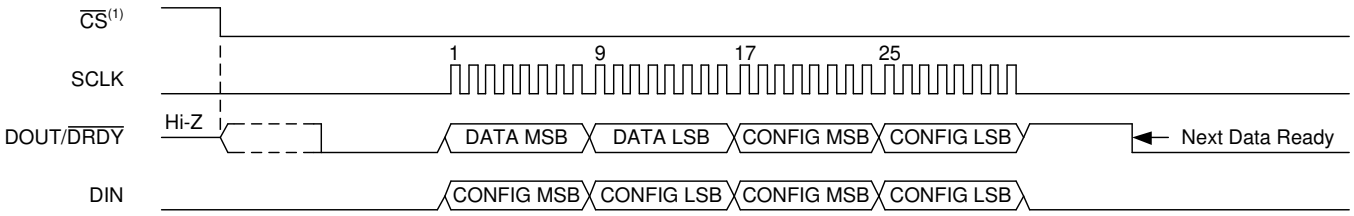
The ADS1118 also offers the possibility of direct readback of the Config register settings in the same data transmission cycle. One complete data transmission cycle consists of either 32 bits (when the Config register data readback is used) or 16 bits (only used when the $\overline{CS}$ line can be controlled and is not permanently tied low).

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9.5.7.1 32-Bit Data Transmission Cycle

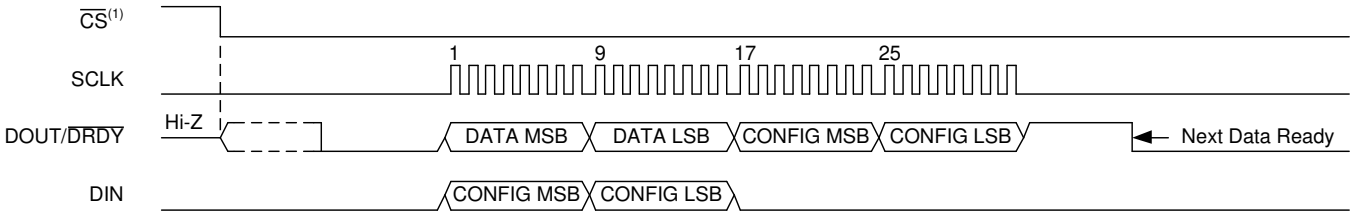
The data in a 32-bit data transmission cycle consists of four bytes: two bytes for the conversion result, and an additional two bytes for the Config Register read back. The device always reads the MSB first.

Write the same Config register setting twice during one transmission cycle as shown in Figure 40. If convenient, write the Config register setting once during the first half of the transmission cycle, and then hold the DIN pin either low (as shown in Figure 41) or high during the second half of the cycle. If no update to the Config register is required, hold the DIN pin either low or high during the entire transmission cycle. The Config register setting written in the first two bytes of a 32-bit transmission cycle is read back in the last two bytes of the same cycle.



(1) CS can be held low if the ADS1118 does not share the serial bus with another device. If CS is low, DOUT/DRDY asserts low indicating new data are available.

Figure 40. 32-Bit Data Transmission Cycle With Config Register Readback



(1) CS can be held low if the ADS1118 does not share the serial bus with another device. If CS is low, DOUT/DRDY asserts low indicating new data are available.

Figure 41. 32-Bit Data Transmission Cycle: DIN Held Low

9.5.7.2 16-Bit Data Transmission Cycle

If Config Register data are not required to be readback, the ADS1118 conversion data can also be clocked out in a short 16-bit data transmission cycle, as shown in Figure 42. Therefore, CS must be taken high after the 16th SCLK cycle. Taking CS high resets the SPI interface. The next time CS is taken low, data transmission starts with the currently buffered conversion result on the first SCLK rising edge. If DOUT/DRDY is low when data retrieval starts, the conversion buffer is already updated with a new result. Otherwise, if DOUT/DRDY is high, the same result from the previous data transmission cycle is read.

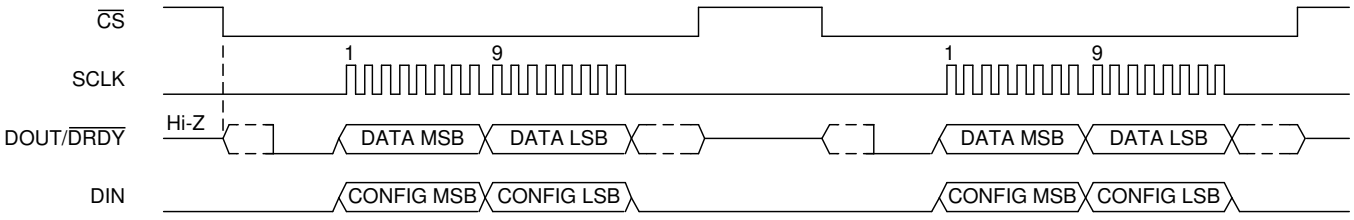


Figure 42. 16-Bit Data Transmission Cycle

9.6 Register Maps

The ADS1118 has two registers that are accessible through the SPI interface. The Conversion Register contains the result of the last conversion. The Config Registerallows the user to change the ADS1118 operating modes and query the status of the devices.

9.6.1 Conversion Register [reset = 0000h]

The 16-bit Conversion register contains the result of the last conversion in binary twos complement format. Following power up, the Conversion register is cleared to 0, and remains 0 until the first conversion is completed. The register format is shown in Figure 43.

Figure 43. Conversion Register

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. Conversion Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	D[15:0]	R	0000h	16-bit conversion result

9.6.2 Config Register [reset = 058Bh]

The 16-bit Config register can be used to control the ADS1118 operating mode, input selection, data rate, full-scale range, and temperature sensor mode. The register format is shown in Figure 44.

Figure 44. Config Register

15	14	13	12	11	10	9	8
SS	MUX[2:0]			PGA[2:0]			MODE
R/W-0h	R/W-0h			R/W-2h			R/W-1h
7	6	5	4	3	2	1	0
DR[2:0]			TS_MODE	PULL_UP_EN	NOP[1:0]		Reserved
R/W-4h			R/W-0h	R/W-1h	R/W-1h		R-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. Config Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SS	R/W	0h	**Single-shot conversion start** This bit is used to start a single conversion. SS can only be written when in power-down state and has no effect when a conversion is ongoing. When writing: 0 = No effect 1 = Start a single conversion (when in power-down state) Always reads back 0 (default).
14:12	MUX[2:0]	R/W	0h	**Input multiplexer configuration** These bits configure the input multiplexer. 000 = AIN_P is AIN0 and AIN_N is AIN1 (default) 001 = AIN_P is AIN0 and AIN_N is AIN3 010 = AIN_P is AIN1 and AIN_N is AIN3 011 = AIN_P is AIN2 and AIN_N is AIN3 100 = AIN_P is AIN0 and AIN_N is GND 101 = AIN_P is AIN1 and AIN_N is GND 110 = AIN_P is AIN2 and AIN_N is GND 111 = AIN_P is AIN3 and AIN_N is GND

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Table 7. Config Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:9	PGA[2:0]	R/W	2h	**Programmable gain amplifier configuration** These bits configure the programmable gain amplifier. 000 = FSR is ±6.144 V(1) 001 = FSR is ±4.096 V(1) 010 = FSR is ±2.048 V (default) 011 = FSR is ±1.024 V 100 = FSR is ±0.512 V 101 = FSR is ±0.256 V 110 = FSR is ±0.256 V 111 = FSR is ±0.256 V
8	MODE	R/W	1h	**Device operating mode** This bit controls the ADS1118 operating mode. 0 = Continuous conversion mode 1 = Power-down and single-shot mode (default)
7:5	DR[2:0]	R/W	4h	**Data rate** These bits control the data rate setting. 000 = 8 SPS 001 = 16 SPS 010 = 32 SPS 011 = 64 SPS 100 = 128 SPS (default) 101 = 250 SPS 110 = 475 SPS 111 = 860 SPS
4	TS_MODE	R/W	0h	**Temperature sensor mode** This bit configures the ADC to convert temperature or input signals. 0 = ADC mode (default) 1 = Temperature sensor mode
3	PULL_UP_EN	R/W	1h	**Pullup enable** This bit enables a weak internal pullup resistor on the DOUT/$\overline{\text{DRDY}}$ pin only when $\overline{\text{CS}}$ is high. When enabled, an internal 400-kΩ resistor connects the bus line to supply. When disabled, the DOUT/$\overline{\text{DRDY}}$ pin floats. 0 = Pullup resistor disabled on DOUT/$\overline{\text{DRDY}}$ pin 1 = Pullup resistor enabled on DOUT/$\overline{\text{DRDY}}$ pin (default)
2:1	NOP[1:0]	R/W	1h	**No operation** The NOP[1:0] bits control whether data are written to the Config register or not. For data to be written to the Config register, the NOP[1:0] bits must be '01'. Any other value results in a NOP command. DIN can be held high or low during SCLK pulses without data being written to the Config register. 00 = Invalid data, do not update the contents of the Config register 01 = Valid data, update the Config register (default) 10 = Invalid data, do not update the contents of the Config register 11 = Invalid data, do not update the contents of the Config register
0	Reserved	R	1h	**Reserved** Writing either 0 or 1 to this bit has no effect. Always reads back 1.

(1) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V must be applied to this device.

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ADS1118 is a precision, 16-bit ΔΣ ADC that offers many integrated features to ease the measurement of the most common sensor types including various type of temperature and bridge sensors. The following sections give example circuits and suggestions for using the ADS1118 in various situations.

10.1.1 Serial Interface Connections

The principle serial interface connections for the ADS1118 are shown in Figure 45.

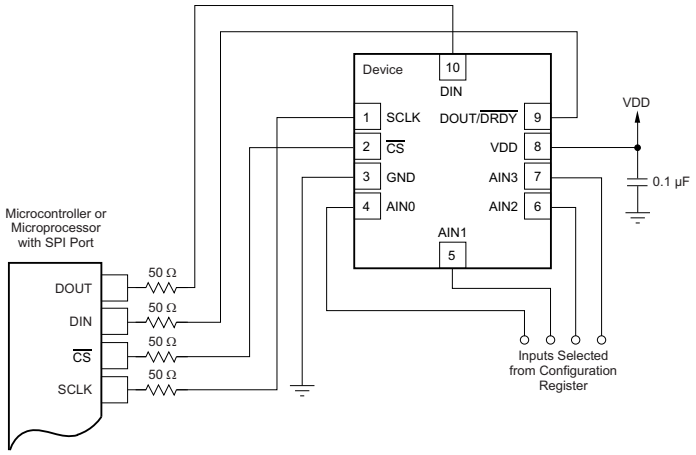


Figure 45. Typical Connections of the ADS1118

Most microcontroller SPI peripherals can operate with the ADS1118. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are launched or changed only on SCLK rising edges; data are latched or read by the master and slave on SCLK falling edges. Details of the SPI communication protocol employed by the ADS1118 can be found in the *Timing Requirements: Serial Interface* section.

It is a good practice to place 50-Ω resistors in the series path to each of the digital pins to provide some short circuit protection. Care must be taken to still meet all SPI timing requirements because these additional series resistors along with the bus parasitic capacitances present on the digital signal lines could slew the signals.

The fully-differential input of the ADS1118 is ideal for connecting to differential sources (such as thermocouples and thermistors) with a moderately low source impedance. Although the ADS1118 can read fully-differential signals, the device cannot accept negative voltages on either of its inputs because of ESD protection diodes on each pin. When an input exceeds supply or drops below ground, these diodes turn on to prevent any ESD damage to the device.

10.1.2 GPIO Ports for Communication

Most microcontrollers have programmable input/output (I/O) pins that can be set in software to act as inputs or outputs. If an SPI controller is not available, the ADS1118 can be connected to GPIO pins and the SPI bus protocol can be simulated. Using GPIO pins to generate the SPI interface only requires that the pins be configured as push or pull inputs or outputs. Furthermore, if the SCLK line is held low for more than 28 ms, the communication times out. This condition means that the GPIO ports must be capable of providing SCLK pulses with no more than 28 ms between pulses.

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Application Information (continued)

10.1.3 Analog Input Filtering

Analog input filtering serves two purposes: first, to limit the effect of aliasing during the sampling process and second, to reduce external noise from being a part of the measurement.

As with any sampled system, aliasing can occur if proper antialias filtering is not in place. Aliasing occurs when frequency components are present in the input signal that are higher than half the sampling frequency of the ADC (also known as the *Nyquist frequency*). These frequency components fold back and show up in the actual frequency band of interest below half the sampling frequency. The filter response of the digital filter repeats at multiples of the sampling frequency, also known as the modulator frequency ($f_{(MOD)}$), as shown in Figure 46. Signals or noise up to a frequency where the filter response repeats are attenuated to a certain amount by the digital filter depending on the filter architecture. Any frequency components present in the input signal around the modulator frequency or multiples thereof are not attenuated and alias back into the band of interest, unless attenuated by an external analog filter.

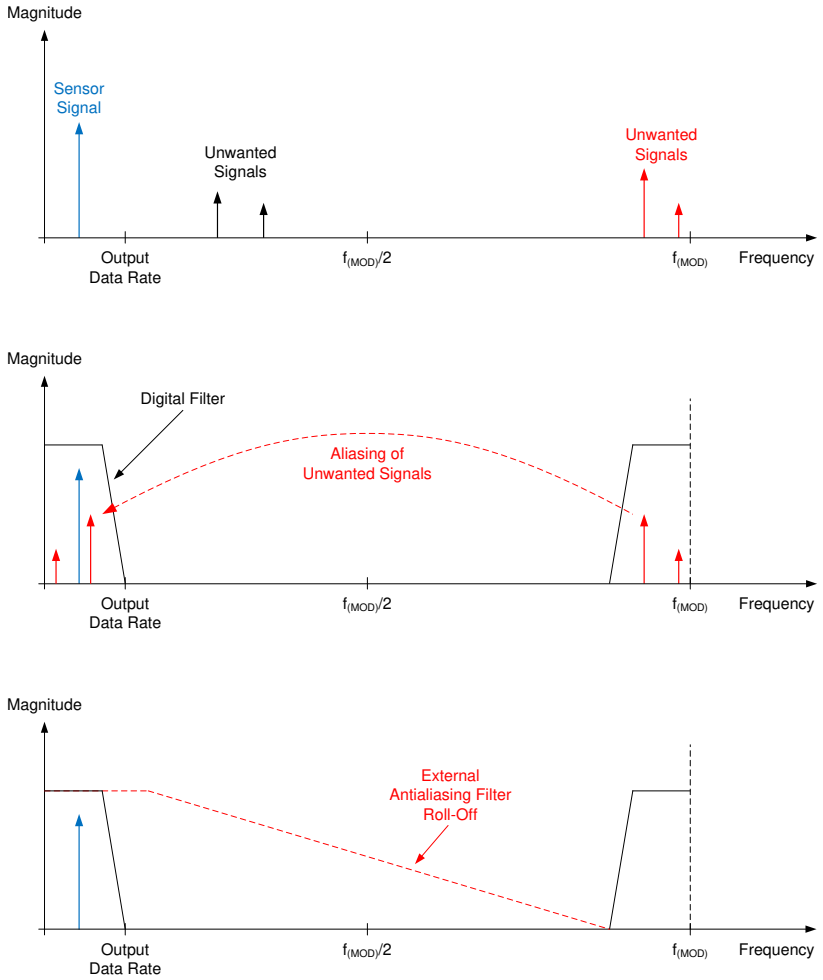


Figure 46. Effect of Aliasing

Many sensor signals are inherently bandlimited; for example, the output of a thermocouple has a limited rate of change. In this case, the sensor signal does not alias back into the pass-band when using a ΔΣ ADC. However, any noise pick-up along the sensor wiring or the application circuitry can potentially alias into the pass-band. Power line-cycle frequency and harmonics are one common noise source. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and cellular phones. Another noise source typically exists on the printed-circuit-board (PCB) itself in the form of clocks and other digital signals. Analog input filtering helps remove unwanted signals from affecting the measurement result.

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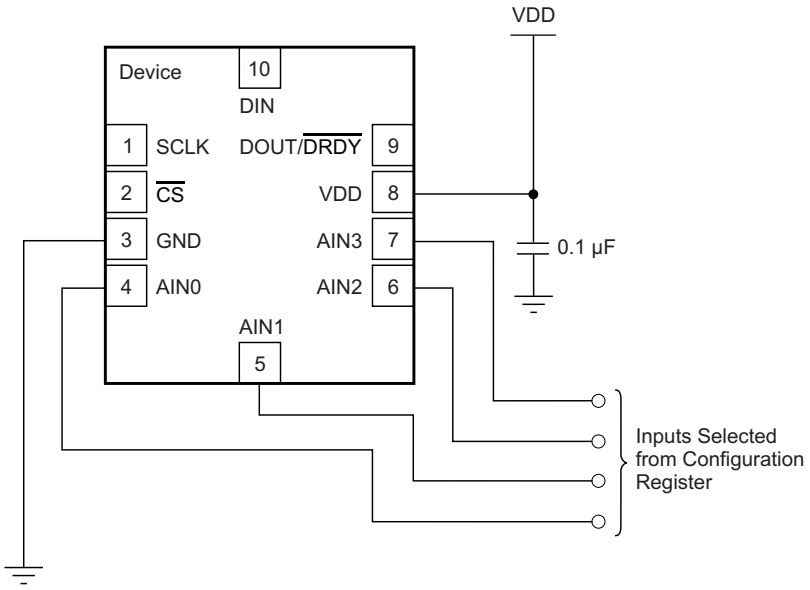
Application Information (continued)

A first-order resistor-capacitor (RC) filter is (in most cases) sufficient to either totally eliminate aliasing, or to reduce the effect of aliasing to a level within the noise floor of the sensor. Ideally, any signal beyond $f_{(MOD)}$ / 2 is attenuated to a level below the noise floor of the ADC. The digital filter of the ADS1118 attenuates signals to a certain degree, as shown in Figure 34. In addition, noise components are usually smaller in magnitude than the actual sensor signal. Therefore, using a first-order RC filter with a cutoff frequency set at the output data rate or 10x higher is generally a good starting point for a system design.

10.1.4 Single-Ended Inputs

Although the ADS1118 has two differential inputs, the device can measure four single-ended signals. Figure 47 shows a single-ended connection scheme. The ADS1118 is configured for single-ended measurement by configuring the MUX to measure each channel with respect to ground. Data are then read out of one input based on the selection in the Config Register. The single-ended signal can range from 0 V up to positive supply or +FS, whichever is lower. Negative voltages cannot be applied to this circuit because the ADS1118 can only accept positive voltages with respect to ground. The ADS1118 does not lose linearity within the input range.

The ADS1118 offers a differential input voltage range of ±FS. The single-ended circuit shown in Figure 47 however only uses the positive half of the ADS1118 FS input voltage range because differentially negative inputs are not produced. Because only half of the FS range is used, one bit of resolution is lost. For optimal noise performance, TI recommends using differential configurations whenever possible. Differential configurations maximize the dynamic range of the ADC and provide strong attenuation of common-mode noise.



NOTE: Digital pin connections omitted for clarity.

Figure 47. Measuring Single-Ended Inputs

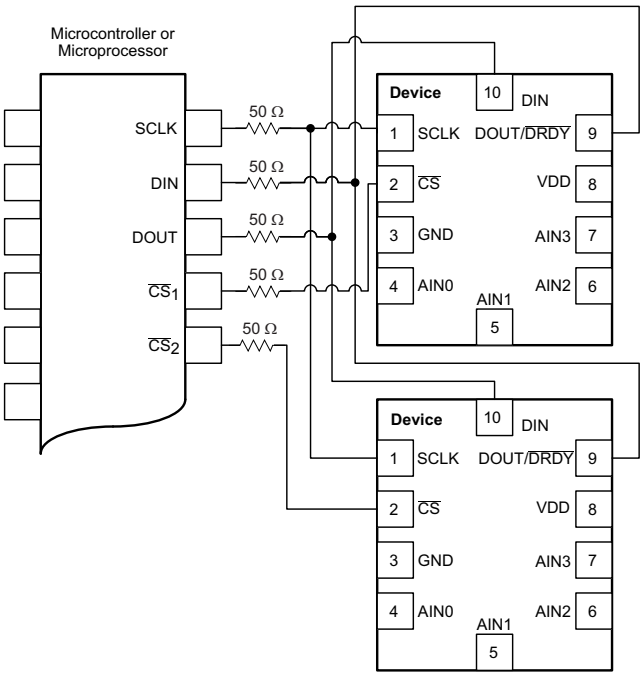
The ADS1118 is also designed to allow AIN3 to serve as a common point for measurements by adjusting the mux configuration. AIN0, AIN1, and AIN2 can all be measured with respect to AIN3. In this configuration the ADS1118 can operate with inputs where AIN3 serves as the common point. This ability improves the usable range over the single-ended configuration because negative differential voltages are allowed when GND < $V_{(AIN3)}$ < VDD; however, common-mode noise attenuation is not offered.

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Application Information (continued)

10.1.5 Connecting Multiple Devices

When connecting multiple ADS1118 devices to a single SPI bus, SCLK, DIN, and DOUT/$\overline{\text{DRDY}}$ can be safely shared by using a dedicated chip-select ($\overline{\text{CS}}$) for each SPI-enabled device. By default, when $\overline{\text{CS}}$ goes high for the ADS1118, DOUT/$\overline{\text{DRDY}}$ is pulled up to VDD by a weak pullup resistor. This feature is intended to prevent DOUT/$\overline{\text{DRDY}}$ from floating near mid-rail and causing excess current leakage on a microcontroller input. If the PULL_UP_EN bit in the Config Register is set to 0, the DOUT/$\overline{\text{DRDY}}$ pin enters a 3-state mode when $\overline{\text{CS}}$ transitions high. The ADS1118 cannot issue a data ready pulse on DOUT/$\overline{\text{DRDY}}$ when $\overline{\text{CS}}$ is high. To evaluate when a new conversion is ready from the ADS1118 when using multiple devices, the master can periodically drop $\overline{\text{CS}}$ to the ADS1118. When $\overline{\text{CS}}$ goes low, the DOUT/$\overline{\text{DRDY}}$ pin immediately drives either high or low. If the DOUT/$\overline{\text{DRDY}}$ line drives low on a low $\overline{\text{CS}}$, new data are currently available for clocking out at any time. If the DOUT/$\overline{\text{DRDY}}$ line drives high, no new data are available and the ADS1118 returns the last read conversion result. Valid data can be retrieved from the ADS1118 at anytime without concern of data corruption. If a new conversion becomes available during data transmission, that conversion is not available for readback until a new SPI transmission is initiated.



NOTE: Power and input connections omitted for clarity.

Figure 48. Connecting Multiple ADS1118s

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Application Information (continued)

10.1.6 Pseudo Code Example

The flow chart in Figure 49 shows a pseudo code sequence with the required steps to set up communication between the device and a microcontroller to take subsequent readings from the ADS1118. As an example, the default Config Register settings are changed to set up the device in FSR = ±0.512 V, continuous conversion mode and 64-SPS data rate.

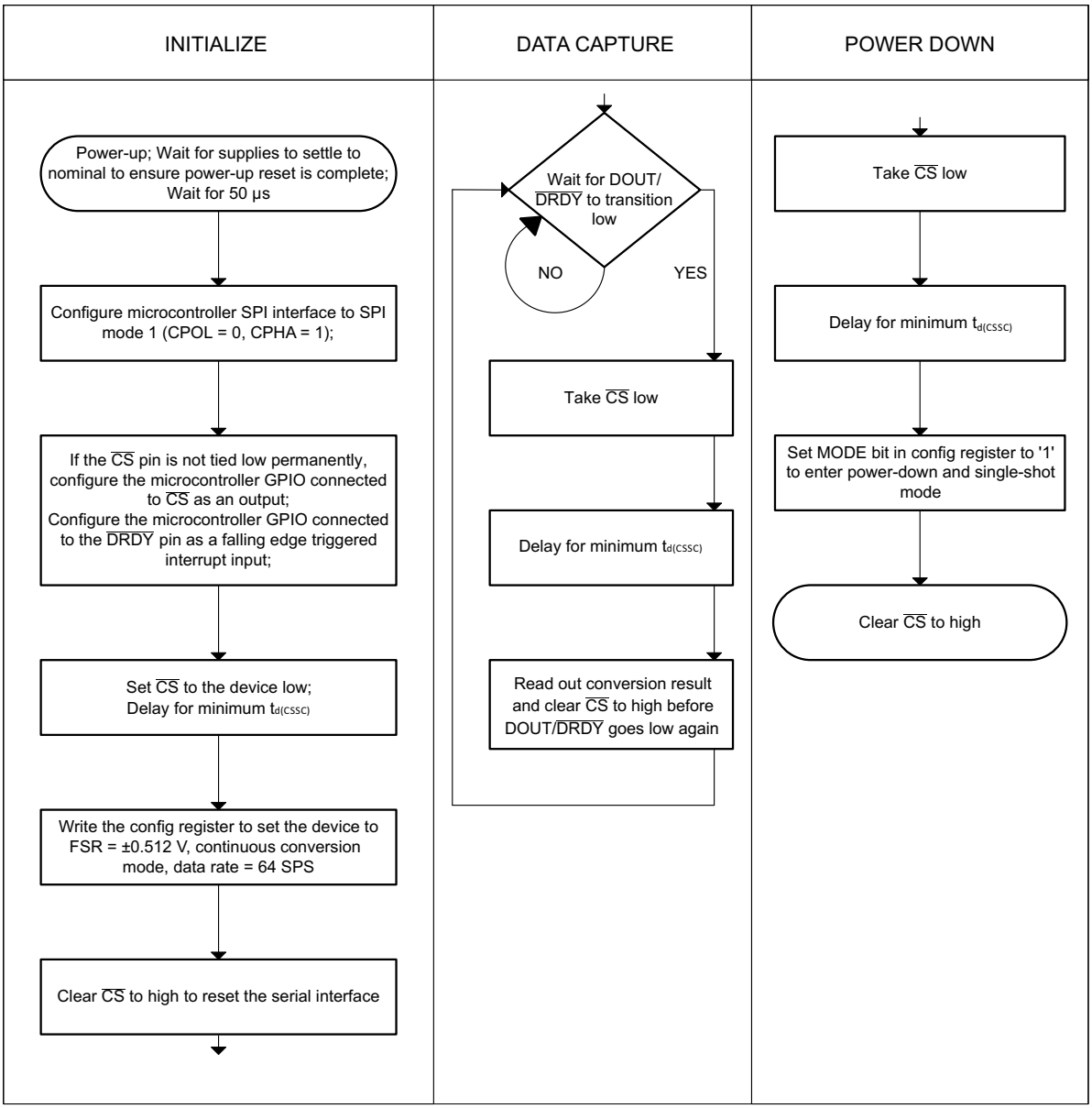


Figure 49. Pseudo Code Example Flow Chart

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10.2 Typical Application

Figure 50 shows the basic connections for an independent, two-channel thermocouple measurement system when using the internal high-precision temperature sensor for cold-junction compensation. Apart from the thermocouples, the only external circuitry required are biasing resistors, first order low-pass, anti-aliasing filters, and a power supply decoupling capacitor.

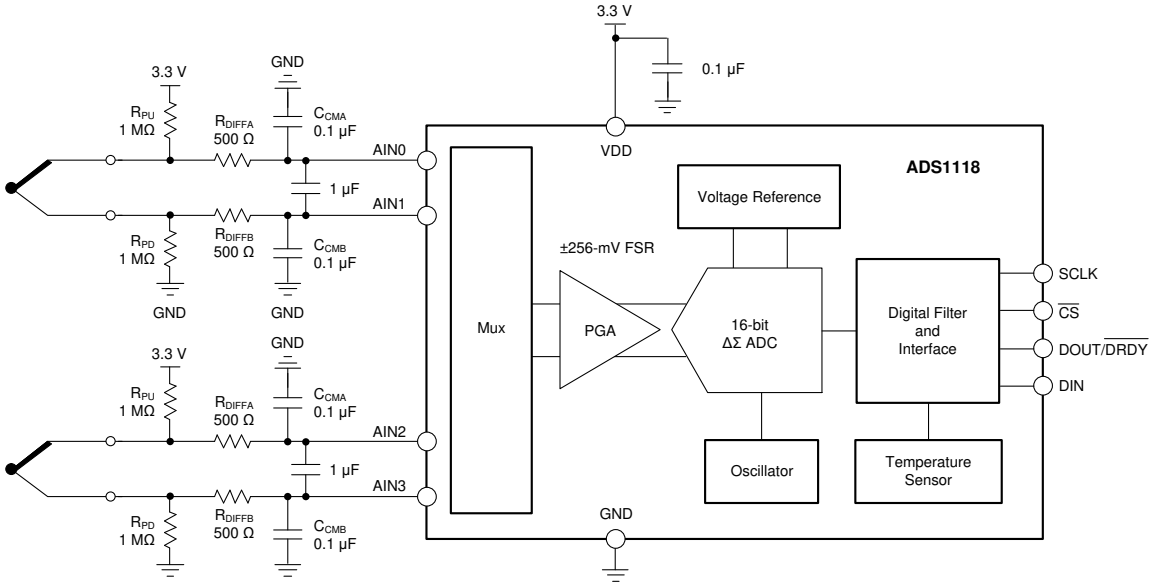


Figure 50. Two-Channel Thermocouple Measurement System

10.2.1 Design Requirements

Table 8 shows the design parameters for this application.

Table 8. Design Parameters

DESIGN PARAMETER	VALUE
Supply voltage	3.3 V
Reference voltage	Internal
Update rate	≥100 readings per second
Thermocouple type	K
Temperature measurement range	–200°C to +1250°C
Measurement accuracy at T_A = 25°C(1)	±0.7°C

(1) With offset calibration, and no gain calibration. Measurement does not account for thermocouple inaccuracy.

10.2.2 Detailed Design Procedure

The biasing resistors (R_{PU} and R_{PD}) serve two purposes. The first purpose is to set the common-mode voltage of the thermocouple to within the specified voltage range of the device. The second purpose is to offer a weak pullup and pulldown to detect an open thermocouple lead. When one of the thermocouple leads fails open, the positive input will be pulled to VDD and the negative input will be pulled to GND. The ADC consequently reads a full-scale value, which is outside the normal measurement range of the thermocouple voltage, to indicate this failure condition. When choosing the values of the biasing resistors, care must be taken so that the biasing current does not degrade measurement accuracy. The biasing current flows through the thermocouple and can cause self-heating and additional voltage drops across the thermocouple leads. Typical values for the biasing resistors range from 1 MΩ to 50 MΩ.

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Although the device digital filter attenuates high-frequency components of noise, TI recommends providing a first-order, passive RC filter at the inputs to further improve performance. The differential RC filter formed by R_{DIFFA}, R_{DIFFB}, and the differential capacitor C_{DIFF} offers a cutoff frequency that is calculated using Equation 5. While the digital filter of the ADS1118 strongly attenuates high-frequency components of noise, TI recommends to provide a first-order, passive RC filter to further suppress high-frequency noise and avoid aliasing. Care must be taken when choosing the filter resistor values because the input currents flowing into and out of the device cause a voltage drop across the resistors. This voltage drop shows up as an additional offset error at the ADC inputs. TI recommends limiting the filter resistor values to below 1 kΩ.

$$f_C = 1 / [2\pi \cdot (R_{DIFFA} + R_{DIFFB}) \cdot C_{DIFF}] \quad (5)$$

Two common-mode filter capacitors (C_{CMA} and C_{CMB}) are also added to offer attenuation of high-frequency, common-mode noise components. TI recommends that the differential capacitor C_{DIFF} be at least an order of magnitude (10x) larger than these common-mode capacitors because mismatches in the common-mode capacitors can convert common-mode noise into differential noise.

The highest measurement resolution is achieved when the largest potential input signal is slightly lower than the FSR of the ADC. From the design requirement, the maximum thermocouple voltage (V_{TC}) occurs at a thermocouple temperature (T_{TC}) of 1250°C. At this temperature, V_{TC} = 50.644 mV, as defined in the tables published by the National Institute of Standards and Technology (NIST) using a cold-junction temperature (T_{CJ}) of 0°C. A thermocouple produces an output voltage that is proportional to the temperature difference between the thermocouple tip and the cold junction. If the cold junction is at a temperature below 0°C, the thermocouple produces a voltage larger than 50.644 mV. The isothermal block area is constrained by the operating temperature range of the device. Therefore, the isothermal block temperature is limited to –40°C. A K-type thermocouple at T_{TC} = 1250°C produces an output voltage of V_{TC} = 50.644 mV – (–1.527 mV) = 52.171 mV when referenced to a cold-junction temperature of T_{CJ} = –40°C. The device offers a full-scale range of ±0.256 V and that is what is used in this application example.

The device integrates a high-precision temperature sensor that can be used to measure the temperature of the cold junction. The temperature sensor mode is enabled by setting bit TS_MODE = 1 in the Config register. The accuracy of the overall temperature sensor depends on how accurately the ADS1118 can measure the cold junction, and hence, careful component placement and PCB layout considerations must be employed for designing an accurate thermocouple system. The ADS1118 Evaluation Module provides a good starting point and offers an example to achieve good cold-junction compensation performance. The ADS1118 Evaluation Module uses the same schematic as shown in Figure 50, except with only one thermocouple channel connected. Refer to the application note, *Precision Thermocouple Measurement With the ADS1118*, SBAA189, for details on how to optimize your component placement and layout to achieve good cold-junction compensation performance.

The calculation procedure to achieve cold-junction compensation can be done in several ways. A typical way is to interleave readings between the thermocouple inputs and the temperature sensor. That is, acquire one on-chip temperature result, T_{CJ}, for every thermocouple ADC voltage measured, V_{TC}. To account for the cold junction, first convert the temperature sensor reading within the ADS1118 to a voltage (V_{CJ}) that is proportional to the thermocouple currently being used. This process is generally accomplished by performing a reverse lookup on the table used for the thermocouple voltage-to-temperature conversion. Adding these two voltages yields the thermocouple-compensated voltage (V_{Actual}), where $V_{Actual} = V_{CJ} + V_{TC}$. V_{Actual} is then converted to a temperature (T_{Actual}) using the same NIST lookup table. A block diagram showing this process is given in Figure 51. Refer to the application note, *Precision Thermocouple Measurement With the ADS1118*, SBAA189, for a detailed explanation of this method.

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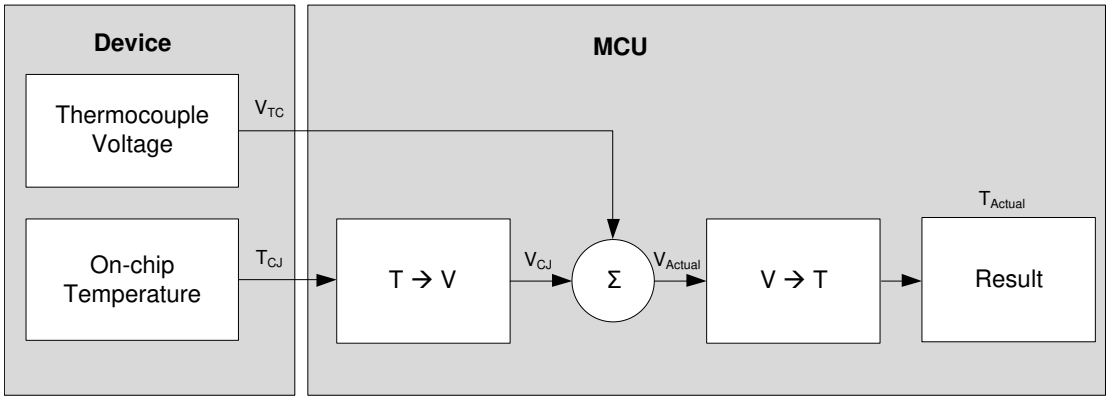


Figure 51. Software Flow Block Diagram

Figure 52 and Figure 53 show the measurement results. The measurements are taken at $T_A = T_{CJ} = 25°C$. A system offset calibration is performed at $T_{TC} = 25°C$ that equates to $V_{TC} = 0$ V when $T_{CJ} = 25°C$. No gain calibration was performed during the measurements. The data in Figure 52 are taken using a precision voltage source as the input signal instead of a thermocouple. The solid black line in Figure 53 is the respective temperature measurement error and is calculated from the data in Figure 52 using the NIST tables. The solid black line in Figure 53 is the measurement error due to the ADC gain and nonlinearity error. The dashed blue lines in Figure 53 include the guard band for the temperature sensor inaccuracy (±0.5°C), in addition to the device gain and nonlinearity error. Note that the measurement results in Figure 52 and Figure 53 do not account for the thermocouple inaccuracy that must also be considered while designing a thermocouple measurement system.

10.2.3 Application Curves

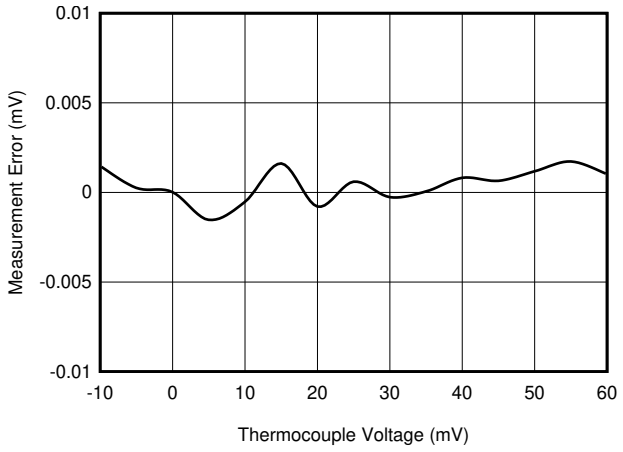


Figure 52. Voltage Measurement Error vs V_{TC}

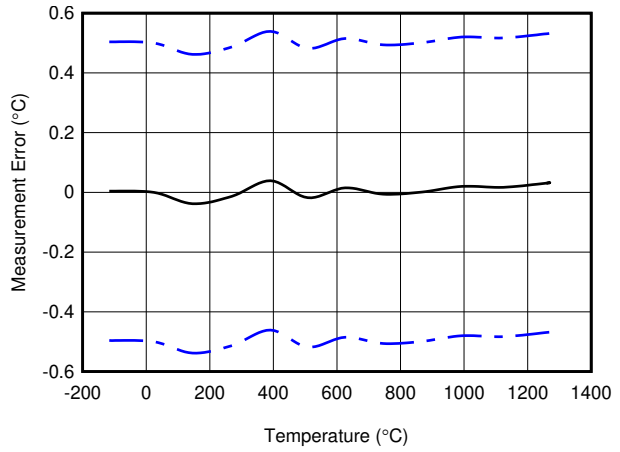


Figure 53. Temperature Measurement Error vs T_{TC}

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11 Power Supply Recommendations

The device requires a single power supply, VDD, to power both the analog and digital circuitry of the device.

11.1 Power-Supply Sequencing

Wait approximately 50 µs after VDD is stabilized before communicating with the device to allow the power-up reset process to complete.

11.2 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. VDD must be decoupled with at least a 0.1-µF capacitor, as shown in Figure 54. The 0.1-µF bypass capacitor supplies the momentary bursts of extra current required from the supply when the ADS1118 is converting. Place the bypass capacitor as close to the power-supply pin of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

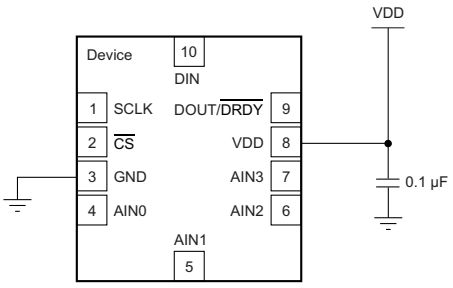


Figure 54. Power Supply Decoupling

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12 Layout

12.1 Layout Guidelines

TI recommends employing best design practices when laying out a printed-circuit-board (PCB) for both analog and digital components. This recommendation generally means that the layout separates analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. An example of good component placement is shown in Figure 55. Although Figure 55 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog component.

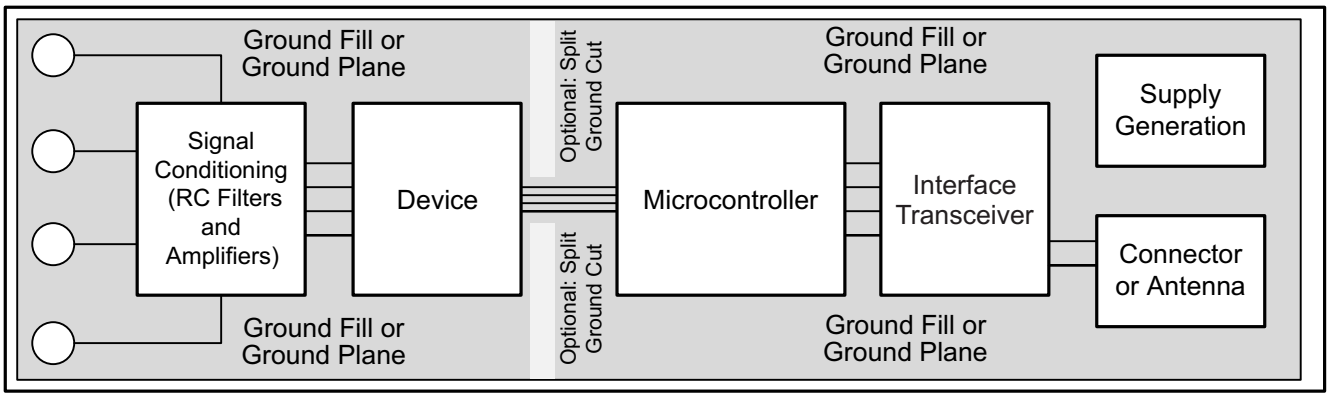


Figure 55. System Component Placement

The use of split analog and digital ground planes is not necessary for improved noise performance (although for thermal isolation this option is a worthwhile consideration). However, the use of a solid ground plane or ground fill in PCB areas with no components is essential for optimum performance. If the system being used employs a split digital and analog ground plane, TI generally recommends that the ground planes be connected together as close to the device as possible. A two-layer board is possible using common grounds for both analog and digital grounds. Additional layers can be added to simplify PCB trace routing. Ground fill may also reduce EMI and RFI issues.

TI also strongly recommends that digital components, especially RF portions, be kept as far as practically possible from analog circuitry in a given system. Additionally, minimize the distance that digital control traces run through analog areas and avoid placing these traces near sensitive analog components. Digital return currents usually flow through a ground path that is as close to the digital path as possible. If a solid ground connection to a plane is not available, these currents may find paths back to the source that interfere with analog performance. The implications that layout has on the temperature-sensing functions are much more significant than for ADC functions.

Supply pins must be bypassed to ground with a low-ESR ceramic capacitor. The optimum placement of the bypass capacitors is as close as possible to the supply pins. The ground-side connections of the bypass capacitors must be low-impedance connections for optimum performance. The supply current flows through the bypass capacitor terminal first and then to the supply pin to make the bypassing most effective.

Analog inputs with differential connections must have a capacitor placed differentially across the inputs. The differential capacitors must be of high quality. The best ceramic chip capacitors are C0G (NPO), which have stable properties and low noise characteristics. Thermally isolate a copper region around the thermocouple input connections to create a thermally-stable cold junction. Obtaining acceptable performance with alternate layout schemes is possible as long as the above guidelines are followed.

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12.2 Layout Example

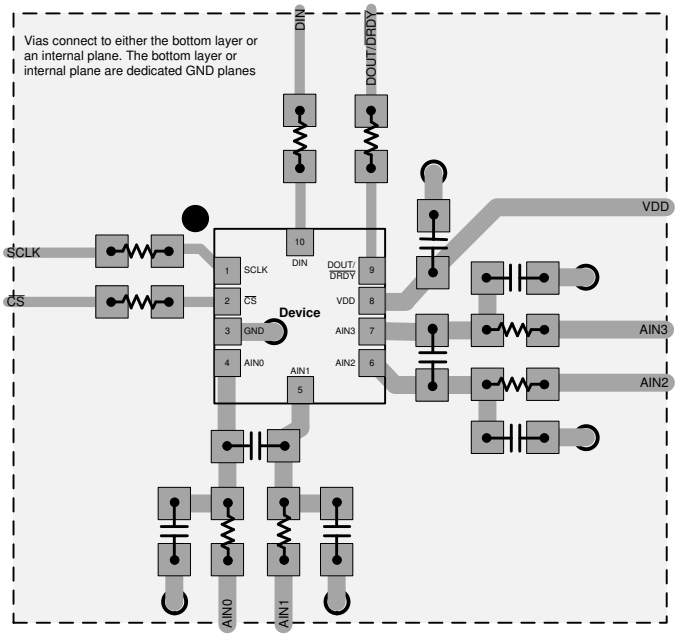


Figure 56. X2QFN Package

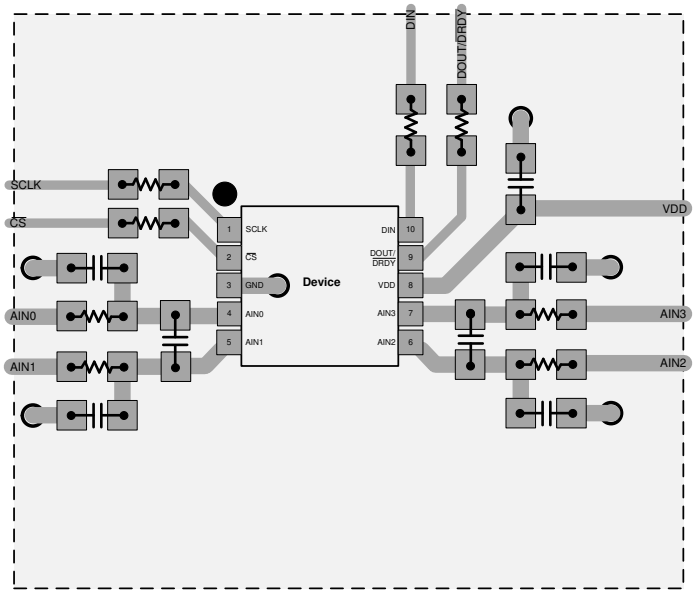


Figure 57. VSSOP Package

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13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《使用 ADS1118 进行精密热电偶测量》* 应用报告
- 德州仪器 (TI)，*《ADS1118EVM 用户指南和软件教程》* 用户指南
- 德州仪器 (TI)，*《430BOOST-ADS1118 Booster Pack》* 用户指南
- 德州仪器 (TI)，*《ADS1118 Boosterpack》* 快速入门
- 德州仪器 (TI)，*《模数规格和性能特性术语表》* 应用报告

13.2 接收文档更新通知

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13.3 社区资源

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS1118IDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BBEI
ADS1118IDGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BBEI
ADS1118IDGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BBEI
ADS1118IDGST	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BBEI
ADS1118IDGST.A	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BBEI
ADS1118IDGST.B	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BBEI
ADS1118IRUGR	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDQ
ADS1118IRUGR.A	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDQ
ADS1118IRUGR.B	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDQ
ADS1118IRUGT	Active	Production	X2QFN (RUG) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDQ
ADS1118IRUGT.A	Active	Production	X2QFN (RUG) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDQ
ADS1118IRUGT.B	Active	Production	X2QFN (RUG) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDQ
ADS1118IRUGTG4	Active	Production	X2QFN (RUG) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDQ
ADS1118IRUGTG4.A	Active	Production	X2QFN (RUG) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDQ
ADS1118IRUGTG4.B	Active	Production	X2QFN (RUG) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ADS1118 :

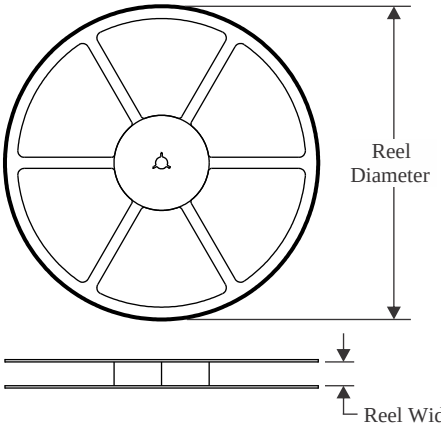
- Automotive : ADS1118-Q1

NOTE: Qualified Version Definitions:

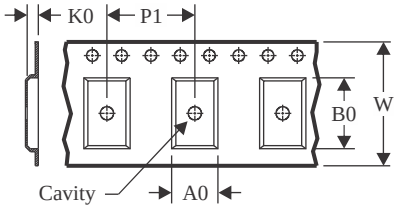
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

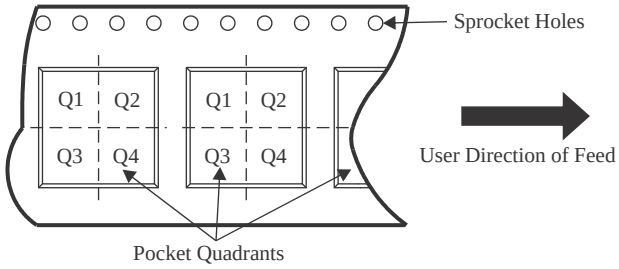


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

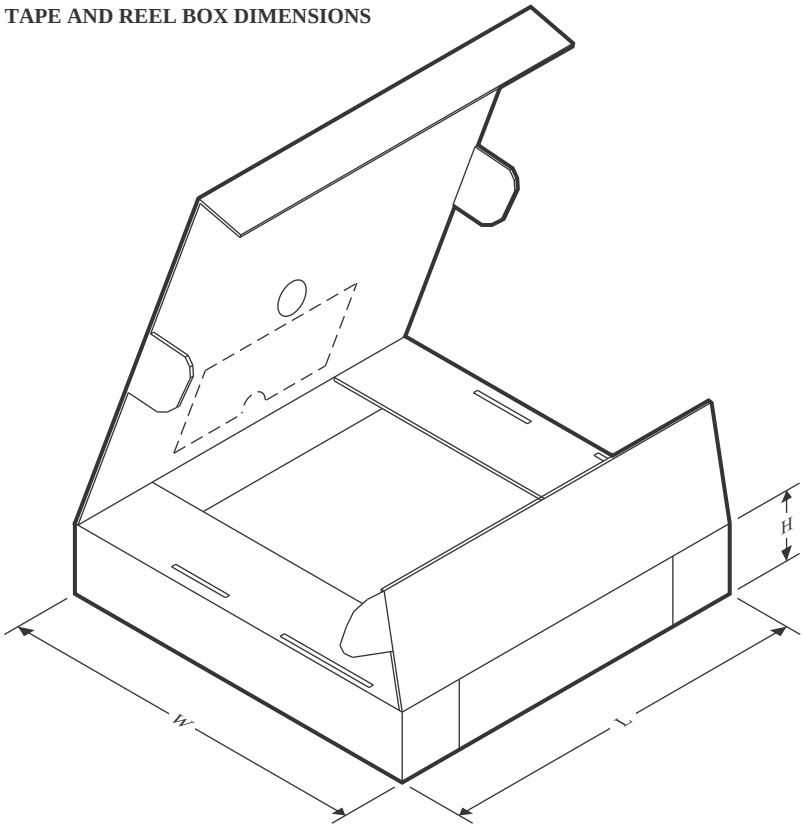
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1118IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
ADS1118IDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
ADS1118IRUGR	X2QFN	RUG	10	3000	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
ADS1118IRUGT	X2QFN	RUG	10	250	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
ADS1118IRUGTG4	X2QFN	RUG	10	250	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1118IDGSR	VSSOP	DGS	10	2500	367.0	367.0	38.0
ADS1118IDGST	VSSOP	DGS	10	250	213.0	191.0	35.0
ADS1118IRUGR	X2QFN	RUG	10	3000	210.0	185.0	35.0
ADS1118IRUGT	X2QFN	RUG	10	250	210.0	185.0	35.0
ADS1118IRUGTG4	X2QFN	RUG	10	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

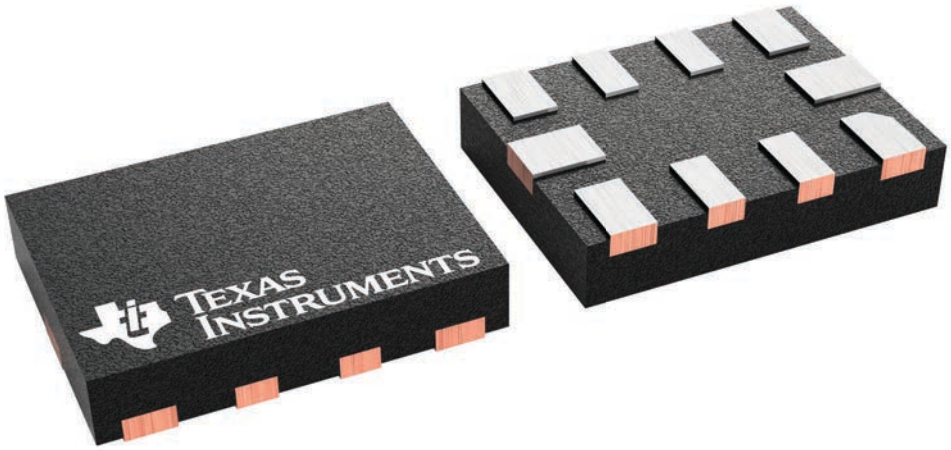
RUG 10

X2QFN - 0.4 mm max height

1.5 x 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



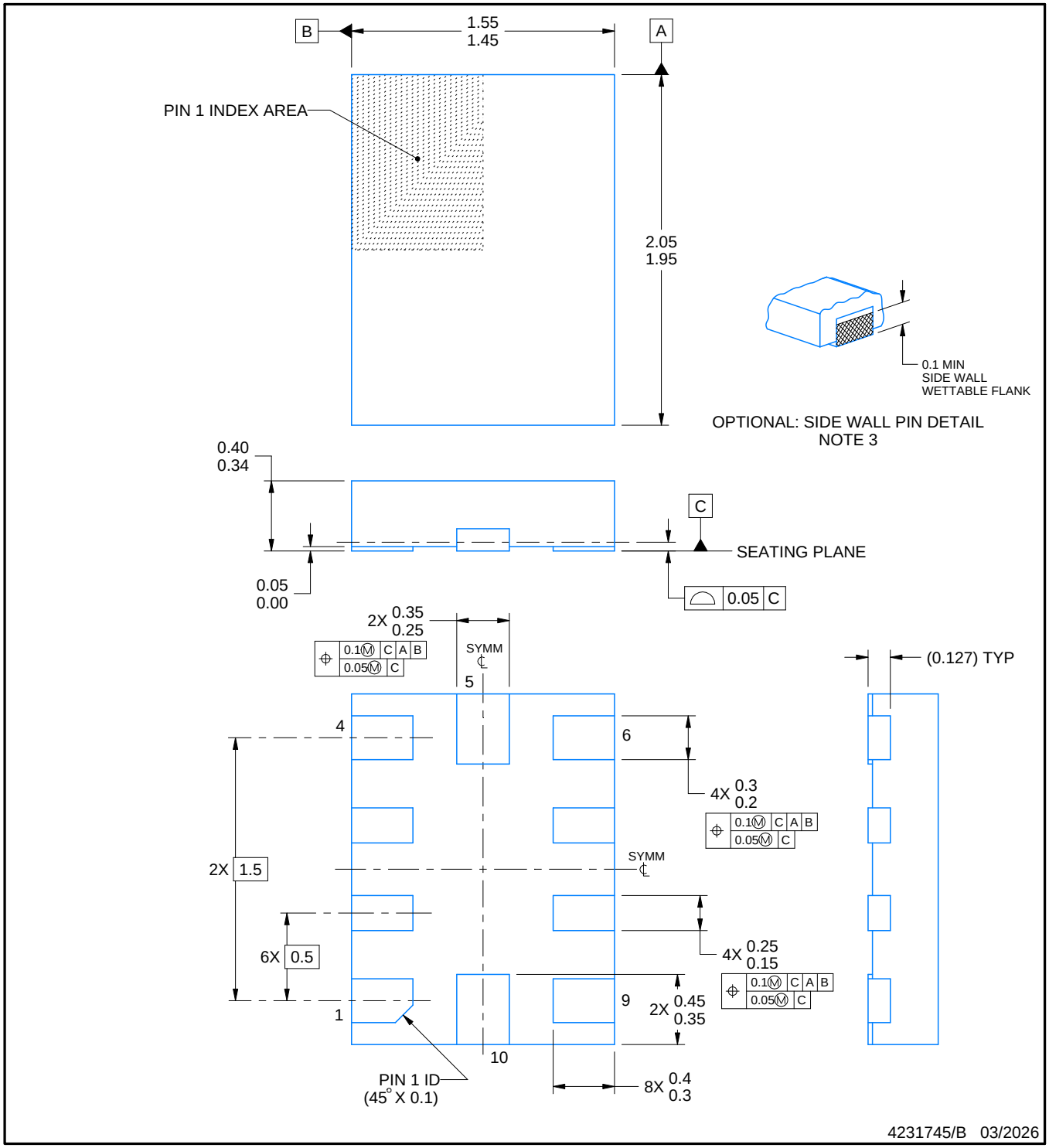
4231768/A

RUG0010A

PACKAGE OUTLINE

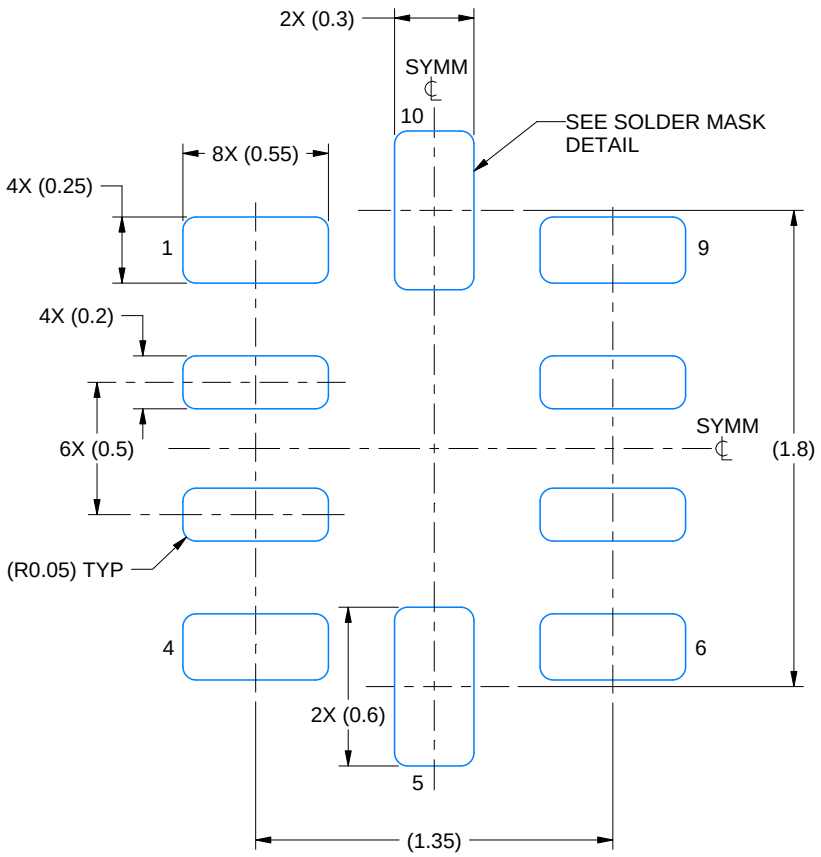
X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

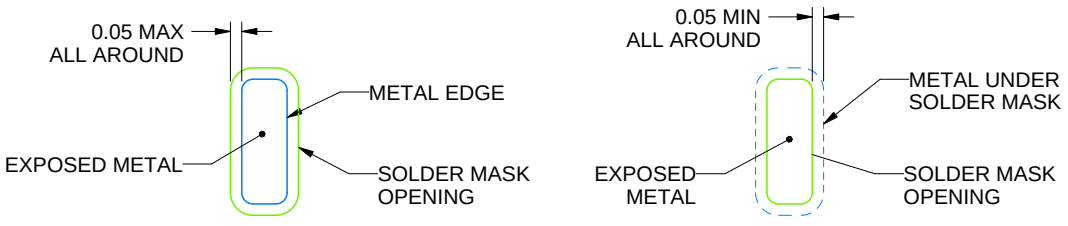


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 35X



SOLDER MASK DETAILS

4231745/B 03/2026

NOTES: (continued)

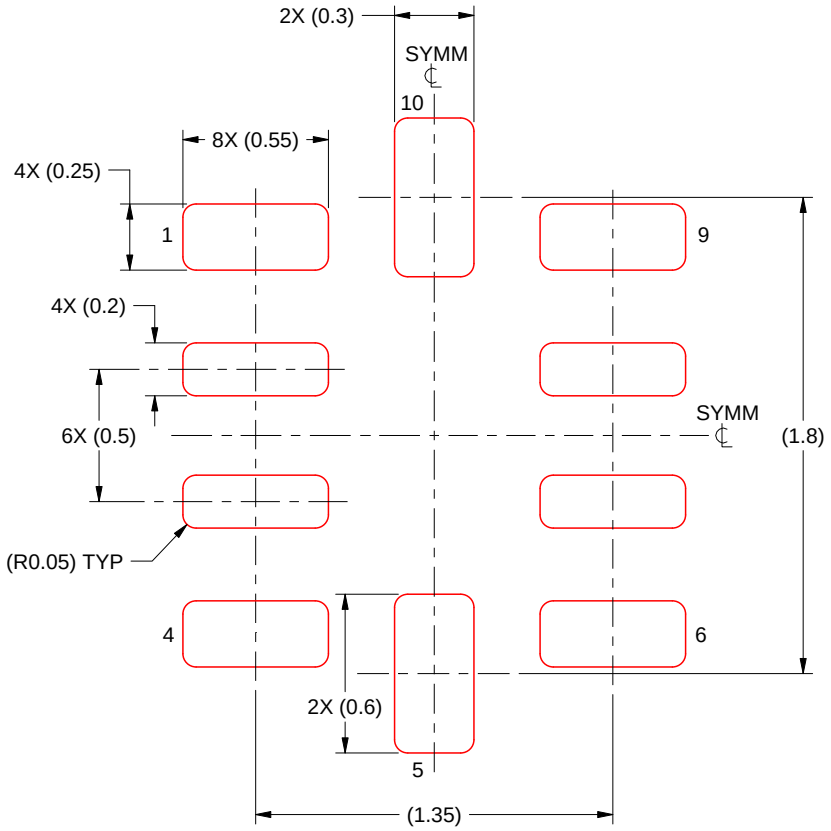
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RUG0010A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 35X

4231745/B 03/2026

NOTES: (continued)

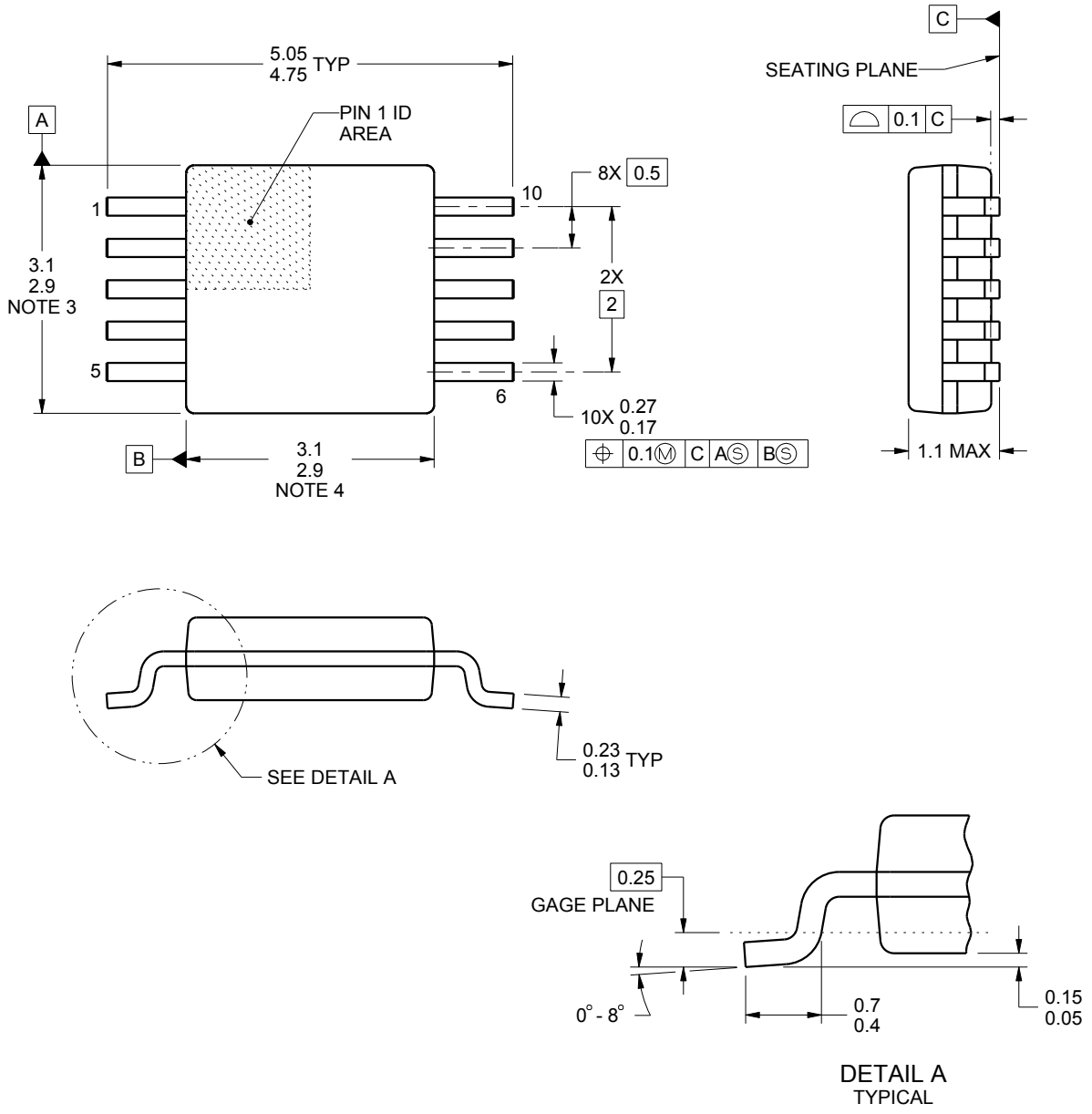
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGS0010A

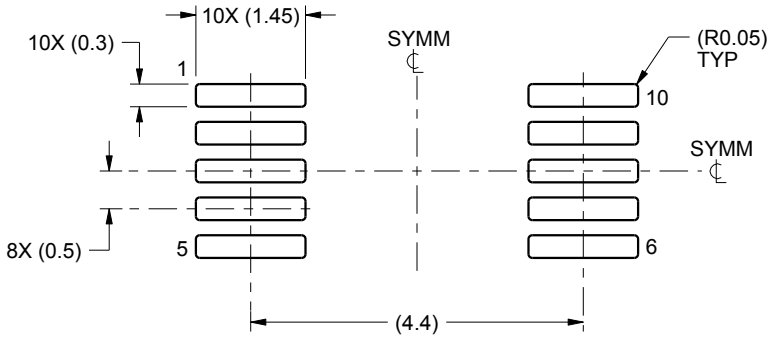
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

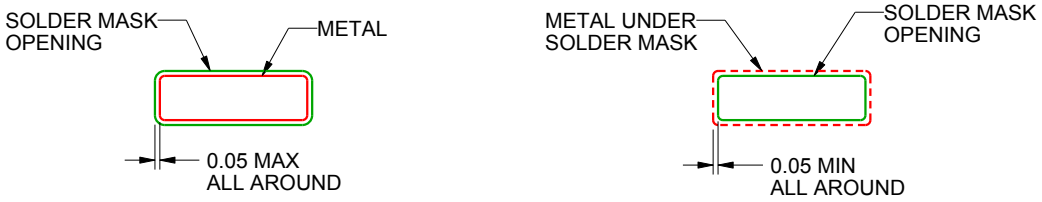


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

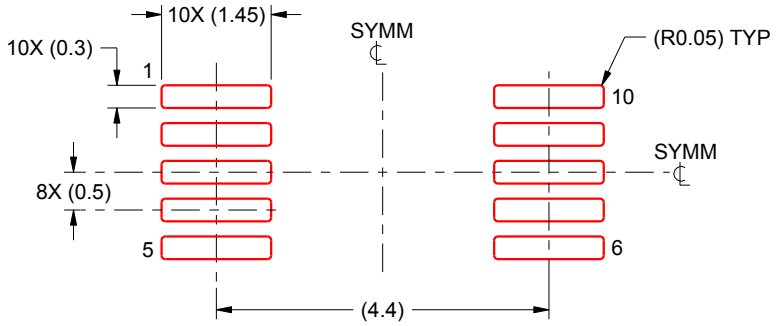


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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