16-BIT, 500-KSPS, SERIAL INTERFACE MICROPOWER, MINIATURE, SAR ANALOG-TO-DIGITAL CONVERTER

Check for Samples: ADS8318

FEATURES

- **500-kHz Sample Rate**
- **16-Bit Resolution**
- **Zero Latency at Full Speed**
- **Unipolar, Differential Input, Range: $-V_{ref}$ to V_{ref}**
- **SPI Compatible Serial Interface with Daisy Chain Option**
- **Excellent Performance:**
  - **95.2dB SNR Typ at 10-kHz I/P**
  - **–108dB THD Typ at 10-kHz I/P**
  - **±1.0 LSB Max INL**
  - **±0.75 LSB Max DNL**
- **Low Power Dissipation: 18 mW Typ at 500 KSPS**
- **Power Scales Linearly with Speed: 3.6 mW/100 KSPS**
- **Power Dissipation During Power-Down State: 0.25 µW Typ**
- **10-Pin MSOP and SON Packages**

APPLICATIONS

- **Battery Powered Equipments**
- **Data Acquisition Systems**
- **Instrumentation and Process Control**
- **Medical Electronics**
- **Optical Networking**

DESCRIPTION

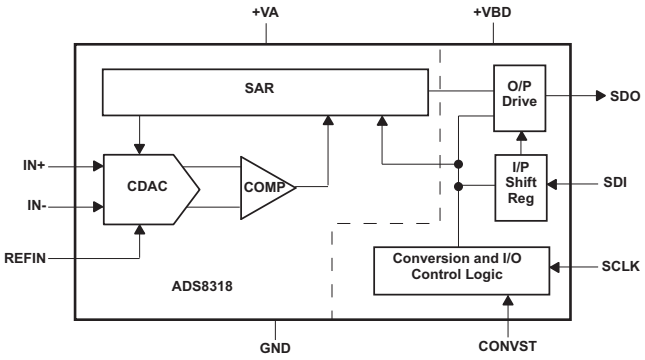
The ADS8318 is a 16-bit, 500-KSPS analog-to-digital converter. It operates with a 2.048-V to 5.5-V external reference. The device includes a capacitor based, SAR A/D converter with inherent sample and hold.

The devices includes a 50-MHz SPI compatible serial interface. The interface is designed to support daisy chaining or cascading of multiple devices. Also a *Busy Indicator* makes it easy to synchronize with the digital host.

The ADS8318 unipolar differential input range supports a differential input swing of $-V_{ref}$ to $+V_{ref}$ with a common-mode of $+V_{ref}/2$.

Device operation is optimized for very low power operation, and the power consumption directly scales with speed. This feature makes it attractive for lower speed applications.

It is available in 10-pin MSOP and SON packages.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

DEVICE	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES AT RESOLUTION (BIT)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	PACKAGE MARKING	ORDERING INFORMATION	TRANSPORT MEDIA QUANTITY
ADS8318I	±1.5	±1	16	10 Pin MSOP	DGS	–40°C to 85°C	CBC	ADS8318IDGST	250
								ADS8318IDGSR	2500
				10 Pin SON	DRC		CBE	ADS8318IDRCT	250
								ADS8318IDRCR	2500
ADS8318IB	±1.0	±0.75	16	10 Pin MSOP	DGS	–40°C to 85°C	CBC	ADS8318IBDGST	250
								ADS8318IBDGSR	2500
				10 Pin SON	DRC		CBE	ADS8318IBDRCT	250
								ADS8318IBDRCR	2500

(1) For the most current specifications and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			VALUE	UNIT
	+IN		–0.3 to +VA + 0.3	V
			±130	mA
	–IN		–0.3 to +VA + 0.3	V
			±130	mA
	+VA to AGND		–0.3 to 7	V
	+VBD to BDGND		–0.3 to 7	V
	Digital input voltage to GND		–0.3 to +VBD + 0.3	V
	Digital output to GND		–0.3 to +VBD + 0.3	V
T_A	Operating free-air temperature range		–40 to 85	°C
T_{stg}	Storage temperature range		–65 to 150	°C
	Junction temperature (T_J max)		150	°C
	MSOP package	Power dissipation	$(T_J Max – T_A)/\theta_{JA}$	°C
		θ_{JA} thermal impedance	180	°C/W
	Maximum MSOP reflow temperature	ADS8318 is rated to MSL2 260°C per the JSTD-020 specification		
	SON package	Power dissipation	$(T_J Max – T_A)/\theta_{JA}$	
		θ_{JA} thermal impedance	70	°C/W
	Maximum SON reflow temperature	ADS8318 is rated to MSL2 260°C per the JSTD-020 specification		

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SPECIFICATIONS

T_A = –40°C to 85°C, +VA = 5 V, +VBD = 5 V to 2.375 V, V_{ref} = 4 V, f_{SAMPLE} = 500 kHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT							
	Full-scale input span (1)		+IN – (–IN)	$–V_{ref}$		V_{ref}	V
	Operating input range		+IN	– 0.1		V_{ref} + 0.1	
			–IN	– 0.1		V_{ref} + 0.1	
	Input common-mode range			0	V_{ref}/2	V_{ref}/2+0.1	V
	Input capacitance		+IN and -IN terminal to GND		59		pF
	Input leakage current		During acquisition		1000		pA
SYSTEM PERFORMANCE							
	Resolution				16		Bits
	No missing codes			16			Bits
INL	Integral linearity(2)	ADS8318I		–1.5	±0.65	1.5	LSB(3)
		ADS8318IB		–1	±0.65	1	
DNL	Differential linearity	ADS8318I	At 16-bit level	–1	±0.4	1	LSB(3)
		ADS8318IB		–0.75	±0.4	0.75	
E_O	Offset error(4)			–1.5	±0.3	1.5	mV
E_G	Gain error			–0.03	±0.003	0.03	%FSR
CMRR	Common-mode rejection ratio		With common mode input signal = 200 mV_{p-p} at 500 kHz		78		dB
PSRR	Power supply rejection ratio		At FFF0h output code		80		dB
	Transition noise				0.25		LSB
SAMPLING DYNAMICS							
t_{CONV}	Conversion time		+VBD = 5 V			1400	ns
			+VBD = 3 V			1400	
	Acquisition time		+VBD = 5 V	600			ns
			+VBD = 3 V	600			
	Maximum throughput rate with or without latency					0.5	MHz
	Aperture delay				2.5		ns
	Aperture jitter, RMS				6		ps
	Step response		Settling to 16-bit accuracy		600		ns
	Overvoltage recovery				600		ns

(1) Ideal input span, does not include gain or offset error.
(2) This is endpoint INL, not best fit.
(3) LSB means least significant bit
(4) Measured relative to actual measured reference.

SPECIFICATIONS (continued)

T_A = –40°C to 85°C, +VA = 5 V, +VBD = 5 V to 2.375 V, V_{ref} = 4 V, f_{SAMPLE} = 500 kHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
THD	Total harmonic distortion (5)		V_{IN} 0.4 dB below FS at 1 kHz, V_{ref} = 5 V		–114		dB
			V_{IN} 0.4 dB below FS at 10 kHz, V_{ref} = 5 V		–108		
			V_{IN} 0.4 dB below FS at 100 kHz, V_{ref} = 5 V		–91.5		
SNR	Signal-to-noise ratio		V_{IN} 0.4 dB below FS at 1 kHz, V_{ref} = 5 V		96		dB
			V_{IN} 0.4 dB below FS at 10 kHz, V_{ref} = 5 V		95.2		
			V_{IN} 0.4 dB below FS at 100 kHz, V_{ref} = 5 V		92.5		
		ADS8318IB	V_{IN} 0.4 dB below FS at 1 kHz, V_{ref} = 5 V	95.5			
SINAD	Signal-to-noise + distortion		V_{IN} 0.4 dB below FS at 1 kHz, V_{ref} = 5 V		96		dB
			V_{IN} 0.4 dB below FS at 10 kHz, V_{ref} = 5 V		95		
			V_{IN} 0.4 dB below FS at 100 kHz, V_{ref} = 5 V		89.5		
SFDR	Spurious free dynamic range		V_{IN} 0.4 dB below FS at 1 kHz, V_{ref} = 5 V		116		dB
			V_{IN} 0.4 dB below FS at 10 kHz, V_{ref} = 5 V		109		
			V_{IN} 0.4 dB below FS at 100 kHz, V_{ref} = 5 V		92		
	–3dB Small signal bandwidth				15		MHz
EXTERNAL REFERENCE INPUT							
V_{ref}	Input range			2.048	4.096	VDD+0.1	V
	Reference input current (6)		During conversion		250		µA
POWER SUPPLY REQUIREMENTS							
	Power supply voltage	+VBD		2.375	3.3	5.5	V
		+VA		4.5	5	5.5	V
	Supply current	+VA	500-kHz Sample rate		3.6	4.5	mA
P_{VA}	Power dissipation		+VA = 5 V, 500-kHz Sample rate		18	22.5	mW
IVA_{pd}	Device power-down current(7)		+VA = 5 V		50	300	nA
LOGIC FAMILY CMOS							
V_{IH}	Logic level		I_{IH} = 5 µA	+(0.7×VBD)		$+V_{BD}$+0.3	V
V_{IL}			I_{IL} = 5 µA	–0.3		+(0.3×VBD)	V
V_{OH}			I_{OH} = 2 TTL loads	$+V_{BD}$–0.3		$+V_{BD}$	V
V_{OL}			I_{OL} = 2 TTL loads	0		0.4	V
TEMPERATURE RANGE							
T_A	Operating free-air temperature			–40		85	°C

(5) Calculated on the first nine harmonics of the input frequency
(6) Can vary ±20%
(7) Device automatically enters power-down state at the end of every conversion, and continues to be in power-down state as long as it is in acquisition phase.

TIMING REQUIREMENTS

All specifications typical at –40°C to 85°C, +VA = 5 V, +VBD ≥ 3.1 V

PARAMETER		REF FIGURE	MIN	TYP	MAX	UNIT
SAMPLING AND CONVERSION RELATED						
t_{acq}	Acquisition time	Figure 46, Figure 48, Figure 50, Figure 52	600			ns
t_{cnv}	Conversion time				1400	ns
t_{cyc}	Time between conversions		2000			ns
t_1	Pulse duration, CONVST high	Figure 46, Figure 48	10			ns
t_6	Pulse duration, CONVST low	Figure 50, Figure 52, Figure 54	20			ns
I/O RELATED						
t_{clk}	SCLK Period	Figure 46, Figure 48, Figure 50, Figure 52, Figure 54, Figure 56	20			ns
t_{clkl}	SCLK Low time		8			ns
t_{clkh}	SCLK High time		8			ns
t_2	SCLK Falling edge to data remains valid		5			ns
t_3	SCLK Falling edge to next data valid delay				16	ns
t_{en}	Enable time, CONVST or SDI Low to MSB valid	Figure 46, Figure 50			15	ns
t_{dis}	Disable time, CONVST or SDI high or last SCLK falling edge to SDO 3-state ($\overline{CS}$ mode)	Figure 46, Figure 48, Figure 50, Figure 52			12	ns
t_4	Setup time, SDI valid to CONVST rising edge	Figure 50, Figure 52	5			ns
t_5	Hold time, SDI valid from CONVST rising edge		5			ns
t_7	Setup time, SCLK valid to CONVST rising edge	Figure 54	5			ns
t_8	Hold time, SCLK valid from CONVST rising edge		5			ns

TIMING REQUIREMENTS

All specifications typical at –40°C to 85°C, +VA = 5 V, +3.1 V > +VBD ≥ 2.375 V

PARAMETER		REF FIGURE	MIN	TYP	MAX	UNIT
SAMPLING AND CONVERSION RELATED						
t_{acq}	Acquisition time	Figure 46, Figure 48, Figure 50, Figure 52	600			ns
t_{cnv}	Conversion time				1400	ns
t_{cyc}	Time between conversions		2000			ns
t_1	Pulse width CONVST high	Figure 46, Figure 48	10			ns
t_6	Pulse width CONVST low	Figure 50, Figure 52, Figure 54	20			ns
I/O RELATED						
t_{clk}	SCLK period	Figure 46, Figure 48, Figure 50, Figure 52, Figure 54, Figure 56	30			ns
t_{clkl}	SCLK low time		13			ns
t_{clkh}	SCLK high time		13			ns
t_2	SCLK falling edge to data remains valid		5			ns
t_3	SCLK falling edge to next data valid delay				24	ns
t_{en}	CONVST or SDI low to MSB valid	Figure 46, Figure 50			22	ns
t_{dis}	CONVST or SDI high or last SCLK falling edge to SDO 3-state ($\overline{CS}$ mode)	Figure 46, Figure 48, Figure 50, Figure 52			15	ns
t_4	SDI valid setup time to CONVST rising edge	Figure 50, Figure 52	5			ns
t_5	SDI valid hold time from CONVST rising edge		5			ns
t_7	SCLK valid setup time to CONVST rising edge	Figure 54	5			ns
t_8	SCLK valid hold time from CONVST rising edge		5			ns

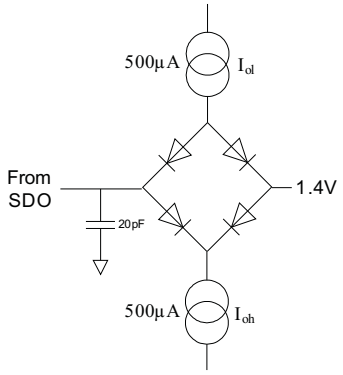


Figure 1. Load Circuit for Digital Interface Timing

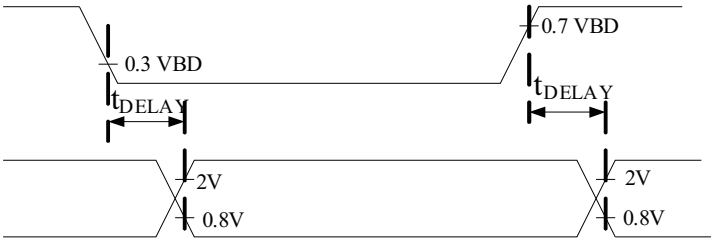
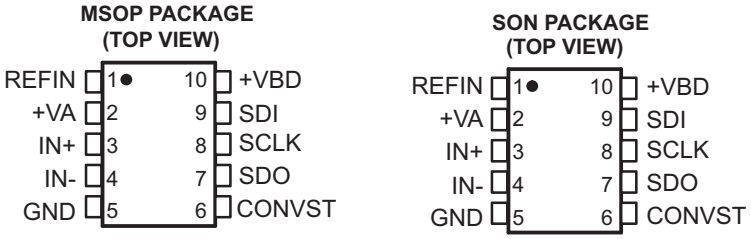


Figure 2. Voltage Levels for Timing

PIN ASSIGNMENTS



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NO.	NAME		
ANALOG PINS			
1	REFIN	I	Reference (positive) input. Decouple with GND pin using 0.1-µF bypass capacitor and 10-µF storage capacitor.
3	+IN	I	Noninverting analog signal input
4	–IN	I	Inverting analog signal input
I/O PINS			
6	CONVST	I	Convert input. It also functions as the $\overline{CS}$ input in 3-wire interface mode. Refer to Description and Timing Diagrams sections for more details.
7	SDO	O	Serial data output.
8	SCLK	I	Serial I/O clock input. Data (on SDO o/p) is synchronized with this clock.
9	SDI	I	Serial data input. The SDI level at the start of a conversion selects the mode of operation such as $\overline{CS}$ or daisy chain mode. It also serves as the $\overline{CS}$ input in 4-wire interface mode. Refer to Description and Timing Diagrmas sections for more details.
POWER SUPPLY PINS			
2	+VA	–	Analog power supply. Decoupled with GND pin.
5	GND	–	Device ground. Note this is a common ground pin for both analog power supply (+VA) and digital I/O supply (+VBD).
10	+VBD	–	Digital I/O power supply. Decouple with GND pin.

TYPICAL CHARACTERISTICS

OFFSET ERROR vs SUPPLY VOLTAGE

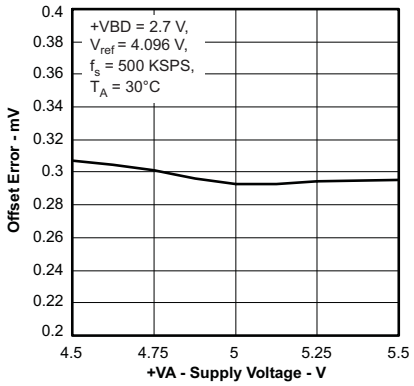


Figure 3.

GAIN ERROR vs SUPPLY VOLTAGE

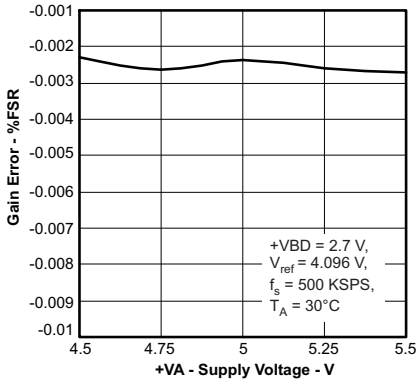


Figure 4.

OFFSET ERROR vs REFERENCE VOLTAGE

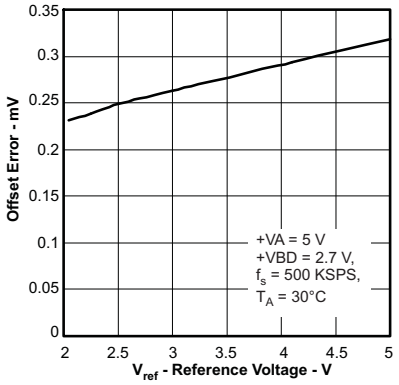


Figure 5.

TYPICAL CHARACTERISTICS (continued)

GAIN ERROR vs REFERENCE VOLTAGE

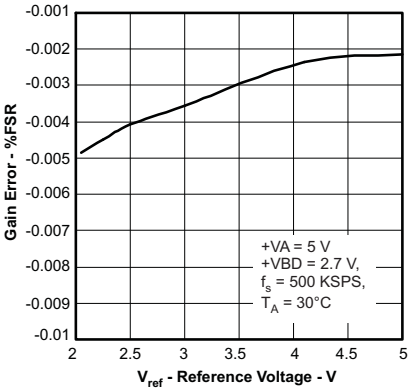


Figure 6.

OFFSET ERROR vs FREE-AIR TEMPERATURE

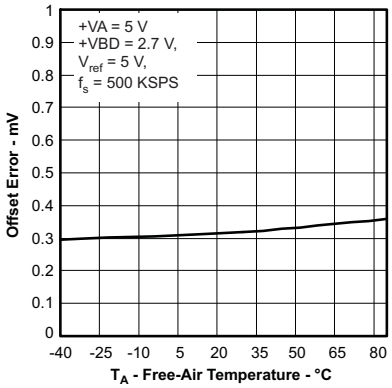


Figure 7.

GAIN ERROR vs FREE-AIR TEMPERATURE

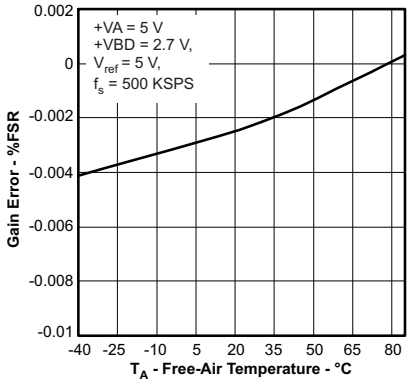


Figure 8.

GAIN ERROR DRIFT HISTOGRAM

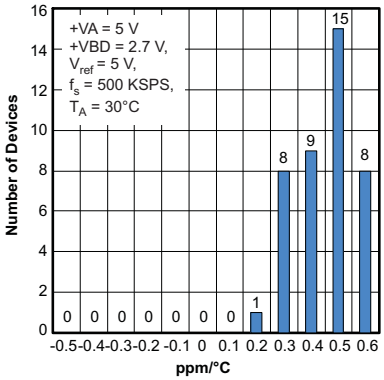


Figure 9.

OFFSET ERROR DRIFT HISTOGRAM

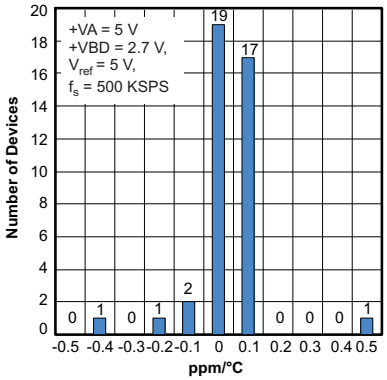


Figure 10.

DIFFERENTIAL NONLINEARITY vs SUPPLY VOLTAGE

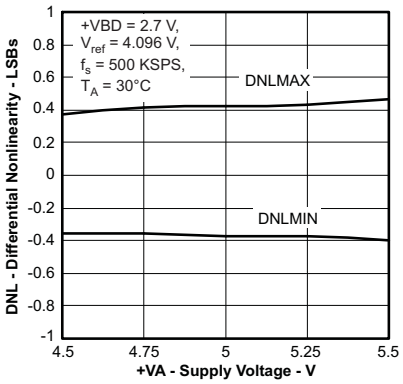


Figure 11.

INTEGRAL NONLINEARITY vs SUPPLY VOLTAGE

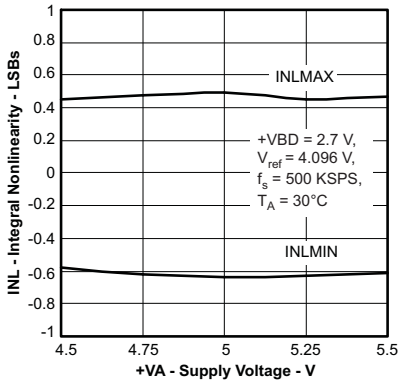


Figure 12.

DIFFERENTIAL NONLINEARITY vs REFERENCE VOLTAGE

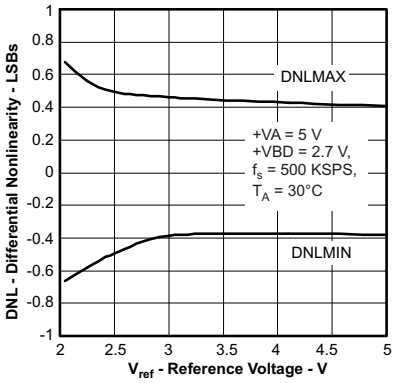


Figure 13.

INTEGRAL NONLINEARITY vs REFERENCE VOLTAGE

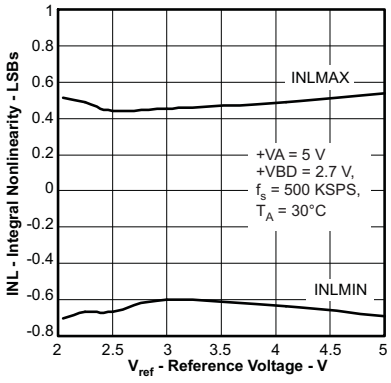


Figure 14.

TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL NONLINEARITY vs FREE-AIR TEMPERATURE

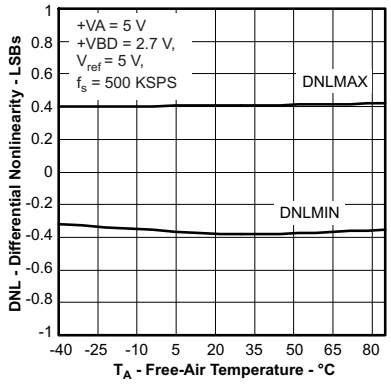


Figure 15.

INTEGRAL NONLINEARITY vs FREE-AIR TEMPERATURE

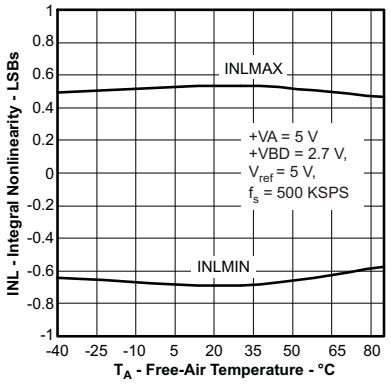


Figure 16.

EFFECTIVE NUMBER OF BITS vs SUPPLY VOLTAGE

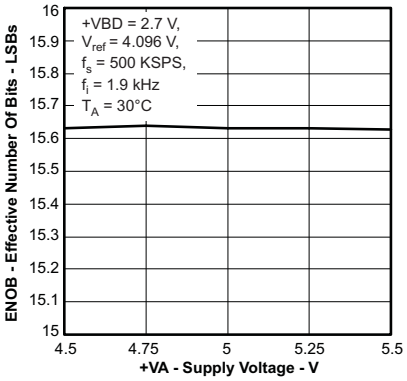


Figure 17.

EFFECTIVE NUMBER OF BITS vs REFERENCE VOLTAGE

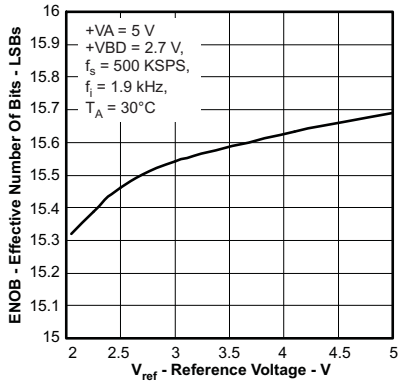


Figure 18.

EFFECTIVE NUMBER OF BITS vs FREE-AIR TEMPERATURE

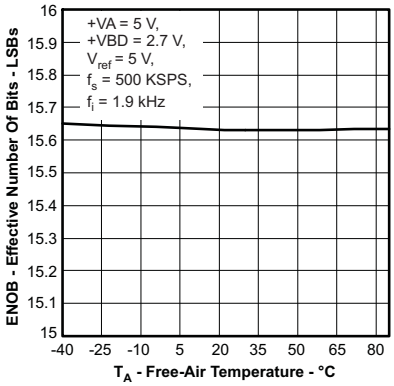


Figure 19.

SPURIOUS FREE DYNAMIC RANGE vs SUPPLY VOLTAGE

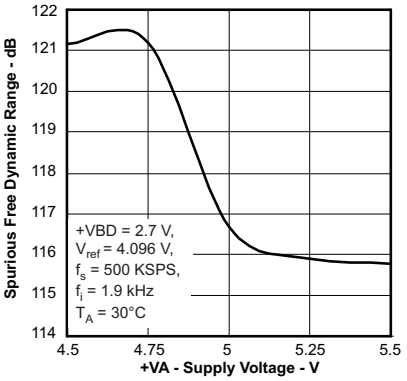


Figure 20.

SIGNAL-TO-NOISE + DISTORTION vs SUPPLY VOLTAGE

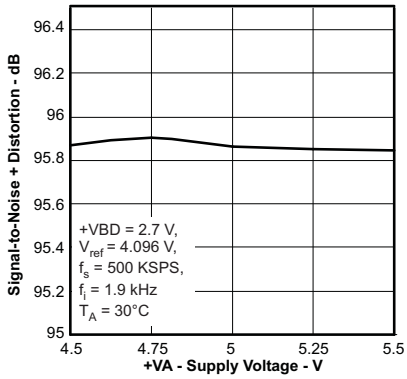


Figure 21.

SIGNAL-TO-NOISE RATIO vs SUPPLY VOLTAGE

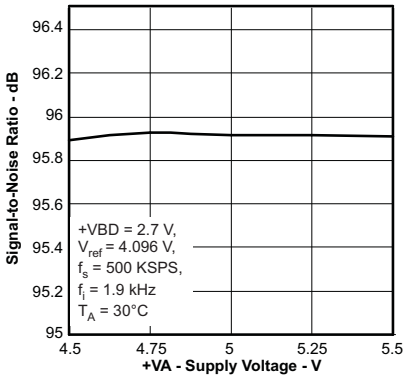


Figure 22.

TOTAL HARMONIC DISTORTION vs SUPPLY VOLTAGE

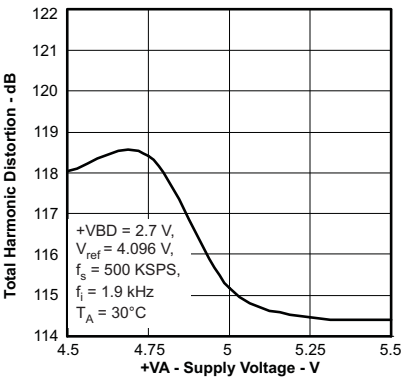


Figure 23.

TYPICAL CHARACTERISTICS (continued)

SPURIOUS FREE DYNAMIC RANGE vs REFERENCE VOLTAGE

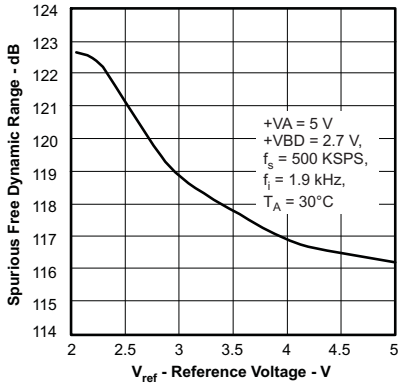


Figure 24.

SIGNAL-TO-NOISE + DISTORTION vs REFERENCE VOLTAGE

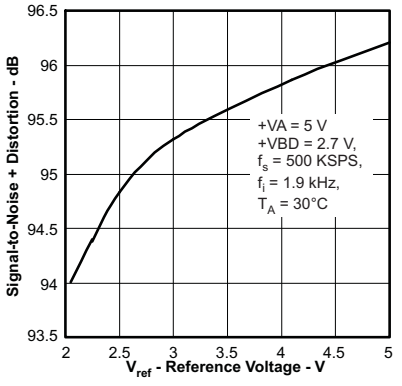


Figure 25.

SIGNAL-TO-NOISE RATIO vs REFERENCE VOLTAGE

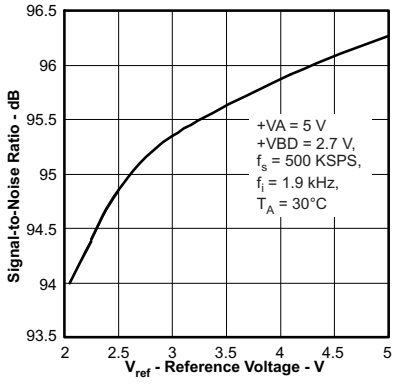


Figure 26.

TOTAL HARMONIC DISTORTION vs REFERENCE VOLTAGE

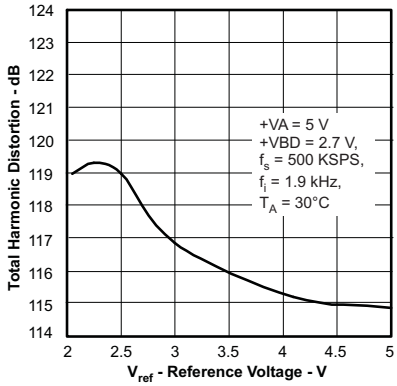


Figure 27.

SPURIOUS FREE DYNAMIC RANGE vs FREE-AIR TEMPERATURE

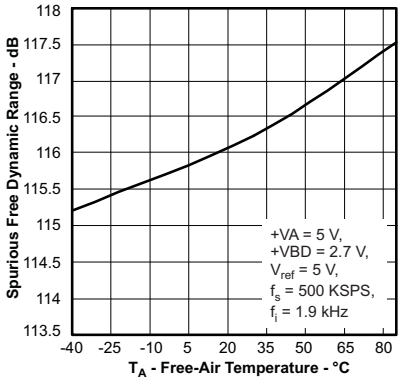


Figure 28.

SIGNAL-TO-NOISE + DISTORTION vs FREE-AIR TEMPERATURE

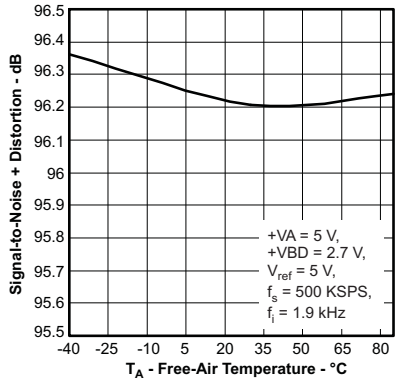


Figure 29.

SIGNAL-TO-NOISE RATIO vs FREE-AIR TEMPERATURE

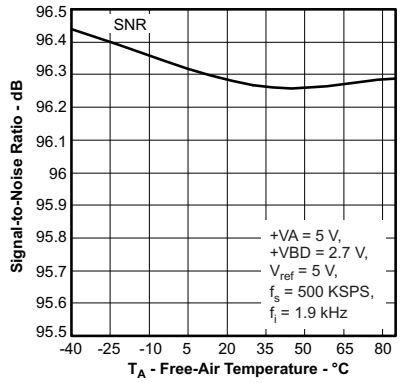


Figure 30.

TOTAL HARMONIC DISTORTION vs FREE-AIR TEMPERATURE

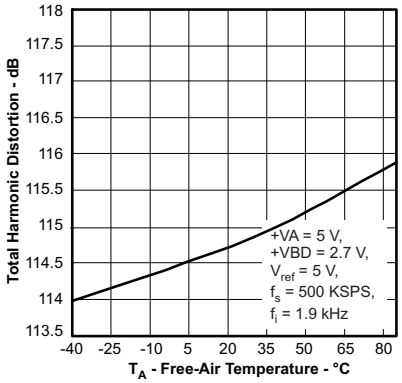


Figure 31.

TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

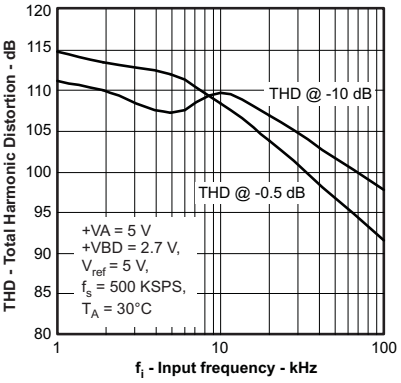


Figure 32.

TYPICAL CHARACTERISTICS (continued)

SIGNAL-TO-NOISE + DISTORTION vs INPUT FREQUENCY

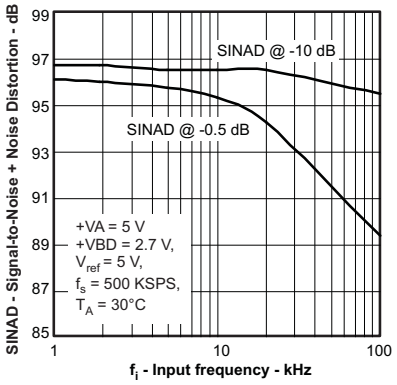


Figure 33.

DC HISTORAM OF ADC CLOSE TO CENTER CODE

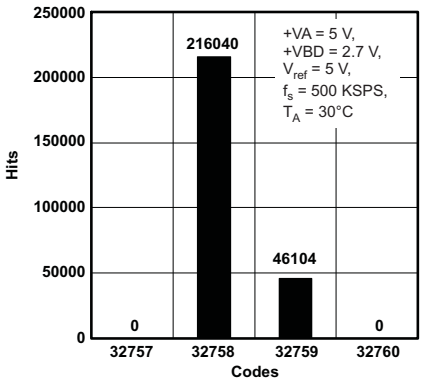


Figure 34.

TOTAL HARMONIC DISTORTION vs SOURCE RESISTANCE

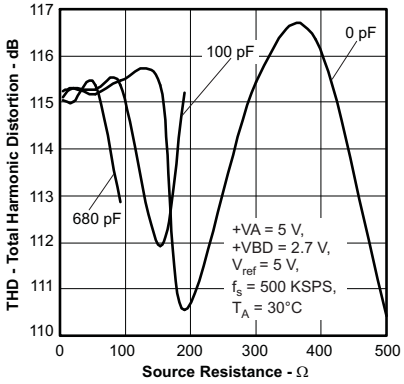


Figure 35.

SUPPLY CURRENT vs SUPPLY VOLTAGE

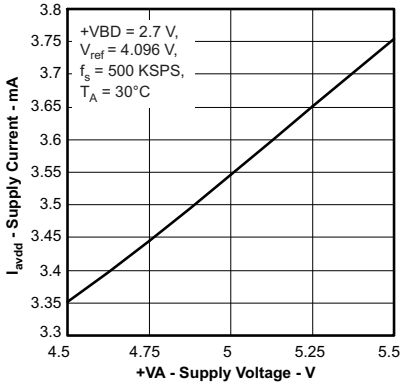


Figure 36.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

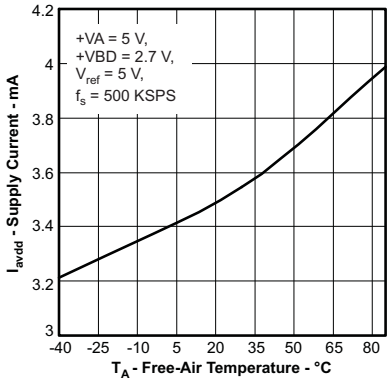


Figure 37.

SUPPLY CURRENT vs SAMPLING FREQUENCY

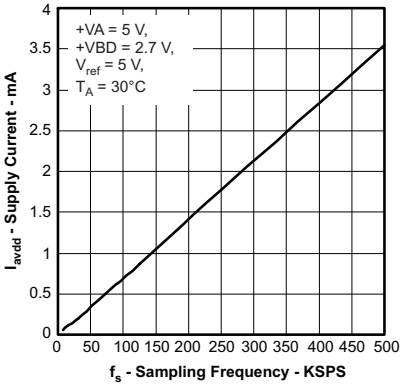


Figure 38.

POWER DISSIPATION vs SAMPLING FREQUENCY

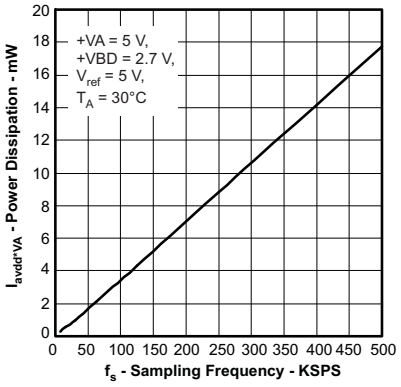


Figure 39.

POWERDOWN CURRENT vs SUPPLY VOLTAGE

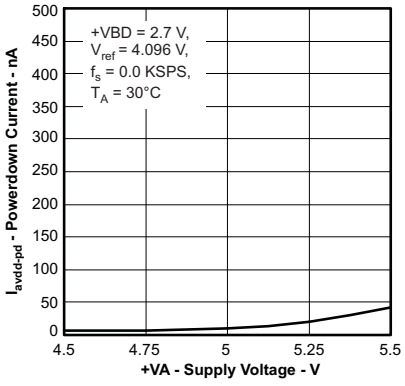


Figure 40.

POWERDOWN CURRENT vs FREE-AIR TEMPERATURE

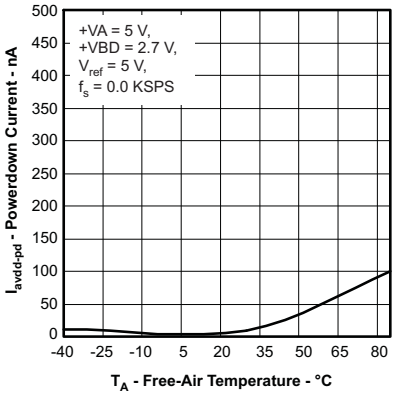


Figure 41.

TYPICAL CHARACTERISTICS (continued)

DNL

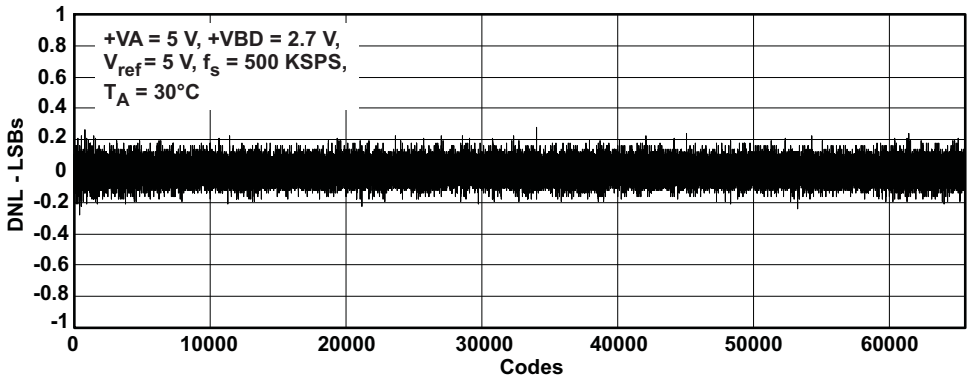


Figure 42.

INL

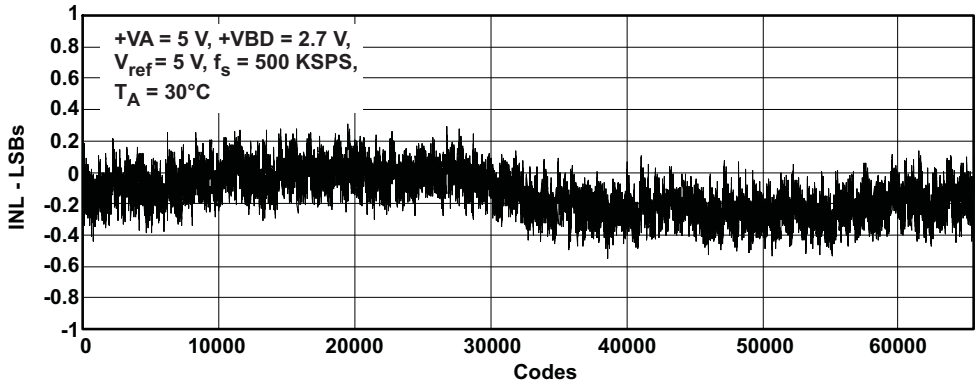


Figure 43.

FFT

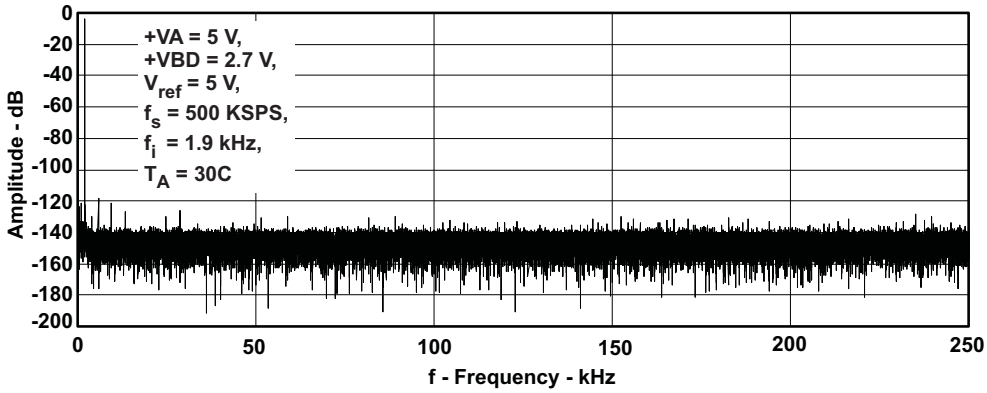


Figure 44.

DETAILED DESCRIPTIONS AND TIMING DIAGRAMS

The ADS8318 is a high-speed, low power, successive approximation register (SAR) analog-to-digital converter (ADC) that uses an external reference. The architecture is based on charge redistribution, which inherently includes a sample/hold function.

The ADS8318 is a single channel device. The analog input is provided to two input pins: +IN and -IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both +IN and -IN inputs are disconnected from any internal function.

The ADS8318 has an internal clock that is used to run the conversion, and hence the conversion requires a fixed amount of time. After a conversion is completed, the device reconnects the sampling capacitors to the +IN and –IN pins, and the device is in the acquisition phase. During this phase the device is powered down and conversion data can be read.

The device digital output is available in SPI compatible format. It easily interfaces with microprocessors, DSPs, or FPGAs.

This is a low pin count device; however, it offers six different options for the interface. They can be grossly classified as *$\overline{CS}$ mode* (3- or 4-wire interface) and *daisy chain mode*. In both modes it can either be with or without a *busy indicator*, where the busy indicator is a bit preceeding the 16-bit serial data.

The *3-wire interface $\overline{CS}$ mode* is useful for applications which need galvanic isolation on-board, where as *4-wire interface $\overline{CS}$ mode* makes it easy to control an individual device while having multiple devices on-board. The *daisy chain mode* is provided to hook multiple devices in a chain like a shift register and is useful to reduce component count and the number signal traces on the board.

$\overline{CS}$ MODE

$\overline{CS}$ Mode is selected if SDI is high at the rising edge of CONVST. As indicated before there are four different interface options available in this mode, namely *3-wire $\overline{CS}$ mode without busy indicator*, *3-wire $\overline{CS}$ mode with busy indicator*, *4-wire $\overline{CS}$ mode without busy indicator*, *4-wire $\overline{CS}$ mode with busy indicator*. The following section discusses these interface options in detail.

3-Wire $\overline{CS}$ Mode Without Busy Indicator

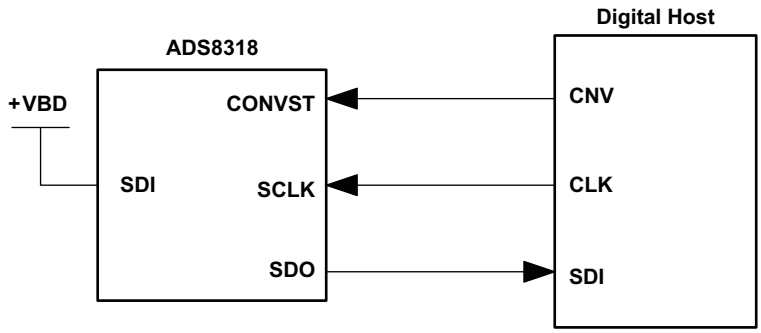


Figure 45. Connection Diagram, 3-Wire $\overline{CS}$ Mode without Busy Indicator (SDI = 1)

The three wire interface option in $\overline{CS}$ mode is selected if SDI is tied to +VBD (see Figure 45). In the three wire interface option, CONVST acts like $\overline{CS}$. As shown in Figure 46, the device samples the input signal and enters the conversion phase on the rising edge of CONVST, at the same time SDO goes to 3-state. Conversion is done with the internal clock and it continues irrespective of the state of CONVST. As a result it is possible to bring CONVST (acting as $\overline{CS}$) low after the start of the conversion to select other devices on the board. But it is absolutely necessary that CONVST is high again before the minimum conversion time (t_{cnv} in timing requirements table) is elapsed. A high level on CONVST at the end of the conversion ensures the device does not generate a busy indicator.

When the conversion is over, the device enters the acquisition phase and powers down. On the falling edge of CONVST, SDO comes out of three state, and the device outputs the MSB of the data. After this, the device outputs the next lower data bits on every falling edge of SCLK. SDO goes to 3-state after the 16th falling edge of SCLK or CONVST high, whichever occurs first. It is necessary that the device sees a minimum of 15 falling edges of SCLK during the low period of CONVST.

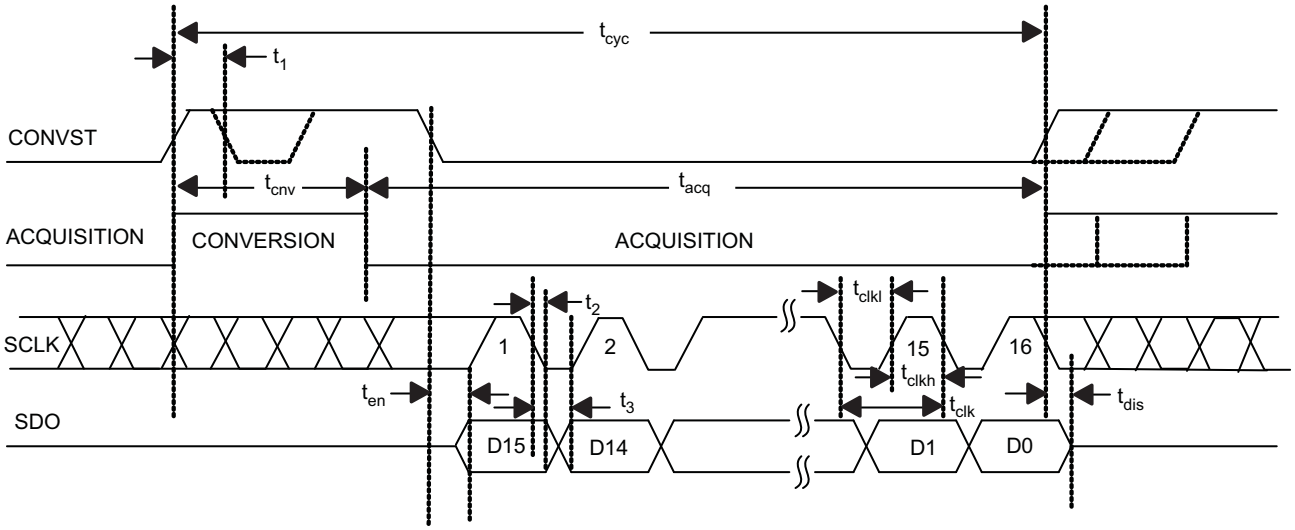


Figure 46. Interface Timing Diagram, 3 Wire $\overline{CS}$ Mode Without Busy Indicator (SDI = 1)

3 Wire $\overline{CS}$ Mode With Busy Indicator

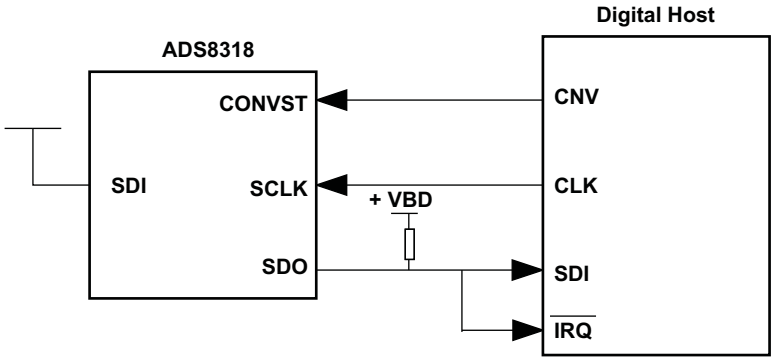


Figure 47. Connection Diagram, 3 Wire $\overline{CS}$ Mode With Busy Indicator

The three wire interface option in $\overline{CS}$ mode is selected if SDI is tied to +VBD (see Figure 47). In the three wire interface option, CONVST acts like $\overline{CS}$. As shown in Figure 48, the device samples the input signal and enters the conversion phase on the rising edge of CONVST, at the same time SDO goes to 3 state. Conversion is done with the internal clock and it continues irrespective of the state of CONVST. As a result it is possible to toggle CONVST (acting as $\overline{CS}$) after the start of the conversion to select other devices on the board. But it is absolutely necessary that CONVST is low again before the minimum conversion time (t_{cnv} in timing requirements table) is elapsed and continues to stay low until the end of maximum conversion time. A low level on the CONVST input at the end of a conversion ensures the device generates a busy indicator.

When the conversion is over, the device enters the acquisition phase and powers down, and the device forces SDO out of three state and outputs a busy indicator bit (low level). The device outputs the MSB of data on the first falling edge of SCLK after the conversion is over and continues to output the next lower data bits on every subsequent falling edge of SCLK. SDO goes to three state after the 17th falling edge of SCLK or CONVST high, whichever occurs first. It is necessary that the device sees a minimum of 16 falling edges of SCLK during the low period of CONVST.

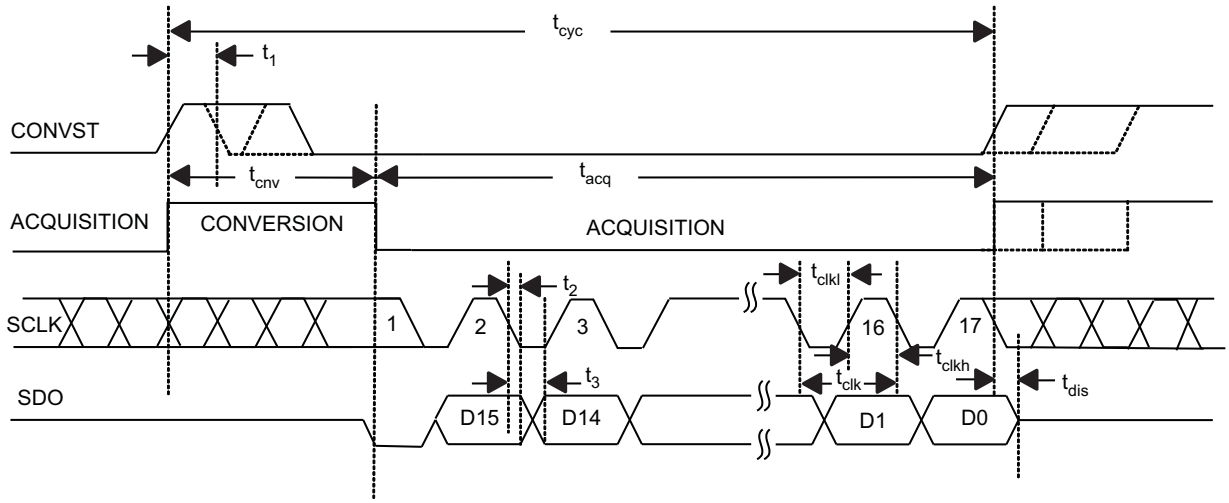


Figure 48. Interface Timing Diagram, 3 Wire $\overline{CS}$ Mode With Busy Indicator (SDI = 1)

4 Wire $\overline{CS}$ Mode Without Busy Indicator

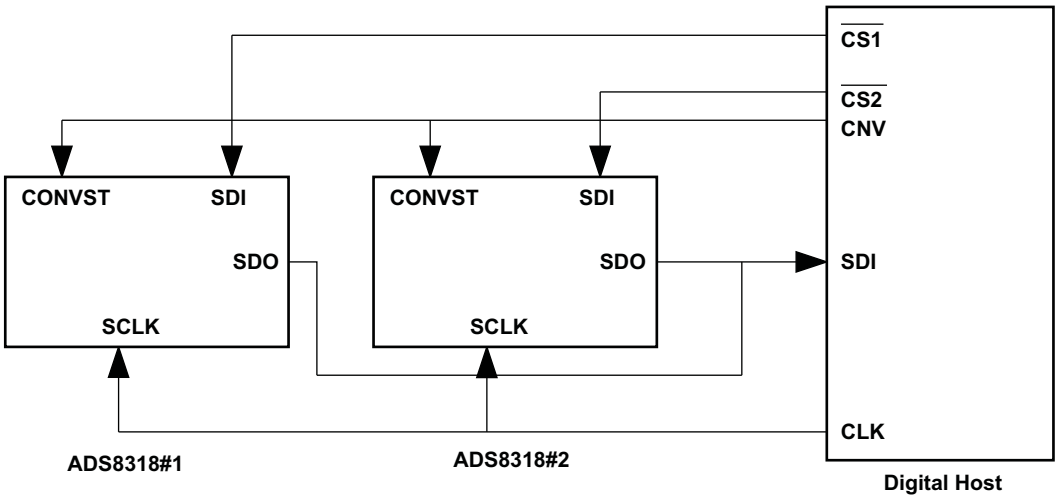


Figure 49. Connection Diagram, 4 Wire $\overline{CS}$ Mode Without Busy Indicator

As mentioned before for selecting *$\overline{CS}$ mode* it is necessary that SDI is high at the time of the CONVST rising edge. Unlike in *three wire interface option*, SDI is controlled by digital host and acts like $\overline{CS}$. As shown in Figure 50, SDI goes to a high level before the rising edge of CONVST. The rising edge of CONVST while SDI is high selects $\overline{CS}$ mode, forces SDO to three state, samples the input signal, and the device enters the conversion phase. In the 4 wire interface option CONVST needs to be at a high level from the start of the conversion until all of the data bits are read. Conversion is done with the internal clock and it continues irrespective of the state of SDI. As a result it is possible to bring SDI (acting as $\overline{CS}$) low to select other devices on the board. But it is absolutely necessary that SDI is high again before the minimum conversion time (t_{cnv} in timing requirements table) is elapsed.

When the conversion is over, the device enters the acquisition phase and powers down. SDI falling edge can occur after the maximum conversion time (t_{cnv} in timing requirements table). Note that it is necessary that SDI is high at the end of the conversion, so that the device does not generate a *busy indicator*. The falling edge of SDI

brings SDO out of 3-state and the device outputs the MSB of the data. Subsequent to this the device outputs the next lower data bits on every falling edge of SCLK. SDO goes to three state after the 16th falling edge of SCLK or SDI ($\overline{CS}$) high, whichever occurs first. As shown in Figure 49, it is possible to hook multiple devices on the same data bus. In this case the second device SDI (acting as $\overline{CS}$) can go low after the first device data is read and device 1 SDO is in three state.

Care needs to be taken so that CONVST and SDI are not low together at any time during the cycle.

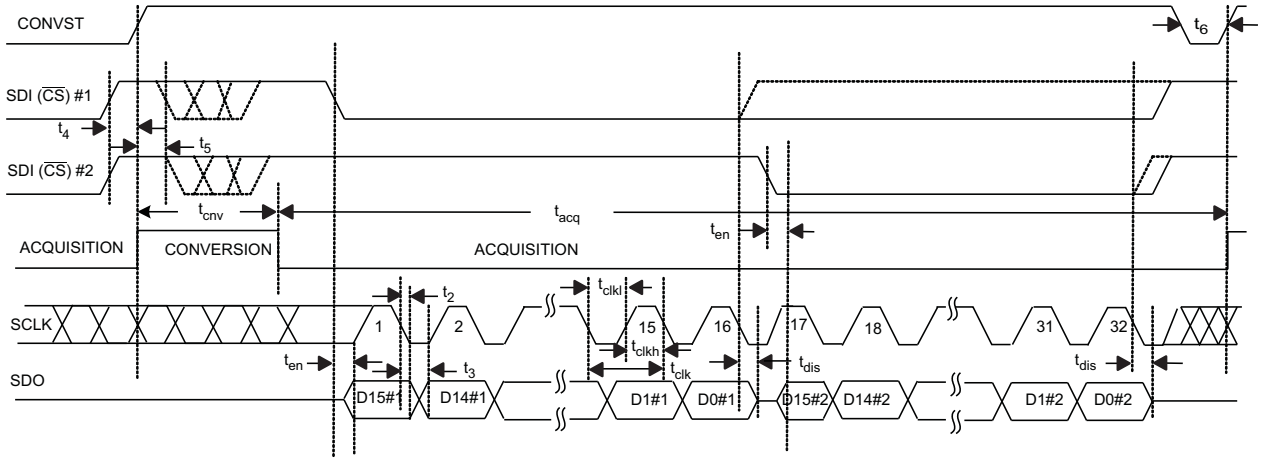


Figure 50. Interface Timing Diagram, 4 Wire $\overline{CS}$ Mode Without Busy Indicator

4 Wire $\overline{CS}$ Mode With Busy Indicator

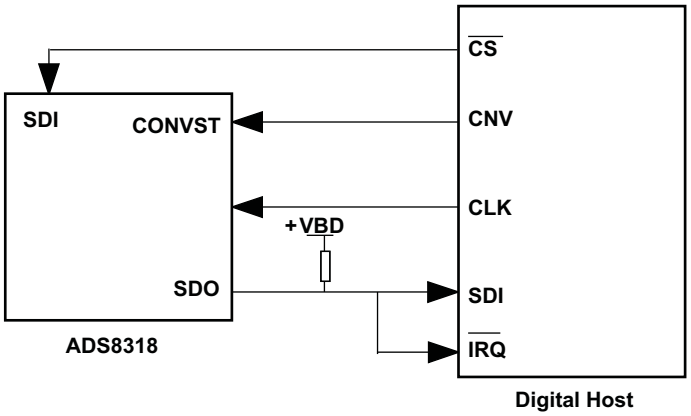


Figure 51. Connection Diagram, 4 Wire $\overline{CS}$ Mode With Busy Indicator

As mentioned before for selecting *$\overline{CS}$ mode* it is necessary that SDI is high at the time of the CONVST rising edge. Unlike in the *three wire interface option*, SDI is controlled by the digital host and acts like $\overline{CS}$. As shown in Figure 52, SDI goes to a high level before the rising edge of CONVST. The rising edge of CONVST while SDI is high selects $\overline{CS}$ mode, forces SDO to three state, samples the input signal, and the device enters the conversion phase. In the 4 wire interface option CONVST needs to be at a high level from the start of the conversion until all of the data bits are read. Conversion is done with the internal clock and it continues irrespective of the state of SDI. As a result it is possible to toggle SDI (acting as $\overline{CS}$) to select other devices on the board. But it is absolutely necessary that SDI is low before the minimum conversion time (t_{cnv} in timing requirements table) is elapsed and continues to stay low until the end of the maximum conversion time. A low level on the SDI input at the end of a conversion ensures the device generates a busy indicator.

When the conversion is over, the device enters the acquisition phase and powers down, forces SDO out of three state, and outputs a busy indicator bit (low level). The device outputs the MSB of the data on the first falling edge of SCLK after the conversion is over and continues to output the next lower data bits on every falling edge of SCLK. SDO goes to three state after the 17th falling edge of SCLK or SDI ($\overline{CS}$) high, whichever occurs first.

Care needs to be taken so that CONVST and SDI are not low together at any time during the cycle.

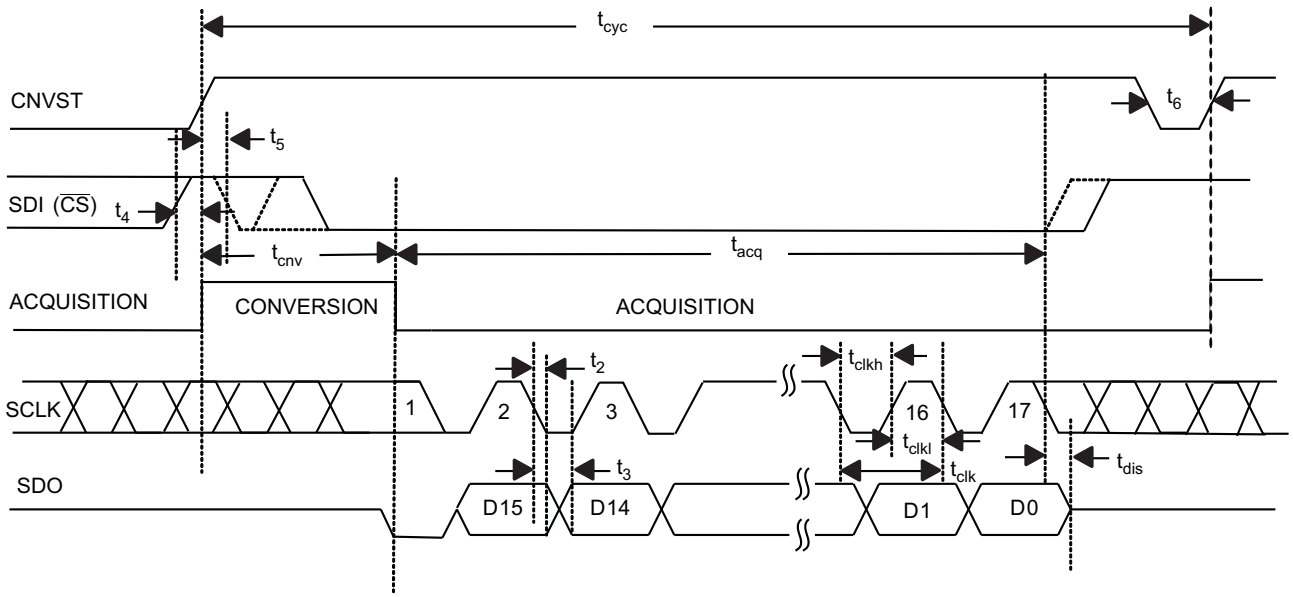


Figure 52. Interface Timing Diagram, 4 Wire $\overline{CS}$ Mode With Busy Indicator

Daisy Chain Mode

Daisy chain mode is selected if SDI is low at the time of CONVST rising edge. This mode is useful to reduce wiring and hardware like digital isolators in the applications where multiple (ADC) devices are used. In this mode all of the devices are connected in a chain (SDO of one device connected to the SDI of the next device) and data transfer is analogous to a shift register.

Like $\overline{CS}$ mode even this mode offers operation with or without a busy indicator. The following section discusses these interface options in detail.

Daisy Chain Mode Without Busy Indicator

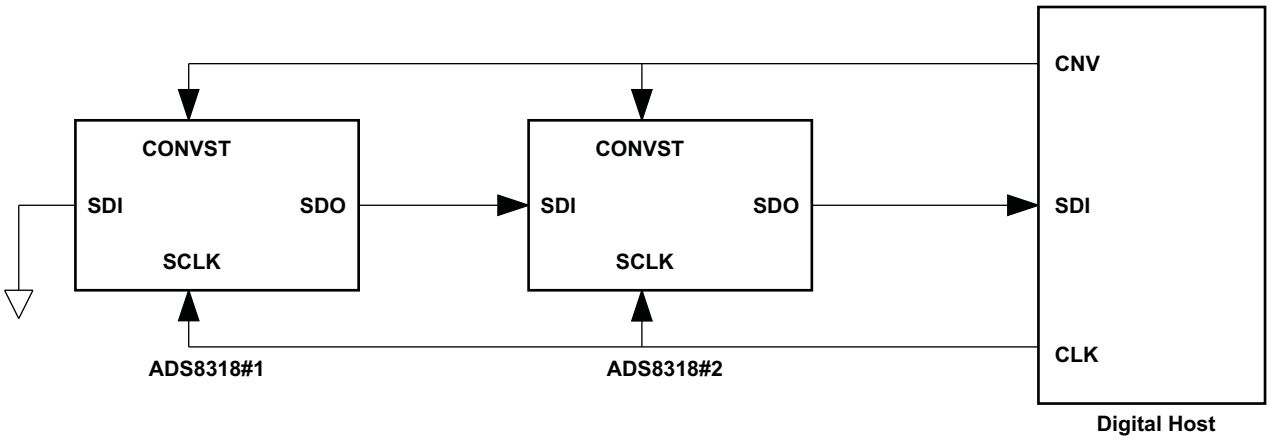


Figure 53. Connection Diagram, Daisy Chain Mode Without Busy Indicator (SDI = 0)

Refer to Figure 53 for the connection diagram. SDI for device 1 is tied to ground and SDO of device 1 goes to SDI of device 2 and so on. SDO of the last device in the chain goes to the digital host. CONVST for all of the devices in the chain are tied together. In this mode there is no $\overline{CS}$ signal. The device SDO is driven low when

SDI and CONVST are low together. The rising edge of CONVST while SDI is low selects daisy chain mode and the device samples the analog input and enters the conversion phase. It is necessary that SCLK is low at the rising edge of CONVST so that the device does not generate a busy indicator at the end of the conversion. In this mode CONVST continues to be high from the start of the conversion until all of the data bits are read. Once started, conversion continues irrespective of the state of SCLK.

At the end of the conversion, every device in the chain initiates output of its conversion data starting with the MSB bit. Further the next lower data bit is output on every falling edge of SCLK. While every device outputs its data on the SDO pin, it also receives previous device data on the SDI pin (other than device #1) and stores it in the shift register. The device latches incoming data on every falling edge of SCLK. SDO of the first device in the chain goes low after the 16th falling edge of SCLK. All subsequent devices in the chain output the stored data from the previous device in MSB first format immediately following their own data word.

It needs 16 × N clocks to read data for N devices in the chain.

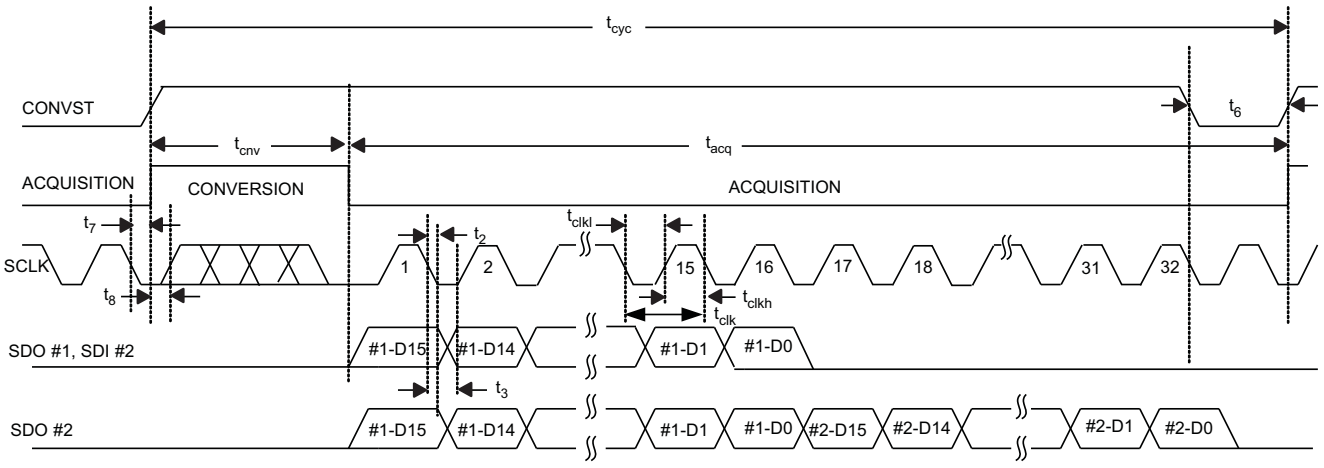


Figure 54. Interface Timing Diagram, Daisy Chain Mode Without Busy Indicator

Daisy Chain Mode With Busy Indicator

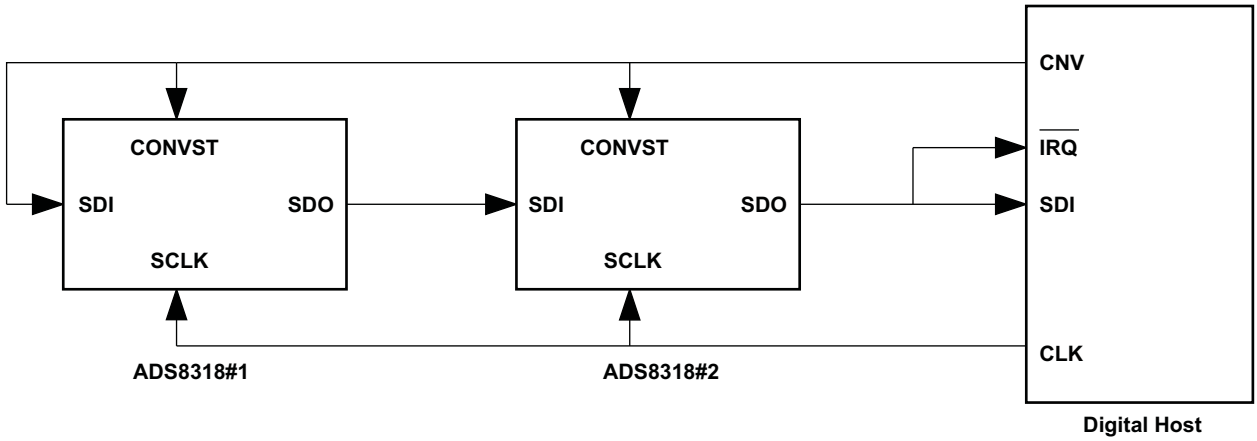


Figure 55. Connection Diagram, Daisy Chain Mode With Busy Indicator (SDI = 0)

Refer to Figure 55 for the connection diagram. SDI for device 1 is wired to it's CONVST and CONVST for all the devices in the chain are wired together. SDO of device 1 goes to SDI of device 2 and so on. SDO of the last device in the chain goes to the digital host. In this mode there is no $\overline{CS}$ signal. On the rising edge of CONVST, all of the device in the chain sample the analog input and enter the conversion phase. For the first device, SDI

and CONVST are wired together, and the setup time of SDI to rising edge of CONVST is adjusted so that the device still enters chain mode even though SDI and CONVST rise together. It is necessary that SCLK is high at the rising edge of CONVST so that the device generates a busy indicator at the end of the conversion. In this mode, CONVST continues to be high from the start of the conversion until all of the data bits are read. Once started, conversion continues irrespective of the state of SCLK.

At the end of the conversion, all the devices in the chain generate busy indicators. On the first falling edge of SCLK following the busy indicator bit, all of the devices in the chain output their conversion data starting with the MSB bit. After this the next lower data bit is output on every falling edge of SCLK. While every device outputs its data on the SDO pin, it also receives the previous device data on the SDI pin (except for device #1) and stores it in the shift register. Each device latches incoming data on every falling edge of SCLK. SDO of the first device in the chain goes high after the 17th falling edge of SCLK. All subsequent devices in the chain output the stored data from the pervious device in MSB first format immediately following their own data word. It needs 16 × N + 1 clock pulses to read data for N devices in the chain.

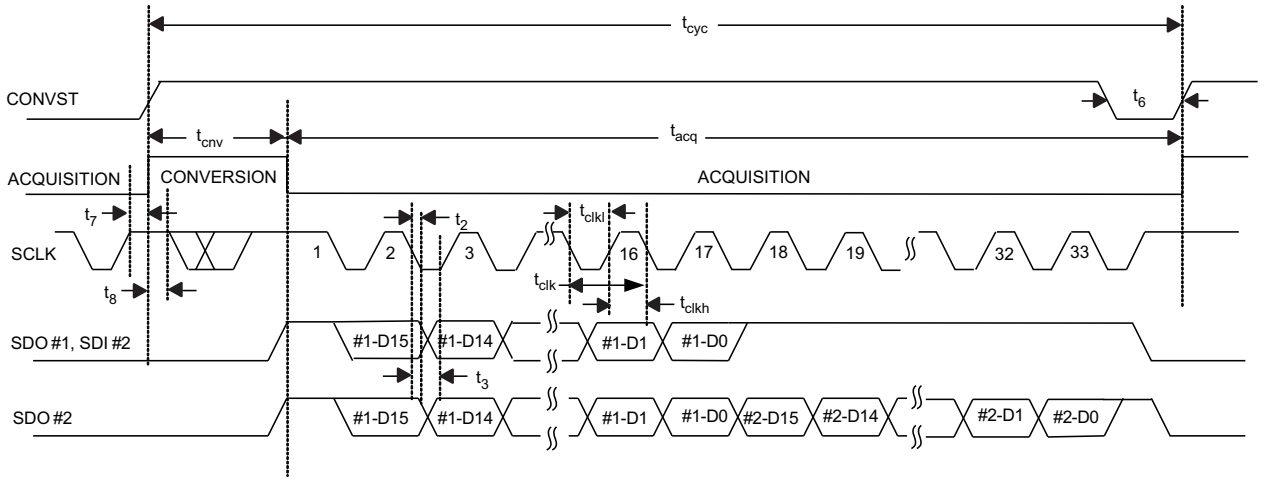


Figure 56. Interface Timing Diagram, Daisy Chain Mode With Busy Indicator

APPLICATION INFORMATION

ANALOG INPUT

When the converter samples the input, the voltage difference between the +IN and -IN inputs is captured on the internal capacitor array. The voltage on the +IN and –IN inputs individually is limited between GND –0.1 V and V_{ref} + 0.1 V; where as the differential signal range [(+IN) – (–IN)] is $2V_{ref}$ ($–V_{ref}$ to $+V_{ref}$) with a common mode of (V_{ref}/2). This allows the input to reject small signals which are common to both the +IN and –IN inputs.

The (peak) input current through the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. The current into the ADS8318 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (59 pF) to a 18-bit settling level within the minimum acquisition time. When the converter goes into hold mode, the input impedance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain linearity of the converter, the +IN and -IN inputs and the span (+IN – (–IN)) should be within the limits specified. Outside of these ranges, converter linearity may not meet specifications.

Care should be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. If this is not observed, the two inputs could have different settling times. This may result in an offset error, gain error, and linearity error which change with temperature and input voltage.

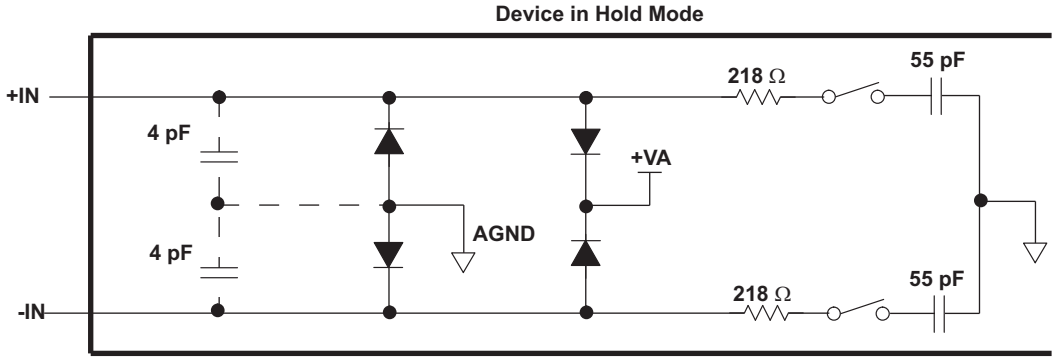


Figure 57. Input Equivalent Circuit

DRIVER AMPLIFIER CHOICE

The analog input to the converter needs to be driven with a low noise, op-amp like the THS4031, OPA211. An RC filter is recommended at the input pins to low-pass filter the noise from the source. Two resistors of 5Ω and a differential capacitor of 1nF is recommended. The input to the converter is a unipolar input voltage in the range 0 V to V_{ref}. The minimum –3dB bandwidth of the driving operational amplifier can be calculated as:

$$f3db = (\ln(2) \times (n+2))/(2\pi \times tACQ)$$

where n is equal to 16, the resolution of the ADC (in the case of the ADS8318). When t_{ACQ} = 600 ns (minimum acquisition time), the minimum bandwidth of the driving circuit is ~3 MHz (including RC following the driver OPA). The bandwidth can be relaxed if the acquisition time is increased by the application.

Typically a low noise OPA with ten times or higher bandwidth is selected. The driving circuit bandwidth is adjusted (to the required value) with a RC following the OPA. The OPA211 or THS4031 from Texas Instruments is recommended for driving high-resolution high-speed ADCs.

DRIVER AMPLIFIER CONFIGURATIONS

Configuration for Unipolar Differential Input

It is better to use a unity gain, noninverting buffer configuration for a unipolar, differential input having a $\pm V_{ref}$ signal range with V_{ref}/2 common-mode. As explained before a RC following the OPA limits the input circuit bandwidth just enough for 16-bit settling. Note higher bandwidth reduces the settling time (beyond what is needed) but increases the noise in the ADC sampled signal, and hence the ADC output.

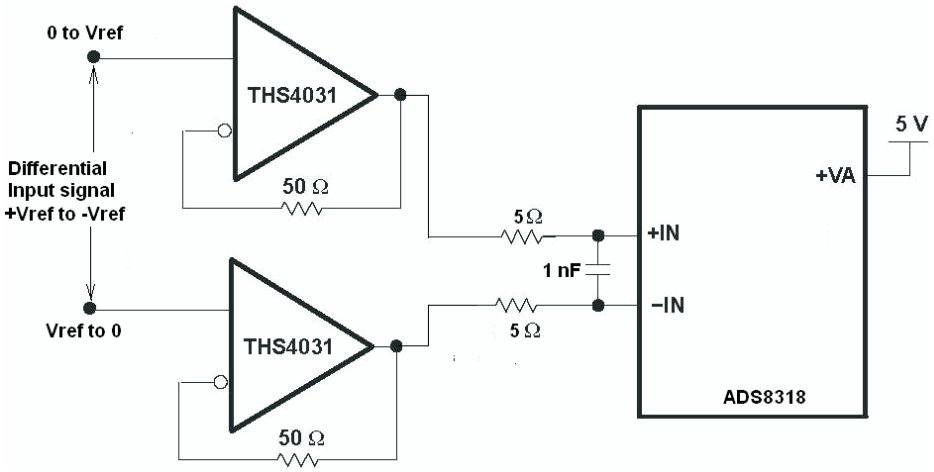
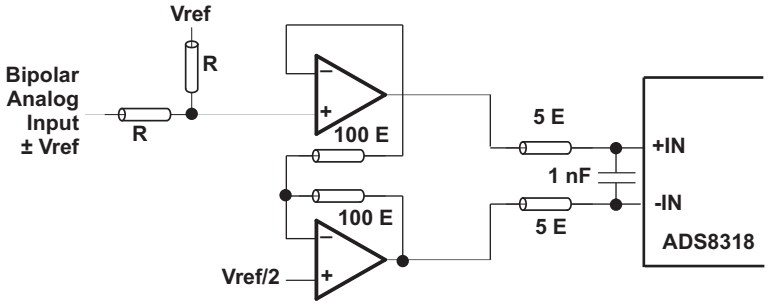


Figure 58. Unipolar Differential Input Drive Configuration

Configuration for Bipolar Single-Ended Input

The following circuit shows a way to convert a single-ended bipolar input to the unipolar differential input needed for for converter. Note that the higher values of the resistors at the input of the top OPA may reduce power consumption of the circuit but increase noise in the driving circuit. One can choose these components based on application needs.



OPA Shown is THS4031 or OPA211

Figure 59. Bipolar Single-Ended Input Drive Configuration

REFERENCE

The ADS8318 can operate with an external reference with a range from 2.048 V to V_{DD} + 0.1 V. A clean, low noise, well-decoupled reference voltage on this pin is required to ensure good performance of the converter. A low noise band-gap reference like the REF5050 can be used to drive this pin as shown in Figure 60 and Figure 61. The capacitor should be placed as close as possible to the pins of the device.

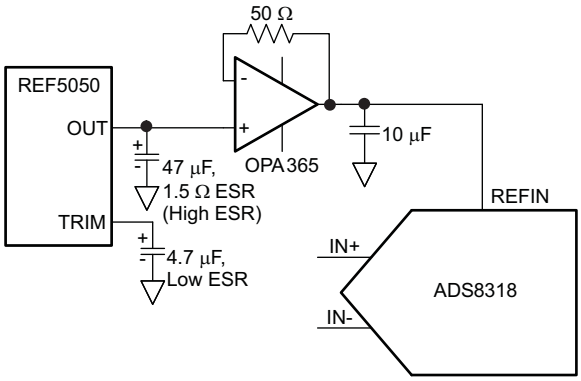


Figure 60. External Reference Driving Circuit

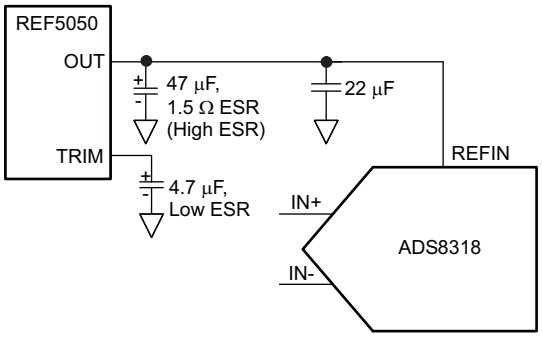


Figure 61. Direct External Reference Driving Circuit

POWER SAVING

The ADS8318 has an auto power-down feature. The device powers down at the end of every conversion. The input signal is acquired on sampling capacitors while the device is in the power-down state, and at the same time the conversion results are available for reading. The device powers up by itself on the start of the conversion. As discussed before, the conversion runs on an internal clock and takes a fixed time. As a result, device power consumption is directly proportional to the speed of operation.

DIGITAL OUTPUT

As discussed before (in the *DESCRIPTION and TIMING DIAGRAMS* sections) the device digital output is SPI compatible. The following table lists the output codes corresponding to various analog input voltages.

DESCRIPTION	ANALOG VALUE (V)	DIGITAL OUTPUT STRAIGHT BINARY	
Full-scale range	$2*V_{ref}$		
Least significant bit (LSB)	$2*V_{ref}/65536$	**BINARY CODE**	**HEX CODE**
Positive full scale	$+V_{ref}$ – 1 LSB	0111 1111 1111 1111	7FFF
Midscale	0 V	0000 0000 0000 0000	0000
Midscale – 1 LSB	0 – 1 LSB	1111 1111 1111 1111	FFFF
Negative full scale	$–V_{ref}$	1000 0000 0000 0000	8000

SCLK INPUT

The device uses SCLK for serial data output. Data is read after the conversion is over and the device is in the acquisition phase. It is possible to use a free running SCLK for the device, but it is recommended to stop the clock during a conversion, as the clock edges can couple with the internal analog circuit and can affect conversion results.

REVISION HISTORY

Changes from Original (May 2008) to Revision A **Page**

- Changed Condition in first TIMING REQUIREMENTS from 4.5 V to 3.1 V 5
- Changed SCLK Low time MIN value from 9ns to 8ns and SCLK High time MIN value from 9ns to 8ns 5
- Changed Condition in second TIMING REQUIREMENTS from +4.5 V to + 3.1 V 6

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS8318IBDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	CBC
ADS8318IBDGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	CBC
ADS8318IBDGST	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	CBC
ADS8318IBDGST.A	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	CBC
ADS8318IBDRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	CBE
ADS8318IBDRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	CBE
ADS8318IDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	CBC
ADS8318IDGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	CBC
ADS8318IDGST	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	CBC
ADS8318IDGST.A	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	CBC
ADS8318IDRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	CBE
ADS8318IDRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	CBE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

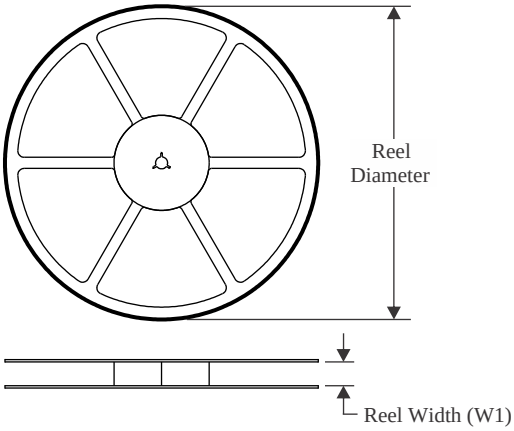
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

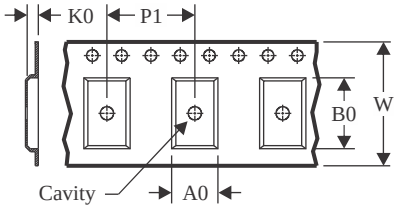
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

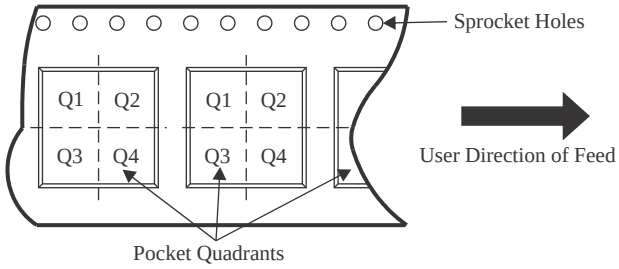


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

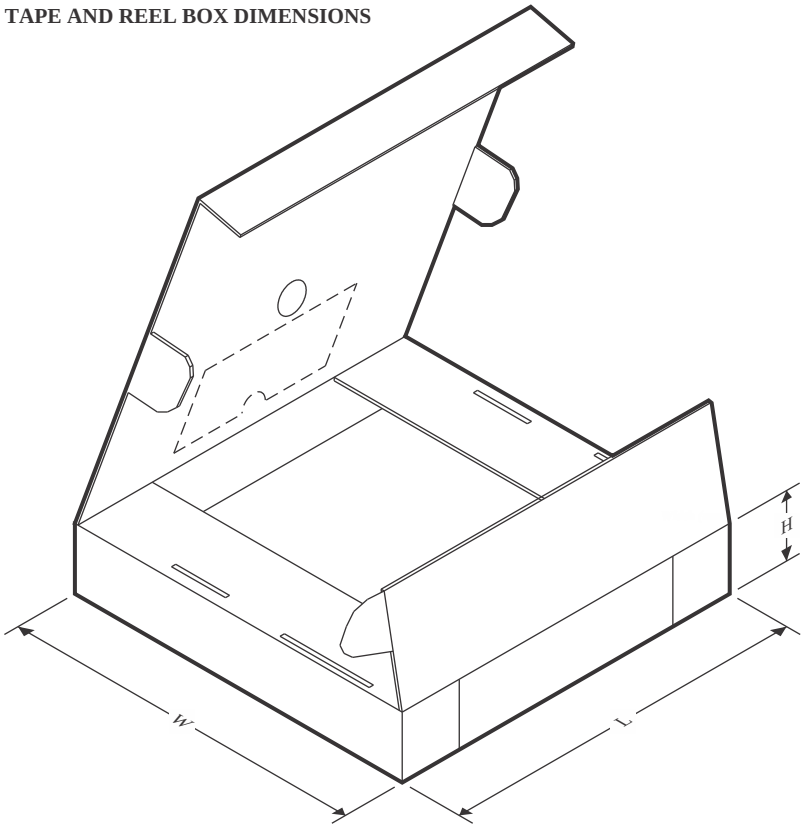
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8318IBDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8318IDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

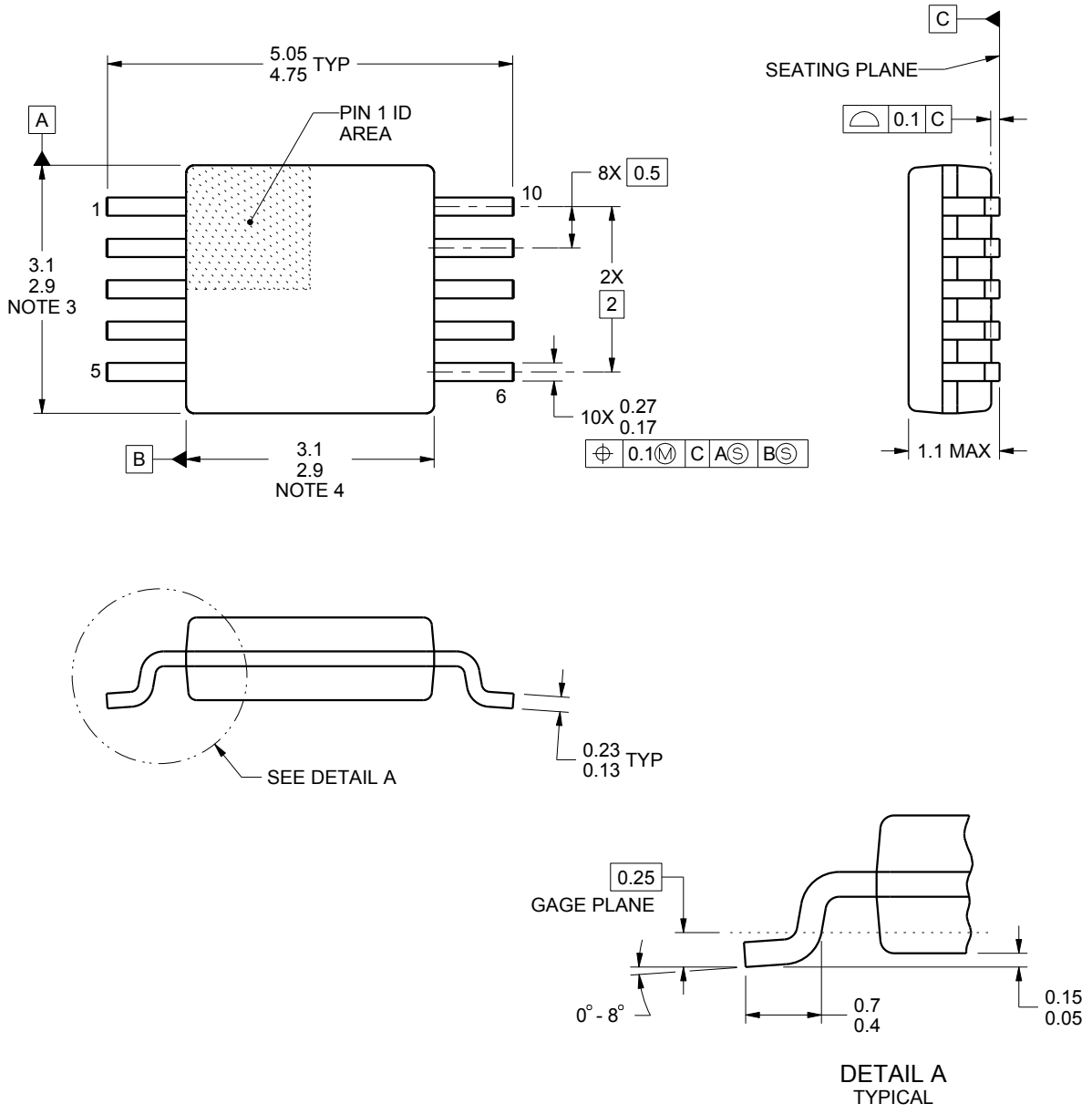
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8318IBDRCT	VSON	DRC	10	250	210.0	185.0	35.0
ADS8318IDRCT	VSON	DRC	10	250	210.0	185.0	35.0

PACKAGE OUTLINE

DGS0010A

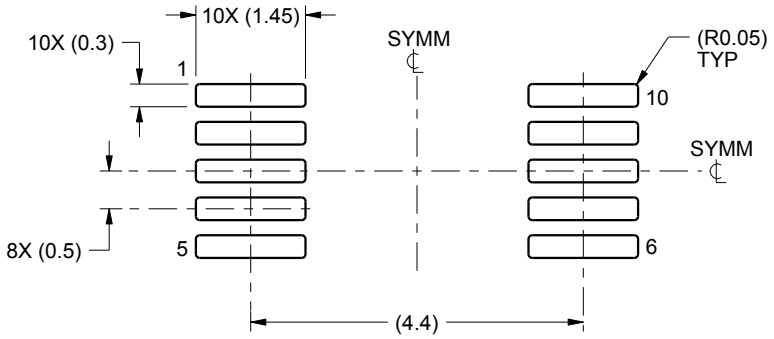
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

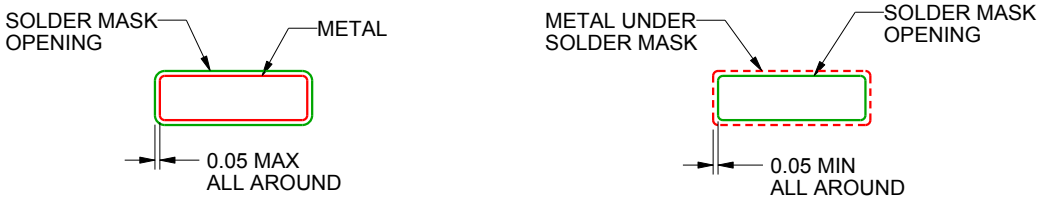


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

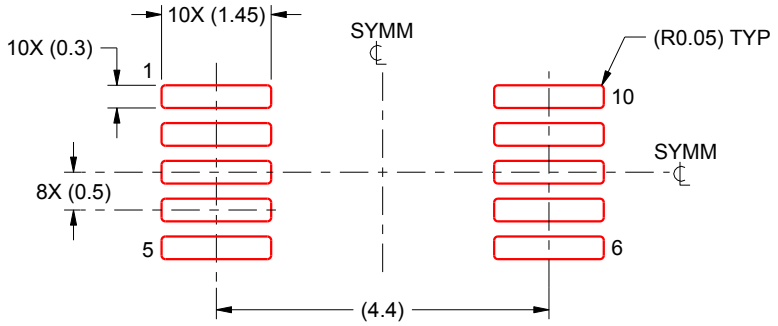


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

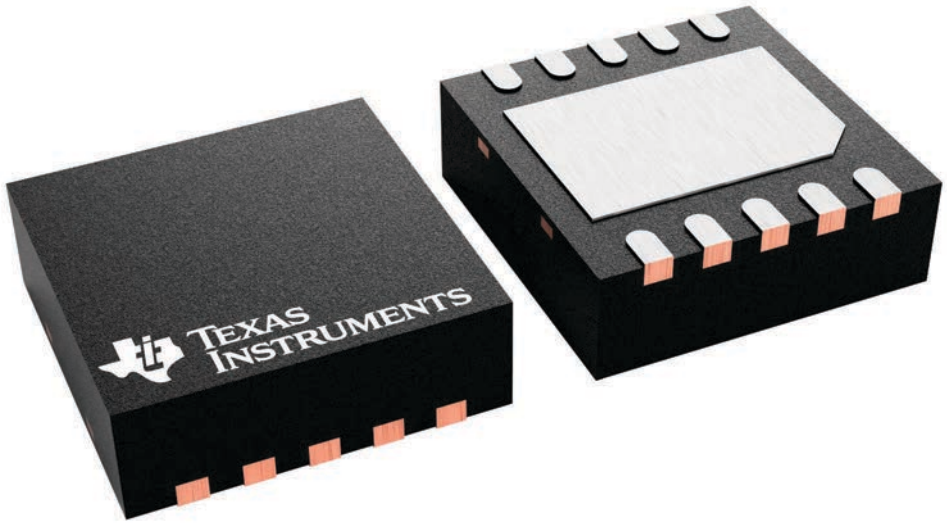
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

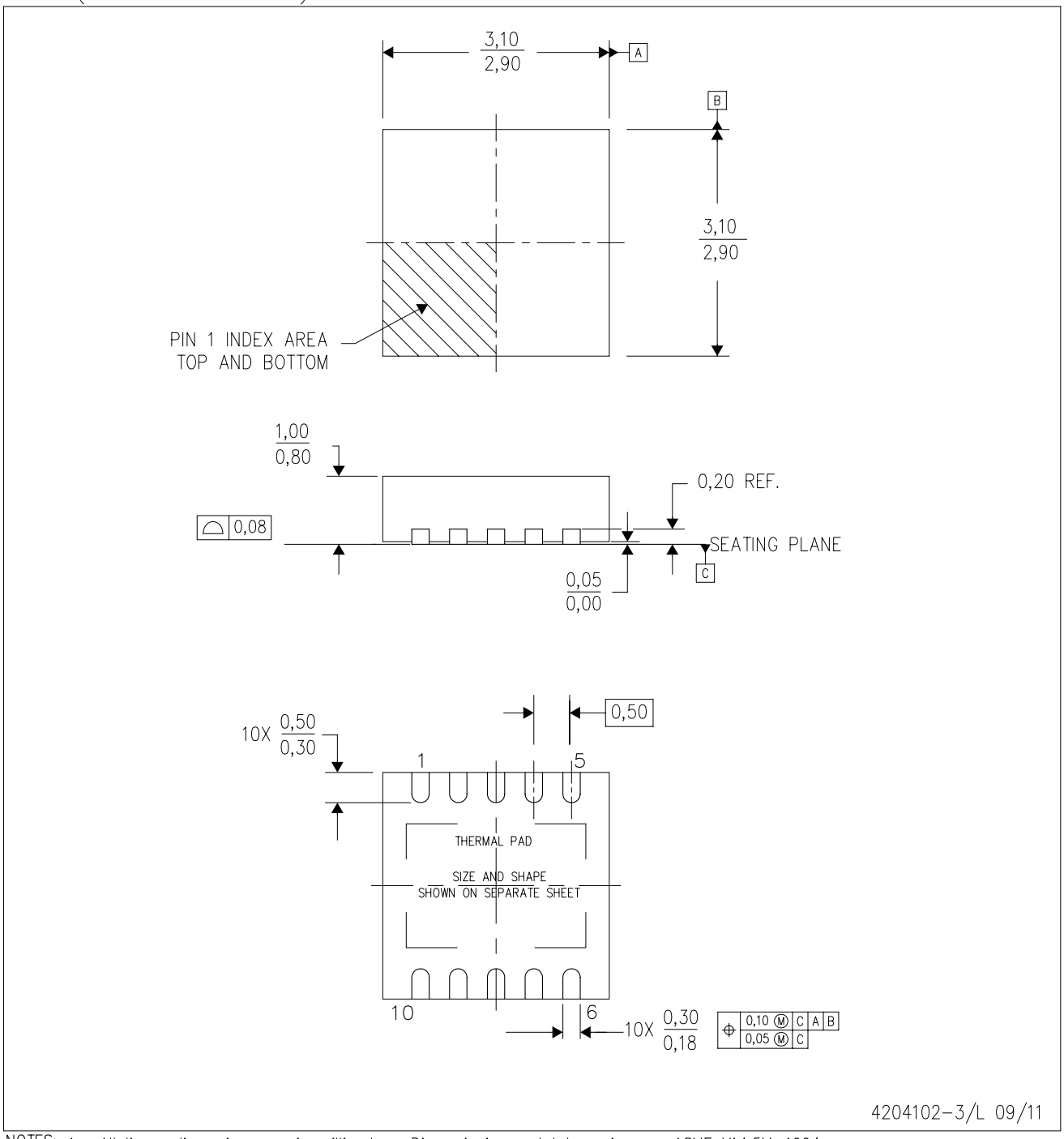
PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226193/A

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



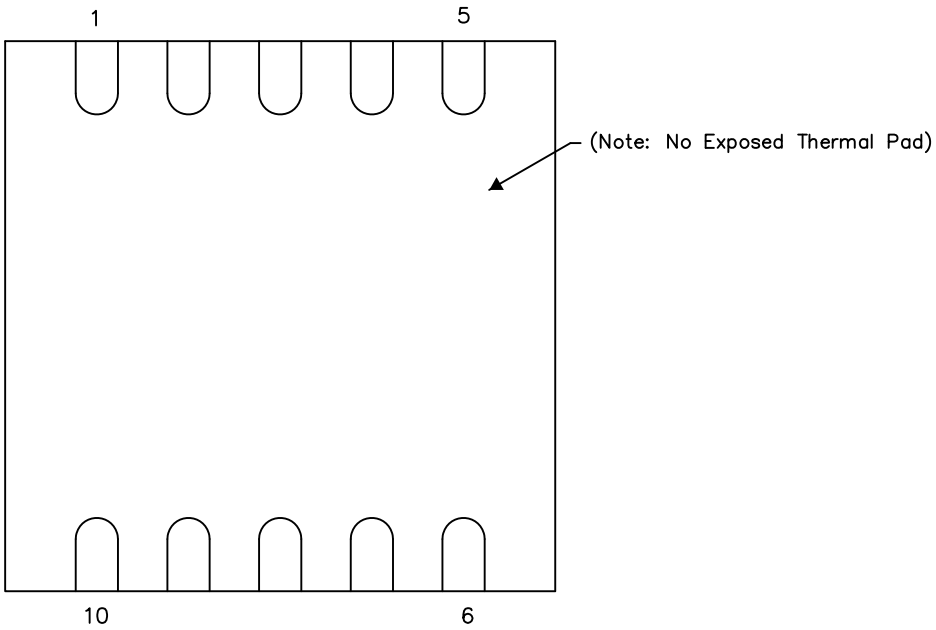
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This version of the package has no exposed thermal pad. This must be accounted for when estimating thermal performance.

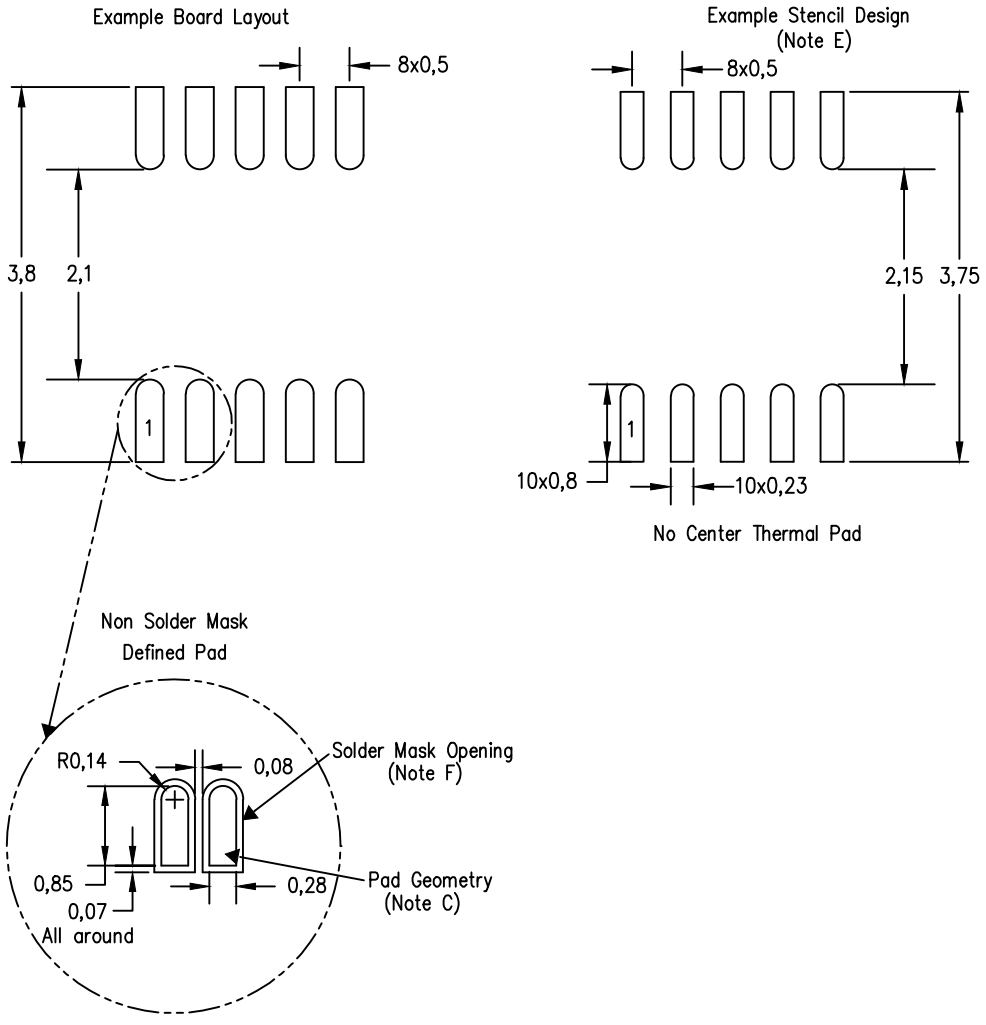
For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.



Bottom View

4206565–5/Y 08/15

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package does not have a center thermal pad. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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