

## VOLTAGE PROTECTION FOR 2-, 3-, OR 4-CELL Lion BATTERIES (2<sup>nd</sup> PROTECTION)

### FEATURES

- 2-, 3-, or 4-Cell Secondary Protection
- Low Power Consumption  $I_{CC} < 2 \mu A$   
[ $V_{CELL(ALL)} < V_{(PROTECT)}$ ]
- High Accuracy Over Sense Voltage:
  - bq29400: 4.35 V  $\pm 25$  mV
  - bq29400A: 4.40 V  $\pm 25$  mV
  - bq29401: 4.45 V  $\pm 25$  mV
  - bq29405: 4.65 V  $\pm 25$  mV
- Prefixed Protection Threshold Voltage
- Programmable Delay Time
- High Power Supply Ripple Rejection
- Stable During Pulse Charge Operation

### APPLICATIONS

- 2<sup>nd</sup> Level Protection in Lion Battery Packs in
  - Notebook PCs
  - Portable Instrumentation
  - Medical and Test Equipment

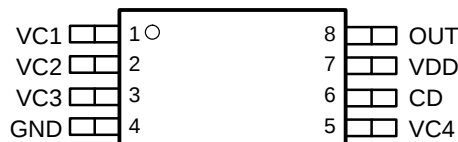
### DESCRIPTION

The bq29400, bq29400A, bq29401, and bq29405 are BiCMOS secondary protection ICs for 2-, 3-, or 4-cell Lithium-Ion battery packs that incorporate a high-accuracy precision over voltage detection circuit. They include a programmable delay circuit for over voltage detection time.

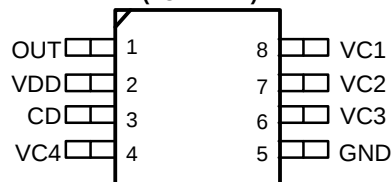
### FUNCTION

Each cell in a multiple cell pack is compared to an internal reference voltage. If one cell reaches an overvoltage condition, the protection sequence begins. The bq2940x device starts charging an external capacitor through the CD pin. When the CD pin voltage reaches 1.2 V, the OUT pin changes from a low level to a high level.

**PW PACKAGE  
(TOP VIEW)**



**DCT PACKAGE  
(TOP VIEW)**



### ORDERING INFORMATION

| $T_A$         | $V_{(PROTECT)}$ | PACKAGE      |        |                           |        |
|---------------|-----------------|--------------|--------|---------------------------|--------|
|               |                 | MSSOP (DCT3) | SYMBOL | TSSOP (PW) <sup>(1)</sup> | SYMBOL |
| –25°C to 85°C | 4.35 V          | bq29400DCT3  | CIQ    | bq29400PW                 | 2400   |
|               | 4.40 V          | bq29400ADCT3 | CIT    | Not Available             | -      |
|               | 4.45 V          | bq29401DCT3  | CIR    | bq29401PW                 | 2401   |
|               | 4.65 V          | bq29405DCT3  | CIS    | Not Available             | -      |

(1) The bq29400, bq29400A, bq29401, and bq29405 are available taped and reeled. Add an R suffix to the device type (e.g., bq29400PWR) to order tape and reel version.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted<sup>(1)(2)</sup>

|                                             |                      | UNIT                         |
|---------------------------------------------|----------------------|------------------------------|
| Supply voltage range                        | (VDD)                | –0.3 V to 28 V               |
| Input voltage range                         | (VC1, VC2, VC3, VC4) | –0.3 V to 28 V               |
| Output voltage range                        | (OUT)                | –0.3 V to 28 V               |
|                                             | (CD)                 | –0.3 V to 28 V               |
| Continuous total power dissipation          |                      | See Dissipation Rating Table |
| Storage temperature range, T <sub>stg</sub> |                      | –65°C to 150°C               |
| Lead temperature (soldering, 10 sec)        |                      | 300°C                        |

- Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltages are with respect to ground of this device except the differential voltage of VC1-VC2, VC2-VC3, VC3-VC4 and VC4-GND.

## PACKAGE DISSIPATION RATINGS

| PACKAGE | T <sub>A</sub> = 25°C<br>POWER RATING | DERATING FACTOR<br>ABOVE T <sub>A</sub> = 25°C | T <sub>A</sub> = 70°C<br>POWER RATING | T <sub>A</sub> = 85°C<br>POWER RATING |
|---------|---------------------------------------|------------------------------------------------|---------------------------------------|---------------------------------------|
| DCT     | 412 mW                                | 3.3 mW/°C                                      | 264 mW                                | 214 mW                                |
| PW      | 525 mW                                | 4.2 mW/°C                                      | 336 mW                                | 273 mW                                |

## RECOMMENDED OPERATING CONDITIONS

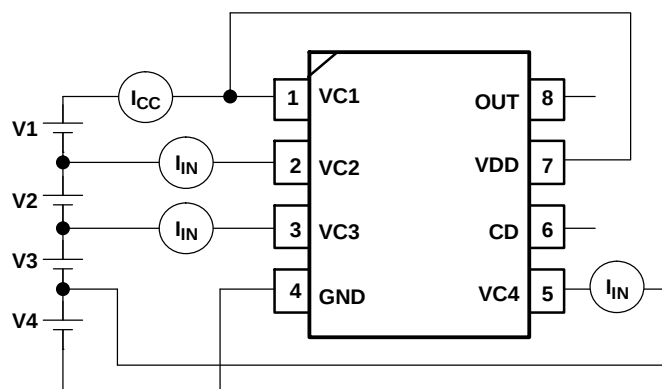
|                    |                                     |                    | MIN  | NOM  | MAX                  | UNIT |
|--------------------|-------------------------------------|--------------------|------|------|----------------------|------|
| V <sub>DD</sub>    | Supply Voltage                      |                    | 4.0  |      | 25                   | V    |
| V <sub>I</sub>     | Input voltage range                 | VC1, VC2, VC3, VC4 | 0    |      | V <sub>DD</sub> +0.3 | V    |
| t <sub>d(CD)</sub> | Delay time capacitance              |                    |      | 0.22 |                      | μF   |
| R <sub>IN</sub>    | Voltage-monitor filter resistance   |                    | 100  | 1k   |                      | Ω    |
| C <sub>IN</sub>    | Voltage-monitor filter capacitance  |                    | 0.01 | 0.1  |                      | μF   |
| R <sub>VD</sub>    | Supply-voltage filter resistance    |                    | 0    |      | 1                    | kΩ   |
| C <sub>VD</sub>    | Supply-voltage filter capacitance   |                    |      | 0.1  |                      | μF   |
| T <sub>A</sub>     | Operating ambient temperature range |                    | –25  |      | 85                   | °C   |

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

| PARAMETER       |                                                  | TEST CONDITION                                                                                                              | MIN | NOM  | MAX | UNIT          |
|-----------------|--------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|-----|------|-----|---------------|
| $V_{(OA)}$      | Over voltage detection accuracy                  |                                                                                                                             |     | 25   | 35  | mV            |
|                 |                                                  | $T_A = -20^\circ\text{C}$ to $85^\circ\text{C}$                                                                             |     | 25   | 50  |               |
| $V_{(PROTECT)}$ | Over voltage detection voltage <sup>(1)</sup>    | bq29400                                                                                                                     |     | 4.35 |     | V             |
|                 |                                                  | bq2940A                                                                                                                     |     | 4.40 |     |               |
|                 |                                                  | bq29401                                                                                                                     |     | 4.45 |     |               |
|                 |                                                  | bq29405                                                                                                                     |     | 4.65 |     |               |
| $V_{hys}$       | Over voltage detection hysteresis <sup>(1)</sup> |                                                                                                                             |     | 300  |     | mV            |
| $I_I$           | Input current                                    | $V_2, V_3, VC4$ input = $VC1-VC2 = VC2-VC3 = VC3-VC4 = VC4-GND = 3.5\text{ V}$                                              |     |      | 0.3 | $\mu\text{A}$ |
| $t_{D1}$        | Over voltage detection delay time                | $CD = 0.22\text{ }\mu\text{F}$                                                                                              | 1.0 | 1.5  | 2.0 | S             |
| $I_{(CD\_dis)}$ | CD GND clamp current                             | $CD = 1\text{ V}$                                                                                                           | 5   | 12   |     | $\mu\text{A}$ |
| $I_{CC}$        | Supply current                                   | $VC1-VC2 = VC2-VC3 = VC3-VC4 = VC4-GND = 3.5\text{ V}$<br>(see Figure 1)                                                    |     | 2.0  | 3.0 | $\mu\text{A}$ |
|                 |                                                  | $VC1 = VC2 = VC3 = VC4 = VC3-VC4 = VC4-GND = 2.3\text{ V}$<br>(see Figure 1)                                                |     | 1.5  | 2.5 |               |
| $V_{(OUT)}$     | OUT pin drive voltage                            | $VC1-VC2 = VC2-VC3 = VC3-VC4 = VC4-GND = V_{(PROTECT)MAX}$ , $VDD = VC1$ , $IOH = 0\text{ mA}$                              |     | 7    |     | V             |
|                 |                                                  | $VC1=VC2=VC3=VC4=V_{(PROTECT)MAX}$ , $VDD=4.3V$ ,<br>$T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ , $IOH = -40\mu\text{A}$ | 1.5 | 2.0  | 2.5 | V             |
| $I_{OH}$        | High-level output current                        | $OUT = 3V$ , $VC1-VC2 = VC2-VC3 = VC3-VC4 = VC4-GND = 4.7\text{ V}$                                                         | -1  |      |     | mA            |
| $I_{OL}$        | Low-level output current                         | $OUT = 0.1\text{ V}$ $VC1-VC2 = VC2-VC3 = VC3-VC4 = VC4-GND = 3.5\text{ V}$                                                 | 5   |      |     | $\mu\text{A}$ |

(1) Levels of the over-voltage detection and the hysteresis can be adjusted. For assistance contact Texas Instruments sales representative.



**Figure 1.  $I_{CC}$ ,  $I_{IN}$  Measurement (TSSOP Package)**

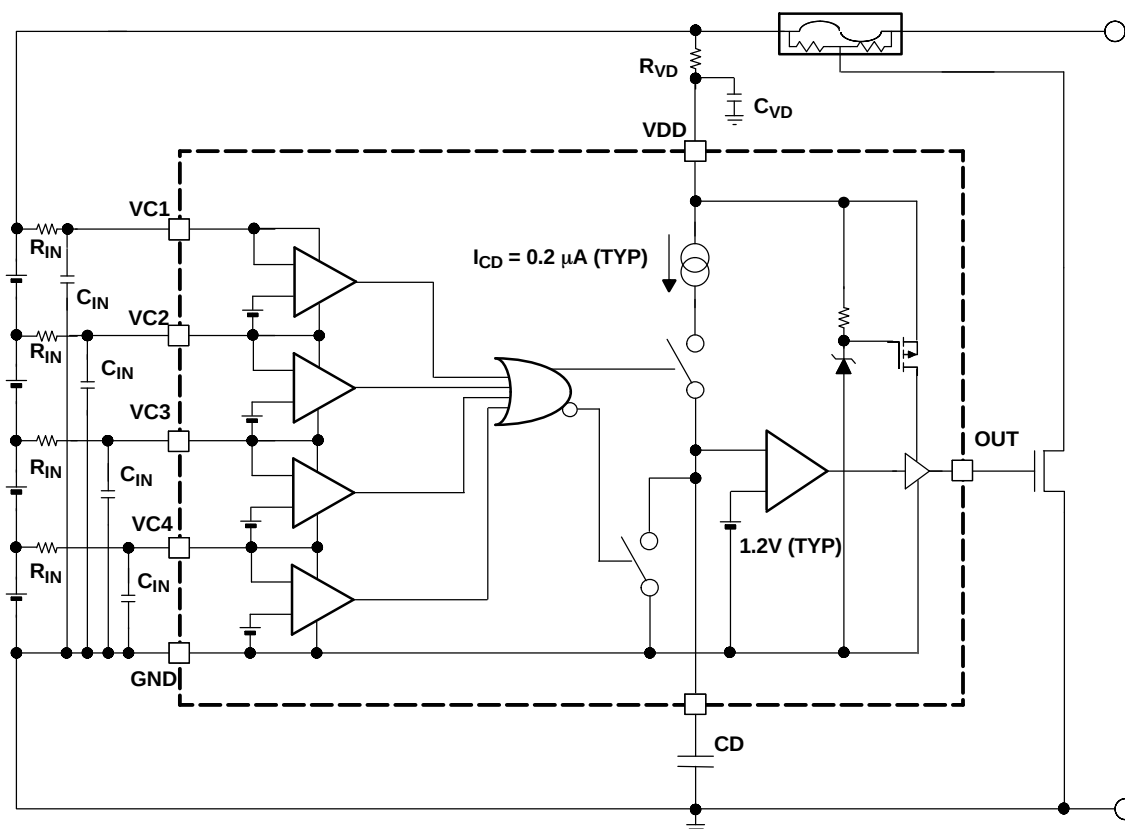
## Terminal Functions

| TERMINAL   |            |      | DESCRIPTION                                       |
|------------|------------|------|---------------------------------------------------|
| MSOP (DTC) | TSSOP (PW) | NAME |                                                   |
| 8          | 1          | VC1  | Sense voltage input for most positive cell        |
| 7          | 2          | VC2  | Sense voltage input for second most positive cell |
| 6          | 3          | VC3  | Sense voltage input for third most positive cell  |
| 5          | 4          | GND  | Ground pin                                        |
| 4          | 5          | VC4  | Sense voltage input for least positive cell       |

### Terminal Functions (continued)

| TERMINAL   |            |      | DESCRIPTION                                                                 |
|------------|------------|------|-----------------------------------------------------------------------------|
| MSOP (DTC) | TSSOP (PW) | NAME |                                                                             |
| 3          | 6          | CD   | An external capacitor is connected to determine the programmable delay time |
| 2          | 7          | VDD  | Power supply                                                                |
| 1          | 8          | OUT  | Output                                                                      |

### FUNCTIONAL BLOCK DIAGRAM



### OVERVOLTAGE PROTECTION

When one of the cell voltages exceeds  $V_{(PROTECT)}$ , an internal current source begins to charge the capacitor,  $C_{(DELAY)}$ , connected to the CD pin. If the voltage at the CD pin,  $V_{CD}$ , reaches 1.2 V, the OUT pin is activated and transitions high. An externally connected NCH FET is activated and blows the external fuse in the positive battery rail, see [Figure 1](#).

If all cell voltages fall below  $V_{(PROTECT)}$  before the voltage at pin CD reaches 1.2 V, the delay time does not run out. An internal switch clamps the CD pin to GND and discharges the capacitor,  $C_{(DELAY)}$ , and secures the full delay time for the next occurring overvoltage event.

Once the pin OUT is activated, it transitions back from high to low after all battery cells reach  $V_{(PROTECT)} - V_{hys}$ .

### DELAY TIME CALCULATION

The delay time is calculated as follows:

$$t_d = \frac{1.2 \text{ V} \times C_{(\text{DELAY})}}{I_{\text{CD}}}$$

$$C_{(\text{DELAY})} = \frac{t_d \times I_{\text{CD}}}{1.2 \text{ V}}$$

Where  $I_{(\text{CD})}$  = CD current source = 0.2  $\mu\text{A}$

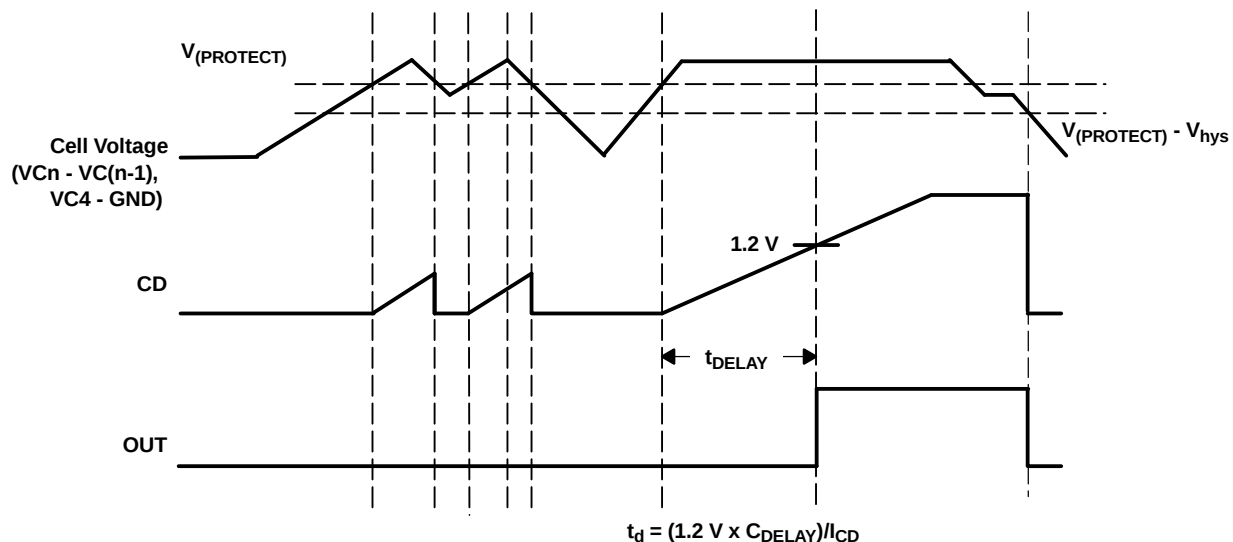


Figure 2. Timing for Overvoltage Sensing

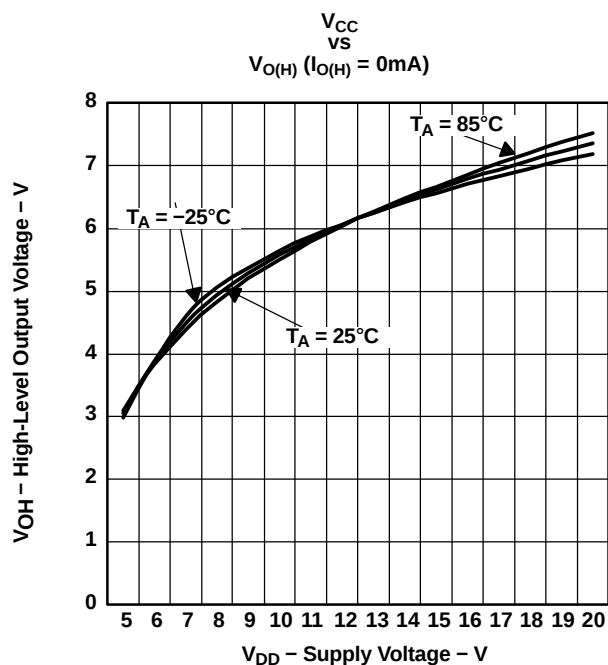


Figure 3.

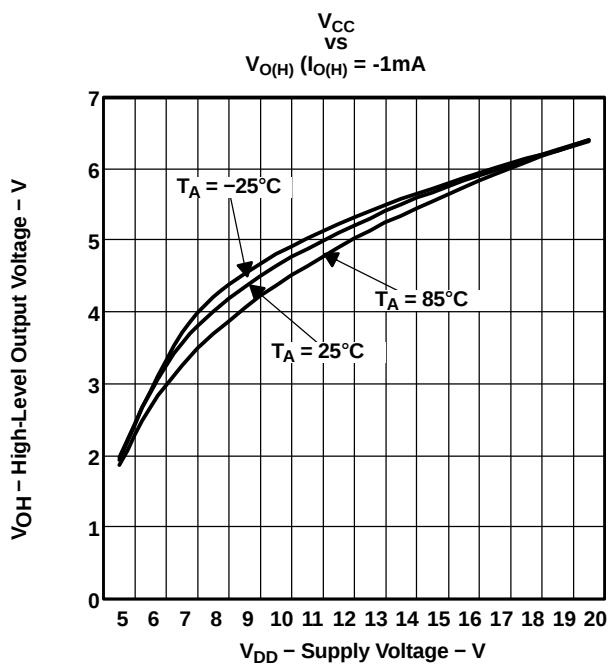


Figure 4.

## APPLICATION INFORMATION

### BATTERY CONNECTIONS

The following diagrams show the TSSOP package device in different cell configurations.

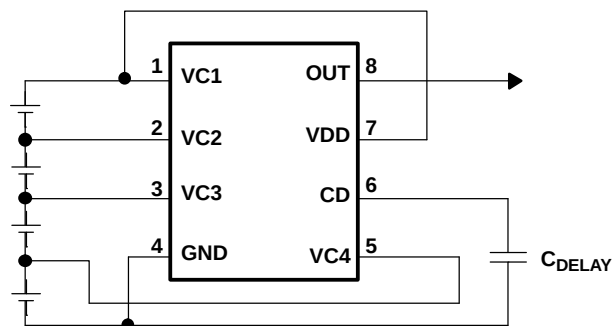


Figure 5. 4-Series Cell Configuration

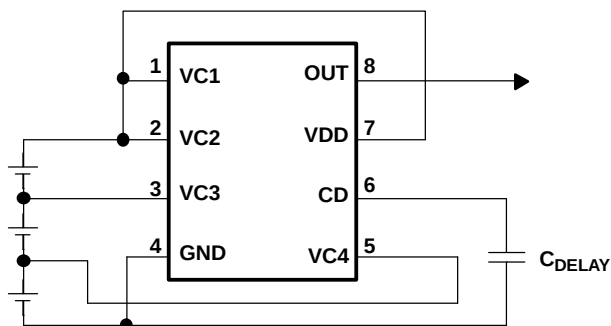


Figure 6. 3-Series Cell Configuration  
(Connect together VC1 and VC2)

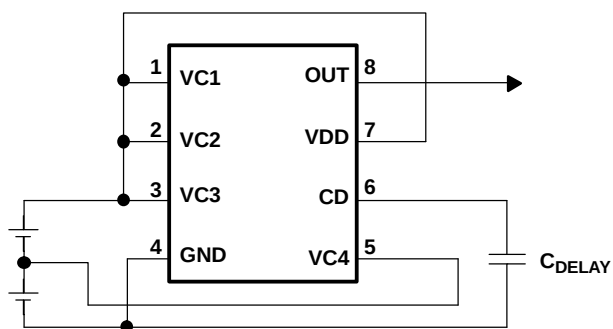


Figure 7. 2-Series Cell Configuration

### CELL CONNECTIONS

To prevent incorrect output activation the following connection sequences must be used.

#### 4-Series Cell Configuration

- VC1(=VDD) → VC2 → VC3 → VC4 → GND or
- GND → VC4 → VC3 → VC2 → VC1(=VDD)

#### 3-Series Cell Configuration

- VC1(=VC2=VDD) → VC3 → VC4 → GND or
- GND → VC4 → VC3 → VC1(=VC2=VDD)

#### 2-Series Cell Configuration

- VC1(=VC2=VC3=VDD) → VC4 → GND or
- GND → VC4 → VC1(=VC2=VC3=VDD)

## PACKAGING INFORMATION

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C)    | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|-----------------|---------------------|
| <a href="#">BQ29400DCT3</a> | Last Time Buy | Production           | SSOP (DCT)   8 | 3000   LARGE T&R      | Yes         | SNBI                                 | Level-1-260C-UNLIM                | -               | CIQ                 |
| BQ29400DCT3.A               | Last Time Buy | Production           | SSOP (DCT)   8 | 3000   LARGE T&R      | Yes         | SNBI                                 | Level-1-260C-UNLIM                | -25 to 85       | CIQ                 |
| BQ29400DCT3E6               | Last Time Buy | Production           | SSOP (DCT)   8 | 3000   LARGE T&R      | Yes         | SNBI                                 | Level-1-260C-UNLIM                | See BQ29400DCT3 | CIQ                 |
| <a href="#">BQ29400PW</a>   | Active        | Production           | TSSOP (PW)   8 | 150   TUBE            | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -25 to 85       | 29400               |
| BQ29400PW.A                 | Active        | Production           | TSSOP (PW)   8 | 150   TUBE            | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -25 to 85       | 29400               |
| <a href="#">BQ29401PW</a>   | Active        | Production           | TSSOP (PW)   8 | 150   TUBE            | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -20 to 85       | 29401               |
| BQ29401PW.A                 | Active        | Production           | TSSOP (PW)   8 | 150   TUBE            | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -20 to 85       | 29401               |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

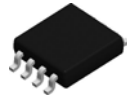
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

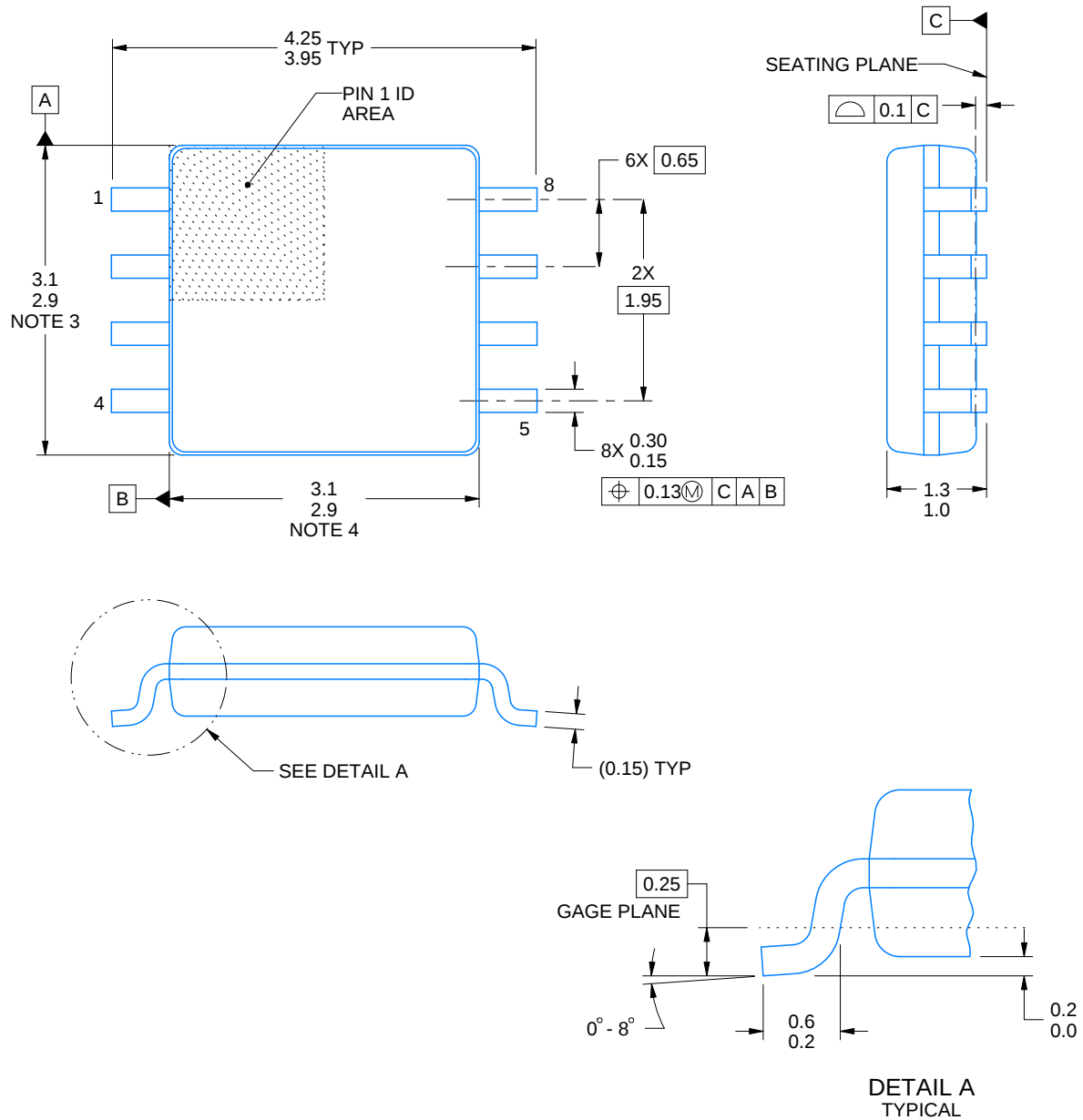
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**DCT0008A****PACKAGE OUTLINE****SSOP - 1.3 mm max height**

SMALL OUTLINE PACKAGE



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**NOTES:**

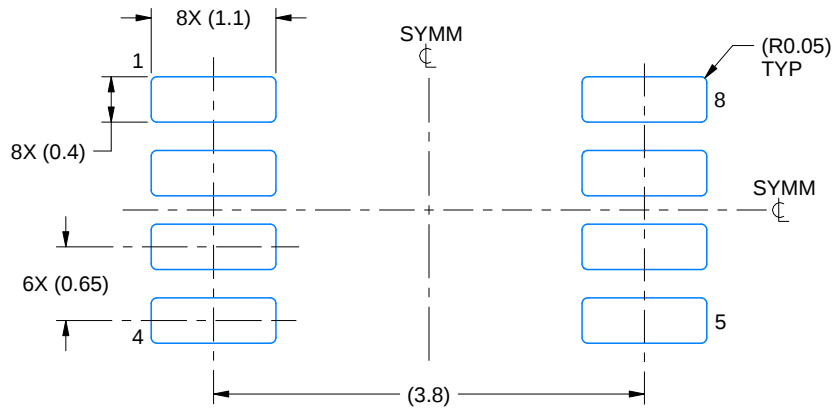
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

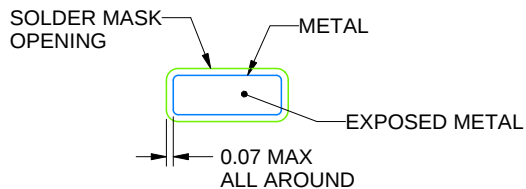
DCT0008A

SSOP - 1.3 mm max height

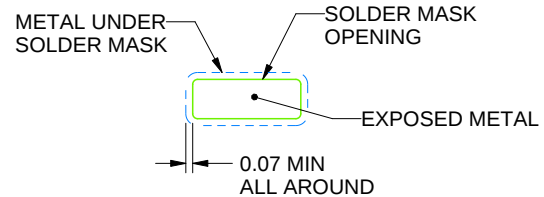
SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

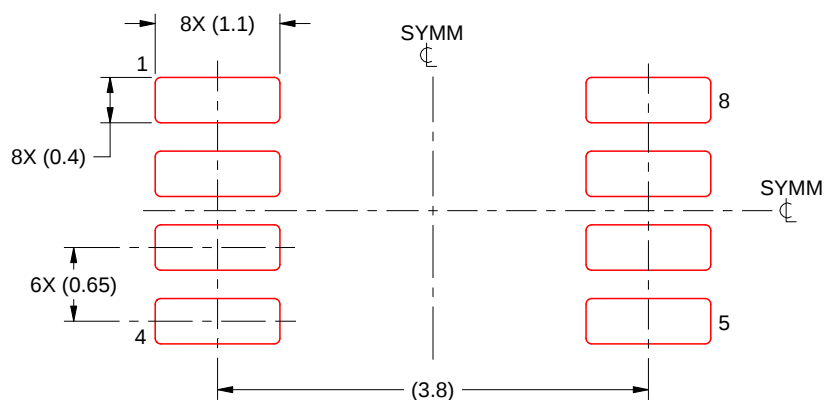
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

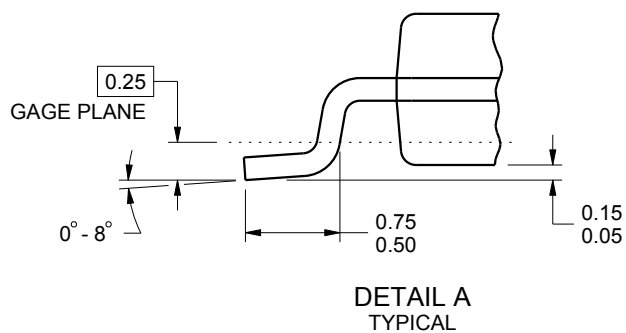
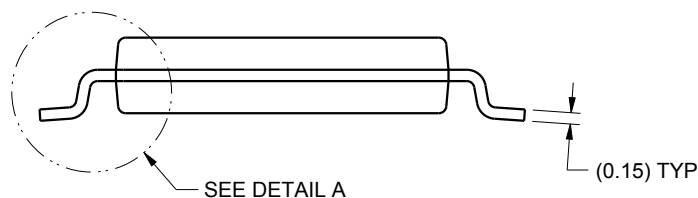
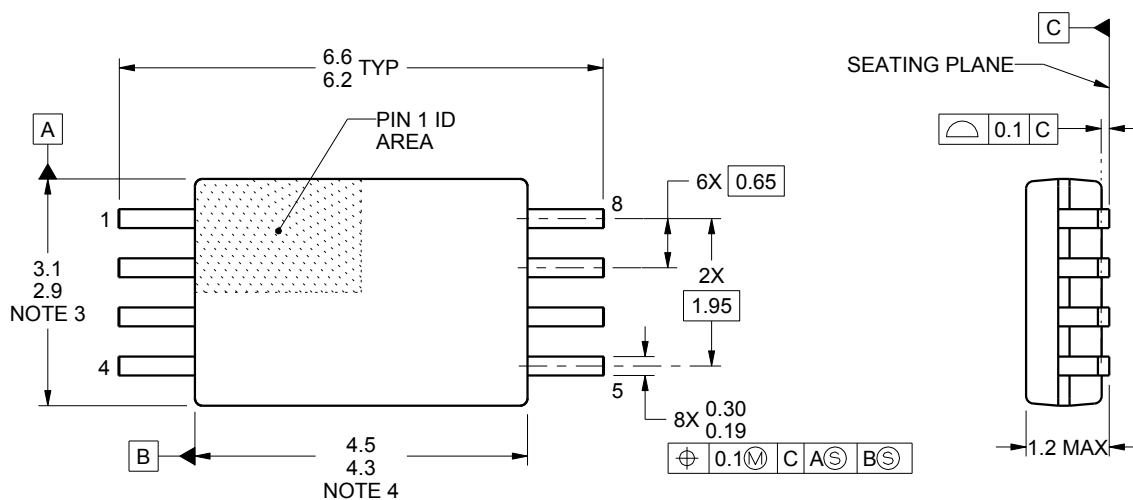
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



## PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

## SMALL OUTLINE PACKAGE



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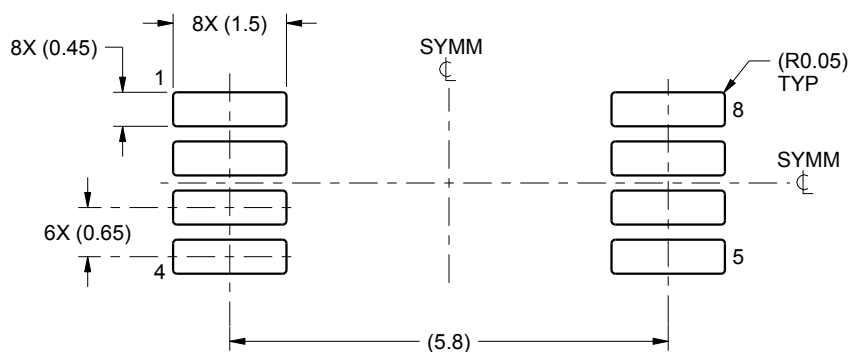
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
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4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

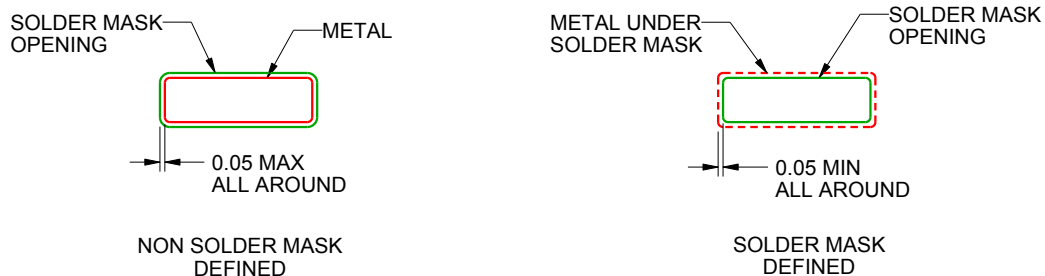
**PW0008A**

## TSSOP - 1.2 mm max height

## SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

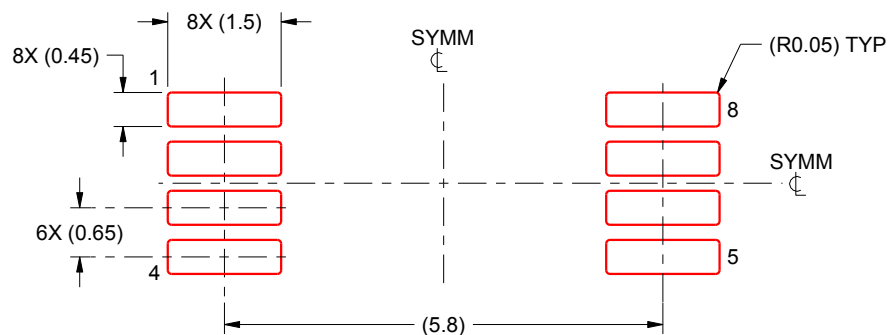
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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