TEXAS INSTRUMENTS

bq33100

ZHCSEJ8B – JANUARY 2011 – REVISED DECEMBER 2015

bq33100 超级电容管理器

1 特性

- 全集成超级电容管理器，适用于 2、3、4 或 5 个电容串联
- 在不提供单独电容监视和均衡功能的前提下，可与多达 9 个串联的电容搭配使用
- 有源电容电压均衡
  - 防止超级电容在充电过程中发生过压
- 电容健康状况监视
  - 电容学习
  - 等效串联电阻 (ESR) 测量
  - 运行状态
  - 充电状态
  - 健康状况
  - 充电电压和电流报告
  - 带可选引脚指示的安全报警
- 集成保护监控
  - 过压
  - 短路
  - 过热
  - 过量电容泄漏
- 2 线 SMBus 串行通信
- 高精度 16 位 Σ-Δ ADC，通过 16 通道多路复用器进行测量
  - 用于电压、电流和温度
- 低功耗
  - < 660µA（正常运行模式）
  - <1µA（关断模式）
- 宽运行温度范围：–40°C 至 +85°C

2 应用

- 备用电池的替代产品
- 缓存控制器
- RAID 系统
- 刀锋服务器卡
- 不间断电源 (UPS)
- 医疗与测试设备
- 便携式仪器

3 说明

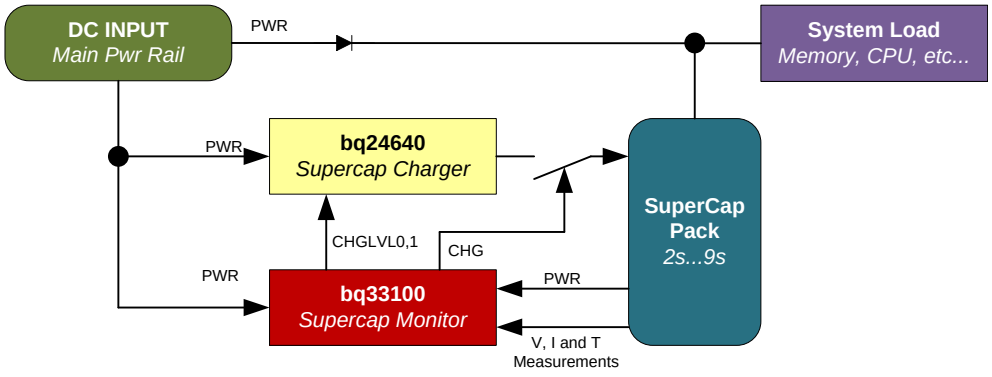
德州仪器 (TI) 的 bq33100 超级电容管理器是一款全集成单片解决方案，其提供有丰富的充电控制、监视和保护 功能， 不仅可为 2、3、4 或 5 个串联超级电容提供单独电容监视与均衡功能，还能够为多达 9 个串联电容提供电池组电压测量。bq33100 采用紧凑型 7.8mm × 6.4mm 24 引脚薄型小外形尺寸 (TSSOP) 封装，最大限度丰富功能和提高安全性的同时，还为超级电容应用极大地改善了易用性、削减了解决方案成本并减小了解决方案 尺寸。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
bq33100	TSSOP (24)	7.80mm × 4.40mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

bq33100 系统图



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (March 2011) to Revision B **Page**

- 已添加 *ESD 额定值表*，*特性 描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- OperationStatus() register bit 9 change from RSVD to CHGOR ... 38

Changes from Original (January 2011) to Revision A **Page**

- Changed SYSTEM PARTITIONING DIAGRAM. ... 14
- Changed Voltage as Current During Learning graphic. ... 15
- Changed equation 1 denominator from (V[D] - [C]) to (V[C] - V[D]) ... 15
- Changed Application Reference Schematic. ... 54

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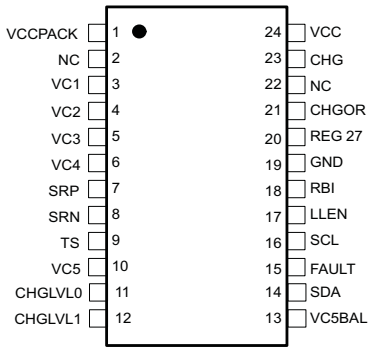
5 说明 （续）

bq33100 利用其集成的高性能模拟外设，测量超级电容的可用电容、健康状况、电压、电流、温度和其他关键参数，保留准确的数据记录，并通过 2 线 SMBus 1.1 兼容接口将这些信息报告给系统主机控制器。

bq33100 通过固件提供了过压、过温及过充保护，并通过硬件提供有放电过流及充放电短路保护。

6 Pin Configuration and Functions

PW Package
24-Pin TSSOP
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
CHG	23	O	P-Channel FET drive for controlling charge
CHGLVL0	11	O	Charge Control Output 0
CHGLVL1	12	O	Charge Control Output 1
CHGOR	21	I	CHG Over Ride input. If not used connect to VSS
FAULT	15	O	Active high output to indicate fault condition.
GND	19	P	Ground
LLEN	17	O	Learn Load Enable Output
NC	2	O	Not used and must be connected to VCC
NC	22	-	No connect, leave pin floating
RBI	18	P	RAM backup pin to provide backup potential to the internal DATA RAM if power is momentarily lost by using a capacitor attached between RBI and GND
REG27	20	P	Internal power supply 2.7-V bias output
SCL	16	I/OD	Serial clock input: Clocks data on SDA
SDA	14	I/OD	Serial Data: Transmits and Receives data
SRN	8	IA	Analog input pin connected to the internal ADC peripheral for measuring a small voltage between SRP and SRN where SRN is the bottom of the sense resistor.
SRP	7	IA	Analog input pin connected to the internal ADC peripheral for measuring a small voltage between SRP and SRN where SRP is the top of the sense resistor.
TS	9	IA	Thermistor input
VC1	3	IA	Sense voltage input terminal and external capacitor voltage balancing drive output for the 5th series capacitor, and stack measurement input. See *Series Capacitor Configuration* for systems with less than 5 series
VC2	4	IA	Sense voltage input terminal and external capacitor voltage balancing drive output for the 4th series capacitor. See *Series Capacitor Configuration* for systems with less than 5 series
VC3	5	IA	Sense voltage input terminal and external capacitor voltage balancing drive output for the 3rd series capacitor. See *Series Capacitor Configuration*for systems with less than 5 series

(1) I = Input, O = Output, P = Power, IA = Analog Input, OD = Open Drain

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Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VC4	6	IA	Sense voltage input terminal and external capacitor voltage balancing drive output for the 2nd series capacitor. See *Series Capacitor Configuration* for systems with less than 5 series
VC5	10	IA	Sense voltage input terminal and external capacitor voltage balancing drive output for the 1st capacitor. See *Series Capacitor Configuration* for systems with less than 5 series
VC5BAL	13	O	Cell balance control output for the least positive capacitor (only used in 5-series capacitor configuration)
VCCPACK	1	P	Power supply from the supercaps. The top of the supercap stack must be connected to this pin.
VCC	24	P	Positive input from power supply

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{MAX}	Supply voltage	VCC w.r.t. GND	–0.3	34	V
V_{IN}	Input voltage	VC1, VCC	V_{VC2} – 0.3	V_{VC2} + 8.5 or 34, whichever is lower	V
		VC2	V_{VC3} – 0.3	V_{VC3} + 8.5	V
		VC3	V_{VC4} – 0.3	V_{VC4} + 8.5	V
		VC4	V_{SRP} – 0.3	V_{SRP} + 8.5	V
		SRP, SRN	–0.3	V_{REG27}	V
		SDA, SCL	–0.3	6.0	V
		CHGOR	–0.3	VCC	V
		TS, VC5, CHGLVL0, CHGLVL1, FAULT	–0.3	V_{REG27} + 0.3	V
V_O	Output voltage	CHG	–0.3	VCC	V
		VC5BAL	–0.3	V_{REG27} + 0.3	V
		RBI, REG27	–0.3	2.75	V
I_{SS}	Maximum combined sink current for input pins			50	mA
T_{FUNC}	Functional temperature		–40	110	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage	VCC			25	V
		VCC	3.8		V_{VC2} + 5	
$V_{STARTUP}$		Start up voltage at VCC		5.2	5.5	V
$V_{SHUTDOWN}$		VCC or VCC, whichever is higher	3	3.2	3.3	V
V_{IN}	Input voltage	VC1, VCC	V_{VC2}		V_{VC2} + 5	V
		VC2	V_{VC3}		V_{VC3} + 5	
		VC3	V_{VC4}		V_{VC4} + 5	
		VC4	V_{SRP}		V_{SRP} + 5	
		VCn – VC(n + 1), (n=1, 2, 3, 4)	0		5	
		VC5	0		1	
		VCC			25	
		CHGOR	0		VCC – 0.3	V
		SRP to SRN	–0.3		1	V
C_{REG27}	External 2.7-V REG capacitor		1			µF
T_{OPR}	Operating temperature		–40		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		bq33100 PW (TSSOP) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: General Purpose I/O

Typical values stated where T_A = 25°C and VCC = VCC = 14.4 V, Minimum and maximum values stated where T_A = –40°C to 85°C and VCC = VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	SDA, SCL, TS, VC5	2			V
V_{IL}	Low-level input voltage	SDA, SCL, TS, VC5			0.8	V
V_{OH}	Output voltage high	SDA, SCL, VC5BAL, CHGLVL0, CHGLVL1, LLEN, FAULT, I_L = –0.5 mA	V_{REG27} – 0.5			V
V_{OL}	Low-level output voltage	SDA, SCL, VC5BAL, CHGLVL0, CHGLVL1, LLEN, FAULT, I_L = 7 mA			0.4	V
C_{IN}	Input capacitance			5		pF
I_{lkg}	Input leakage current	SDA, SCL, TS, VC5, CHGLVL0, CHGLVL1, LLEN, FAULT SDA and SCL pulldown disabled			1	µA
V_{CHGOR}	CHG Over Ride active high		0.8	2	3.2	V
$R_{PD(SMBx)}$	SDA and SCL pulldown	T_A = –40°C to 100°C	600	950	1300	kΩ
R_{PAD}	Pad resistance	TS		87	110	Ω

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7.6 Supply Current

Typical values stated where T_A = 25°C and VCC = VCC = 14.4 V, Minimum and maximum values stated where T_A = –40°C to 85°C and VCC = VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Normal mode	Firmware running, no flash writes		660		µA
$I_{SHUTDOWN}$	Shutdown mode	T_A = –40°C to 110°C		0.5	1	µA

7.7 REG27 LDO

Typical values stated where T_A = 25°C and VCC = VCC = 14.4 V, Minimum and maximum values stated where T_A = –40°C to 85°C and VCC = VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REG}–	Regulator output voltage	I_{REG27} = 10 mA	T_A = –40°C to 85°C	2.5	2.7	2.75	V
$V_{REG27IT–}$	Negative-going POR voltage	At REG27		2.22	2.35	2.34	V
$V_{REG27IT+}$	Positive-going POR voltage	At REG27		2.25	2.5	2.6	V
$\Delta V_{(REGTEMP)}$	Regulator output change with temperature	I_{REG} = 10 mA	T_A = –40°C to 85°C		±0.5%		
$\Delta V_{(REGLINE)}$	Line regulation	I_{REG} = 10 mA			±2	±4	mV
$\Delta V_{(REGLOAD)}$	Load regulation	I_{REG} = 0.2 to 10 mA			±20	±40	mV
$I_{(REGMAX)}$	Current limit			25		50	mA

7.8 Coulomb Counter

Typical values stated where T_A = 25°C and VCC = VCC = 14.4 V, Minimum and maximum values stated where T_A = –40°C to 85°C and VCC = VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		–0.2		0.25	V
Conversion time	Single conversion		250		ms
Effective resolution	Single conversion	15			Bits
Integral nonlinearity	T_A = –25°C to 85°C		±0.007	±0.034	%FSR
Offset error(1)	T_A = –25°C to 85°C		10		µV
Offset error drift			0.3	0.5	µV/°C
Full-scale error(2)		–0.8%	0.2%	0.8%	
Full-scale error drift				150	PPM/°C
Effective input resistance		2.5			MΩ

(1) Post Calibration Performance
(2) Uncalibrated performance. This gain error can be eliminated with external calibration.

7.9 ADC

Typical values stated where T_A = 25°C and VCC = VCC = 14.4 V, Minimum and maximum values stated where T_A = –40°C to 85°C and VCC = VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input voltage range	TS, VC5	–0.2		0.8 × V_{REG27}	V
Conversion time			31.5		ms
Resolution (no missing codes)		16			Bits
Effective resolution		14	15		Bits
Integral nonlinearity				±0.02	%FSR
Offset error(1)			70	160	µV
Offset error drift			1		µV/°C
Full-scale error	V_{IN} = 1 V	–0.8%	±0.2%	0.4%	
Full-scale error drift				150	PPM/°C
Effective input resistance		8			MΩ

(1) Channel to channel offset

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7.10 External Capacitor Voltage Balance Drive

Typical values stated where T_A = 25°C and VCC = VCC = 14.4 V, Minimum and maximum values stated where T_A = –40°C to 85°C and VCC = VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{BAL_drive}	Internal pulldown resistance for external capacitor voltage balance	Capacitor voltage balance ON for VC1, VCi – VCi + 1 = 4 V, where i = 1 to approximately 4		5.7		kΩ
		Capacitor voltage balance ON for VC2, VCi – VCi + 1 = 4 V, where = i = 1 to approximately 4		3.7		
		Capacitor voltage balance ON for VC3, VCi – VCi + 1 = 4 V, where = i = 1 to approximately 4		1.75		
		Capacitor voltage balance ON for VC4, VCi – VCi + 1 = 4 V, where = i = 1 to approximately 4		0.85		

7.11 Capacitor Voltage Monitor

Typical values stated where T_A = 25°C and VCC = VCC = 14.4 V, Minimum and maximum values stated where T_A = –40°C to 85°C and VCC = VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CAPACITOR Voltage Measurement Accuracy	T_A = –10°C to 60°C		±10	±20	mV
	T_A = –40°C to 85°C		±10	±35	

7.12 Internal Temperature Sensor

Typical values stated where T_A = 25°C and VCC = VCC = 14.4 V, Minimum and maximum values stated where T_A = –40°C to 85°C and VCC = VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{(TEMP)}$	Temperature sensor accuracy			±3%		°C

7.13 Thermistor Measurement Support

Typical values stated where T_A = 25°C and VCC = VCC = 14.4 V, Minimum and maximum values stated where T_A = –40°C to 85°C and VCC = VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ERR}	Internal resistor drift			–230		ppm/°C
R	Internal resistor	TS		17	20	kΩ

7.14 Internal Thermal Shutdown

Typical values stated where T_A = 25°C and VCC = VCC = 14.4 V, Minimum and maximum values stated where T_A = –40°C to 85°C and VCC = VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{MAX}	Maximum REG27 temperature		125		175	°C
$T_{RECOVER}$	Recovery hysteresis temperature			10		°C

(1) Parameters assured by design. Not production tested.

7.15 High-Frequency Oscillator

Typical values stated where T_A = 25°C and VCC = VCC = 14.4 V, Minimum and maximum values stated where T_A = –40°C to 85°C and VCC = VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Operating frequency of CPU clock			2.097		MHz
$f_{(EIO)}$	Frequency error(1)	T_A = –20°C to 70°C	–2%	±0.25%	2%	
		T_A = –40°C to 85°C	–3%	±0.25%	3%	
$t_{(SXO)}$	Start-up time(2)	T_A = –25°C to 85°C		3	6	ms

(1) The frequency drift is included and measured from the trimmed frequency at VCC = VCC = 14.4 V, T_A = 25°C
(2) The start-up time is defined as the time it takes for the oscillator output frequency to be ±3% when the device is already powered.

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7.16 Low-Frequency Oscillator

Typical values stated where T_A = 25°C and VCC = VCC = 14.4 V, Minimum and maximum values stated where T_A = –40°C to 85°C and VCC = VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(LOSC)}$	Operating frequency			32.768		MHz
$f_{(LEIO)}$	Frequency error(1)	T_A = –20°C to 70°C	–1.5%	±0.25%	1.5%	
		T_A = –40°C to 85°C	–2.5%	±0.25%	2.5%	
$t_{(LSXO)}$	Start-up time(2)	T_A = –25°C to 85°C			100	ms

(1) The frequency drift is included and measured from the trimmed frequency at VCC = VCC = 14.4 V, T_A = 25°C.
(2) The start-up time is defined as the time it takes for the oscillator output frequency to be ±3%.

7.17 RAM Backup

Typical values stated where T_A = 25°C and VCC = VCC = 14.4 V, Minimum and maximum values stated where T_A = –40°C to 85°C and VCC = VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(RBI)}$	RBI data-retention input current	$V_{RBI} > V_{(RBI)MIN}$, $V_{REG27} < V_{REG27IT-}$, T_A = 70°C to 110°C		20	1500	nA
		$V_{RBI} > V_{(RBI)MIN}$, $V_{REG27} < V_{REG27IT-}$, T_A = –40°C to 70°C			500	
$V_{(RBI)}$	RBI data-retention voltage(1)		1			V

(1) Specified by design. Not production tested.

7.18 Flash

Typical values stated where T_A = 25°C and VCC = VCC = 14.4 V, Minimum and maximum values stated where T_A = –40°C to 85°C and VCC = VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention		10			Years
	Flash programming write-cycles		20k			Cycles
$t_{(ROWPROG)}$	Row programming time				2	ms
$t_{(MASSERASE)}$	Mass-erase time				250	ms
$t_{(PAGEERASE)}$	Page-erase time				25	ms
$I_{CC(PROG)}$	Flash-write supply current			4	6	mA
$I_{CC(ERASE)}$	Flash-erase supply current	T_A = –40°C to 0°C		8	22	mA
		T_A = 0°C to 85°C		3	15	

(1) Specified by design. Not production tested

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7.19 Current Protection Thresholds

Typical values stated where T_A = 25°C and VCC = VCC = 14.4 V, Minimum and maximum values stated where T_A = –40°C to 85°C and VCC = VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(OCD)}$	OCD detection threshold voltage range, typical	RSNS = 0	RSNS is set in STATE_CTL register	50		200	mV
		RSNS = 1		25		100	
$\Delta V_{(OCDT)}$	OCD detection threshold voltage program step	RSNS = 0			10		mV
		RSNS = 1			5		
$V_{(SCCT)}$	SCC detection threshold voltage range, typical	RSNS = 0		–100		–300	mV
		RSNS = 1		–50		–225	
$\Delta V_{(SCCT)}$	SCC detection threshold voltage program step	RSNS = 0			–50		mV
		RSNS = 1			–25		
$V_{(SCDT)}$	SCD detection threshold voltage range, typical	RSNS = 0		100		450	mV
		RSNS = 1		50		225	
$\Delta V_{(SCDT)}$	SCD detection threshold voltage program step	RSNS = 0			50		mV
		RSNS = 1			25		
$V_{(OFFSET)}$	SCD, SCC and OCD offset			–10		10	mV
$V_{(Scale_Err)}$	SCD, SCC and OCD scale error			–10%		10%	

7.20 Current Protection Timing

Typical values stated where T_A = 25°C and VCC = VCC = 14.4 V, Minimum and maximum values stated where T_A = –40°C to 85°C and VCC = VCC = 3.8 V to 25 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$t_{(OCDD)}$	Overcurrent in discharge delay		1		31	ms
$t_{(OCDD_STEP)}$	OCDD step options			2		ms
$t_{(SCDD)}$	Short circuit in discharge delay	AFE.STATE_CNTL[SCDDx2] = 0	0		915	µs
		AFE.STATE_CNTL[SCDDx2] = 1	0		1830	
$t_{(SCDD_STEP)}$	SCDD step options	AFE.STATE_CNTL[SCDDx2] = 0		61		µs
		AFE.STATE_CNTL[SCDDx2] = 1		122		
$t_{(SCCD)}$	Short circuit in charge delay		0		915	µs
$t_{(SCCD_STEP)}$	SCCD step options			61		µs
$t_{(DETECT)}$	Current fault detect time	$V_{SRP-SRN} = V_{THRESH}$ + 12.5 mV, T_A = –40°C to 85°C		35	160	µs
t_{ACC}	Overcurrent and short circuit delay time accuracy	Accuracy of typical delay time with WDI active	–20%		20%	
		Accuracy of typical delay time with no WDI input	–50%		50%	

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7.21 Timing Requirements: SMBus

Typical values stated where T_A = 25°C and VCC = VCC = 14.4 V, Minimum and maximum values stated where T_A = –40°C to 85°C and VCC = VCC = 3.8 V to 25 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
f_{SMB}	SMBus operating frequency	Slave mode, SCL 50% duty cycle	10		100	kHz
f_{MAS}	SMBus master clock frequency	Master mode, no clock low slave extend		51.2		kHz
t_{BUF}	Bus free time between start and stop		4.7			µs
$t_{HD:STA}$	Hold time after (repeated) start		4			µs
$t_{SU:STA}$	Repeated start setup time		4.7			µs
$t_{SU:STO}$	Stop setup time		4			µs
$t_{HD:DAT}$	Data hold time	Receive mode	0			ns
		Transmit mode	300			
$t_{SU:DAT}$	Data setup time		250			ns
$t_{TIMEOUT}$	Error signal and detect	See (1)	25		35	ms
t_{LOW}	Clock low period		4.7			µs
t_{HIGH}	Clock high period	See (2)	4		50	µs
$t_{LOW:SEXT}$	Cumulative clock low slave extend time	See (3)			25	ms
$t_{LOW:MEXT}$	Cumulative clock low master extend time	See (4)			10	ms
t_F	Clock and data fall time	See (5)			300	ns
t_R	Clock and data rise time	See (6)			1000	ns

(1) The bq33100 times out when any clock low exceeds $t_{TIMEOUT}$
(2) t_{HIGH} maximum is the minimum bus idle time. SCL = SDA = 1 for t > 50 µs causes reset of any transaction involving bq33100 that is in progress.
(3) $t_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(4) $t_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.
(5) Rise time $t_R = V_{ILMAX} – 0.15$) to ($V_{IHMIN} + 0.15$)
(6) Fall time $t_F = 0.9V_{DD}$ to ($V_{ILMAX} – 0.15$)

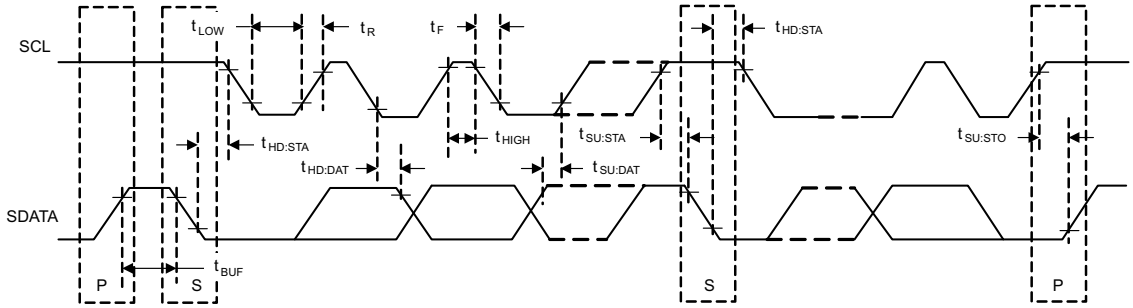


Figure 1. SMBus Timing

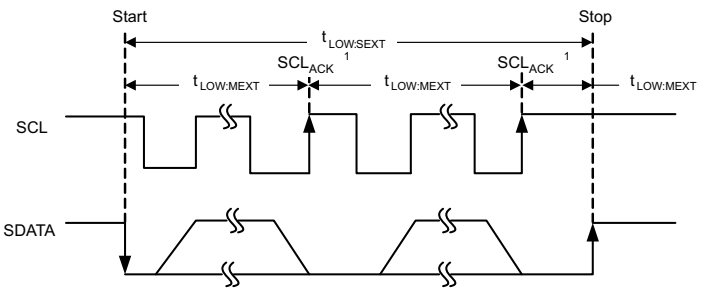


Figure 2. SMBus $t_{TIMEOUT}$

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7.22 Typical Characteristics

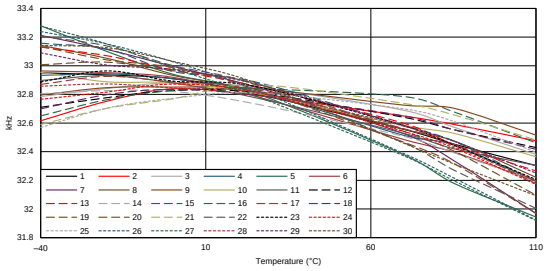


Figure 3. Low Frequency Oscillator (LFO) Value Across Temperature With REG27 = 2.5 V

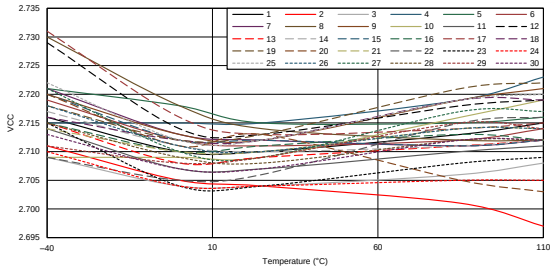


Figure 4. REG27 Output Voltage Variation Across Temperature With a Nominal Load of 2 mA

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8 Detailed Description

8.1 Overview

The bq33100 is a Super Capacitor monitor, balancing controller and overall system manger. The device can individually monitor up to 5 series capacitors and up to 9 when monitoring the total stack.

The device can also interact with a external charging solution to provide Capacitance and Effective Series Resistance (ESR) data on the stack.

NOTE

The following notation is used in this document, if SBS commands and Data Flash values are mentioned within a text block:

- SBS commands are set in italic, for example: *Voltage*
- SBS bits and flags are capitalized, set in italic and enclosed with square brackets, for example: *[SS]*
- Data Flash values are set in bold italic, for example: ***OV Threshold***
- All Data Flash bits and flags are capitalized, set in bold italic and enclosed with square brackets, for example: ***[OV]***

All SBS commands, Data Flash values and flags mentioned in a chapter are listed at the beginning of each chapter for reference.

The reference format for SBS commands is:
SBS:Command Name(Command No.):Manufacturer Access(MA No.)[Flag], for example:

SBS:Voltage(0x09), or SBS:ManufacterAccess(0x00):Seal Device(0x0020)

8.1.1 Super Capacitor Measurements

The bq33100 measures the series capacitor voltages or stack voltage, current and temperature using a delta-sigma analog-to-digital converter (ADC). The bq33100 uses this measured data and advanced algorithms to determine the State-of-Health and available capacitance of the Super Capacitor.

8.1.1.1 Voltage

The bq33100 has two separate modes, Normal mode and Stack mode, where measurements and taken and managed differently. The setting of ***Operation Cfg [STACK]*** to 1 enables Stack mode otherwise the bq33100 operates in normal mode.

The bq33100 updates the individual series capacitor voltages and stack voltage at one (1) second intervals when in Normal mode and measurers the stack voltage at one (1) second intervals when in Stack mode. The internal ADC of the bq33100 measures the voltage, scales, and offsets, and calibrates it appropriately. To ensure an accurate differential voltage sensing, the IC ground must be connected directly to the most negative terminal of the Super Capacitor stack, not to the positive side of the sense resistor. This minimizes the voltage drop across the PCB trace.

8.1.1.2 Current, Charge and Discharge Counting

The delta-sigma ADC measures the system current of the Super Capacitor by measuring the voltage drop across a small-value sense resistor (typically 5 mΩ to 20 mΩ typical) between the SRP and SRN pins. The ADC measures bipolar signals from –0.20 V to 0.25 V.

8.1.1.3 Device Calibration

The bq33100 requires voltage calibration to maximize accuracy of the monitoring system, the bq33100 evaluation software can perform this calibration. The external filter resistors, connected from each capacitor to the VCx input of the bq33100, are required to be 1 kΩ.

The bq33100 can automatically calibrate its offset between the A to D converter and the input of the high voltage translation circuit during normal operation for maximum capacitor voltage measurement accuracy.

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Overview (continued)

8.1.1.4 Temperature

The bq33100 has an internal temperature sensor and input for an external temperature sensor input, TS. The external input is used in conjunction with an NTC thermistor (default is Semitec 103AT) to sense the Super Capacitor temperature. The bq33100 can be configured to use internal or external temperature sensors.

8.1.1.5 Series Capacitor Configuration

The bq33100 can be used to monitor 2, 3, 4 or 5 capacitors in series. The appropriate connectivity for the different options are detailed in Table 1.

Table 1. Series Capacitor Connectivity

bq33100 PIN	5-SERIES	4-SERIES	3-SERIES	2-SERIES
VC1	P of Top (5th) Cap	P of 4th Cap	Short to VC2	Short to VC2
VC2	P of 4th Cap, N of 5th Cap	P of 3rd Cap, N of 4th Cap	P of 3rd Cap	Short to VC3
VC3	P of 3rd Cap, N of 4th Cap	P of 2nd Cap, N of 3rd Cap	P of 2nd Cap, N of 3rd Cap	P of 2nd Cap
VC4	P of 2nd Cap, N of 3rd Cap	P of Bottom (1st) Cap, N of 2nd Cap	P of Bottom (1st) Cap, N of 2nd Cap	P of Bottom (1st) Cap, N of 2nd Cap
VC5	P of Bottom (1st) Cap, N of 2nd Cap	N of Bottom Cap (1st)	N of Bottom Cap (1st)	N of Bottom Cap (1st)
VSS	N of Bottom Cap (1st)	Short to VC5	Short to VC5	Short to VC5

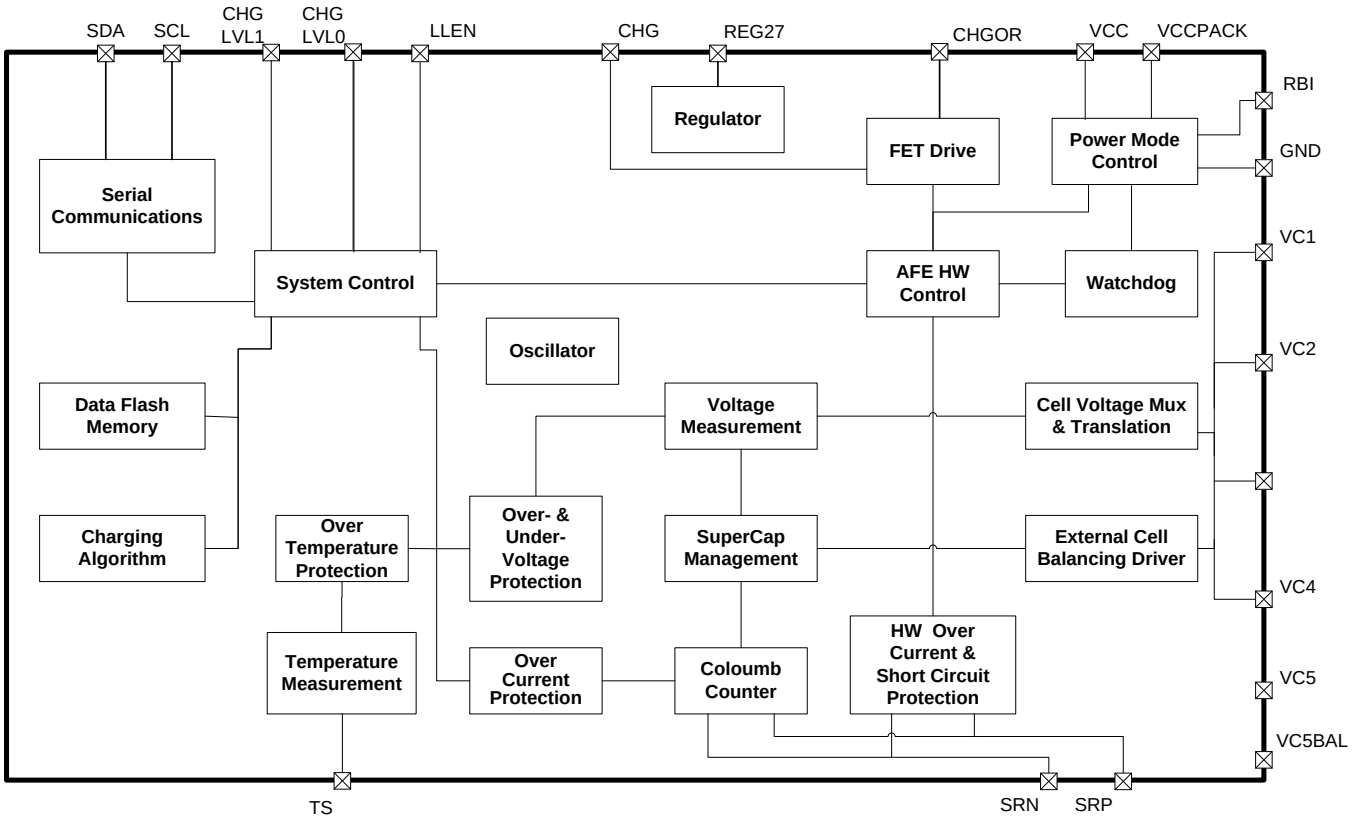
NOTE

The CC0...CC2 bits in Operation Cfg must be programmed to match the corresponding configuration.

When in Stack mode (Operation Cfg [STACK] =1) VC1 must be connected to VC2 and VC3 connected to VC4. Additionally a *divide-by-2* resistor divider must connect between the top and bottom of the capacitor array with VC1,2 being the top and VC3,4 being the middle and VSS being the bottom. In this configuration pins VC5 and VC5BAL are not used and must be connected to VSS.

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8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Capacitance Monitoring and Learning

8.3.1.1 Monitoring and Control Operational Overview

The bq33100 periodically determines the capacitance and equivalent series resistance (ESR) of the super capacitor array during normal operation. The ***Learning Frequency*** is a register that sets the time between automatic learning cycles of the Super Capacitor which can also be manually executed by issuing a *Learn* command. The bq33100 uses the learning cycles to update the *Capacitance* and *ESR* registers accordingly and both are accessible through the SMBus interface.

Learning process is a multi-step procedure fully controlled by the bq33100 that will perform the following sequence to learn Capacitance and ESR:

1. Charge to ***V Learn Max***
2. Discharge using constant current load to a minimum voltage of the present charging voltage and internally record voltage and time
3. Charge to ***V Learn Max***
4. Discharge using constant current load and internally record current and time
5. Calculate Capacitance and ESR based on recorded voltage and current
6. Determine new Charging Voltage

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Feature Description (continued)

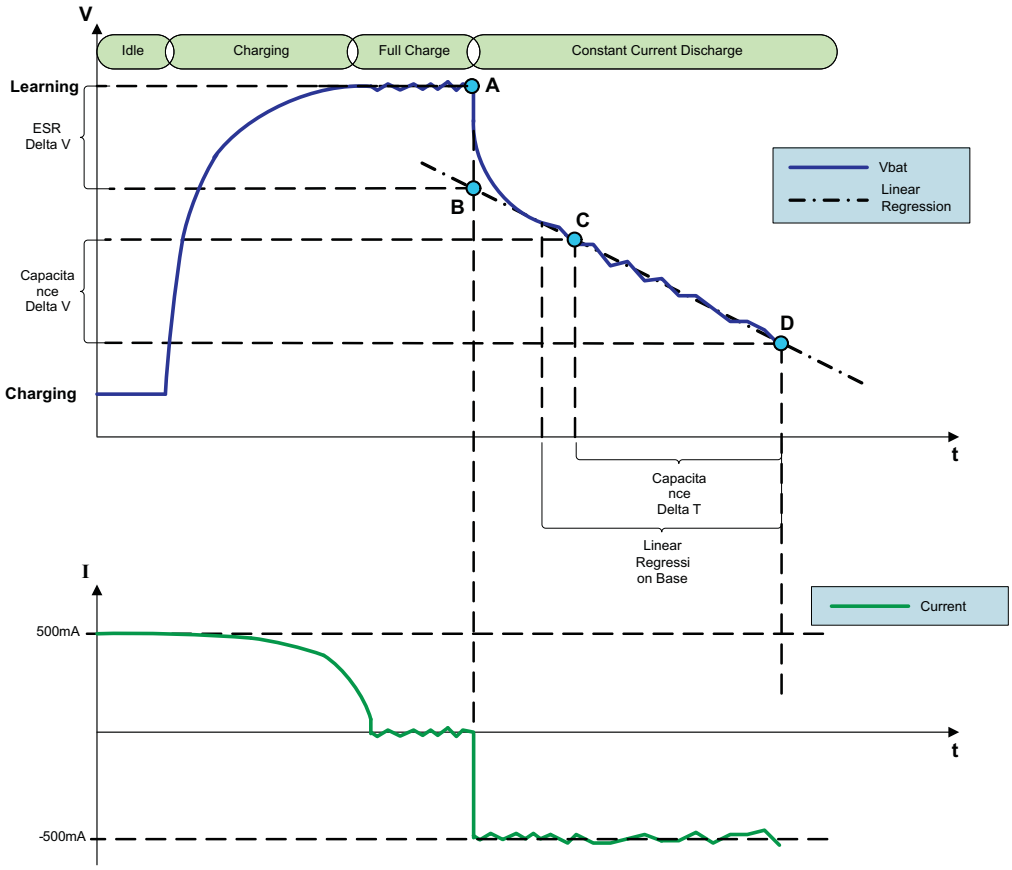


Figure 5. Voltage as Current During Learning

where:

$$C = I \times (t[D]–t[C])/(V[C]–V[D]) \quad (1)$$

and

$$ESR = (V[A]–V[B])/I \quad (2)$$

8.3.1.2 Main Monitoring Registers

Capacitance represents the total capacitance in the capacitor array and presents the value in units of F (Farads) to 1 decimal place.

On initialization, the bq33100 sets *Capacitance* to the data flash value stored in ***Initial Capacitance***. During subsequent learning cycles, the bq33100 updates *Capacitance* with the last measured capacitance of the . Once updated, the bq33100 writes the new *Capacitance* value to data flash to ***Capacitance***. *Capacitance* represents the full Super Capacitor reference for relative state of charge calculations.

InitialCapacitance — The first updated value of Super Capacitor capacitance and represented in units of F.

RelativeStateOfCharge (RSOC) represents the % of available energy. Use Equation 3 to calculate the RSOC.

(*Voltage* – ***Min voltage***) / (Charging Voltage – ***Min voltage***) (3)

Learning Frequency — The Learning Frequency register sets the time between automatic learning cycles of the Super Capacitor which can also be manually executed by issuing a *ManufacturerAccess Learn* command. The bq33100 uses the learning cycles to measure the Super Capacitor capacitance and update the Capacitance register accordingly. When the bq33100 is in Unsealed Mode then a value of 250 is used to set the Learning Frequency to 10 minutes for test purposes.

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Feature Description (continued)

8.3.1.3 Initial Capacitance at Device Reset

The bq33100 estimates the initial capacitance of a at device reset, which is the case when the capacitors are first attached to the application circuit. This gives a reasonably accurate Capacitance and RSOC value, however, Super Capacitor capacitance learning is required in order to improve the accuracy of Capacitance and RSOC.

8.3.1.4 Qualified Capacitance Learning

The bq33100 updates Capacitance with an amount based on the value learned during a qualified learning cycle. Once updated, the bq33100 writes the new *Capacitance* value to data flash to ***Capacitance***.

The bq33100 sets *[CL]* = 1 and clears *[LPASS]* in *Operation Status* when a qualified capacitance learning cycle begins. The period of time that the learning takes is set by ***CL Time*** although the first learning cycle after a device reset will not occur until after an elapsed time of ***Learning Frequency***. When a qualified learn has occurred *[LPASS]* in *Operation Status* is set.

During the learning process there are specific timeouts to protect from over charge or over discharge of the super capacitor array. At the beginning of each phase of charge and discharge a timer is started. If the timer exceeds ***Max Discharge Time*** during the discharging phase then *Operation Status [LDTO]* is set if the timer exceeds ***Max Charge Time*** for the charging phase then *Operation Status [LCTO]* is set. the flags are cleared upon the beginning of the next learning cycle.

8.3.1.5 Health Determination

The bq33100 uses Equation 4 to determine the relative health of the capacitor.

$$Health = (Capacitance / InitialCapacitance) \quad (4)$$

The bq33100 will determine a new *ChargingVoltage* at end of the learning cycle based on the newly learned *Capacitance*. The following warnings will be set based on the changes in *ChargingVoltage* and the capacitors ability to provide the minimum power needs.

ChargingVoltage = ***V Chg Nominal*** then *SafetyStatus[HLOW]*, *[HWARN]* and *[HFAIL]* are cleared.

If *ChargingVoltage* is set to ***V Chg A*** or ***V Chg B*** then *SafetyStatus[HLOW]* is set.

If *ChargingVoltage* is set to ***V Chg Max*** then *SafetyStatus [HWARN]* is set.

If *ChargingVoltage* is set to ***V Chg Max*** and the bq33100 determines that the newly learned *Capacitance* cannot provide the minimum power requirements then *SafetyStatus [HFAIL]* is set.

The minimum power requirements is determined by the ***Min Power***, ***Required Time*** and ***Min Voltage*** data flash values.

If the corresponding ***[HLOW]***, ***[HWARN]*** or ***[HFAIL]*** bits are set in ***FAULT*** when the *SafetyStatus[HLOW]* or *[HWARN]* bit is set then the FAULT pin is set.

8.3.1.6 ESR Measurement

The bq33100 measures the voltage on the capacitor stack when the LLEN pin (pin 17) is high with the initial learned value stored in ***Initial ESR*** which is only updated once. The LLEN pin is controlled by firmware to enable a circuit that presents a constant current load to the full capacitor stack. With the known voltage and known current the ESR of the capacitor array can be determined. The final reported value of *ESR* is also adjusted by the data flash value of ***ESR Offset***. The original value of the capacitor array *ESR* is stored in ***Design ESR*** but is not used by the bq33100.

The final value of *ESR* can be read from the bq33100 through *ESR* which is in mΩ.

8.3.1.7 Monitor Operating Modes

Entry and exit of each mode is controlled by data flash parameters. In Discharge Mode, the *[DSG]* flag in *Operation Status* is set. Discharge mode is entered when *Current* goes below (-)***Dsg Current Threshold***. Discharge mode is exited when *Current* goes above ***Chg Current Threshold*** threshold for more than 1 second.

Charge mode is entered when *Current* goes above ***Chg Current Threshold***. Charge mode is exited when *Current* goes below ***Dsg Current Threshold*** for more than 1 second.

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Feature Description (continued)

8.3.2 Capacitor Voltage Balancing

Capacitor voltage balancing in the bq33100 is accomplished by connecting an external parallel bypass load to each capacitor, and enabling the bypass load depending on each individual capacitors voltage level. The bypass load is typically formed by a P-ch MOSFET and a resistor connected in series across each capacitor. The filter resistors that connect the capacitor tabs to VC1 to approximately VC4 pins of the bq33100 are required to be 1 k ohms to support this function on all capacitors other than the lowest. The lowest capacitor bypass is enabled through the VC5BAL pin. Capacitor Voltage Balancing is only operational after the *ManufacturerAccess* Lifetime and Capacitor Balancing Enable (0x21) command is sent to the bq33100.

Using this circuit, the bq33100 balances the capacitors during charge and after charge termination by discharging those capacitors with voltage above the threshold set in ***CB Threshold*** and if the ΔV in capacitor voltages exceeds the value programmed in ***CB Min***. During capacitor voltage balancing, the bq33100 measures the capacitor voltages periodically (during which time the voltage balancing circuit is turned off) and based on the capacitor voltages, the bq33100 selects the appropriate capacitor to discharge. When ΔV of *CapacitorVoltage5...1* < ***CB Min*** then capacitor voltage balancing stops. Capacitor voltage balancing restarts when ΔV of *CapacitorVoltage5...1* ≥ ***CB Restart*** to avoid balancing start-stop oscillations.

Capacitor voltage balancing only occurs when:

- Charging current is detected (*Current* > ***Chg Current Threshold*** OR
- The *[FC]* flag in *OperationStatus* has been set AND
- Δ*CapacitorVoltage5...1* ≥ ***CB Restart***

Capacitor voltage balancing stops when:

- Δ*CapacitorVoltage5...1* < ***CB Min***
- Discharging current detected (*Current* > ***Dsg Current Threshold***)

This feature is disabled when in Stack mode, when ***Operation Cfg [STACK]*** =1.

8.3.3 Charge Control

The bq33100 supports two main charge control architectures, discrete control and smart control. In a discrete charge control implementation the CHGLVL0 and CHGLVL1 pins can be used to adjust the charging voltage of an external supply (see reference schematic for example).

As the super capacitors age a higher charging voltage can be configured to offset the deteriorating super capacitor ESR and Capacitance due to aging. With the discrete control method there are 4 levels of charging voltages that can be chosen, ***V Chg Nominal***, ***V Chg A***, ***V Chg B*** and ***V Chg Max***. The setting of the charging voltage is determined by the value of the latest determined required *Charging Voltage*.

The CHGLVL0 and CHGLVL1 pin states are defined by the V Chg X parameters selected per Table 2:

Table 2. ChargingVoltage Parameters

CHARGINGVOLTAGE	CHGLVL1 (PIN 12)	CHGLVL0 (PIN11)
V Chg Nominal	0	0
V Chg A	0	1
V Chg B	1	0
V Chg Max	1	1

In a smart control architecture the bq33100 makes the appropriate maximum charging current and charging voltage per the charging algorithm available through the *ChargingCurrent* and *ChargingVoltage* SMBus commands respectively. This enables either an SMBus master or smart charger to manage the charging of the super capacitor pack.

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8.3.3.1 Charge Termination

The bq33100 determines charge termination if:

- The average charge current < ***Taper Current*** during 2 consecutive ***Current Taper Window*** time periods, AND
- *Voltage* + ***Taper Voltage*** ≥ *ChargingVoltage*

NOTE

To make sure that the charge terminates properly, TI recommends that ***Taper Current*** be set to a value greater than the maximum charger voltage inaccuracy. In other words, the charger taper current must be set to a lower value than the taper current programmed in the dataflash to ensure proper charge termination and the FC bit gets set.

The bq33100 sets the *[FC]* flag in *Operation Status* when a valid charge termination occurs and cleared when *RelativeStateOfCharge* is less than ***FC Clear %***.

The ***taper voltage*** must be set to a value less than the ***OV threshold***. This prevents an over voltage condition from occuring after the CL bit clears upon learning completion.

The bq33100 can also determine charge termination if the RSOC is at a value equal to or greater than ***FC set %***. If this is not the desired means of charge termination, ***FC set %*** must be set to -1%.

8.3.3.2 CHG Over Ride Control

During the normal operation of the bq33100 the CHG output of the bq33100 is typically controlled automatically but can be over ridden through the CHGOR pin (pin 21). On a low-to-high transition the CHG output is released turning off the external CHG FET and on a high-to-low transition the CHG output is pulled low after a programmable delay ***CHG Enable Delay***. If ***CHG Enable Delay*** is programmed to 0 the delay is a maximum of 250 ms. If the CHG over ride function is not needed then the CHGOR pin must connect to VSS.

8.3.4 Lifetime Data Gathering

8.3.4.1 Lifetime Maximum Temperature

During the operation lifetime of the bq33100 it gathers temperature data. During this time the bq33100 can be enabled to record the maximum value that the measured temperature reached. If the [*LTE*] flag is set in *OperationStatus*, ***Lifetime Max Temp*** value is updated if one of the following conditions are met:

- internal measurement temperature – ***Lifetime Max Temp*** > 1 °C.
- internal measurement temperature > ***Lifetime Max Temp*** for a period > 60 seconds
- internal measurement temperature > ***Lifetime Max Temp*** AND any other lifetime value is updated.

Table 3. Lifetime Maximum Temperature

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
59	Lifetime Data	0	Lifetime Max Temp	Integer	2	0	1400	350	0.1°C

8.3.4.2 Lifetime Minimum Temperature

During the operation lifetime of the bq33100 it gathers temperature data. During this time the bq33100 can be enabled to record the Minimum value that the measured temperature reached. If the [*LTE*] flag is set, ***Lifetime Min Temp*** is updated if one of the following conditions are met:

- ***Lifetime Min Temp*** – internal measurement temperature > 1 °C.
- ***Lifetime Min Temp*** > internal measurement temperature for a period > 60 seconds
- ***Lifetime Min Temp*** > internal measurement temperature > AND any other lifetime value is updated.

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Table 4. Lifetime Minimum Temperature

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
59	Lifetime Data	2	Lifetime Min Temp	Integer	2	–600	1400	50	0.1°C

8.3.4.3 Lifetime Maximum Capacitor Voltage

During the operation lifetime of the bq33100 it gathers voltage data and if in Single mode (***Operation Cfg [STACK]*** =0). During this time the bq33100 can be enabled to record the Maximum value that the measured voltage reached. If the [*LTE*] flag is set, ***Lifetime Max Capacitor Voltage*** is updated if one of the following conditions are met:

- any internally measured capacitor voltage – ***Lifetime Max Capacitor Voltage*** > 25 mV
- any internally measured capacitor voltage > ***Lifetime Max Capacitor Voltage*** for a period > 60 seconds
- any internally measured capacitor voltage ***Lifetime Max Capacitor Voltage*** AND any other lifetime value is updated.

Table 5. Lifetime Max Capacitor Voltage

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
59	Lifetime Data	4	Lifetime Max Capacitor Voltage	Integer	2	0	32767	0	mV

8.3.5 Safety Detection Features

The bq33100 supports a wide range of Super Capacitor and system safety detection and protection features that are easily configured or enabled through the integrated data flash. These features are intended, through various configuration options, to provide a level of safety from external influences causing damage to components with the power path, for example: limiting the period of time the CHG FET is exposed to high current pulse charge conditions

8.3.5.1 Capacitor Overvoltage (OV)

The bq33100 can detect capacitor overvoltage condition and protect capacitors from damage.

When any *CapacitorVoltage5...1* exceeds (*ChargingVoltage* / number of capacitors (see ***Operation Cfg [CC2,1,0]***) + ***OV Threshold***) the *[OV]* flag in *SafetyAlert* is set.

When any *CapacitorVoltage5...1* exceeds (*ChargingVoltage* / number of capacitors (see ***Operation Cfg [CC2,1,0]***) + ***OV Threshold***) for a period greater than ***OV Time*** the *[OV]* flag in *SafetyStatus* is set.

When the bq33100 is configured for Pack Mode, when ***Operation Cfg [STACK]*** =1, then a fault is detected when *Voltage* exceeds (*ChargingVoltage* + ***OV Threshold***) the *[OV]* flag in *SafetyAlert* is set.

When the bq33100 is configured for Pack Mode, when ***Operation Cfg [STACK]*** =1, then a fault is detected when *Voltage* exceeds (*ChargingVoltage* + ***OV Threshold***) for a period greater than ***OV Time*** the *[OV]* flag in *SafetyStatus* is set.

This function is disabled if ***OV Time*** is set to zero.

In an overvoltage condition charging is disabled and the CHG FET is turned off, *ChargingCurrent* and *ChargingVoltage* are set to zero.

The bq33100 recovers from a capacitor overvoltage condition if all *CapacitorVoltages5..1* are equal to or lower than (*ChargingVoltage* / number of capacitors (see ***Operation Cfg [CC2,1,0]***) + ***OV Recovery***. If the bq33100 is configured for Pack Mode then the recover occurs when *Voltage* is equal to or lower than (*ChargingVoltage* + ***OV Recovery***.

On recovery the *[OV]* flag is reset, and *ChargingCurrent* and *ChargingVoltage* are set back to appropriate values per the charging algorithm.

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NOTE

When *ChargingVoltage* has been set to 0 due to a detected condition then the capacitor overvoltage function is suspended.

8.3.5.2 Capacitor Voltage Imbalance (CIM)

The bq33100 starts capacitor voltage imbalance detection when *Current* is less than or equal to ***CIM Current*** AND ALL *CapacitorVoltage5..1* > ***Min CIM Check Voltage***.

When the difference between highest capacitor voltage and lowest capacitor voltage exceeds ***CIM Fail Voltage*** the *[CIM]* flag in *SafetyAlert* is set.

When the difference between highest capacitor voltage and lowest capacitor voltage exceeds ***CIM Fail Voltage*** for a period greater than ***CIM Time*** the *[CIM]* flag in *SafetyStatus* is set and *ChargingCurrent* and *ChargingVoltage* are set to 0 and the CHG FET is turned off. *SafetyStatus() [CIM]* is cleared and CHG FET is allowed to turn ON when the differences between the highest capacitor voltage and lowest capacitor voltage is less than ***CIM Recovery***.

This function is disabled if ***CIM Time*** is set to zero.

The capacitor voltage imbalance detection is cleared when the difference between highest capacitor voltage and lowest capacitor voltage is less than ***CIM Fail Voltage***. When this is detected then the CHG FET is allowed to be turned on, if other safety and configuration states permit, *ChargingCurrent* and *ChargingVoltage* are set to the appropriate value per the charging algorithm, and the *[CIM]* flag in *SafetyStatus* is reset.

8.3.5.3 Weak Capacitor (CLBAD)

When the capacitor array has been fully charged (indicated by *OperationStatus [FC]* being set) then it is monitored for excessive leakage.

When *Current* exceeds ***CLBAD Current*** the *[CLBAD]* flag in *SafetyAlert* is set.

When *Current* exceeds ***CLBAD*** for a period greater than ***CLBAD Time*** the *[CLBAD]* flag in *SafetyStatus* is set.

This function is disabled if ***CLBAD Time*** is set to zero.

In a weak capacitor condition charging is disabled and the CHG FET is turned off, *ChargingCurrent* and *ChargingVoltage* are set to zero.

The weak capacitor fault is cleared when *Current* falls equal to or below the ***CLBAD Recovery*** limit. When the recovery condition is detected, then the CHG FET is allowed to be turned on, if other safety and configuration states permit, *ChargingCurrent* and *ChargingVoltage* are set to the appropriate value per the charging algorithm, and the *[CLBAD]* flag in *SafetyStatus* is reset.

8.3.5.4 Overtemperature (OT)

The bq33100 has overtemperature protection to prevent charging at excessive temperatures.

When *Temperature* exceeds ***OT Chg*** the *[OT]* flag in *SafetyAlert* is set.

When *Temperature* exceeds ***OT Chg*** for a period greater than ***OT Chg Time*** the *[OT]* flag in *SafetyStatus* is set.

This function is disabled if ***OT Chg Time*** is set to zero.

In an overtemperature condition charging is disabled and the CHG FET is turned off, *ChargingCurrent* and *ChargingVoltage* are set to zero.

The overtemperature fault is cleared when *Temperature* falls equal to or below the ***OT Chg Recovery*** limit. When the recovery condition is detected, then the CHG FET is allowed to be turned on, if other safety and configuration states permit, *ChargingCurrent* and *ChargingVoltage* are set to the appropriate value per the charging algorithm, and the *[OT]* flag in *SafetyStatus* is reset.

8.3.5.5 Overcurrent During Charging (OC Chg)

The bq33100 has an independent level of recoverable overcurrent protection during charging.

When *Current* exceeds ***OC Chg*** the *[OCC]* flag in *SafetyAlert* is set.

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When *Current* exceeds ***OC Chg*** for a period greater than ***OC Chg Time*** the *[OCC]* flag in *SafetyStatus* is set and *ChargingCurrent* and *ChargingVoltage* are set to 0.

This function is disabled if ***OC Chg Time*** is set to zero.

The overcurrent fault is cleared when *Current* falls below ***OC Chg Recovery***. When a charging-fault recovery condition is detected, then the CHG FET is allowed to be turned on, if other safety and configuration states permit, *ChargingCurrent* and *ChargingVoltage* are set to the appropriate value per the charging algorithm, and the *[OCC]* flag in *SafetyStatus* is reset.

8.3.5.6 Overcurrent During Discharging (OC Dsg)

The bq33100 overcurrent is discharge detection executed by the integrated AFE is configured by the bq33100 data flash ***OC Dsg*** and ***OC Dsg Time*** registers.

When the integrated AFE detects a overcurrent in discharge condition the charge FET is turned off and the *[OCD]* flag in *SafetyStatus* is set, the internal current recovery timer is reset and *ChargingCurrent* and *ChargingVoltage* are set to 0.

The recovery is controlled by the bq33100 and requires that *Current* be ≤ ***OC Dsg Recovery*** threshold and that the internal AFE current recovery timer ≥ ***Current Recovery Time***.

When the recovery condition is detected, *ChargingCurrent* and *ChargingVoltage* are set to the appropriate value per the charging algorithm, and the *[OCD]* flag in*SafetyStatus* is reset.

8.3.5.7 Short-Circuit During Charging (SC Chg)

The bq33100 short-circuit during charging protection is executed by the integrated AFE is configured by the bq33100 data flash ***SC Chg Cfg*** register.

When the integrated AFE detects a short circuit fault the charge FET is turned off and the *[SCC]* flag in *SafetyStatus* is set, the internal current recovery timer is reset and *ChargingCurrent* and *ChargingVoltage* are set to 0.

The recovery is controlled by the bq33100 and requires that *AverageCurrent* be ≤ ***SC Recovery*** threshold and that the internal AFE current recovery timer ≥ ***Current Recovery Time***.

When the recovery condition is detected, *ChargingCurrent* and *ChargingVoltage* are set to the appropriate value per the charging algorithm, and the *[SCC]* flag in*SafetyStatus* is reset.

8.3.5.8 Short-Circuit During Discharging (SC Dsg)

The bq33100 short-circuit during discharging detection is executed by the integrated AFE is configured by the bq33100 data flash ***SC Dsg Cfg*** register.

When the integrated AFE detects a short circuit fault the charge FET is turned off and the *[SCD]* flag in *SafetyStatus* is set, the internal current recovery timer is reset and *ChargingCurrent* and *ChargingVoltage* are set to 0.

The recovery is controlled by the bq33100 and requires that *Current* be ≤ ***SC Recovery*** threshold and that the internal AFE current recovery timer ≥ ***Current Recovery Time***.

When the recovery condition is detected, *ChargingCurrent* and *ChargingVoltage* are set to the appropriate value per the charging algorithm, and the *[SCD]* flag in*SafetyStatus* is reset.

8.3.5.9 AFE Watchdog (WDF)

The integrated AFE automatically turns off the CHG FET and sets the *[WDF]* flag in *SafetyStatus* if the integrated AFE does not receive the appropriate frequency on the internal watchdog input (WDI) signal.

8.3.5.10 Integrated AFE Communication Fault (AFE_C)

After a full reset the bq33100 and the AFE offset and gain values are read twice and compared. The ***AFE Init Limit*** sets the maximum difference in A/D counts of two successful readings of offset and gain, which the device still considers as the same value. If the gain and offset values are still not considered the same after ***AFE Init Retry Limit*** comparison retries, the device reports a permanent failure error by setting *SafetyStatus() [AFE_C]*.

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Additionally, the bq33100 periodically validates its read and write communications with the integrated AFE. If either a read or write verify fails, an internal AFE_Fail_Counter is incremented. If the AFE_Fail_Counter reaches AFE Fail Limit, the bq33100 sets the [AFE_C] flag in SafetyStatus. An AFE communication fault condition can also be declared if, after a full reset, the initial gain and offset values read from the AFE cannot be verified. These values are A to D readings of the integrated AFE VCx signal. The integrated AFE offset values are verified by reading the values twice and confirming that the readings are within acceptable limits. The maximum number of read retries, if offset and gain value verification fails and [AFE_C] fault is declared, is set in AFE Fail Limit If the AFE Fail Limit is set to 0, this feature is disabled.

8.3.5.11 Data Flash Fault (DFF)

The bq33100 can detect if the data flash is not operating correctly. A permanent failure is reported when either: (i) After a full reset the instruction flash checksum does not verify; (ii) if any data flash write does not verify; or (iii) if any data flash erase does not verify

When a data flash fault is detected then the *[DFF]* flag in *SafetyStatus* is set.

8.3.5.12 FAULT Indication (FAULT Pin)

The bq33100 provides the status of the safety detection through *SafetyStatus*. To provide an extra indication of a fault state (*SafetyStatus* ≠ 0x00) the bq33100 will set the FAULT pin (pin 15) if the corresponding *SafetyStatus* bit is set in ***Fault***.

8.3.6 Communications

The bq33100 uses SMBus v1.1 for host communications although an SMBus slave can be communicated with through an I^2C master.

8.3.6.1 SMBus On and Off State

The bq33100 detects a SMBus off state when SCL and SDA are logic-low for ≥ 2 seconds. Clearing this state requires either SCL or SDA to transition high. Within 1 ms, the communication bus is available.

8.3.7 Security (Enables and Disables Features)

There are two levels of secured operation within the bq33100, Sealed and Unsealed. To switch between the levels, different operations are needed with different codes.

1.Unsealed to Sealed — The use of the *Seal* command instructs the bq33100 to limit access to the SBS functions and data flash space and sets the *[SS]* flag. In sealed mode, available standard SBS functions have access per the Smart Battery Data Specification (SBS). Extended SBS Functions and data flash are not accessible. Once in sealed mode, the part can never permanently return to Unsealed mode.

2. Sealed to Unsealed — Instructs the bq33100 to extend access to the SBS and data flash space and clears the *[SS]* flag. In unsealed mode, all data, SBS, and DF have read and write access. Unsealing is a 2 step command performed by writing the 1st word of the *UnSealKey* to *ManufacturerAccess* followed by the second word of the *UnSealKey* to *ManufacturerAccess*. The unseal key can be read and changed through the extended SBS block command *UnSealKey* when in Unsealed Mode. To return to the Sealed mode, either a hardware reset is needed, or the *ManufacturerAccess Seal* command is needed.

8.3.8 Measurement System Calibration

The bq33100 does not require calibration, but can be calibrated for improved measurement accuracy.

8.3.8.1 Coulomb Counter Deadband

The bq33100 does not accumulate charge or discharge for monitoring when the current input is below the ***Deadband*** threshold which must be set sufficiently high to prevent false signal detection with no charge or discharge flowing through the sense resistor.

8.3.8.2 Auto Calibration

The bq33100 provides an auto-calibration feature to cancel the voltage offset error across SRP and SRN for maximum charge measurement accuracy. The bq33100 performs auto-calibration when the SMBus lines stay low continuously for a minimum of 5 s and *Temperature* is within bounds of 5°C and 45°C.

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8.3.8.3 Current Gain

Current Gain sets the mA current scale factor for the coulomb counter. Use calibration routines to set this value.

Table 6. Current Gain

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
104	Data	0	Current Gain	Floating point	4	1.0E-01	4.0E+00	0.9419	mΩ

8.3.8.4 CC Delta

CC Delta sets the mF capacitance scale factor for the coulomb counter. Use calibration routines to set this value.

Table 7. CC Delta

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
104	Data	4	CC Delta	Floating point	4	2.9826E+04	1.193046E+06	280932.825	mΩ

8.3.8.5 Cap1 K-factor

This register value stores the ADC voltage translation factor for the top capacitor (Capacitor 1), which is connected between the VC1 and VC2 pins. By default, this value is not used and the factory calibration are in effect. This value overrides the factory calibration when the K-factor Override Flag is set to 0x9669 by the software calibration process. The calibration routine sets this value, however the value can be manually modified according to Equation 5:

New StackVoltageKfactor = Existing StackVoltageKfactor × Actual Applied Voltage / Reported Voltage (5)

Table 8. Cap1 K-factor

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
104	Data	8	Cap1 K-factor	Integer	2	0	32767	20500	

8.3.8.6 Cap2 K-factor

This register value stores the ADC voltage translation factor for Capacitor 2, which is connected between the VC2 and VC3 pins. By default, this value is not used and the factory calibration are in effect. This value overrides the factory calibration when the K-factor Override Flag is set to 0x9669 by the software calibration process. The calibration routine sets this value, however the value can be manually modified according to Equation 6:

New StackVoltageKfactor = Existing StackVoltageKfactor × Actual Applied Voltage / Reported Voltage (6)

Table 9. Cap2 K-factor

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
104	Data	10	Cap2 K-factor	Integer	2	0	32767	20500	

8.3.8.7 Cap3 K-factor

This register value stores the ADC voltage translation factor for Capacitor 3, which is connected between the VC3 and VC4 pins. By default, this value is not used and the factory calibration are in effect. This value overrides the factory calibration when the K-factor Override Flag is set to 0x9669 by the software calibration process. The calibration routine sets this value, however the value can be manually modified according to Equation 7:

New StackVoltageKfactor = Existing StackVoltageKfactor × Actual Applied Voltage / Reported Voltage (7)

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Table 10. Cap3 K-factor

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
104	Data	12	Cap3 K-factor	Integer	2	0	32767	20500	

8.3.8.8 Cap4 K-factor

This register value stores the ADC voltage translation factor for Capacitor 4, which is connected between the VC4 and VC5 pins. By default, this value is not used and the factory calibration are in effect. This value overrides the factory calibration when the K-factor Override Flag is set to 0x9669 by the software calibration process. The calibration routine sets this value, however the value can be manually modified according to Equation 8:

New StackVoltageKfactor = Existing StackVoltageKfactor × Actual Applied Voltage / Reported Voltage (8)

Table 11. Cap4 K-factor

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
104	Data	14	Cap4 K-factor	Integer	2	0	32767	20500	

8.3.8.9 Cap5 K-factor

This register value stores the ADC voltage translation factor for the bottom capacitor (Capacitor 5), which is connected between the VC5 and VSS pins. The calibration routine sets this value, however the value can be manually modified according to Equation 9:

New StackVoltageKfactor = Existing StackVoltageKfactor × Actual Applied Voltage / Reported Voltage (9)

Table 12. Cap5 K-factor

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
104	Data	16	Cap5 K-factor	Integer	2	0	32767	20500	

8.3.8.10 K-factor Override Flag

This register value is by default 0, indicating that the factory calibrated K-factors are being used. If this register is set to 0x9669, Cap1 to approximately Cap5 K-factors in the data flash are used for voltage translation.

Table 13. K-factor Override Flag

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
104	Data	18	K-factor Override Flag	Hex	2	0x0	0xffff	0x0	

8.3.8.11 System Voltage K-factor

This register value stores the scale factor for the PackVoltage, voltage measured at the VCCPACK pin of the bq33100. The calibration routine sets this value, however the value can be manually modified according to Equation 10:

New StackVoltageKfactor = Existing StackVoltageKfactor × Actual Applied Voltage / Reported Voltage (10)

Table 14. System Voltage K-factor

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
104	Data	20	System Voltage K-factor	Integer	2	0	32767	24500	

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8.3.8.12 Stack Voltage K-factor

This register value stores the scale factor for the Stack Voltage, voltage measured at the VCC pin of the bq33100. The calibration routine sets this value, however the value can be manually modified according to Equation 11:

New StackVoltageKfactor = Existing StackVoltageKfactor × Actual Applied Voltage / Reported Voltage (11)

Table 15. Stack Voltage K-factor

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
104	Data	22	Stack Voltage K-factor	Integer	2	0	32767	24500	

8.3.8.13 K-factor Stack Override Flag

This register value is by default 0, indicating that the factory calibrated stack K-factor is being used. If this register is set to 0x9669, Stack Voltage K-factor in the data flash are used for stack voltage translation.

Table 16. K-factor Stack Override Flag

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
104	Data	24	K-factor stack Override Flag	Hex	2	0x0	0xffff	0x0	

8.3.8.14 CC Offset

This register value stores the coulomb counter offset compensation. It is set during CC Offset calibration, or by automatic calibration of the bq33100 before the gauge enters shutdown. TI does not recommend to manually change this value.

Table 17. CC Offset

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
104	Data	20	CC Offset	Integer	2	–32768	32767	–7744	(mV)

8.3.8.15 Board Offset

This register value stores the compensation for the PCB dependant coulomb counter offset. TI recommends to use characterization data of the actual PCB to set this value.

Table 18. Board Offset

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
104	Data	22	Board Offset	Integer	2	–32767	32767	0	uV

8.3.8.16 Int Temp Offset

This register value stores the internal temperature sensor offset compensation. Use calibration routines to set this value

Table 19. Int Temp Offset

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
104	Data	24	Int Temp Offset	Integer	1	–128	127	0	0.1ºC

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8.3.8.17 Ext1 Temp Offset

This register value stores the temperature sensor offset compensation for the external temperature sensor 1 connected at the TS pin of the bq33100. Use calibration routines to set this value

Table 20. Ext1 Temp Offset

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
104	Data	25	Ext1 Temp Offset	Integer	1	–128	127	0	0.1ºC

8.3.8.18 CC Current

This value sets the current used for the CC calibration when in calibration mode.

Table 21. CC Current

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
105	Config	0	CC Current	Integer	2	0	32767	3000	mA

8.3.8.19 Voltage Signal

This value sets the voltage used for calibration when in calibration mode.

Table 22. Voltage Signal

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
105	Config	2	Voltage Signal	Integer	2	0	32767	12600	mV

8.3.8.20 Temp Signal

This value sets the temperature used for the temperature calibration in calibration mode.

Table 23. Temp Signal

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
105	Config	4	Temp Signal	Integer	2	0	32767	298	0.1ºK

8.3.8.21 CC Offset Time

This value sets the time used for the CC Offset calibration in calibration mode. More time means more accuracy. The legitimate values for this constant are integer multiples of 250. Numbers less than 250 will cause a CC Offset calibration error. Numbers greater than 250 will be rounded down to the nearest multiple of 250.

Table 24. CC Offset Time

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
105	Config	6	CC Offset Time	Unsigned Integer	2	0	65535	250	s (ms)

8.3.8.22 ADC Offset Time

This constant defines the time for the ADC Offset calibration in calibration mode. More time means more accuracy. The legitimate values for this constant are integer multiples of 32. Numbers less than 32 will cause an ADC offset calibration error. Numbers greater than 32 will be rounded down to the nearest multiple of 32.

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Table 25. ADC Offset Time

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
105	Config	8	ADC Offset Time	Unsigned Integer	2	0	65535	32	ms

8.3.8.23 Current Gain Time

This constant defines the time for the Current Gain calibration in calibration mode. More time means more accuracy. The legitimate values for this constant are integer multiples of 250. Numbers less than 250 will cause a Current gain calibration error. Numbers greater than 250 will be rounded down to the nearest multiple of 250.

Table 26. Current Gain Time

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
105	Config	10	Current Gain Time	Unsigned Integer	2	0	65535	250	ms

8.3.8.24 Voltage Time

This constant defines the time for the voltage calibration in calibration mode. More time means more accuracy. The legitimate values for this constant are integer multiples of 1984. Numbers less than 1984 will cause a voltage calibration error. Numbers greater than 1984 will be rounded down to the nearest multiple of 1984.

Table 27. Voltage Time

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
105	Config	12	Voltage Time	Unsigned Integer	2	0	65535	1888	ms

8.3.8.25 Temperature Time

This constant defines the time for the temperature calibration in calibration mode. More time means more accuracy. The legitimate values for this constant are integer multiples of 32. Numbers less than 32 will cause a temperature calibration error. Numbers greater than 32 will be rounded down to the nearest multiple of 32.

Table 28. Temperature Time

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
105	Config	14	Temperature Time	Unsigned Integer	2	0	65535	32	ms

8.3.8.26 Cal Mode Timeout

The bq33100 will exit calibration mode automatically after a ***Cal Mode Timeout*** period.

Table 29. Cal Mode Timeout

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
105	Config	17	Cal Mode Timeout	Unsigned Integer	2	0	65535	38400	1/128 s (s)

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8.3.8.27 Ext Coef a1..a5, b1..b4, Ext rc0, Ext adc0

These values characterize the external thermistor connected to the TS pin of the bq33100. The default values characterize the Semitec 103AT NTC thermistor. Do not modify these values without consulting TI.

Table 30. Ext Coef a1..a5, b1..b4, Ext rc0, Ext adc0

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
106	Temp Model	0	Ext Coef a1	Integer	2	–32768	32767	–11130	num
		2	Ext Coef a2					19142	
		4	Ext Coef a3					–19262	
		6	Ext Coef a4					28203	
		8	Ext Coef a5					892	
		10	Ext Coef b1					328	
		12	Ext Coef b2					–605	
		14	Ext Coef b3					–2443	
		16	Ext Coef b4					4696	
		18	Ext rc0					11703	
		20	Ext adc0					11338	

8.3.8.28 Rpad

This value characterize the pad resistance of the bq33100. Do not modify without consulting TI.

Table 31. Rpad

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
106	Temp Model	22	Rpad	Integer	2	–32768	32767	87	Ω

8.3.8.29 Rint

This value characterize the internal resistance of the bq3100. Do not modify without consulting TI.

Table 32. Rint

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
106	Temp Model	24	Rint	Integer	2	–32768	32767	17740	Ω

8.3.8.30 Int Coef 1..4, Int Min AD, Int Max Temp

These values characterize the internal thermistor of the bq33100. Do not modify these values without consulting TI.

Table 33. Int Coef 1..4, Int Min AD, Int Max Temp

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
106	Temp Model	26	Int Coef 1	Integer	2	–32768	32767	0	s
		28	Int Coef 2					0	
		30	Int Coef 3					–12263	
		32	Int Coef 4					6106	
		34	Int Min AD					0	
		36	Int Max Temp					6106	0.1°K

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8.3.8.31 Filter

Filter defines the filter constant used in the AverageCurrent calculation, Equation 12:

AverageCurrent new = a x *AverageCurrent* old + (1 – a) x Current

where

- a = <***Filter***> / 256; the time constant = 1 sec/ln(1/a) (default 14.5 sec) (12)

Table 34. Filter

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
107	Current	0	Filter	Unsigned Integer	1	0	255	239	

8.3.8.32 Deadband

Any current within ±***DeadBand*** will be reported as 0 mA by the *Current* function

Table 35. Deadband

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
107	Current	1	Deadband	Unsigned Integer	1	0	255	0	mA

8.3.8.33 CC Deadband

This constant defines the Deadband voltage for the measured voltage between the SR1 and SR2 pins used for capacitance accumulation in units of 294 nV. Any voltages within ±***CC Deadband*** do not contribute to capacitance accumulation.

Table 36. CC Deadband

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
107	Current	2	Deadband	Unsigned Integer	1	0	255	10	294 nV

8.4 Device Functional Modes

The bq33100 supports 2 different power modes:

- In Normal Mode, the bq33100 performs measurements, calculations, protection decisions and data updates in 1 second intervals. Between these intervals, the bq33100 is in a reduced power mode.
- In Shutdown mode the bq33100 is powered down with only a voltage based wake function operating

8.4.1 Operating Power Modes

The bq33100 has two operating power modes, Normal and Shutdown Mode.

Normal Mode — During normal operation, the bq33100 takes *Current*, *Voltage* and *Temperature* measurements, performs calculations, updates SBS data, and makes protection and status decisions at one-second intervals. Between these periods of activity, the bq33100 is in a reduced power state.

Shutdown — The bq33100 enters Shutdown mode if the following conditions are met:

- V_{VCC} ≤ Minimum Operating voltage
- *ManufacturerAccess*: *Shutdown* command received AND *Current* = 0 AND *Voltage* < ***Shutdown Voltage*** threshold.

Upon initial power up or a reset of the bq33100, application of a voltage > $V_{STARTUP}$ must be applied to the VCCPACK pin. The bq33100 will then power up and enter Normal Mode.

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8.5 Programming

8.5.1 Communications

The bq33100 uses SMBus v1.1 with optional packet error checking (PEC) per the SMBus specification.

8.5.1.1 bq33100 Slave Address

The bq33100 uses the address 0x16 on SMBus for communication.

8.5.1.2 SMBus On and Off State

The bq33100 detects an SMBus off state when SCL and SDA are logic-low for ≥ 2 seconds. Clearing this state requires either SCL or SDA to transition high. Within 1 ms, the communication bus is available.

8.5.1.3 Packet Error Checking

The bq33100 can receive data with or without PEC.

In the write-word protocol, the bq33100 receives the PEC after the last byte of data from the host. If the host does not support PEC, the last byte of data is followed by a stop condition. After receipt of the PEC, the bq33100 compares the value to its calculation. If the PEC is correct, the bq33100 responds with an ACKNOWLEDGE. If it is not correct, the bq33100 responds with a NOT ACKNOWLEDGE.

8.5.2 SBS Commands

All SBS Values are updated in 1-second intervals. The extended SBS commands are only available when the bq33100 device is in unsealed mode.

8.5.2.1 SBS Command Summary

Table 37. SBS Commands

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x00	R/W	ManufacturerAccess	hex	2	0x0000	0xffff	—	
0x08	R	Temperature	unsigned int	2	0	65535	—	0.1ºK
0x09	R	Voltage	unsigned int	2	0	65535	—	mV
0x0a	R	Current	signed int	2	–32768	32767	—	mA
0x0b	R	ESR	unsigned int	2	0	65535	—	mΩ
0x0d	R	RelativeStateOfCharge	unsigned int	1	0	100	—	%
0x0e	R	Health	unsigned int	1	0	100	—	%
0x10	R	Capacitance	unsigned int	2	0	65535	—	F
0x14	R	ChargingCurrent	unsigned int	2	0	65534	—	mA
0x15	R	ChargingVoltage	unsigned int	2	0	65534	—	mV
0x3b	R	CapacitorVoltage5	unsigned int	2	0	65534	—	mV
0x3c	R	CapacitorVoltage4	unsigned int	2	0	65535	—	mV
0x3d	R	CapacitorVoltage3	unsigned int	2	0	65535	—	mV
0x3e	R	CapacitorVoltage2	unsigned int	2	0	65535	—	mV
0x3f	R	CapacitorVoltage1	unsigned int	2	0	65535	—	mV

Table 38. Extended SBS Commands

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x46	R/W	FETControl	Hex	2	0x0000	0xffff	—	
0x50	R	SafetyAlert	Hex	2	0x0000	0xffff	—	
0x51	R	SafetyStatus	Hex	2	0x0000	0xffff	—	
0x54	R	OperationStatus	Hex	2	0x0000	0xf7f7	—	

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Table 38. Extended SBS Commands (continued)

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x5a	R	SystemVoltage	unsigned int	2	0	65535	—	mV
0x60	R/W	UnSealKey	Hex	4	0x00000000	0xffffffff	—	
0x70	R/W	ManufurerInfo	String	31+1	—	—	—	

8.5.2.2 SBS Command Details

The following provides detailed descriptions of the SBS Commands

8.5.2.2.1 ManufacturerAccess (0x00)

This read- or write-word function provides Super Capacitor data to system along with access to bq33100 controls and security features.

Table 39. ManufacturerAccess

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x00	R/W	ManufacturerAccess	hex	2	0x0000	0xffff	—	

Table 40. MAC Command Summary Table

SBS CMD	MODE	NAME	DESCRIPTION
0x0001	R	Device Type	Returns the IC part number.
0x0002	R	Firmware Version	Returns the firmware version.
0x0003	R	Hardware Version	Returns the hardware version
0x0004	R	DF Checksum	Generates a checksum of the full Data Flash (DF) array
0x0020	W	Seal	Enters Sealed mode with limited access to the extended SBS functions and data flash space
0x0021	R/W	Lifetime and Capacitor Balancing Enable	0 = Disables logging of lifetime data to non-volatile memory and disables capacitor balancing 1 = Enables logging of lifetime data to non-volatile memory and enables capacitor balancing
0x0022	R	IF Checksum	Returns the value of the Instruction Flash (IF) checksum
0x0023	W	Learn	This write function instructs the bq33100 to enter a capacitance learning cycle(Capacitance Update).
0x0024	W	Learn Value Reset	This write function instructs the bq33100 to reset the capacitance learned values (Capacitance) to initial default values.
0x0025	W	Learn Initialization	This write function instructs the bq33100 to enter a capacitance learning cycle(Capacitance Update) and update Initial values for Capacitance and ESR
0x0030	W	FAULT Activation	Drives the FAULT pin high
0x0031	W	FAULT Clear	Sets FAULT pin low
0x0032	W	Charge Level Nominal	Drives the CHGLVL0,1 pins low
0x0033	W	Charge Level A	Drives the CHGLVL0,1 pins high, low
0x0034	W	Charge Level B	Drives the CHGLVL0,1 pins low, high
0x0035	W	Charge Level Max	Drives the CHGLVL0,1 pins high
0x0036	R	Read AD Current	Read A-to-D Converter Current Measurement
0x0037	W	Learn Load Activation	Drives the LLEN pin high (does not activate actual learning algorithm, see 0x0023)
0x0038	W	Learn Load Clear	Sets the LLEN pin low
0x0040	W	Calibration Mode	Places bq33100 into calibration mode
0x0041	W	Reset	bq33100 undergoes complete reset
Unseal Key	W	Unseal Device	Enables access to SBS and DF space

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Table 40. MAC Command Summary Table (continued)

SBS CMD	MODE	NAME	DESCRIPTION
Extended SBS	R/W	*Extended SBS Commands*	Access to Extended SBS commands

8.5.2.2.1.1 Device Type (0x0001)

Returns the IC part number.

Table 41. Device Type

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x0001	R	Device Type	Hex	2	—	—	—	

8.5.2.2.1.2 Firmware Version (0x0002)

Returns the firmware version. The format is most-significant byte (MSB) = Decimal integer, and the least-significant byte (LSB) = sub-decimal integer, for example: 0x0120 = version 01.20.

Table 42. Firmware Version

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x0002	R	Firmware Version	Hex	2	—	—	—	

8.5.2.2.1.3 Hardware Version (0x0003)

Returns the hardware version stored in a single byte of reserved data flash, for example: 0x00a7 = Version A7.

Table 43. Hardware Version

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x00	R	Hardware Version	Hex	2	—	—	—	

8.5.2.2.1.4 DF Checksum (0x0004)

This function is only available when the bq33100 is in unsealed mode, indicated by the [*SS*] *OperationStatus* flag. A write to this command forces the bq33100 to generate a checksum of the full Data Flash (DF) array. The generated checksum is then returned within 45 ms.

NOTE

If another SMBus command is received while the checksum is being generated, the DF Checksum is generated but the response may time out.

Table 44. DF Checksum

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x0004	R	DF Checksum	Hex	2	—	—	—	

8.5.2.2.1.5 Seal Device (0x0020)

Instructs the bq33100 to limit access to the extended SBS functions and data flash space, sets the [SS] flag. This command is only available when the bq33100 is in Unsealed mode. See *Security (Enables and Disables Features)* for detailed information.

8.5.2.2.1.6 Lifetime and Capacitor Balancing Enable (0x0021)

Enables and Disables the logging of Lifetime data to non-volatile memory and Capacitor balancing

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8.5.2.2.1.7 FAULT Activation (0x0030)

This command drives the FAULT pin high. This command is only available when the bq33100 is in Unsealed mode.

8.5.2.2.1.8 FAULT Clear (0x0031)

This command sets the FAULT pin back to low. This command is only available when the bq33100 is in Unsealed mode.

8.5.2.2.1.9 CHGLVL0 Activation (0x0032)

This command drives the CHGLVL0 pin high. This command is only available when the bq33100 is in Unsealed mode.

8.5.2.2.1.10 CHGLVL0 Clear (0x0033)

This command sets the CHGLVL0 pin back to low. This command is only available when the bq33100 is in Unsealed mode.

8.5.2.2.1.11 CHGLVL1 Activation (0x0033)

This command drives the CHGLVL0 pin high. This command is only available when the bq33100 is in Unsealed mode.

8.5.2.2.1.12 CHGLVL1 Clear (0x0034)

This command sets the CHGLVL0 pin back to low. This command is only available when the bq33100 is in Unsealed mode.

8.5.2.2.1.13 Learn Load Activation (0x0037)

This command drives the LLEN pin high. This command is only available when the bq33100 is in Unsealed mode.

8.5.2.2.1.14 Learn Load Clear (0x0038)

This command sets the LLEN pin back to low. This command is only available when the bq33100 is in Unsealed mode.

8.5.2.2.1.15 Calibration Mode (0x0040)

Places the bq33100 into calibration mode. This command is only available when the bq33100 is in Unsealed mode

8.5.2.2.1.16 Reset (0x0041)

The bq33100 undergoes a full reset. The bq33100 holds the clock line down for a few milliseconds to complete the reset. If *ChargingVoltage* < *Voltage* after a reset, then the pack is discharged using the capacitor voltage balancing circuitry. This command is only available when the bq33100 is in Unsealed mode.

8.5.2.2.1.17 Unseal Device (UnsealKey)

Instructs the bq33100 to enable access to the SBS functions and data flash space and clear the [SS] flag. This 2 step command needs to be written to *ManufacturerAccess* in the following order: 1st word of the UnSealKey followed by the 2nd word of the UnSealKey. If the command fails 4 seconds must pass before the command can be reissued. This command is only available when the bq33100 is in Sealed mode. See *Security (Enables and Disables Features)* for detailed information.

8.5.2.2.1.18 Extended SBS Commands

Also available through *ManufacturerAccess* in unsealed mode are some of the extended SBS commands. The result of these commands need to be read from *ManufacturerAccess* after a write to *ManufacturerAccess*.

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8.5.2.2.2 Temperature (0x08)

This read-word function returns an unsigned integer value of the temperature in units of 0.1°K, as measured by the bq33100. It has a range of 0 to 6553.5°K. The source of the measured temperature is configured by the ***[TEMP1]*** and ***[TEMP0]*** bits in the ***Operation Cfg*** register.

Table 45. Temperature

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x08	R	Temperature	Unsigned Integer	2	0	65535	—	0.1°K

8.5.2.2.3 Voltage (0x09)

This read-word function returns an unsigned integer value of the capacitor stack array (voltage at the VC1 input) in mV with a range of 0 to 20000 mV

Table 46. Voltage

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x09	R	Voltage	Unsigned Integer	2	0	20000	—	mV

8.5.2.2.4 Current (0x0a)

This read-word function returns a signed integer value of the measured current being supplied (or accepted) by the super capacitor pack in mA, with a range of –32768 to 32767. A positive value indicates charge current and a negative value indicates discharge.

Any current value within the ***Deadband*** will be reported as 0 mA by the *Current* function.

Table 47. Current

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x0a	R	Current	Unsigned Integer	2	–32768	32767	—	mA

8.5.2.2.5 ESR (0x0b)

This read-word function returns an unsigned integer value of the Super Capacitor array total ESR in mΩ with a range of 0 to 65535 mΩ

Table 48. ESR

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x0b	R	ESR	Unsigned Integer	2	0	65535	—	mΩ

8.5.2.2.6 RelativeStateofCharge (0x0d)

This read-word function returns an unsigned integer value of the predicted remaining super capacitor capacitance expressed as a percentage of *Capacitance* with a range of 0 to 100%, with fractions of % rounded up.

If the ***[RSOCL]*** bit in ***Operation Cfg*** is set then *RelativeStateofCharge* is held at 99% until primary charge termination occurs and only displays 100% upon entering primary charge termination.

If the ***[RSOCL]*** bit in***Operation Cfg*** is cleared then *RelativeStateofCharge* is not held at 99% until primary charge termination occurs. Fractions of % greater than 99% are rounded up to display 100%.

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Table 49. RelativeStateofCharge

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x0d	R	RelativeStateofCharge	Unsigned Integer	1	0	100	—	%

8.5.2.2.7 Health (0x0e)

This read-word function returns an unsigned integer value of the predicted health of the super capacitor pack expressed as a percentage of *Capacitance* / ***InitialCapacitance*** with a range of 0 to 100%, with fractions of % rounded up.

Table 50. Health

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x0e	R	Health	Unsigned Integer	1	0	100	—	%

8.5.2.2.8 Capacitance (0x10)

This read- or write-word function returns an unsigned integer value, with a range of 0 to 65535, of the predicted full charge capacitance in the super capacitor pack. This value is expressed in F.

Table 51. Capacitance

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x10	R/W	Capacitance	Unsigned Integer	2	0	65534	—	F

8.5.2.2.9 ChargingCurrent (0x14)

This read-word function returns an unsigned integer value of the desired charging current, in mA, with a range of 0 to 65534.

Table 52. ChargingCurrent

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x14	R	ChargingCurrent	Unsigned Integer	2	0	65534	—	mA

8.5.2.2.10 ChargingVoltage (0x15)

This read-word function returns an unsigned integer value of the desired charging voltage, in mV, where the range is 0 to 65534.

Table 53. ChargingVoltage

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x15	R	ChargingVoltage	Unsigned Integer	2	0	65534	—	mV

8.5.2.2.11 CapacitorVoltage5..1 (0x3b..0x3f)

These read-word functions return an unsigned value of the calculated individual capacitor voltages, in mV, with a range of 0 to 65535. *CapacitorVoltage1* corresponds to the bottom most series capacitor element, while *CapacitorVoltage5* corresponds to the top most series capacitor element.

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Table 54. CapacitorVoltage5..1

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x3b	R	CapacitorVoltage 5	Unsigned Integer	2	0	65535	—	mV
0x3c		CapacitorVoltage 4						
0x3d		CapacitorVoltage 3						
0x3e		CapacitorVoltage 2						
0x3f		CapacitorVoltage 1						

8.5.2.2.12 Extended SBS Commands

Also available through *ManufacturerAccess* in sealed mode are some of the extended SBS commands. The commands available are listed below. The result of these commands need to be read from *ManufacturerAccess* after a write to *ManufacturerAccess.*

8.5.2.2.12.1 FETControl(0x46)

This write- and read-word function allows direct control of the CHG FET for test purposes. The bq33100 overrides this command unless in normal mode.

Table 55. FETControl

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x46	R	FETControl	hex	2	0x0000	0xffff	—	

Figure 6. FETControl Registers

15	14	13	12	11	10	9	8
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	RSVD	CHG	RSVD	RSVD

LEGEND: All Values Read-Only

CHG — Charge (CHG) FET Control

0 = CHG FET is turned OFF.

1 = CHG FET is turned ON.

8.5.2.2.12.2 SafetyAlert (0x50)

This read-word function returns indications of pending safety issues, such as running safety timers, or fail counters that are nonzero but have not reached the required time or value to trigger a *SafetyStatus* failure. These flags do not cause the FAULT pin to be set.

Table 56. SafetyAlert

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x50	R	SafetyAlert	hex	2	0x0000	0xffff	—	

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Figure 7. SafetyAlert Registers

15	14	13	12	11	10	9	8
CLBAD	RSVD	RSVD	RSVD	RSVD	OTC	CIM	OV
7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	OCC	OCD	SCC	SCD

LEGEND: All Values Read-Only

CLBAD 1 = Excessive capacitor leakage alert

OTC 1 = Charge overtemperature alert

CIM 1 = Capacitor voltage Imbalance permanent failure alert

OV 1 = Capacitor overvoltage alert

OCC 1= Overcurrent during charge alert

OCD 1= AFE overcurrent during discharge alert

SCC 1= AFE short circuit during charge alert

SCD 1= AFE short circuit during discharge alert

8.5.2.2.12.3 SafetyStatus (0x51)

This read-word function returns the status of the safety features. These flags do not cause the FAULT pin to be set unless the corresponding bit in ***FAULT*** is set.

Table 57. SafetyStatus

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x51	R	SafetyStatus	hex	2	0x0000	0xffff	—	

Figure 8. SafetyStatus Registers

15	14	13	12	11	10	9	8
CLBAD	HFAIL	HWARN	HLOW	RSVD	OT	CIM	OV
7	6	5	4	3	2	1	0
DFF	RSVD	AFE_C	WDF	OCC	OCD	SCC	SCD

LEGEND: All Values Read-Only

CLBAD 1 = Excessive capacitor leakage fault

HWARN 1 = Health low warning

HLOW 1 = Health low indication

HFAIL 1 = Health failure

OT 1 = Charge overtemperature fault

CIM 1 = Capacitor voltage Imbalance fault

OV 1 = Capacitor overvoltage fault

DFF 1 = Data Flash Fault permanent failure fault

AFE_C 1 = Permanent AFE Communications failure fault

WDF 1 = AFE Watchdog fault

OCC 1= Overcurrent during charge fault

OCD 1= AFE overcurrent during discharge fault

SCC 1= AFE short circuit during charge fault

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SCD 1= AFE short circuit during discharge fault

8.5.2.2.12.4 OperationStatus (0x54)

This read-word function returns the current operation status.

Table 58. OperationStatus

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x54	R	OperationStatus	hex	2	0x0000	0xf7f7	—	

Figure 9. OperationStatus Registers

15	14	13	12	11	10	9	8
RSVD	DSG	SS	FC	LTE	RSVD	CHGOR	CB
7	6	5	4	3	2	1	0
LDTO	LCTO	LPASS	CL	RSVD	CFET	RSVD	RSVD

DSG Discharging

0 = bq33100 is in charging mode

1 = bq33100 is in discharging mode, relaxation mode, or valid charge termination has occurred

SS 1 = Sealed security mode

FC 1 = Fully Charged

LTE 1 = Lifetime data and CHG FET operation enabled

CHGOR 1 = Charge Override Enabled

CB 1 = Capacitor voltage balancing in progress

CL 1 = Capacitance learning in progress

LPASS 1 = Learning complete and successful

LCTO 1 = Learning charging phase time out

LDTO 1 = Learning discharging phase time out

8.5.2.2.12.5 SystemVoltage (0x5a)

This read-word function returns an unsigned integer value of the voltage at VCC (pin 24) in mV with a range of 0 to 20000 mV.

Table 59. SystemVoltage

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x5a	R	SystemVoltage	Unsigned Integer	2	0	20000	—	mV

8.5.2.2.12.6 UnSealKey(0x60)

This read- or write-block command allows the user to change the Unseal key for the Sealed-to-Unsealed security-state transition. This function is only available when the bq33100 is in the Unsealed mode, indicated by a cleared *[SS]* flag.

The order of the bytes, when entered in *ManufacturerAccess*, is the reverse of what is written to or read from the part. For example, if the 1st and 2nd word of the UnSealKey block read returns 0x1234 and 0x5678, then in *ManufacturerAccess,* 0x3412 and 0x7856 must be entered to unseal the part.

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Table 60. UnSealKey

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x60	R/W	UnSealKey	Hex	4	0x00000000	0xffffffff	—	

8.5.2.2.12.7 ManufacturerInfo(0x70)

This read and write block function returns the data stored in Manuf. Info where byte 0 is the MSB with a maximum length of 31 data + 1 length byte. When the bq33100 is in Unsealed mode, this block is read and write. When the bq33100 is in Sealed mode, this block is read only.

Table 61. ManufacturerInfo

SBS CMD	MODE	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
0x70	R/W	ManufacturerInfo	String	31+1	—	—	—	

8.5.3 Data Flash

NOTE

Take care when mass programming the data flash space using previous versions of data flash memory map files (such as *.gg files) to make sure that all public locations are updated correctly.

Data Flash can only be updated if *Voltage* ≥ ***Flash Update OK Voltage***. Data flash reads and writes are verified according to the method detailed in the *Data Flash Fault (DFF)* section of this data sheet.

8.5.3.1 Accessing Data Flash

In different security modes, the data flash access conditions change. See *Security (Enables and Disables Features)* and *ManufacturerAccess (0x00)* sections for further details.

8.5.3.2 Data Flash Interface

The bq33100 data flash is organized into subclasses where each data flash variable is assigned an offset within its numbered subclass. For example: the OT Time location is defined as:

- Class = Safety
- SubClass = Temperature = 2
- Offset = 2

NOTE

Data Flash commands are NACKed if the bq33100 is in sealed mode (*[SS]* flag is set).

Each subclass can be addressed individually by using the *DataFlashSubClassID* (0x77) command and the data within each subclass is accessed by using the *DataFlashSubClassPage1..8* (0x78...0x7f) commands. Reading and Writing subclass data are block operations which are each 32 Bytes long. Data can be written in shorter block sizes, however. The final block in one subclass can be shorter than 32 bytes so take care not to write over the subclass boundary. None of the values written are bounded by the bq33100 and the values are not rejected by the bq33100. Writing an incorrect value may result in hardware failure due to firmware program interpretation of the invalid data. The data written is persistent, so a Power On Reset does resolve the fault.

8.5.3.3 Data Flash Summary

The following notation is used in Table 62 with regards to the Data Type column:

The **Alpha Character**

- H = Hexadecimal value
- I = Integer value

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- S = String
- U = Unsigned Integer value

The **Numeric Value** following the Alpha Character is the length of the data in bytes, for example: ***OT Time*** Data Type = U1 = Unsigned Integer of 1 byte in length

Table 62. Data Flash Values

CLASS NAME	SUBCLASS ID	SUBCLASS NAME	OFFSET	PARAMETER NAME	DATA TYPE	MIN	MAX	DEFAULT	UNITS
Safety	0	Voltage	0	OV Threshold	I2	0	1000	100	mV
Safety	0	Voltage	2	OV Recovery	I2	–500	1000	0	mV
Safety	0	Voltage	4	OV Time	U1	0	255	2	Sec
Safety	0	Voltage	5	CIM Fail Voltage	I2	0	5000	550	mVolt
Safety	0	Voltage	7	CIM Time	U1	0	240	10	Seconds
Safety	0	Voltage	8	CIM Recovery	I2	0	5000	500	mV
Safety	0	Voltage	10	Min CIM Check Voltage	U2	0	65535	1000	mV
Safety	1	Current	0	OC Chg	I2	0	5000	1000	mAmp
Safety	1	Current	2	OC Chg Time	U1	0	240	5	mAmp
Safety	1	Current	3	OC Chg Recovery	I2	–1000	5000	900	mAmp
Safety	1	Current	5	CLBAD Current	I2	0	30000	15	milliAmp
Safety	1	Current	7	CLBAD Time	U1	0	240	60	Seconds
Safety	1	Current	8	CLBAD Recovery	I2	0	1000	10	mAmp
Safety	1	Current	10	Current Recovery Time	U1	0	240	5	Seconds
Safety	1	Current	11	OC Dsg	H1	0	f	F	hex
Safety	1	Current	12	OC Dsg Time	H1	0	f	F	hex
Safety	1	Current	13	OC Dsg Recovery	I2	5	1000	5	mAmp
Safety	1	Current	15	SC Chg Cfg	H1	0	f7	f4	hex
Safety	1	Current	16	SC Dsg Cfg	H1	0	f7	f7	hex
Safety	1	Current	17	SC Recovery	I2	0	200	1	mAmp
Safety	2	Temperature	0	OT Chg	I2	0	1200	680	0.1ºC
Safety	2	Temperature	2	OT Chg Time	U1	0	240	2	Seconds
Safety	2	Temperature	3	OT Chg Recovery	I2	0	1200	630	0.1ºC
Safety	3	AFE Verification	1	AFE Fail Limit	U1	0	255	100	Counts
Safety	3	AFE Verification	3	AFE Init Retry Limit	U1	0	255	6	num
Safety	3	AFE Verification	4	AFE Init Limit	U1	0	255	20	Counts
Charge Control	34	Charge Cfg	0	Chg Voltage	I2	0	32767	8400	mV
Charge Control	34	Charge Cfg	2	Chg Current	I2	0	20000	500	mA
Charge Control	34	Charge Cfg	4	Chg Enable Delay	U2	0	65000	0	mSeconds
Charge Control	35	Full Charge Cfg	0	Taper Current	I2	0	1000	3	mAmp
Charge Control	35	Full Charge Cfg	2	Taper Voltage	I2	0	1000	100	mVolt
Charge Control	35	Full Charge Cfg	4	Current Taper Window	U1	0	240	2	Seconds

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Table 62. Data Flash Values (continued)

CLASS NAME	SUBCLASS ID	SUBCLASS NAME	OFFSET	PARAMETER NAME	DATA TYPE	MIN	MAX	DEFAULT	UNITS
Charge Control	35	Full Charge Cfg	5	FC Set %	I1	-1	100	–1	Percent
Charge Control	35	Full Charge Cfg	6	FC Clear %	I1	-1	100	98	Percent
Charge Control	36	Capacitance Balancing Cfg	0	CB Threshold	I2	0	5000	1500	mVolt
Charge Control	36	Capacitance Balancing Cfg	2	CB Min	U1	0	255	5	mVolt
Charge Control	36	Capacitance Balancing Cfg	3	CB Restart	U1	0	255	10	mVolt
System Data	48	Data	0	Design Voltage	I2	0	18000	8400	mVolt
System Data	48	Data	2	Manuf Date	U2	0	65535	0	Day + Mo × 32 + (Yr – 1980) × 256
System Data	48	Data	4	Ser. Num.	H2	0	ffff	1	hex
System Data	48	Data	6	Design Capacitance	I2	0	65535	250	F
System Data	48	Data	8	Init 1st Capacitance	I2	0	65535	250	F
System Data	48	Data	10	Capacitance	I2	0	65535	250	F
System Data	48	Data	12	Design ESR	I2	0	65535	320	mΩ
System Data	48	Data	14	Initial ESR	I2	0	65535	320	mΩ
System Data	48	Data	16	ESR	I2	0	65535	320	mΩ
System Data	48	Data	18	Manuf Name	S12	x	x	Texas Instruments	—
System Data	48	Data	30	Device Name	S8	x	x	bq33100	—
System Data	48	Data	38	Init Safety Status	H2	0	ffff	0	hex
System Data	56	Manufacturer Data	0	Pack Lot Code	H2	0	ffff	0	—
System Data	56	Manufacturer Data	2	PCB Lot Code	H2	0	ffff	0	—
System Data	56	Manufacturer Data	4	Firmware Version	H2	0	ffff	0	—
System Data	56	Manufacturer Data	6	Hardware Revision	H2	0	ffff	0	—
System Data	58	Manufacturer Info	0	Manuf. Info	S32	x	x	0123456789ABCDEF0123456789ABCDE	—
System Data	59	Lifetime Data	0	Lifetime Max Temp	I2	0	1400	0	0.1ºC
System Data	59	Lifetime Data	2	Lifetime Min Temp	I2	–600	1400	500	0.1ºC
System Data	59	Lifetime Data	4	Lifetime Max Capacitor Voltage	I2	0	32767	0	mVolt
Configuration	64	Registers	0	Operation Cfg	H2	0	FFFF	308	flags
Configuration	64	Registers	4	FET Action	H2	0	FFFF	0	flags
Configuration	64	Registers	8	Fault	H2	0	FFFF	0	flags
Configuration	65	AFE	1	AFE State_CTL	H1	0	ff	0	flags
Configuration	67	Power	0	Flash Update OK Voltage	I2	0	20000	4000	mVolt
Configuration	67	Power	2	Shutdown Voltage	I2	0	5500	4000	mVolt
Monitoring	86	System Requirement	0	Min Power	I2	0	16800	10	Watt/100
Monitoring	86	System Requirement	2	Required Time	I2	0	32767	60	Seconds

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Table 62. Data Flash Values (continued)

CLASS NAME	SUBCLASS ID	SUBCLASS NAME	OFFSET	PARAMETER NAME	DATA TYPE	MIN	MAX	DEFAULT	UNITS
Monitoring	86	System Requirement	4	Min Voltage	I2	0	10000	4000	mVolt
Monitoring	87	Charging Voltage	0	V Chg Nominal	I2	0	32767	8400	mVolt
Monitoring	87	Charging Voltage	2	V Chg A	I2	0	32767	8900	mVolt
Monitoring	87	Charging Voltage	4	V Chg B	I2	0	32767	9500	mVolt
Monitoring	87	Charging Voltage	6	V Chg Max	I2	0	32767	10000	mVolt
Monitoring	87	Charging Voltage	8	V Learn Max	I2	0	32767	10000	mVolt
Monitoring	88	Learning Configuration	0	Learning Frequency	U1	0	255	2	week
Monitoring	88	Learning Configuration	1	Measurement Margin %	U1	0	100	10	Percent
Monitoring	88	Learning Configuration	2	Max Chg Time	I2	0	32767	300	Seconds
Monitoring	88	Learning Configuration	4	Max Dsg Time	I2	0	32767	10	Seconds
Monitoring	88	Learning Configuration	6	Learn Delta Voltage	I2	0	2000	500	mVolt
Monitoring	88	Learning Configuration	8	Cap Start Time	U2	0	65535	320	msec
Monitoring	81	Current Thresholds	0	Dsg Current Threshold	I2	0	2000	10	mAmp
Monitoring	81	Current Thresholds	2	Chg Current Threshold	I2	0	2000	0	mAmp
Calibration	104	Data	0	Current Gain	F4	1.00E – 01	4.00E + 00	0.47095	Number
Calibration	104	Data	4	CC Delta	F4	2.98E + 04	1.19E + 06	140466.3	Number
Calibration	104	Data	8	Cap1 K-factor	I2	0	32767	20500	—
Calibration	104	Data	10	Cap2 K-factor	I2	0	32767	20500	—
Calibration	104	Data	12	Cap3 K-factor	I2	0	32767	20500	—
Calibration	104	Data	14	Cap4 K-factor	I2	0	32767	20500	—
Calibration	104	Data	16	Cap5 K-factor	I2	0	32767	20500	—
Calibration	104	Data	18	K-factor cap override flag	H2	0	FFFF	0	num
Calibration	104	Data	20	System Voltage K-factor	I2	0	32767	24500	—
Calibration	104	Data	22	Stack Voltage K-factor	I2	0	32767	24500	—
Calibration	104	Data	24	K-factor stack override flag	H2	0	FFFF	0	num
Calibration	104	Data	26	CC Offset	I2	–32768	32767	–7744	num
Calibration	104	Data	28	Board Offset	I2	–32767	32767	0	uV
Calibration	104	Data	30	Int Temp Offset	I1	–128	127	0	0.1ºC
Calibration	104	Data	31	Ext1 Temp Offset	I1	–128	127	0	0.1ºC
Calibration	104	Data	32	Ext2 Temp Offset	I1	–128	127	0	0.1ºC
Calibration	104	Data	33	ESR Offset	I1	–128	127	0	mΩ
Calibration	105	Config	0	CC Current	I2	0	32767	3000	mAmp
Calibration	105	Config	2	Voltage Signal	I2	0	32767	8400	mVolt
Calibration	105	Config	4	Temp Signal	I2	0	32767	2980	0.1ºK
Calibration	105	Config	6	CC Offset Time	U2	0	65535	250	Seconds

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Table 62. Data Flash Values (continued)

CLASS NAME	SUBCLASS ID	SUBCLASS NAME	OFFSET	PARAMETER NAME	DATA TYPE	MIN	MAX	DEFAULT	UNITS
Calibration	105	Config	8	ADC Offset Time	U2	0	65535	32	Seconds
Calibration	105	Config	10	CC Gain Time	U2	0	65535	250	Seconds
Calibration	105	Config	12	Voltage Time	U2	0	65535	1984	MilliSeconds
Calibration	105	Config	14	Temperature Time	U2	0	65535	32	Seconds
Calibration	105	Config	17	Cal Mode Timeout	U2	0	65535	38400	Seconds/128
Calibration	106	Temp Model	0	Ext Coef a1	I2	–32768	32767	–14812	num
Calibration	106	Temp Model	2	Ext Coef a2	I2	–32768	32767	24729	num
Calibration	106	Temp Model	4	Ext Coef a3	I2	–32768	32767	–21265	num
Calibration	106	Temp Model	6	Ext Coef a4	I2	–32768	32767	28353	num
Calibration	106	Temp Model	8	Ext Coef a5	I2	–32768	32767	759	num
Calibration	106	Temp Model	10	Ext Coef b1	I2	–32768	32767	–399	num
Calibration	106	Temp Model	12	Ext Coef b2	I2	–32768	32767	764	num
Calibration	106	Temp Model	14	Ext Coef b3	I2	–32768	32767	–3535	num
Calibration	106	Temp Model	16	Ext Coef b4	I2	–32768	32767	5059	num
Calibration	106	Temp Model	18	Ext rc0	I2	–32768	32767	11703	num
Calibration	106	Temp Model	20	Ext adc0	I2	–32768	32767	11813	num
Calibration	106	Temp Model	22	Rpad	I2	–32768	32767	87	Ω
Calibration	106	Temp Model	24	Rint	I2	–32768	32767	17740	Ω
Calibration	106	Temp Model	26	Int Coef 1	I2	–32768	32767	0	Seconds
Calibration	106	Temp Model	28	Int Coef 2	I2	–32768	32767	0	Seconds
Calibration	106	Temp Model	30	Int Coef 3	I2	–32768	32767	–12263	Seconds
Calibration	106	Temp Model	32	Int Coef 4	I2	–32768	32767	6106	Seconds
Calibration	106	Temp Model	34	Int Min AD	I2	–32768	32767	0	Seconds
Calibration	106	Temp Model	36	Int Max Temp	I2	–32768	32767	6106	0.1ºK
Calibration	107	Current	0	Filter	U1	0	255	239	Number
Calibration	107	Current	1	Dead Band	U1	0	255	5	mAmp
Calibration	107	Current	2	CC Deadband	U1	0	255	10	294 nV

8.5.3.4 Specific Data Flash Programming Details

In this section the data flash values that are not detailed elsewhere in this data sheet are shown in detail and others are summarized for easy reference.

8.5.3.4.1 OC Dsg

The *OC Dsg* is programmed into the OCDV register of the integrated AFE device. The *OC Dsg* sets the overcurrent in discharging voltage threshold. Changes to this data flash value requires a firmware full reset or a power reset of the bq33100 to take effect.

Table 63. OC Dsg

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
1	Current	16	OC Dsg	Hex	1	0x00	0x0F	0x0F	—

Figure 10. OCDV Register

7	6	5	4	3	2	1	0
—	—	—	—	OCDV3	OCDV2	OCDV1	OCDV0

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0000 is the bq33100 power on reset default.

OCDV3, OCDV2, OCDV1, OCDV0 — Sets the overcurrent voltage threshold (VSRP-VSRN)) in discharging of the integrated AFE.

0x0 - 0xf = sets the short circuit in discharging delay between 0ms - 915ms in 61ms steps.

[RSNS] = 0, 0x0 - 0xf sets the voltage threshold between 50 mV and 200 mV in 10 mV steps.

[RSNS] = 1, 0x0 - 0xf sets the voltage threshold between 20 mV and 100 mV in 5 mV steps.

OCDV (b7...b4) — Not used.

Table 64. OCDV (b2-b0) Configuration Bits with Corresponding Voltage Threshold When STATE_CTL[RSNS] = 0

SETTING	THRESHOLD		SETTING	THRESHOLD
0x00	0.050 V		0x08	0.130 V
0x01	0.060 V		0x09	0.140 V
0x02	0.070 V		0x0a	0.150 V
0x03	0.080 V		0x0b	0.160 V
0x04	0.090 V		0x0c	0.170 V
0x05	0.100 V		0x0d	0.180 V
0x06	0.110 V		0x0e	0.190 V
0x07	0.120 V		0x0f	0.200 V

Table 65. OCDV (b2-b0) Configuration Bits with Corresponding Voltage Threshold When STATE_CTL[RSNS] = 1

SETTING	THRESHOLD		SETTING	THRESHOLD
0x00	0.025 V		0x08	0.065 V
0x01	0.050 V		0x09	0.070V
0x02	0.035 V		0x0a	0.075 V
0x03	0.040 V		0x0b	0.080 V
0x04	0.045 V		0x0c	0.085 V
0x05	0.050 V		0x0d	0.090 V
0x06	0.055 V		0x0e	0.095V
0x07	0.060 V		0x0f	0.100 V

8.5.3.4.2 OC Dsg Time

The *OC Dsg Time* is programmed into the OCDD register of the integtrated AFE device. The *OC Dsg Time* sets the overcurrent in discharging delay. Changes to this data flash value requires a firmware full reset or a power reset of the bq33100 to take effect.

Table 66. OC Dsg Time

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
1	Current	17	OC Dsg Time	Hex	1	0x00	0x0F	0x0F	—

Figure 11. OCDD Register

7	6	5	4	3	2	1	0
—	—	—	—	OCDD3	OCDD2	OCDD1	OCDD0

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0000 is the bq33100 power on reset default.

OCDD3, OCDD2, OCDD1, OCDD0 — Sets the overcurrent in discharging delay of the integrated AFE.

0x0 - 0xf = sets the overvoltage trip delay between 1 ms to 31 ms in 2 ms steps

OCDD (b7...b4) — Not used.

Table 67. OCDD (b7-b4) Configuration Bits With Corresponding Delay Time

SETTING	DELAY	SETTING	DELAY	SETTING	DELAY	SETTING	DELAY
0x00	1 ms	0x04	9 ms	0x08	17 ms	0x0c	25 ms
0x01	3 ms	0x05	11 ms	0x09	19 ms	0x0d	27 ms
0x02	5 ms	0x06	13 ms	0x0a	21 ms	0x0e	29 ms
0x03	7 ms	0x07	15 ms	0x0b	23 ms	0x0f	31 ms

8.5.3.4.3 SC Dsg Cfg

The *SC Dsg Cfg* is programmed into the SCD register of the integtrated AFE device. The *SC Dsg Cfg* sets the short circuit in discharging voltage threshold and the short circuit in discharging delay. Changes to this data flash value requires a firmware full reset or a power reset of the bq33100 to take effect.

Table 68. SC Dsg Cfg

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
1	Current	21	SC Dsg Cfg	Hex	1	0x00	0x0F	0x0F	—

Figure 12. SCD Register

7	6	5	4	3	2	1	0
SCDD3	SCDD2	SCDD1	SCDD0	—	SCDV2	SCDV1	SCDV0

0000 is the bq33100 power on reset default.

SCDD3, SCDD2, SCDD1, SCDD0 — Sets the short circuit delay in discharging of the integrated AFE.

0x0 - 0xf = sets the short circuit in discharging delay between 0 ms to 915 ms in 61 ms steps.

If **STATE_CTL[SCDDx2]** is set, the delay time is double of that programmed in this register.

SCDV2, SCDV1, SCDV0 — Sets the short circuit voltage threshold (VSRP-VSRN)) in discharging of the integrated AFE

[RSNS] = 0, 0x0 - 0x7 sets the short circuit voltage threshold between 100 mV and 450 mV in 50 mV steps

[RSNS] = 1, 0x0 - 0x7 sets the short circuit voltage threshold between 50 mV and 475 mV in 25 mV steps

SCD (b3)— Not used.

Table 69. SCDV (b2-b0) Configuration Bits with Corresponding Voltage Threshold When STATE_CTL[RSNS] = 0

SETTING	THRESHOLD	SETTING	THRESHOLD
0x00	0.100 V	0x04	0.300 V
0x01	0.150 V	0x05	0.350 V
0x02	0.200 V	0x06	0.400 V
0x03	0.250 V	0x07	0.450 V

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Table 70. SCDV (b2-b0) Configuration Bits with Corresponding Voltage Threshold When STATE_CTL[RSNS] = 1

SETTING	THRESHOLD	SETTING	THRESHOLD
0x00	0.050 V	0x04	0.150 V
0x01	0.075 V	0x05	0.175 V
0x02	0.100 V	0x06	0.200 V
0x03	0.125 V	0x07	0.225 V

Table 71. SCDD (b7-b4) Configuration Bits with Corresponding Delay Time

SETTING	DELAY	SETTING	DELAY	SETTING	DELAY	SETTING	DELAY
0x00	0 us	0x04	244 us	0x08	488 us	0x0c	732 us
0x01	61 us	0x05	305 us	0x09	549 us	0x0d	793 us
0x02	112 us	0x06	366 us	0x0a	610 us	0x0e	854 us
0x03	183 us	0x07	427 us	0x0b	671 us	0x0f	915 us

8.5.3.4.4 SC Chg Cfg

The *SC Chg Cfg* is programmed into the SCC register of the integtrated AFE device. The *SC Chg Cfg* sets the short circuit in charging voltage threshold and the short circuit in charging delay. Changes to this data flash value requires a firmware full reset or a power reset of the bq33100 to take effect.

Table 72. SC Chg Cfg

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
1	Current	20	SC Chg Cfg	Hex	1	0x00	0xF7	0xF7	—

Figure 13. SCC Register

7	6	5	4	3	2	1	0
SCCD3	SCCD2	SCCD1	SCCD0	—	SCCV2	SCCV1	SCCV0

0000 is the bq33100 power on reset default.

SCCD3, SCCD2, SCCD1, SCCD0 — Sets the short circuit delay in charging of the integrated AFE.

0x0 - 0xf = sets the short circuit in charging delay between 0 ms to 915 ms in 61 ms steps.

If **STATE_CTL[SCDDx2]** is set, the delay time is double of that programmed in this register.

SCCV2, SCCV1, SCCV0 — Sets the short circuit voltage threshold (VSRP-VSRN)) in charging of the integrated AFE

[RSNS] = 0, 0x0 - 0x7 sets the short circuit voltage threshold between 100 mV and 450 mV in 50 mV steps

[RSNS] = 1, 0x0 - 0x7 sets the short circuit voltage threshold between 50 mV and 475 mV in 25 mV steps

SCC (b3) — Not used.

Table 73. SCCV (b2-b0) Configuration Bits with Corresponding Voltage Threshold When STATE_CTL[RSNS] = 0

SETTING	THRESHOLD	SETTING	THRESHOLD
0x00	–0.100 V	0x04	–0.300 V
0x01	–0.150 V	0x05	n/a
0x02	–0.200 V	0x06	n/a
0x03	–0.250 V	0x07	n/a

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Table 74. SCCV (b2-b0) Configuration Bits with Corresponding Voltage Threshold When STATE_CTL[RSNS] = 1

SETTING	THRESHOLD	SETTING	THRESHOLD
0x00	–0.050 V	0x04	–0.150 V
0x01	–0.075 V	0x05	–0.175 V
0x02	–0.100 V	0x06	–0.200 V
0x03	–0.125 V	0x07	–0.225 V

Table 75. SCCD (b7-b4) Configuration Bits with Corresponding Delay Time

SETTING	DELAY	SETTING	DELAY	SETTING	DELAY	SETTING	DELAY
0x00	0 us	0x04	244 us	0x08	488 us	0x0c	732 us
0x01	61 us	0x05	305 us	0x09	549 us	0x0d	793 us
0x02	112 us	0x06	366 us	0x0a	610 us	0x0e	854 us
0x03	183 us	0x07	427 us	0x0b	671 us	0x0f	915 us

8.5.3.4.5 Initial Full Charge Capacitance

The value of ***Initial Full Charge Capacitance*** is used in the health and other calculations.

Table 76. Initial Full Charge Capacitance

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
48	Data	22	Initial Full Charge Capacitance	Integer	2	0	65535	250	F

8.5.3.4.6 Full Charge Capacitance

This value is used as the *Full Charge Capacitance* at device reset. This value is updated by the gauging algorithm when a qualified learning cycle has completed.

Table 77. Full Charge Capacitance

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
48	Data	26	Full Charge Capacitance	Integer	2	0	65535	250	F

8.5.3.4.7 Firmware Version

The *ManufacturerAccess* function reports ***Firmware Version*** as part of its return value.

Table 78. Firmware Version

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
56	Manufacturer Data	4	Firmware Version	Hex	2	0x0000	0xffff	0x00000	—

8.5.3.4.8 Hardware Revision

The *ManufacturerAccess* function reports ***Hardware Version*** as part of its return value.

Table 79. Hardware Revision

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
56	Manufacturer Data	6	Hardware Revision	Hex	2	0x0000	0xffff	0x0000	—

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8.5.3.4.9 Manuf. Info

The *ManufacturerInfo* function returns the string stored in ***Manuf. Info***. The maximum text length is 31 characters.

Table 80. Manuf. Info

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
58	Manufacturer Info	0	Manuf. Info	String	32	—	—	012345678 9ABCDEF0 123456789 ABCDE	

8.5.3.4.10 Operation Cfg

This register enables, disables or configures various features of the bq33100.

Table 81. Operation Cfg

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
64	Registers	0	Operation Cfg	Hex	2	0x0000	0xffff	0x04a8	

Figure 14. Operation Cfg Register

15	14	13	12	11	10	9	8
RSVD	RSVD	RSVD	RSVD	RSVD	CC2	CC1	CC0
7	6	5	4	3	2	1	0
RSVD	LT_EN	RSVD	TEMP1	TEMP0	RSVD	RSVD	STACK

LEGEND: RSVD = Reserved and must be programmed to 0 unless otherwise specified

CC2, CC1, CC0 —These bits configure the bq33100 for the number of series capacitors in the Super Capacitor stack.

0,0,0 = Reserved

0,0,1 = 2 capacitors

0,1,0 = 3 capacitors (default)

0,1,1 = 4 capacitors

1,0,0 = 5 capacitors

LT_EN — Lifetime Data logging bit; this bit enables or disables Lifetime Data logging from occurring; This bit can be directly set by the *Lifetime Enable* command.

0 = All Lifetime Data logging is prevented from occurring.

1 = All Lifetime Data logging are allowed

TEMP1, TEMP0 —These bits configure the source of the Temperature function

0,0 = Internal Temperature Sensor

0,1 = TS Input (default)

STACK —This bit configure the bq33100 to measure all series voltages up to 5 series cells or just the stack voltage.

0 = Each series cell is measured and can be balanced up to 5 series capacitors

1 = The capacitor stack is measured and Capacitor Balancing and Cell Imbalance Detection are disabled

8.5.3.4.11 FET ACTION

The ***FET Action*** register enables the charge FET to turn off when a safety condition occurs. The charge FET turns off when the a bit in the *SafetyStatus* register is set that corresponds to a set bit in the *FET action* register.

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Table 82. FET Action

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
64	Registers	4	FET Action	Hex	2	0x0000	0xffff	0x0000	

Figure 15. FET Action Register

15	14	13	12	11	10	9	8
CLBAD	HFAIL	HWARN	HLOW	RSVD	OTC	CIM	OV
7 7	6	5	4	3	2	1	0
DFF	RSVD	AFE_C	WDF	OCC	OCD	SCC	SCD

CLBAD: Weak capacitor condition

HFAIL: Health fault condition

HWARN: Health warning condition

HLOW: Health low condition

AFE_C: AFE Communications failure condition

CIM: Capacitor voltage imbalance condition

DFF: Data Flash Fault failure condition

OTC: Charge overtemperature condition

OV: Capacitor overvoltage condition

WDF: AFE Watchdog fault condition

OCC: Charge overcurrent condition

OCD: AFE overcurrent on discharge condition

SCC: AFE short circuit on charge condition

SCD: AFE short circuit on discharge condition

OV: Capacitor overvoltage condition

8.5.3.4.12 FAULT

The ***FAULT*** register enables or disables the use of the FAULT pin when the corresponding bit in *SafetyStatus* is set.

Table 83. FAULT

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
64	Registers	8	FAULT	Hex	2	0x0000	0xffff	0x0000	

Figure 16. FAULT Register

15	14	13	12	11	10	9	8
CLBAD	HFAIL	HWARN	HLOW	RSVD	OTC	CIM	OV
7	6	5	4	3	2	1	0
DFF	RSVD	AFE_C	WDF	OCC	OCD	SCC	SCD

CLBAD: Weak capacitor condition

HFAIL: Health fault condition

HWARN: Health warning condition

HLOW: Health low condition

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AFE_C: AFE Communications failure condition

CIM: Capacitor voltage imbalance condition

DFF: Data Flash Fault failure condition

OTC: Charge overtemperature condition

OV: Capacitor overvoltage condition

WDF: AFE Watchdog fault condition

OCC: Charge overcurrent condition

OCD: AFE overcurrent on discharge condition

SCC: AFE short circuit on charge condition

SCD: AFE short circuit on discharge condition

8.5.3.4.13 AFE State_CTL

This register adjusts the AFE hardware overcurrent and short circuit detection thresholds and delay.

Table 84. AFE State_CTL

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
65	AFE	1	AFE State_CTL	Hex	1	0x00	0xff	0x00	

Figure 17. AFE State_CTL Register

7	6	5	4	3	2	1	0
RSVD	RSVD	SCDDX2	RSNS	RSVD	RSVD	RSVD	RSVD

LEGEND: RSVD = Reserved and must be programmed to 0

SCDDX2— Set this bit to double the SCD delay periods 0 (default) = Short Circuit current protection delay is as programmed

1 = Short Circuit current protection delay is twice that programmed

RSNS— This bit, if set, configures the SCD threshold into a range suitable for a low sense resistor value by dividing the SCDV selected voltage threshold by 2 0 (default) = Current protection voltage thresholds as programmed

1 = Current protection voltage threshold divided by 2 as programmed

8.5.3.4.14 Measurement Margin %

Measurement Margin % provides any needed addition margin for measurement error or other error sources

Table 85. Measurement Margin %

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
86	Capacitance Estimation	0	Measurement Margin %	Unsigned Integer	1	0	100	10	%

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8.5.3.4.15 Timer

Timer provides the maximum amount of time for a learning cycle to complete

Table 86. Timer

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
86	Capacitance Estimation	4	Timer	Integer	2	0	32767	10	s

8.5.3.4.16 V Chg Nominal

Nominal charging voltage(min) representing CHGLVL1 = Low (0) and CHGLVL0 = Low (0).

Table 87. V Chg Nominal

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
86	Capacitance Estimation	6	V Chg Nominal	Integer	2	0	25000	10400	mV

8.5.3.4.17 V Chg A

Charging voltage representing CHGLVL1 = Low (0) and CHGLVL0 = High (1).

Table 88. V Chg A

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
86	Capacitance Estimation	8	V Chg A	Integer	2	0	25000	11125	mV

8.5.3.4.18 V Chg B

Charging voltage representing CHGLVL1 = High (1) and CHGLVL0 = Low (0).

Table 89. V Chg B

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
86	Capacitance Estimation	10	V Chg B	Integer	2	0	25000	11875	mV

8.5.3.4.19 V Chg Max

Charging voltage(max) representing CHGLVL1 = High (1) and CHGLVL0 = High (1).

Table 90. V Chg Max

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
86	Capacitance Estimation	12	V Chg Max	Integer	2	0	25000	125000	mV

8.5.3.4.20 Min Voltage

Min Voltage is the minimum voltage which the Super Capacitor must discharge. ***Min Voltage*** is used in Capacitance estimation which defines the Super Capacitor usage range.

Table 91. Min Voltage

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
86	Capacitance Estimation	16	Min Voltage	Integer	2	0	10000	4000	mV

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8.5.3.4.21 Learning Frequency

Learning Frequency is the amount of time elapsed between automatic learning cycles.

NOTE

A value of 250 is used to set the Learning Frequency to 10 minutes for test purposes.

Table 92. Learning Frequency

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
86	Capacitance Estimation	18	Learning Frequency	Unsigned Integer	1	0	255	2	week

8.5.3.4.22 Dsg Current Threshold

The bq33100 enters discharge mode from charge mode if *Current* < (-) ***Dsg Current Threshold***.

Table 93. Dsg Current Threshold

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
81	Current Thresholds	0	Dsg Current Threshold	Integer	2	0	2000	10	mA

8.5.3.4.23 Chg Current Threshold

The bq33100 enters charge mode from discharge mode if *Current* > ***Chg Current Threshold.***

Table 94. Chg Current Threshold

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
81	Current Thresholds	2	Chg Current Threshold	Integer	2	0	2000	0	mA

8.5.3.4.24 Quit Current

The bq33100 enters relaxation mode from charge mode if *Current* goes below ***Quit Current*** for 60 seconds. The bq33100 enters relaxation mode from discharge mode if *Current* goes above (-)***Quit Current*** for 60 seconds.

Table 95. Quit Current

SUBCLASS ID	SUBCLASS NAME	OFFSET	NAME	FORMAT	SIZE IN BYTES	MIN VALUE	MAX VALUE	DEFAULT VALUE	UNIT
81	Current Thresholds	4	Quit Current	Integer	2	0	1000	0	mA

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq33100 is a super capacitor monitor that can provide Capacitance and ESR measurements for up to 9 series capacitors and balancing for systems with up to 5 series capacitors. This section of the data sheet provides practical applications information for hardware and systems engineers designing the bq33100 into their end equipment.

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9.2 Typical Application

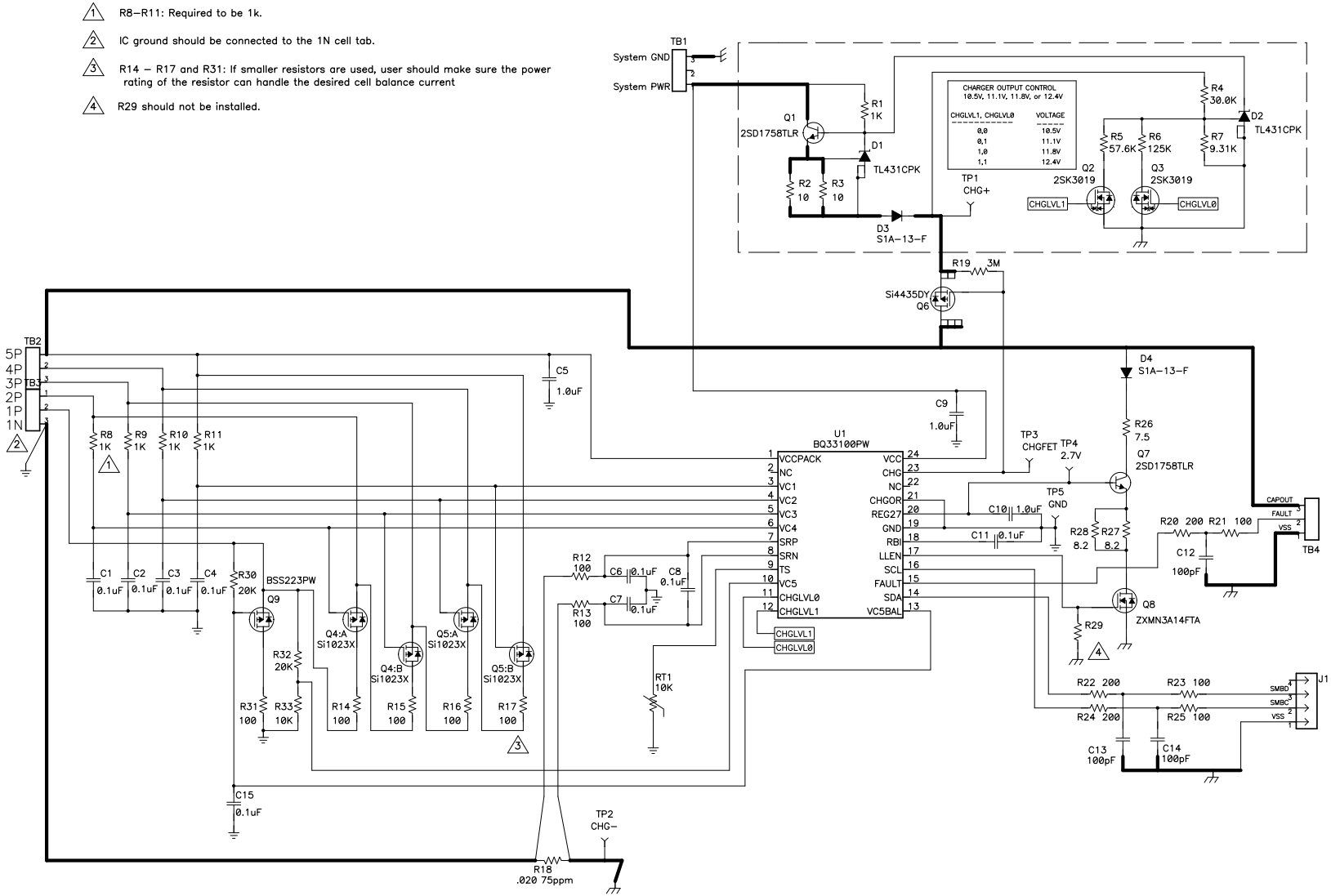


Figure 18. Application Reference Schematic

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9.2.1 Design Requirements

The bq33100 comes programmed to support 4 series capacitor systems with cell balancing enabled. Other key configuration defaults are shown in Table 96.

Table 96. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Number of Series Cells	4
Design Capacitance	250 F
Design ESR	320 mΩ
Cell Balancing	Enabled
V CHG Nominal	8400 mV
V CHG A	8900 mV
V CHG	9500 mV
V CHG MAX	10000 mV
Learn Frequency	2 weeks
Learn Delta Voltage	500 mV

Use the bqEVSW tool to update the settings to meet the specific application or pack configuration requirements.

9.2.2 Detailed Design Procedure

This section provides information on selecting key device configuration options. More information on these and other configuration options is available in *bq33100 Super Capacitor Manager - Top 13 Design Considerations*, SLUA751.

9.2.2.1 Selecting Number of Series Capacitor Support

The bq33100 can support 2 to 5 series capacitors when Operation Cfg [STACK] = 0 or 2 to 9 series capacitors when [STACK] = 1. The main difference is that when [STACK] = 1 the bq33100 will not perform cell balancing.

9.2.2.2 Selecting Charging Voltage Values

The bq33100 learning algorithm requires that the capacitors not be charged to their maximum charging value, for example: 2.5 V, under normal conditions. This allows for the bq33100 to charge up the capacitors a small amount and then enable a discharge as part of the learning process. The value to which the capacitors must charge up to is configured in **V Learn Max** and is expected to the be the maximum charging voltage as specified by the capacitor manufacturer, for example: 2.5 V. This is typically also the V CHG MAX value although some capacitor manufactures will allow a higher voltage for the short learning period compared to the DC value it is held at during normal charging.

The nominal charging voltage must be selected to enable the capacitor array to provide the required amount of energy from the capacitance at that voltage. This data is available from the capacitor manufacturer data sheet. The default value is 2.1 V per capacitor and as the device is configured as a 4 series system then the programmed value in V Chg Nominal is 8400 mV.

V CHG A and V CHG B must be selected to be evenly spread between V CHG Nominal and V Chg Max, for example: V CHG A = 8900 mV (2.225 V per cap) and V CHG B = 9500 (2.375 V per cap).

9.2.2.3 Learning Frequency Selection

The default learning frequency of the bq33100 is set to 2 weeks. The capacitance and ESR changes relatively slowly over time so selecting a period such as 2 weeks or longer allows for a change to be detected.

Setting an automatic update to occur on a very slow rate, for: 2 weeks, and then enabling the host system to update at a faster, for example: each day, or synchronized to a host system event, for example, after a host system reboot, is common.

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9.2.3 Application Curve

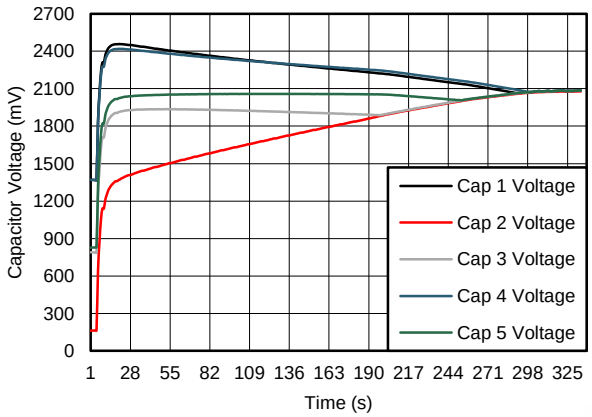


Figure 19. Voltage Convergence During Capacitor Balancing

10 Power Supply Recommendations

The device manages its supply voltage dynamically according to the operation conditions. Normally, the VCC and PACK input is the primary power source to the device. The VCC and PACK pin must be connected to the positive termination of the capacitor array. The input voltage for the VCC and PACK pin ranges from 3.8 V to 25 V. A 1-uF capacitor must be connected to the VCC and PACK as close to the device as possible for supply decoupling.

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11 Layout

11.1 Layout Guidelines

A capacitance monitor circuit board is a challenging environment due to the fundamental incompatibility of high current traces and ultra-low current semiconductor devices. The best way to protect against unwanted trace-to-trace coupling is with a component placement, where the high-current section is on the opposite side of the board from the electronic devices. Every attempt must be made to route high-current traces away from signal traces, which enter the bq33100 directly. IC references and registers can be disturbed and in rare cases damaged due to magnetic and capacitive coupling from the high-current path.

NOTE

During surge current and ESD events, the high-current traces appear inductive and can couple unwanted noise into sensitive nodes of the gas gauge electronics.

The learning load components can become heated depending on the component values selected. TI recommends that any heat is dissipated away from the bq33100 to ensure its maxim operating temperature is not exceeded.

11.2 Layout Example

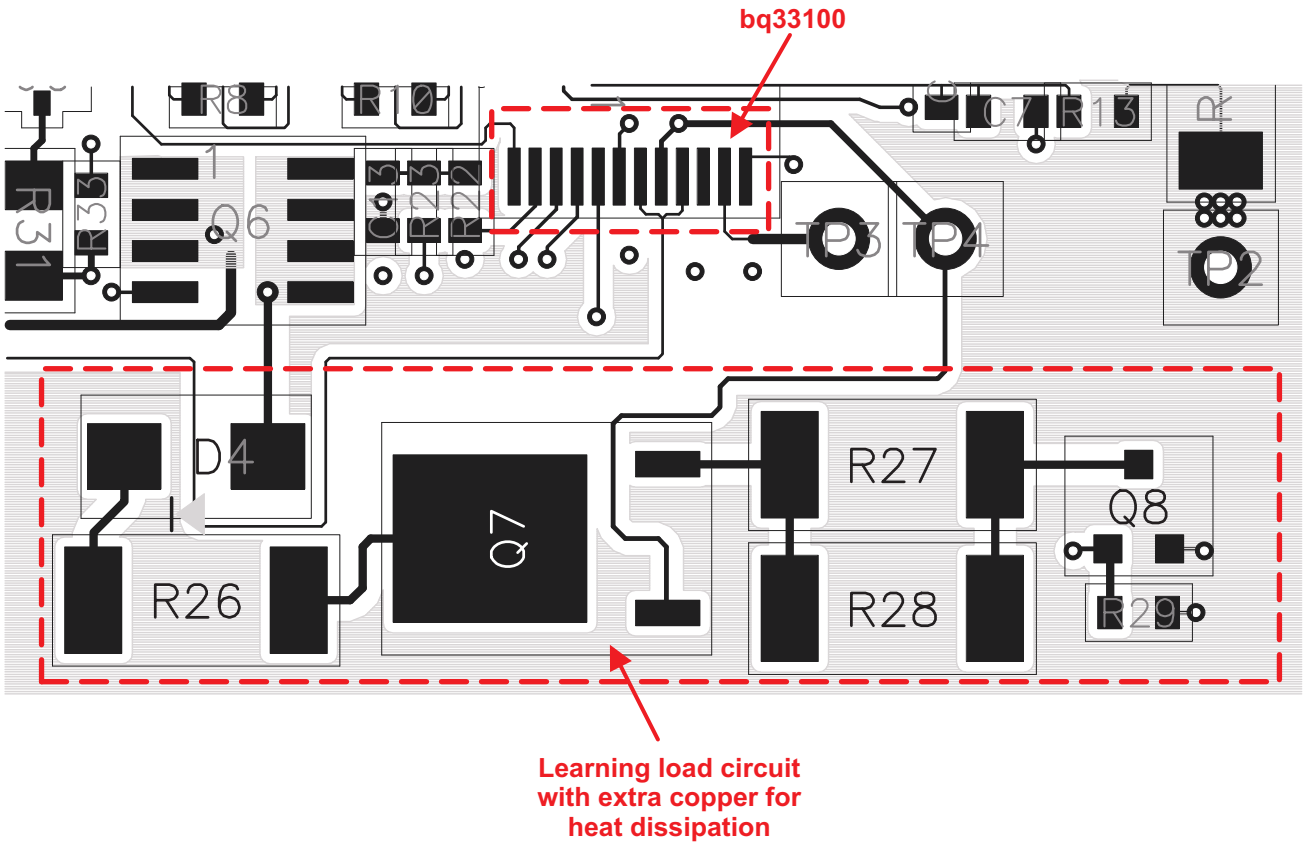


Figure 20. bq33100 Board Layout

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Layout Example (continued)

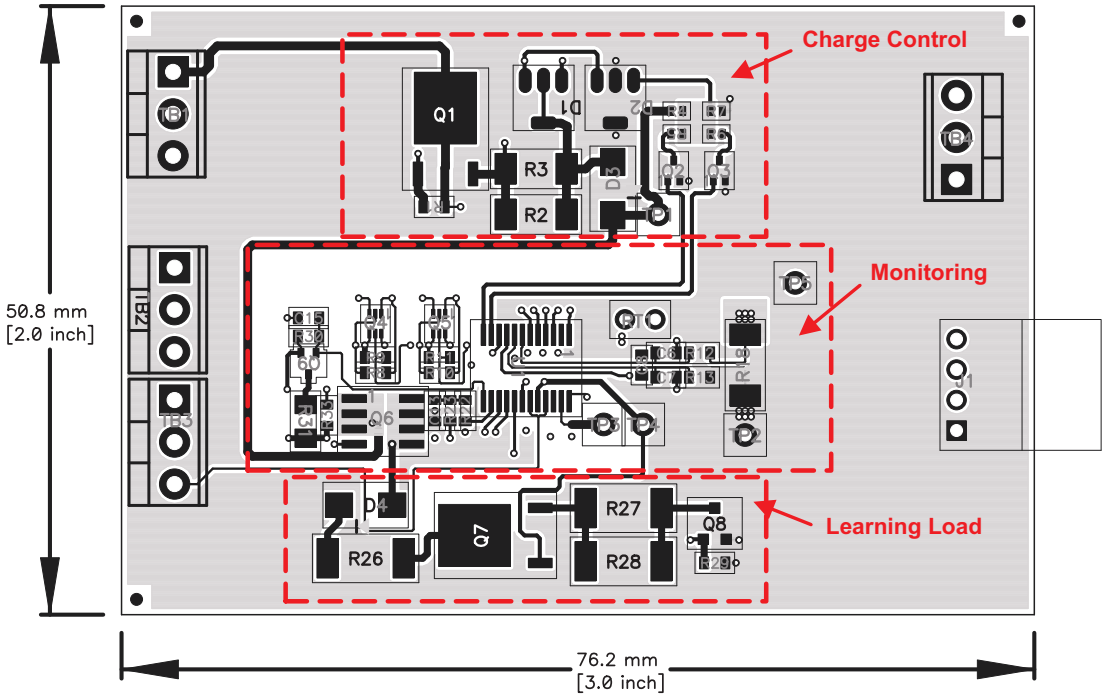


Figure 21. Top Layer

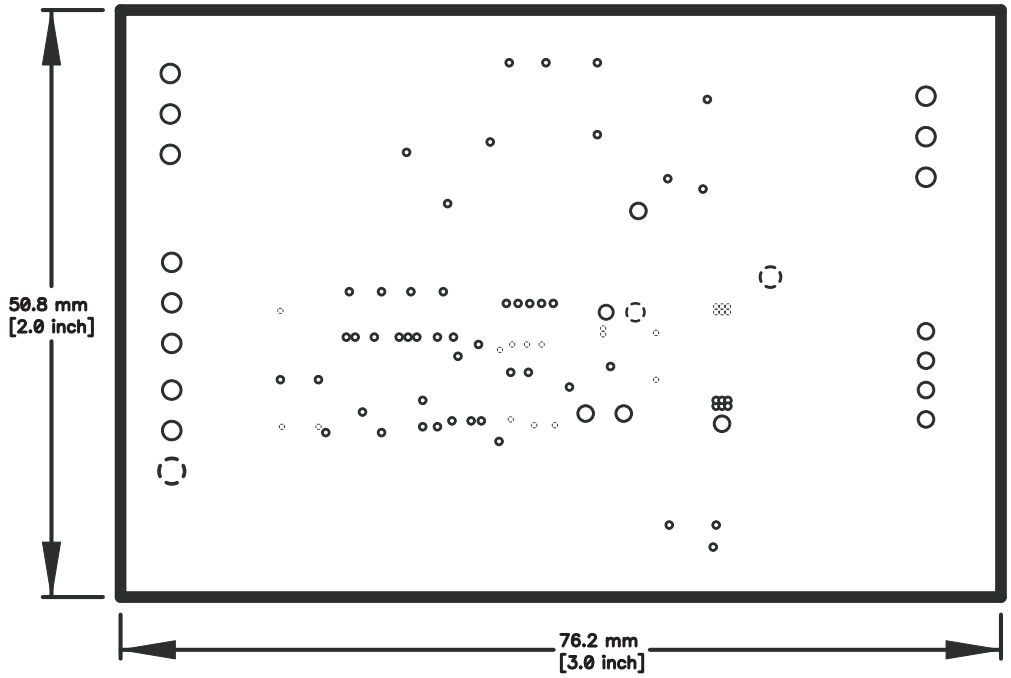


Figure 22. Internal Layer 1

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Layout Example (continued)

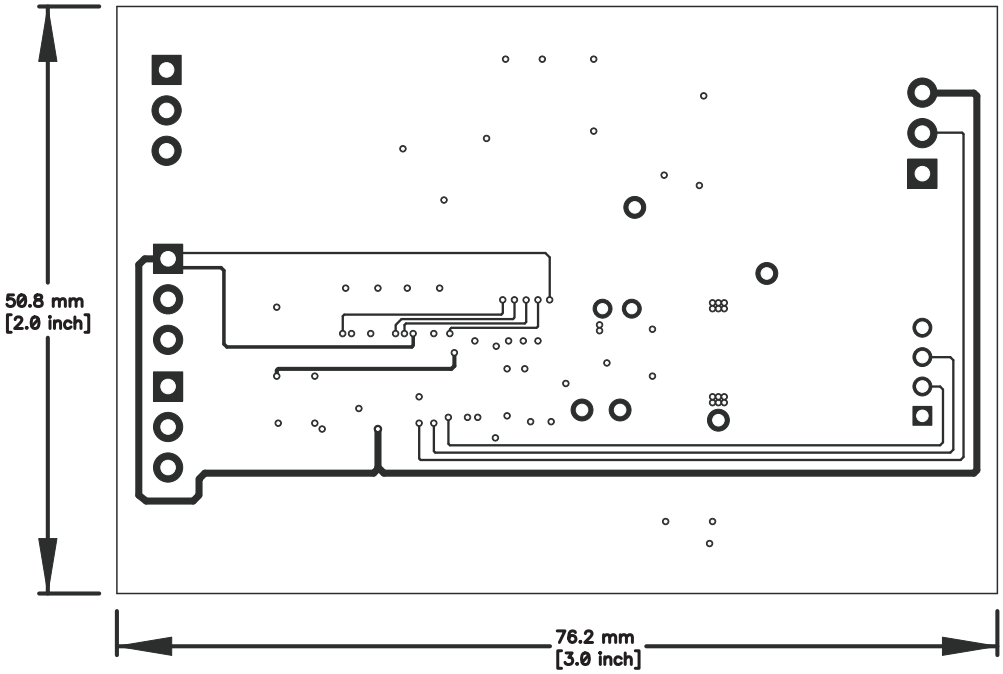


Figure 23. Internal Layer 2

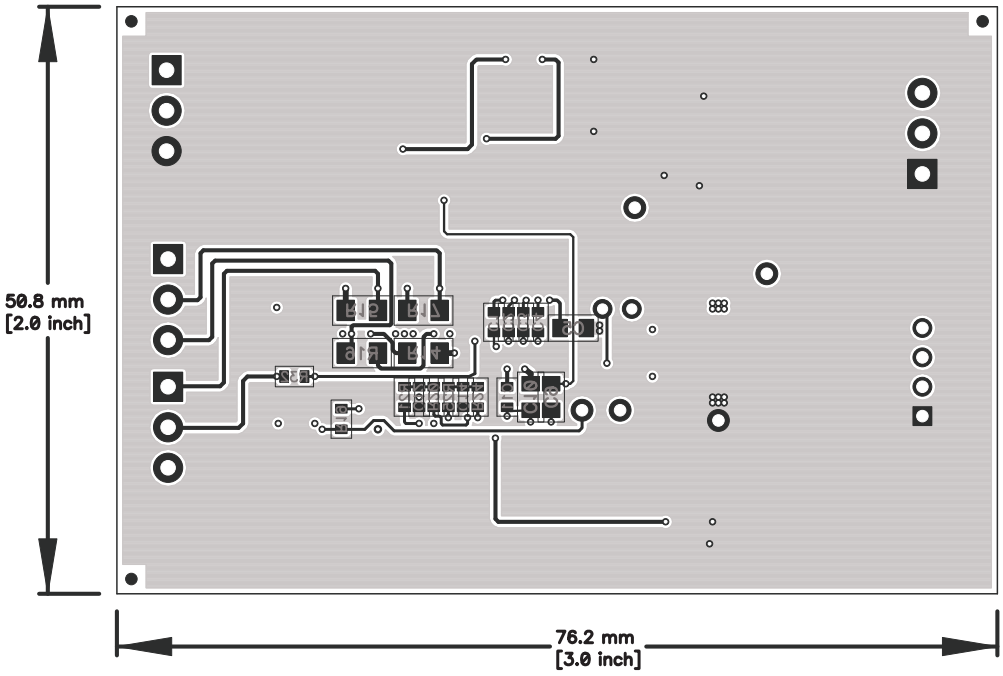


Figure 24. Bottom Layer

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

《bq33100 超级电容管理器 - 13 个关键的设计注意事项》，SLUA751

12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ33100PW	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	33100
BQ33100PW.A	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	33100
BQ33100PWR	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	33100
BQ33100PWR.A	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	33100

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

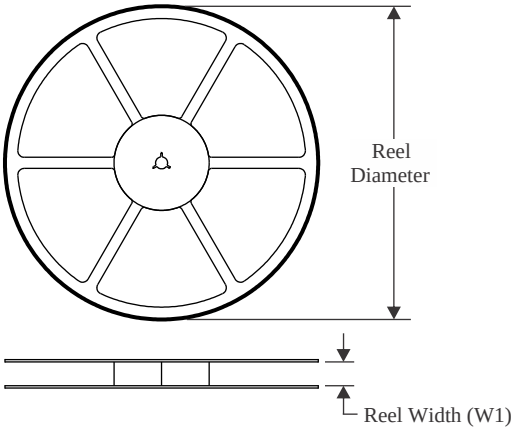
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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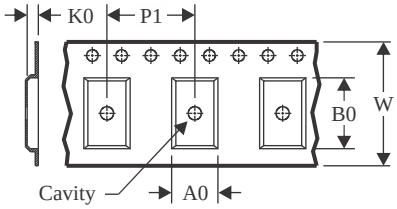
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

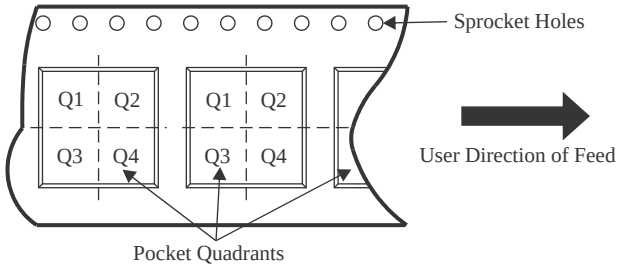


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

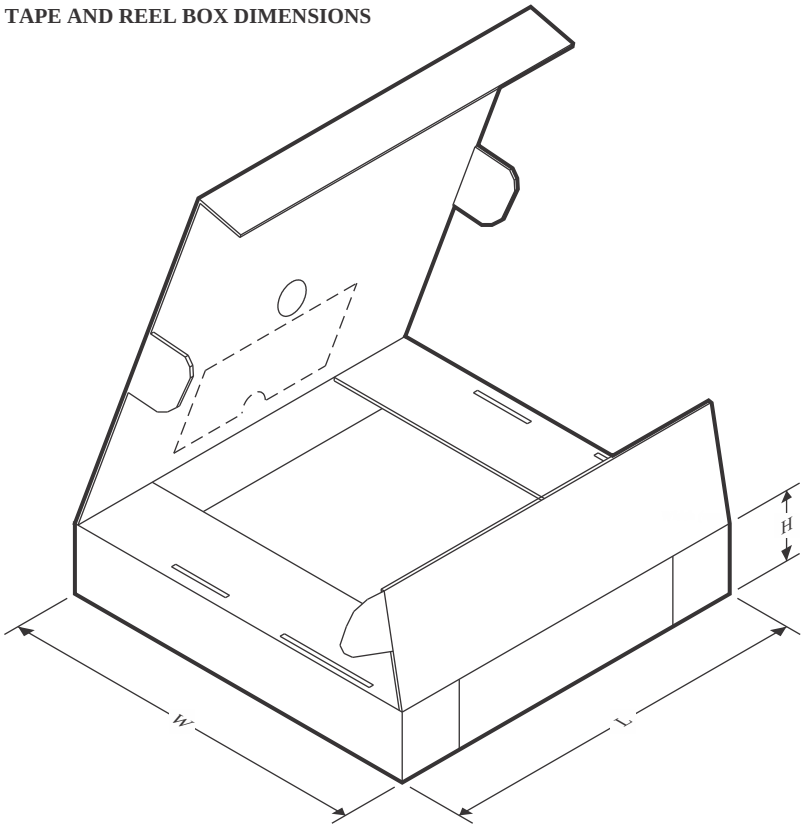
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ33100PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

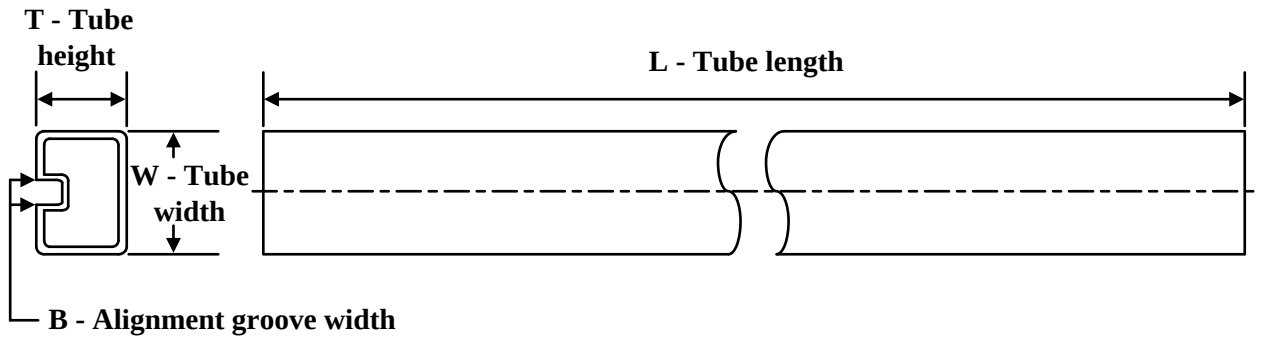
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ33100PWR	TSSOP	PW	24	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

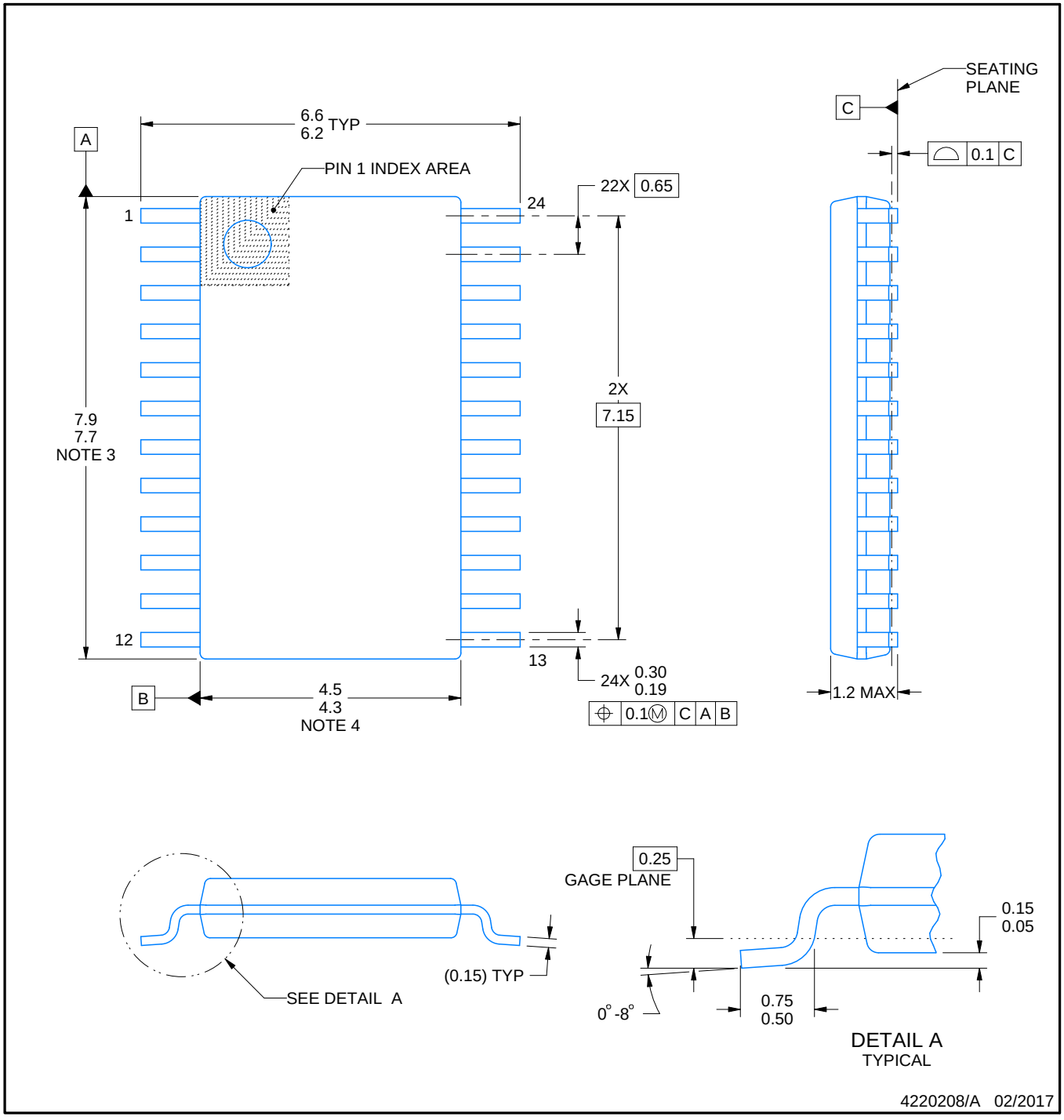
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BQ33100PW	PW	TSSOP	24	60	530	10.2	3600	3.5
BQ33100PW.A	PW	TSSOP	24	60	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0024A

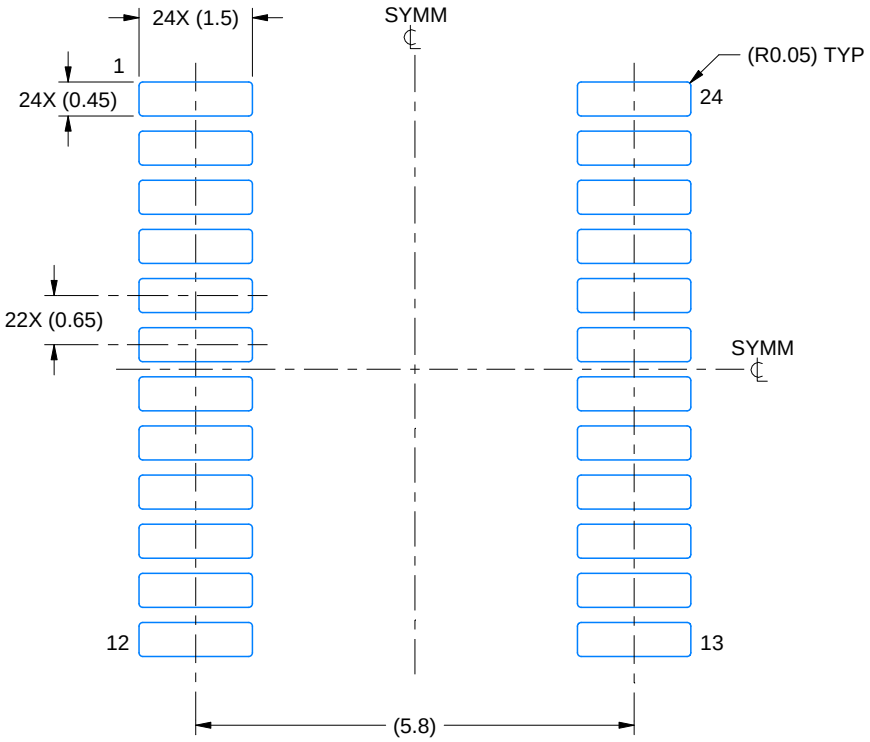
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

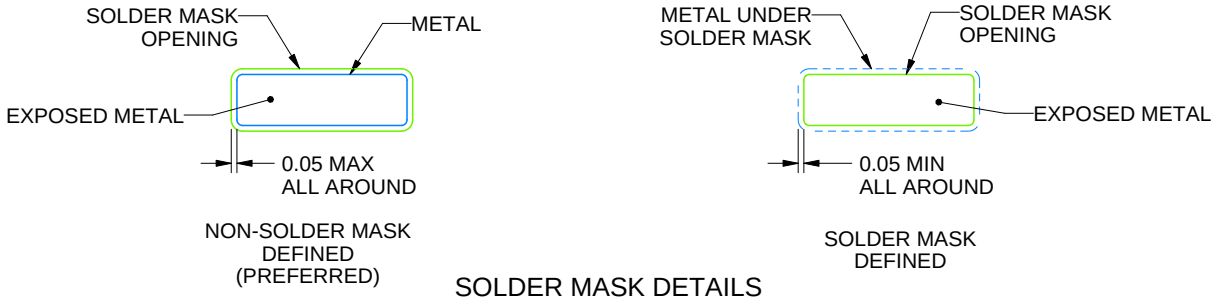


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

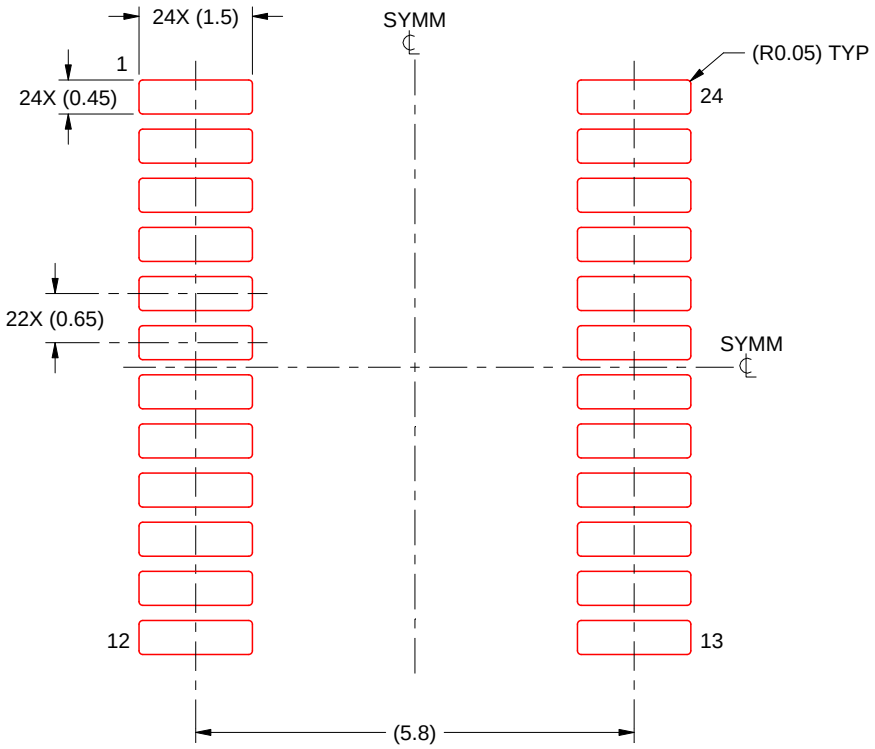


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月