BQ40Z50-R2 1 节、2 节、3 节和 4 节串联锂离子电池组管理器

1 特性

- 完全集成的 1 节、2 节、3 节和 4 节串联锂离子或锂聚合物电池组管理器和保护
- 获得专利的新一代 Impedance Track™ 技术可准确测量锂离子和锂聚合物电池中的可用电量
- 高侧 N 沟道保护 FET 驱动器
- 充电或者静止状态时具有集成的电池平衡功能
- 适合于 100mAh 和 29Ah 之间的电池
- 全面的可编程保护功能
  - 电压
  - 电流
  - 温度
  - 充电终止时间
  - CHG/DSG FET
  - 模拟前端 (AFE)
- 精密的充电算法
  - JEITA
  - 增强型充电
  - 自适应充电
  - 电池均衡
- 支持涡轮模式 2.0
- 支持电池跳闸点 (BTP)
- 诊断使用寿命数据监控器和黑盒记录器
- LED 显示屏
- 支持双线制 SMBus v1.1 接口
- 安全散列算法 (SHA-1) 认证
- IATA 支持
- 紧凑型封装：32 引线 QFN (RSM)

2 应用

- 平板电脑
- 无人机
- UPS/电池备用系统
- 医疗设备
- 手持式真空吸尘器和扫地机器人

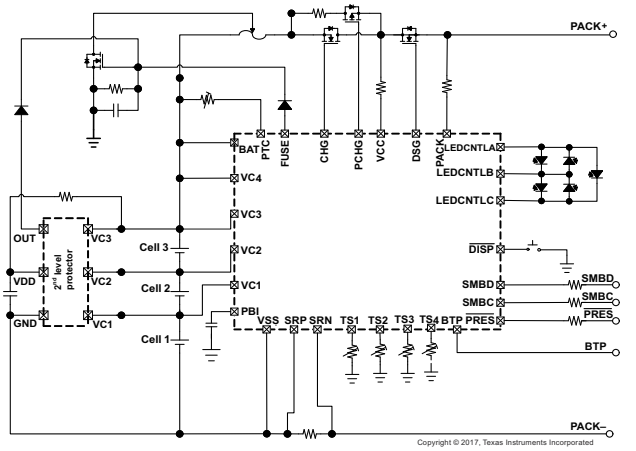
3 说明

BQ40Z50-R2 器件采用已获专利的 Impedance Track™ 技术，是一个全集成、单芯片、基于电池组的解决方案，可为 1 节、2 节、3 节和 4 节串联锂离子和锂聚合物电池组提供电量监测、保护和认证等各种特性。

BQ40Z50-R2 器件利用其集成的高性能模拟外设，测量锂离子或锂聚合物电池的可用容量、电压、电流、温度和其他关键参数，保留准确的数据记录，并通过 SMBus v1.1 兼容接口将这些信息报告给系统主机控制器。

器件信息

器件型号	封装	封装尺寸（标称值）
BQ40Z50-R2	VQFN (32)	4.00mm × 4.00mm



简化版原理图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (July 2018) to Revision C (April 2021)	Page
• 将整个数据表中出现的所有 OCD 更改为 OLD	1

Changes from Revision A (October 2017) to Revision B (July 2018)	Page
• Changed *Pin Configuration and Functions*	5
• Changed *System Present*	34

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5 Description (continued)

The BQ40Z50-R2 device supports TURBO Mode 2.0 by providing the available max power and max current to the host system. The device also supports Battery Trip Point to send a BTP interrupt signal to the host system at the preset state of charge thresholds.

The BQ40Z50-R2 provides software-based 1st- and 2nd-level safety protection against overvoltage, undervoltage, overcurrent, short-circuit current, overload, and overtemperature conditions, as well as other pack- and cell-related faults.

SHA-1 authentication, with secure memory for authentication keys, enables identification of genuine battery packs.

The compact 32-lead QFN package minimizes solution cost and size for smart batteries while providing maximum functionality and safety for battery gauging applications.

6 Pin Configuration and Functions

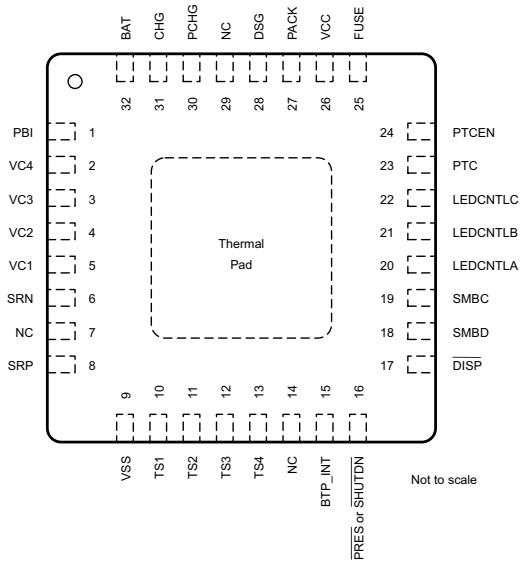


表 6-1. Pin Functions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	PBI	P(1)	Power supply backup input pin. Connect to the 2.2-µF capacitor to VSS.
2	VC4	IA	Sense voltage input pin for the most positive cell, and balance current input for the most positive cell. Should be connected to the positive terminal of the fourth cell from the bottom of the stack with a 100-Ω series resistor and a 0.1-µF capacitor to VC3. If not used, connect to VC3.
3	VC3	IA	Sense voltage input pin for the third-most positive cell, balance current input for the third-most positive cell, and return balance current for the most positive cell. Should be connected to the positive terminal of the third cell from the bottom of the stack with a 100-Ω series resistor and a 0.1-µF capacitor to VC2. If not used, connect to VC2.
4	VC2	IA	Sense voltage input pin for the second-most positive cell, balance current input for the second-most positive cell, and return balance current for the third-most positive cell. Should be connected to the positive terminal of the second cell from the bottom of the stack with a 100-Ω series resistor and a 0.1-µF capacitor to VC1. If not used, connect to VC1.
5	VC1	IA	Sense voltage input pin for the least positive cell, balance current input for the least positive cell, and return balance current for the second-most positive cell. Should be connected to the positive terminal of the first cell from the bottom of the stack with a 100-Ω series resistor and a 0.1-µF capacitor to VSS.

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表 6-1. Pin Functions (continued)

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
6	SRN	I	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN where SRP is the top of the sense resistor.
7	NC	—	Not internally connected. It is okay to leave floating or to tie to VSS.
8	SRP	I	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN where SRP is the top of the sense resistor.
9	VSS	P	Device ground
10	TS1	IA	Temperature sensor 1 thermistor input pin. Connect to thermistor-1. If not used, connect directly to VSS and configure data flash accordingly.
11	TS2	IA	Temperature sensor 2 thermistor input pin. Connect to thermistor-2. If not used, connect directly to VSS and configure data flash accordingly.
12	TS3	IA	Temperature sensor 3 thermistor input pin. Connect to thermistor-3. If not used, connect directly to VSS and configure data flash accordingly.
13	TS4	IA	Temperature sensor 4 thermistor input pin. Connect to thermistor-4. If not used, connect directly to VSS and configure data flash accordingly.
14	NC	—	Not internally connected. It is okay to leave floating or to tie to VSS.
15	BTP_INT	O	Battery Trip Point (BTP) interrupt output. If not used, connect directly to VSS.
16	$\overline{\text{PRES}}$ or $\overline{\text{SHUTDN}}$	I	Host system present input for removable battery pack or emergency system shutdown input for embedded pack. A pullup is not required for this pin. If not used, connect directly to VSS.
17	$\overline{\text{DISP}}$	—	Display control for LEDs. If not used, connect directly to VSS.
18	SMBD	I/OD	SMBus data pin
19	SMBC	I/OD	SMBus clock pin
20	LEDCNTLA	—	LED display segment that drives the external LEDs depending on the firmware configuration. If LEDs are not used, these pins can be left floating or connected to VSS through a 20-kΩ resistor.
21	LEDCNTLB	—	LED display segment that drives the external LEDs depending on the firmware configuration. If LEDs are not used, these pins can be left floating or connected to VSS through a 20-kΩ resistor.
22	LEDCNTLC	—	LED display segment that drives the external LEDs depending on the firmware configuration. If LEDs are not used, these pins can be left floating or connected to VSS through a 20-kΩ resistor.
23	PTC	IA	Safety PTC thermistor input pin. To disable, connect both PTC and PTCEN to VSS.
24	PTCEN	IA	Safety PTC thermistor enable input pin. Connect to BAT. To disable, connect both PTC and PTCEN to VSS.
25	FUSE	O	Fuse drive output pin. If not used, connect directly to VSS.
26	VCC	P	Secondary power supply input
27	PACK	IA	Pack sense input pin
28	DSG	O	NMOS Discharge FET drive output pin. If not used, it can be left floating or connected to VSS through a 20-kΩ resistor.
29	NC	—	Not internally connected. It is okay to leave floating or to tie to VSS.
30	PCHG	O	PMOS Precharge FET drive output pin. If not used, it can be left floating or connected to VSS through a 20-kΩ resistor.
31	CHG	O	NMOS Charge FET drive output pin. If not used, it can be left floating or connected to VSS through a 20-kΩ resistor.
32	BAT	P	Primary power supply input pin

(1) P = Power Connection, O = Digital Output, AI = Analog Input, I = Digital Input, I/OD = Digital Input/Output

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6.1 Pin Equivalent Diagrams

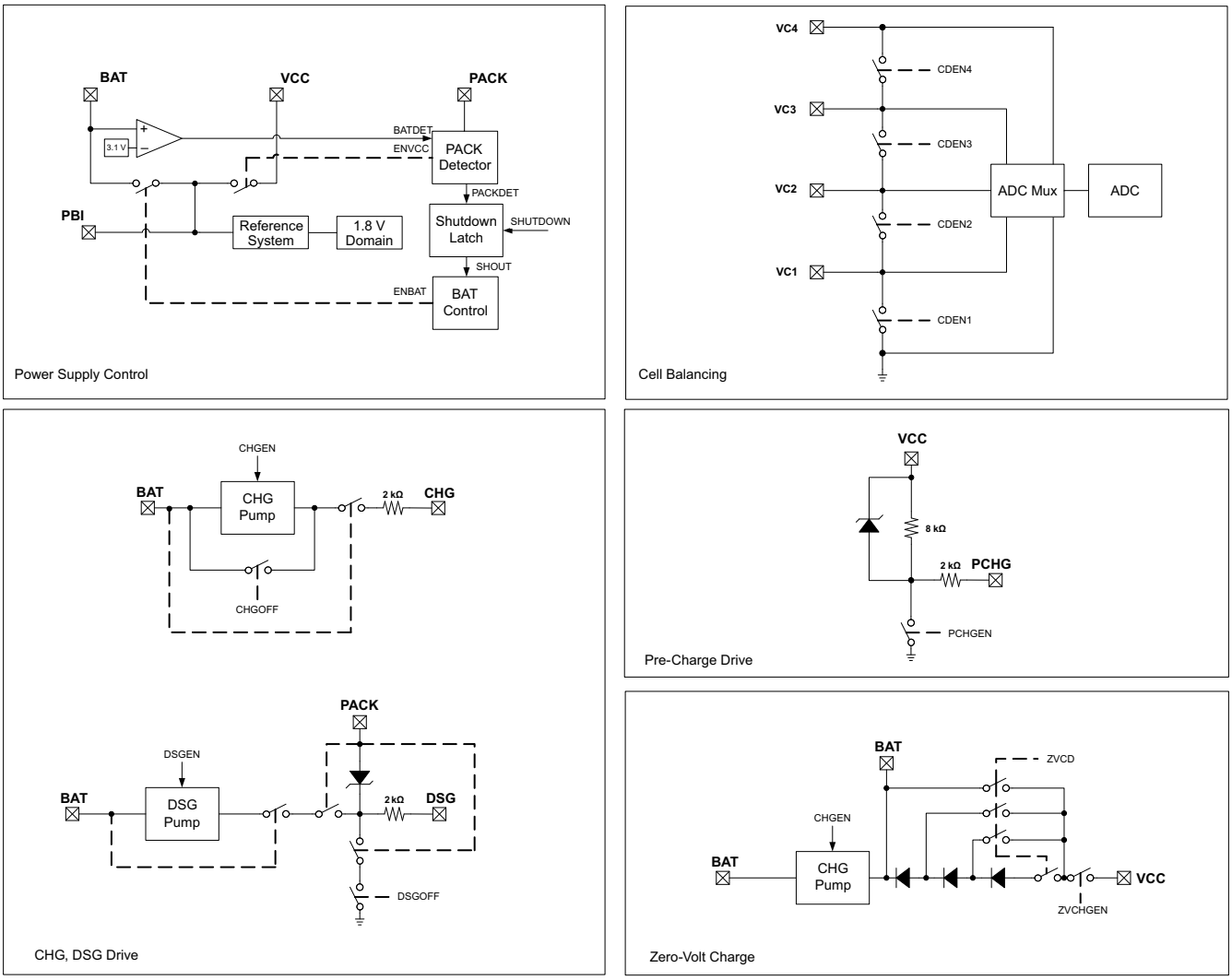


图 6-1. Pin Equivalent Diagram 1

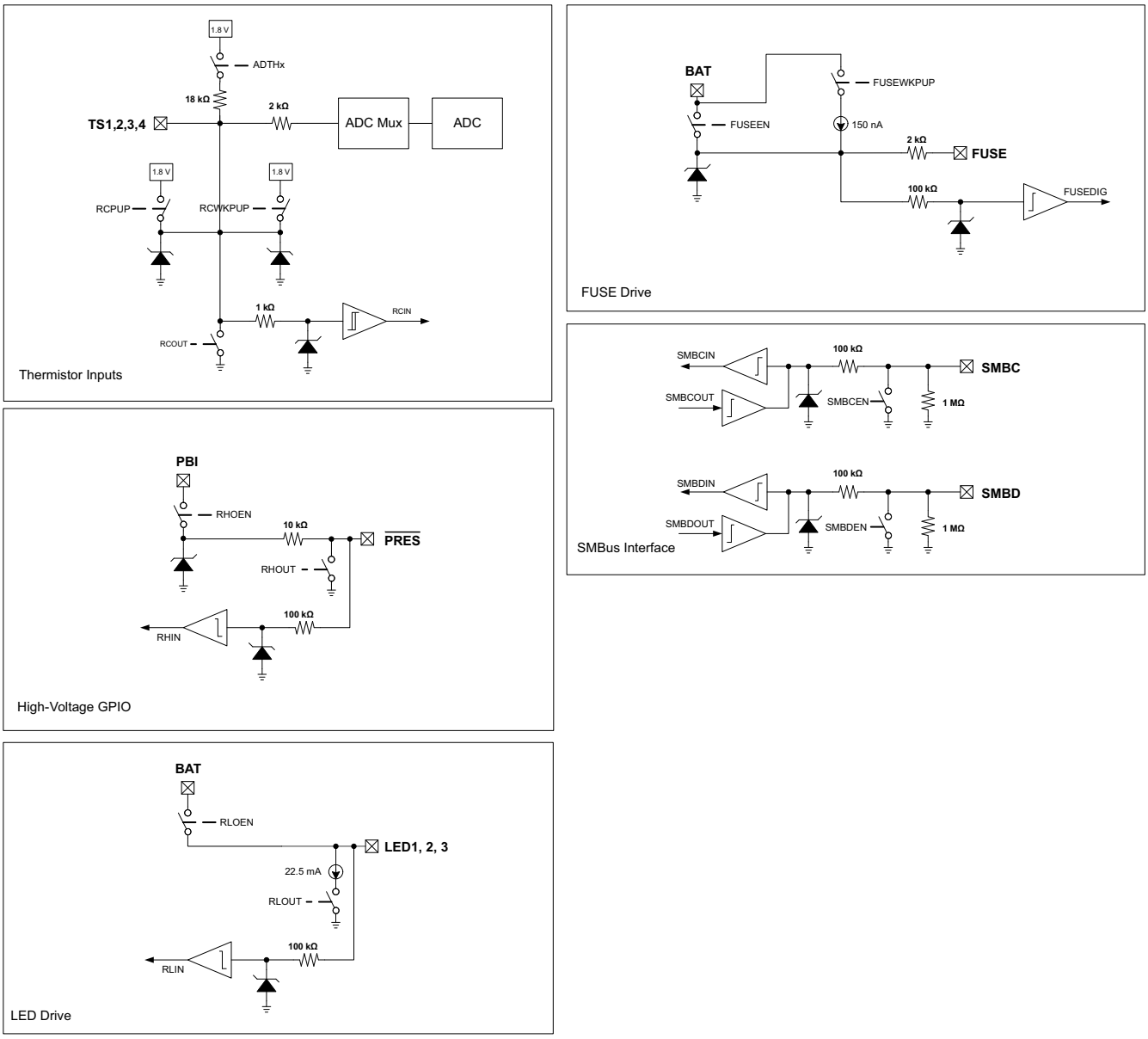


图 6-2. Pin Equivalent Diagram 2

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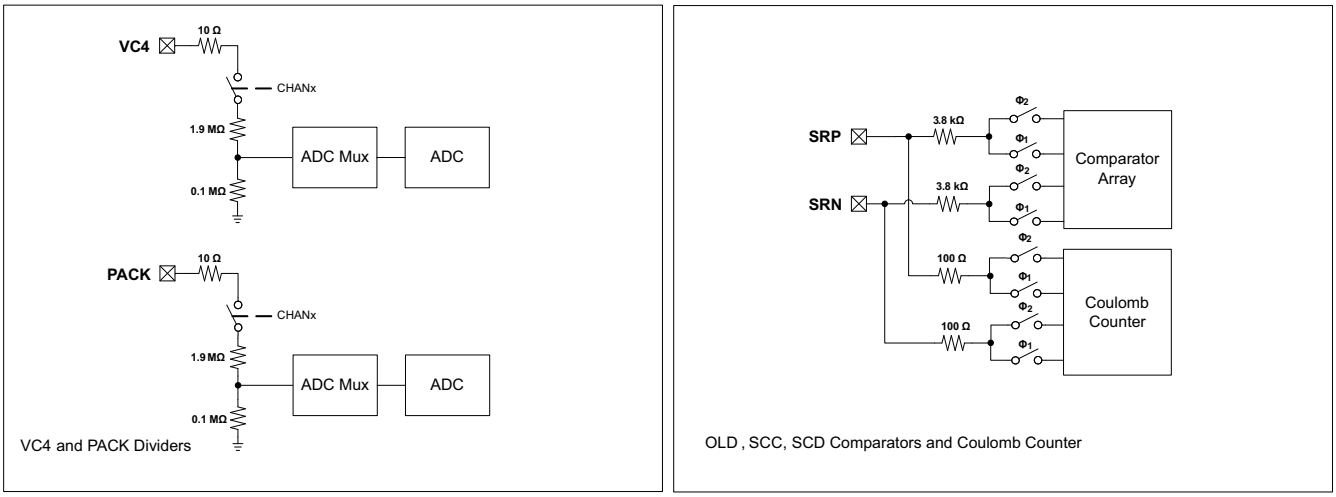


图 6-3. Pin Equivalent Diagram 3

7 Specifications

7.1 Absolute Maximum Ratings

Over-operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range, V_{CC}	BAT, VCC, PBI	–0.3	30	V
Input voltage range, V_{IN}	PACK, SMBC, SMBD, $\overline{PRES}$ or $\overline{SHUTDN}$, BTP_INT, $\overline{DISP}$	–0.3	30	V
	TS1, TS2, TS3, TS4	–0.3	V_{REG} + 0.3	V
	PTC, PTCEN, LEDCNTLA, LEDCNTLB, LEDCNTLC	–0.3	V_{BAT} + 0.3	V
	SRP, SRN	–0.3	0.3	V
	VC4	VC3 – 0.3	VC3 + 8.5, or VSS + 30	V
	VC3	VC2 – 0.3	VC2 + 8.5, or VSS + 30	V
	VC2	VC1 – 0.3	VC1 + 8.5, or VSS + 30	V
	VC1	VSS – 0.3	VSS + 8.5, or VSS + 30	V
Output voltage range, V_O	CHG, DSG	–0.3	32	
	PCHG, FUSE	–0.3	30	V
Maximum VSS current, I_{SS}			50	mA
Storage temperature, T_{STG}		–65	150	°C
Lead temperature (soldering, 10 s), T_{SOLDER}			300	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute – maximum – rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	BAT, VCC, PBI	2.2		26	V
$V_{SHUTDOWN-}$	Shutdown voltage	$V_{PACK} < V_{SHUTDOWN-}$	1.8	2.0	2.2	V
$V_{SHUTDOWN+}$	Start-up voltage	$V_{PACK} > V_{SHUTDOWN-} + V_{HYS}$	2.05	2.25	2.45	V
V_{HYS}	Shutdown voltage hysteresis	$V_{SHUTDOWN+} – V_{SHUTDOWN-}$		250		mV

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7.3 Recommended Operating Conditions (continued)

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	PACK, SMBC, SMBD, $\overline{PRES}$, BTP_IN, $\overline{DISP}$			26	V
		TS1, TS2, TS3, TS4			V_{REG}	
		PTC, PTCEN, LEDCNTLA, LEDCNTLB, LEDCNTLC			V_{BAT}	
		SRP, SRN	–0.2		0.2	
		VC4	V_{VC3}		V_{VC3} + 5	
		VC3	V_{VC2}		V_{VC2} + 5	
		VC2	V_{VC1}		V_{VC1} + 5	
		VC1	V_{VSS}		V_{VSS} + 5	
V_O	Output voltage range	CHG, DSG, PCHG, FUSE			26	V
C_{PBI}	External PBI capacitor		2.2			µF
T_{OPR}	Operating temperature		–40		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		BQ40Z50-R2 RSM (QFN) 32 PINS	UNIT
$R_{\theta JA, High K}$	Junction-to-ambient thermal resistance	47.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	40.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.4	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Supply Current

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 20 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{NORMAL}	NORMAL mode	CHG on. DSG on, no Flash write		336		µA
I_{SLEEP}	SLEEP mode	CHG off, DSG on, no SBS communication		75		µA
		CHG off, DSG off, no SBS communication		52		
$I_{SHUTDOWN}$	SHUTDOWN mode			1.6		µA

7.6 Power Supply Control

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{SWITCHOVER-}$	BAT to V_{CC} switchover voltage	$V_{BAT} < V_{SWITCHOVER-}$	1.95	2.1	2.2	V
$V_{SWITCHOVER+}$	V_{CC} to BAT switchover voltage	$V_{BAT} > V_{SWITCHOVER-} + V_{HYS}$	2.9	3.1	3.25	V

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7.6 Power Supply Control (continued)

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{HYS}	Switchover voltage hysteresis	$V_{SWITCHOVER+}$ – $V_{SWITCHOVER-}$		1000		mV
I_{LKG}	Input Leakage current	BAT pin, BAT = 0 V, VCC = 25 V, PACK = 25 V			1	µA
		PACK pin, BAT = 25 V, VCC = 0 V, PACK = 0 V			1	
		BAT and PACK terminals, BAT = 0 V, VCC = 0 V, PACK = 0 V, PBI = 25 V			1	

7.7 AFE Power-On Reset

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REGIT-}	Negative-going voltage input	V_{REG}	1.51	1.55	1.59	V
V_{HYS}	Power-on reset hysteresis	V_{REGIT+} – V_{REGIT-}	70	100	130	mV
t_{RST}	Power-on reset time		200	300	400	µs

7.8 AFE Watchdog Reset and Wake Timer

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{WDT}	AFE watchdog timeout	t_{WDT} = 500	372	500	628	ms
		t_{WDT} = 1000	744	1000	1256	
		t_{WDT} = 2000	1488	2000	2512	
		t_{WDT} = 4000	2976	4000	5024	
t_{WAKE}	AFE wake timer	t_{WAKE} = 250	186	250	314	ms
		t_{WAKE} = 500	372	500	628	
		t_{WAKE} = 1000	744	1000	1256	
		t_{WAKE} = 512	1488	2000	2512	
t_{FETOFF}	FET off delay after reset	t_{FETOFF} = 512	409	512	614	ms

7.9 Current Wake Comparator

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{WAKE}	Wake voltage threshold	V_{WAKE} = ±0.625 mV	±0.3	±0.625	±0.9	mV
		V_{WAKE} = ±1.25 mV	±0.6	±1.25	±1.8	
		V_{WAKE} = ±2.5 mV	±1.2	±2.5	±3.6	
		V_{WAKE} = ±5 mV	±2.4	±5.0	±7.2	
$V_{WAKE(DRIFT)}$	Temperature drift of V_{WAKE} accuracy			0.5%		°C
t_{WAKE}	Time from application of current to wake interrupt				700	µs

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7.9 Current Wake Comparator (continued)

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{WAKE(SU)}$	Wake comparator startup time			500	1000	µs

7.10 VC1, VC2, VC3, VC4, BAT, PACK

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K	Scaling factor	VC1 – VSS, VC2 – VC1, VC3 – VC2, VC4 – VC3	0.1980	0.2000	0.2020	—
		BAT – VSS, PACK – VSS	0.049	0.050	0.051	
		V_{REF2}	0.490	0.500	0.510	
V_{IN}	Input voltage range	VC1 – VSS, VC2 – VC1, VC3 – VC2, VC4 – VC3	–0.2		5	V
		BAT – VSS, PACK – VSS	–0.2		20	
I_{LKG}	Input leakage current	VC1, VC2, VC3, VC4, cell balancing off, cell detach detection off, ADC multiplexer off			1	µA
R_{CB}	Internal cell balance resistance	$R_{DS(ON)}$ for internal FET switch at 2 V < V_{DS} < 4 V			200	Ω
I_{CD}	Internal cell detach check current	VCx > VSS + 0.8 V	30	50	70	µA

7.11 SMBD, SMBC

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input voltage high	SMBC, SMBD, V_{REG} = 1.8 V	1.3			V
V_{IL}	Input voltage low	SMBC, SMBD, V_{REG} = 1.8 V			0.8	V
V_{OL}	Output low voltage	SMBC, SMBD, V_{REG} = 1.8 V, I_{OL} = 1.5 mA			0.4	V
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	µA
R_{PD}	Pulldown resistance		0.7	1.0	1.3	MΩ

7.12 $\overline{PRES}$, BTP_INT, $\overline{DISP}$

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input		1.3			V
V_{IL}	Low-level input				0.55	V
V_{OH}	Output voltage high	V_{BAT} > 5.5 V, I_{OH} = –0 µA	3.5			V
		V_{BAT} > 5.5 V, I_{OH} = –10 µA	1.8			
V_{OL}	Output voltage low	I_{OL} = 1.5 mA			0.4	V
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	µA
R_O	Output reverse resistance	Between $\overline{PRES}$ or BTP_INT or $\overline{DISP}$ and PBI	8			kΩ

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7.13 LEDCNTLA, LEDCNTLB, LEDCNTLC

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input		1.45			V
V_{IL}	Low-level input				0.55	V
V_{OH}	Output voltage high	V_{BAT} > 3.0 V, I_{OH} = –22.5 mA	V_{BAT} – 1.6			V
V_{OL}	Output voltage low	I_{OL} = 1.5 mA			0.4	V
I_{SC}	High level output current protection		–30	–45	–60	mA
I_{OL}	Low level output current	V_{BAT} > 3.0 V, V_{OH} = 0.4 V	15.75	22.5	29.25	mA
$I_{LEDCNTLx}$	Current matching between LEDCNTLx	V_{BAT} = $V_{LEDCNTLx}$ + 2.5 V		±1%		
C_{IN}	Input capacitance			20		pF
I_{LKG}	Input leakage current				1	µA
$f_{LEDCNTLx}$	Frequency of LED pattern			124		Hz

7.14 Coulomb Counter

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		–0.1		0.1	V
Full scale range		–V_{REF1}/10		V_{REF1}/10	V
Integral nonlinearity(1)	16-bit, best fit over input voltage range		±5.2	±22.3	LSB
Offset error	16-bit, Post-calibration		±5	±10	µV
Offset error drift	15-bit + sign, Post-calibration		0.2	0.3	µV/°C
Gain error	15-bit + sign, over input voltage range		±0.2%	±0.8%	FSR
Gain error drift	15-bit + sign, over input voltage range			150	PPM/°C
Effective input resistance		2.5			MΩ

(1) 1 LSB = $V_{REF1}/(10 \times 2^N) = 1.215/(10 \times 2^{15}) = 3.71$ µV

7.15 CC Digital Filter

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Conversion time	Single conversion		250		ms
Effective resolution	Single conversion	15			Bits

7.16 ADC

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range	Internal reference (V_{REF1})	–0.2		1	V
	External reference (V_{REG})	–0.2		0.8 × V_{REG}	
Full scale range	V_{FS} = V_{REF1} or V_{REG}	–V_{FS}		V_{FS}	V

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7.16 ADC (continued)

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Integral nonlinearity(1)	16-bit, best fit, –0.1 V to 0.8 × V_{REF1}			±6.6	LSB
	16-bit, best fit, –0.2 V to –0.1 V			±13.1	
Offset error(2)	16-bit, Post-calibration, V_{FS} = V_{REF1}		±67	±157	µV
Offset error drift	16-bit, Post-calibration, V_{FS} = V_{REF1}		0.6	3	µV/°C
Gain error	16-bit, –0.1 V to 0.8 × V_{FS}		±0.2%	±0.8%	FSR
Gain error drift	16-bit, –0.1 V to 0.8 × V_{FS}			150	PPM/°C
Effective input resistance		8			MΩ

(1) 1 LSB = $V_{REF1}/(2^N)$ = 1.225/(2^{15}) = 37.4 µV (when t_{CONV} = 31.25 ms)
(2) For VC1 – VSS, VC2 – VC1, VC3 – VC2, VC4 – VC3, VC4 – VSS, PACK – VSS, and V_{REF1}/2, the offset error is multiplied by (1/ADC multiplexer scaling factor (K)).

7.17 ADC Digital Filter

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Conversion time	Single conversion		31.25		ms
	Single conversion		15.63		
	Single conversion		7.81		
	Single conversion		1.95		
Resolution	No missing codes	16			Bits
Effective resolution	With sign, t_{CONV} = 31.25 ms	14	15		Bits
	With sign, t_{CONV} = 15.63 ms	13	14		
	With sign, t_{CONV} = 7.81 ms	11	12		
	With sign, t_{CONV} = 1.95 ms	9	10		

7.18 CHG, DSG FET Drive

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output voltage ratio	$Ratio_{DSG}$ = (V_{DSG} – V_{BAT})/V_{BAT}, 2.2 V < V_{BAT} < 4.92 V, 10 MΩ between PACK and DSG	2.133	2.333	2.433	—
		$Ratio_{CHG}$ = (V_{CHG} – V_{BAT})/V_{BAT}, 2.2 V < V_{BAT} < 4.92 V, 10 MΩ between BAT and CHG	2.133	2.333	2.433	
$V_{(FETON)}$	Output voltage, CHG and DSG on	$V_{DSG(ON)}$ = V_{DSG} – V_{BAT}, V_{BAT} ≥ 4.92 V, 10 MΩ between PACK and DSG, V_{BAT} = 18 V	10.5	11.5	12	V
		$V_{CHG(ON)}$ = V_{CHG} – V_{BAT}, V_{BAT} ≥ 4.92 V, 10 MΩ between BAT and CHG, V_{BAT} = 18 V	10.5	11.5	12	
$V_{(FETOFF)}$	Output voltage, CHG and DSG off	$V_{DSG(OFF)}$ = V_{DSG} – V_{PACK}, 10 MΩ between PACK and DSG	–0.4		0.4	V
		$V_{CHG(OFF)}$ = V_{CHG} – V_{BAT}, 10 MΩ between BAT and CHG	–0.4		0.4	

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7.18 CHG, DSG FET Drive (continued)

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time	V_{DSG} from 0% to 35% $V_{DSG\ (ON)(TYP)}$, $V_{BAT} \geq$ 2.2 V, C_L = 4.7 nF between DSG and PACK, 5.1 kΩ between DSG and C_L, 10 MΩ between PACK and DSG		200	500	µs
		V_{CHG} from 0% to 35% $V_{CHG\ (ON)(TYP)}$, $V_{BAT} \geq$ 2.2 V, C_L = 4.7 nF between CHG and BAT, 5.1 kΩ between CHG and C_L, 10 MΩ between BAT and CHG		200	500	
t_F	Fall time	V_{DSG} from $V_{DSG(ON)(TYP)}$ to 1 V, $V_{BAT} \geq$ 2.2 V, C_L = 4.7 nF between DSG and PACK, 5.1 kΩ between DSG and C_L, 10 MΩ between PACK and DSG		40	300	µs
		V_{CHG} from $V_{CHG(ON)(TYP)}$ to 1 V, $V_{BAT} \geq$ 2.2 V, C_L = 4.7 nF between CHG and BAT, 5.1 kΩ between CHG and C_L, 10 MΩ between BAT and CHG		40	200	

7.19 PCHG FET Drive

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(FETON)}$	Output voltage, PCHG on	$V_{PCHG(ON)}$ = VV_{CC} – V_{PCHG}, 10 MΩ between V_{CC} and PCHG	6	7	8	V
$V_{(FETOFF)}$	Output voltage, PCHG off	$V_{PCHG(OFF)}$ = VV_{CC} – V_{PCHG}, 10 MΩ between V_{CC} and PCHG	–0.4		0.4	V
t_R	Rise time	V_{PCHG} from 10% to 90% $V_{PCHG(ON)(TYP)}$, $VV_{CC} \geq$ 8 V, C_L = 4.7 nF between PCHG and V_{CC}, 5.1 kΩ between PCHG and C_L, 10 MΩ between V_{CC} and CHG		40	200	µs
t_F	Fall time	V_{PCHG} from 90% to 10% $V_{PCHG(ON)(TYP)}$, $V_{CC} \geq$ 8 V, C_L = 4.7 nF between PCHG and V_{CC}, 5.1 kΩ between PCHG and C_L, 10 MΩ between V_{CC} and CHG		40	200	µs

7.20 FUSE Drive

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output voltage high	$V_{BAT} \geq$ 8 V, C_L = 1 nF, $I_{AFEFUSE}$ = 0 µA	6	7	8.65	V
		V_{BAT} < 8 V, C_L = 1 nF, $I_{AFEFUSE}$ = 0 µA	V_{BAT} – 0.1		V_{BAT}	
V_{IH}	High-level input		1.5	2.0	2.5	V
$I_{AFEFUSE(PU)}$	Internal pullup current	$V_{BAT} \geq$ 8 V, $V_{AFEFUSE}$ = VSS		150	330	nA
$R_{AFEFUSE}$	Output impedance		2	2.6	3.2	kΩ
C_{IN}	Input capacitance			5		pF
t_{DELAY}	Fuse trip detection delay		128		256	µs
t_{RISE}	Fuse output rise time	$V_{BAT} \geq$ 8 V, C_L = 1 nF, V_{OH} = 0 V to 5 V		5	20	µs

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7.21 Internal Temperature Sensor

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TEMP}	Internal temperature sensor voltage drift	V_{TEMPP}	–1.9	–2.0	–2.1	mV/°C
		V_{TEMPP} – V_{TEMPN}, assured by design	0.177	0.178	0.179	

7.22 TS1, TS2, TS3, TS4

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	TS1, TS2, TS3, TS4, V_{BIAS} = V_{REF1}	–0.2		0.8 × V_{REF1}	V
		TS1, TS2, TS3, TS4, V_{BIAS} = V_{REG}	–0.2		0.8 × V_{REG}	
$R_{NTC(PU)}$	Internal pullup resistance	TS1, TS2, TS3, TS4	14.4	18	21.6	kΩ
$R_{NTC(DRIFT)}$	Resistance drift over temperature	TS1, TS2, TS3, TS4	–360	–280	–200	PPM/°C

7.23 PTC, PTCEN

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{PTC(TRIP)}$	PTC trip resistance		1.2	2.5	3.95	MΩ
$V_{PTC(TRIP)}$	PTC trip voltage	$V_{PTC(TRIP)}$ = V_{PTCEN} – V_{PTC}	200	500	890	mV
I_{PTC}	Internal PTC current bias	T_A = –40°C to 110°C	200	290	350	nA
$t_{PTC(DELAY)}$	PTC delay time	T_A = –40°C to 110°C	40	80	145	ms

7.24 Internal 1.8-V LDO

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG}	Regulator voltage		1.6	1.8	2.0	V
$\Delta V_{O(TEMP)}$	Regulator output over temperature	$\Delta V_{REG}/\Delta T_A$, I_{REG} = 10 mA		±0.25%		
$\Delta V_{O(LINE)}$	Line regulation	$\Delta V_{REG}/\Delta V_{BAT}$, V_{BAT} = 10 mA	–0 .6%		0.5%	
$\Delta V_{O(LOAD)}$	Load regulation	$\Delta V_{REG}/\Delta I_{REG}$, I_{REG} = 0 mA to 10 mA	–1.5%		1.5%	
I_{REG}	Regulator output current limit	V_{REG} = 0.9 × $V_{REG(NOM)}$, V_{IN} > 2.2 V	20			mA
I_{SC}	Regulator short-circuit current limit	V_{REG} = 0 × $V_{REG(NOM)}$	25	40	55	mA
$PSRR_{REG}$	Power supply rejection ratio	$\Delta V_{BAT}/\Delta V_{REG}$, I_{REG} = 10 mA ,V_{IN} > 2.5 V, f = 10 Hz		40		dB
V_{SLEW}	Slew rate enhancement voltage threshold	V_{REG}	1.58	1.65		V

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7.25 High-Frequency Oscillator

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{HFO}	Operating frequency			16.78		MHz
$f_{HFO(ERR)}$	Frequency error	T_A = –20°C to 70°C, includes frequency drift	–2.5%	±0.25%	2.5%	
		T_A = –40°C to 85°C, includes frequency drift	–3.5%	±0.25%	3.5%	
$t_{HFO(SU)}$	Start-up time	T_A = –20°C to 85°C, oscillator frequency within +/–3% of nominal			4	ms
		oscillator frequency within +/–3% of nominal			100	µs

7.26 Low-Frequency Oscillator

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LFO}	Operating frequency			262.144		kHz
$f_{LFO(ERR)}$	Frequency error	T_A = –20°C to 70°C, includes frequency drift	–1.5%	±0.25%	1.5%	
		T_A = –40°C to 85°C, includes frequency drift	–2.5	±0.25	2.5	
$f_{LFO(FAIL)}$	Failure detection frequency		30	80	100	kHz

7.27 Voltage Reference 1

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF1}	Internal reference voltage	T_A = 25°C, after trim	1.21	1.215	1.22	V
$V_{REF1(DRIFT)}$	Internal reference voltage drift	T_A = 0°C to 60°C, after trim		±50		PPM/°C
		T_A = –40°C to 85°C, after trim		±80		

7.28 Voltage Reference 2

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF2}	Internal reference voltage	T_A = 25°C, after trim	1.22	1.225	1.23	V
$V_{REF2(DRIFT)}$	Internal reference voltage drift	T_A = 0°C to 60°C, after trim		±50		PPM/°C
		T_A = –40°C to 85°C, after trim		±80		

7.29 Instruction Flash

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention		10			Years
	Flash programming write cycles		1000			Cycles
$t_{PROGWORD}$	Word programming time	T_A = –40°C to 85°C			40	µs

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7.29 Instruction Flash (continued)

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{MASSERASE}$	Mass-erase time	T_A = –40°C to 85°C			40	ms
$t_{PAGEERASE}$	Page-erase time	T_A = –40°C to 85°C			40	ms
$I_{FLASHREAD}$	Flash-read current	T_A = –40°C to 85°C			2	mA
$I_{FLASHWRITE}$	Flash-write current	T_A = –40°C to 85°C			5	mA
$I_{FLASHERASE}$	Flash-erase current	T_A = –40°C to 85°C			15	mA

7.30 Data Flash

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention		10			Years
	Flash programming write cycles		20000			Cycles
$t_{PROGWORD}$	Word programming time	T_A = –40°C to 85°C			40	µs
$t_{MASSERASE}$	Mass-erase time	T_A = –40°C to 85°C			40	ms
$t_{PAGEERASE}$	Page-erase time	T_A = –40°C to 85°C			40	ms
$I_{FLASHREAD}$	Flash-read current	T_A = –40°C to 85°C			1	mA
$I_{FLASHWRITE}$	Flash-write current	T_A = –40°C to 85°C			5	mA
$I_{FLASHERASE}$	Flash-erase current	T_A = –40°C to 85°C			15	mA

7.31 OLD, SCC, SCD1, SCD2 Current Protection Thresholds

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OLD}	OLD detection threshold voltage range	V_{OLD} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 1	–16.6		–100	mV
		V_{OLD} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 0	–8.3		–50	
ΔV_{OLD}	OLD detection threshold voltage program step	V_{OLD} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 1		–5.56		mV
		V_{OLD} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 0		–2.78		
V_{SCC}	SCC detection threshold voltage range	V_{SCC} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 1	44.4		200	mV
		V_{SCC} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 0	22.2		100	
ΔV_{SCC}	SCC detection threshold voltage program step	V_{SCC} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 1		22.2		mV
		V_{SCC} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 0		11.1		
V_{SCD1}	SCD1 detection threshold voltage range	V_{SCD1} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 1	–44.4		–200	mV
		V_{SCD1} = V_{SRP} – V_{SRN}, AFE PROTECTION CONTROL[RSNS] = 0	–22.2		–100	

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7.31 OLD, SCC, SCD1, SCD2 Current Protection Thresholds (continued)

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_{SCD1}	SCD1 detection threshold voltage program step	$V_{SCD1} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 1		–22.2		mV
		$V_{SCD1} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 0		–11.1		
V_{SCD2}	SCD2 detection threshold voltage range	$V_{SCD2} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 1	–44.4		–200	mV
		$V_{SCD2} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 0	–22.2		–100	
ΔV_{SCD2}	SCD2 detection threshold voltage program step	$V_{SCD2} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 1		–22.2		mV
		$V_{SCD2} = V_{SRP} – V_{SRN}$, AFE PROTECTION CONTROL[RSNS] = 0		–11.1		
V_{OFFSET}	OLD, SCC, and SCDx offset error	Post-trim	–2.5		2.5	mV
V_{SCALE}	OLD, SCC, and SCDx scale error	No trim	–10%		10%	—
		Post-trim	–5%		5%	

7.32 Timing Requirements: OLD, SCC, SCD1, SCD2 Current Protection Timing

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
t_{OLD}	OLD detection delay time		1		31	ms
Δt_{OLD}	OLD detection delay time program step			2		ms
t_{SCC}	SCC detection delay time		0		915	µs
Δt_{SCC}	SCC detection delay time program step			61		µs
t_{SCD1}	SCD1 detection delay time	AFE PROTECTION CONTROL[SCDDx2] = 0	0		915	µs
		AFE PROTECTION CONTROL[SCDDx2] = 1	0		1850	
Δt_{SCD1}	SCD1 detection delay time program step	AFE PROTECTION CONTROL[SCDDx2] = 0		61		µs
		AFE PROTECTION CONTROL[SCDDx2] = 1		121		
t_{SCD2}	SCD2 detection delay time	AFE PROTECTION CONTROL[SCDDx2] = 0	0		458	µs
		AFE PROTECTION CONTROL[SCDDx2] = 1	0		915	
Δt_{SCD2}	SCD2 detection delay time program step	AFE PROTECTION CONTROL[SCDDx2] = 0		30.5		µs
		AFE PROTECTION CONTROL[SCDDx2] = 1		61		
t_{DETECT}	Current fault detect time	$V_{SRP} – V_{SRN} = V_T – 3$ mV for OLD, SCD1, and SC2, $V_{SRP} – V_{SRN} = V_T + 3$ mV for SCC			160	µs
t_{ACC}	Current fault delay time accuracy	Max delay setting	–10%		10%	

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7.33 Timing Requirements: SMBus

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
f_{SMB}	SMBus operating frequency	SLAVE mode, SMBC 50% duty cycle	10		100	kHz
f_{MAS}	SMBus master clock frequency	MASTER mode, no clock low slave extend		51.2		kHz
t_{BUF}	Bus free time between start and stop		4.7			µs
$t_{HD(START)}$	Hold time after (repeated) start		4.0			µs
$t_{SU(START)}$	Repeated start setup time		4.7			µs
$t_{SU(STOP)}$	Stop setup time		4.0			µs
$t_{HD(DATA)}$	Data hold time		300			ns
$t_{SU(DATA)}$	Data setup time		250			ns
$t_{TIMEOUT}$	Error signal detect time		25		35	ms
t_{LOW}	Clock low period		4.7			µs
t_{HIGH}	Clock high period		4.0		50	µs
t_R	Clock rise time	10% to 90%			1000	ns
t_F	Clock fall time	90% to 10%			300	ns
$t_{LOW(SEXT)}$	Cumulative clock low slave extend time				25	ms
$t_{LOW(MEXT)}$	Cumulative clock low master extend time				10	ms

7.34 Timing Requirements: SMBus XL

Typical values stated where T_A = 25°C and VCC = 14.4 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 26 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
f_{SMBXL}	SMBus XL operating frequency	SLAVE mode	40		400	kHz
t_{BUF}	Bus free time between start and stop		4.7			µs
$t_{HD(START)}$	Hold time after (repeated) start		4.0			µs
$t_{SU(START)}$	Repeated start setup time		4.7			µs
$t_{SU(STOP)}$	Stop setup time		4.0			µs
$t_{TIMEOUT}$	Error signal detect time		5		20	ms
t_{LOW}	Clock low period				20	µs
t_{HIGH}	Clock high period				20	µs

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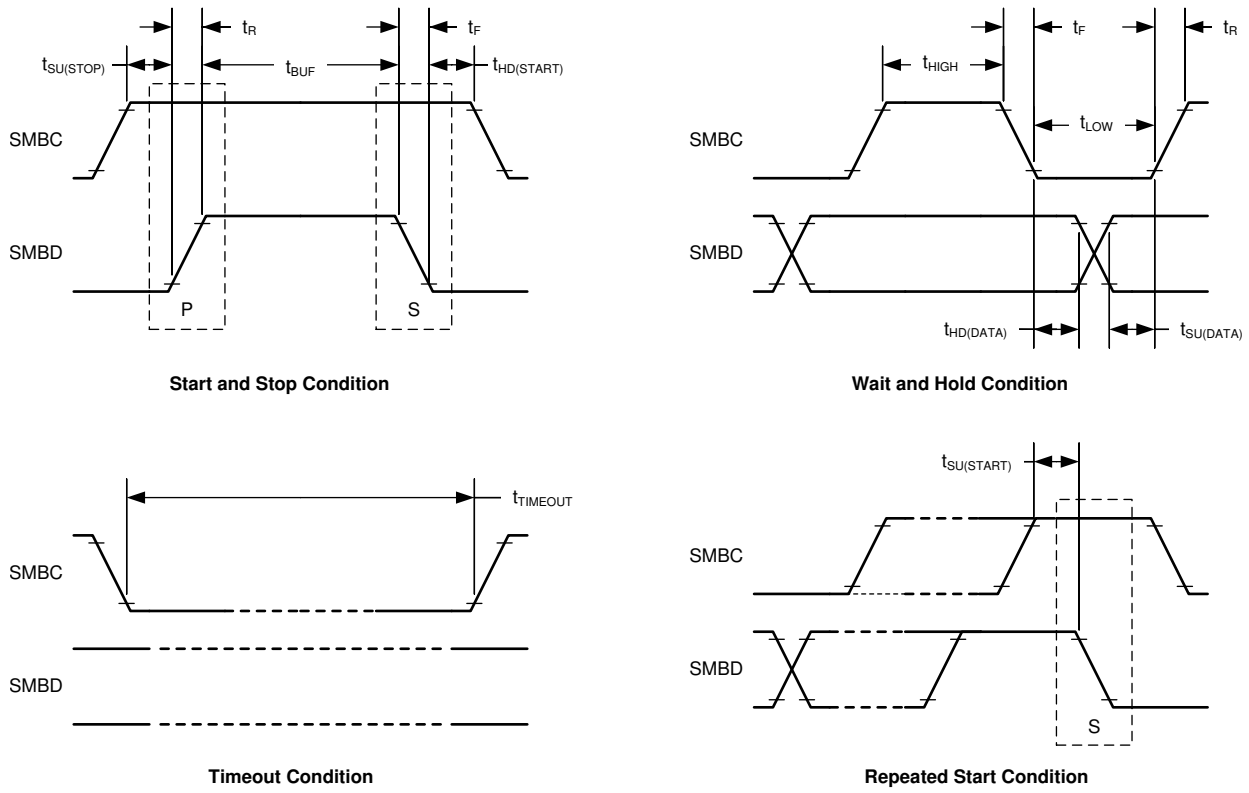


图 7-1. SMBus Timing Diagram

7.35 Typical Characteristics

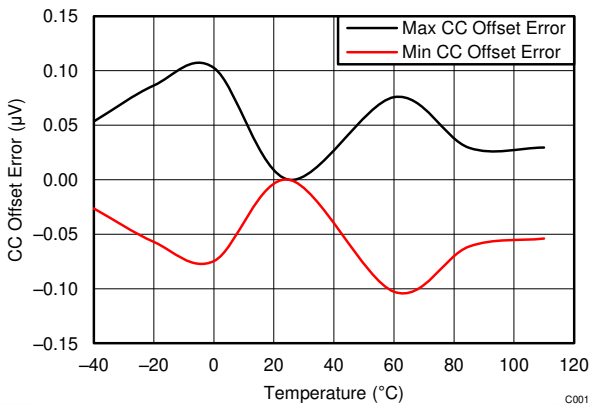


图 7-2. CC Offset Error vs. Temperature

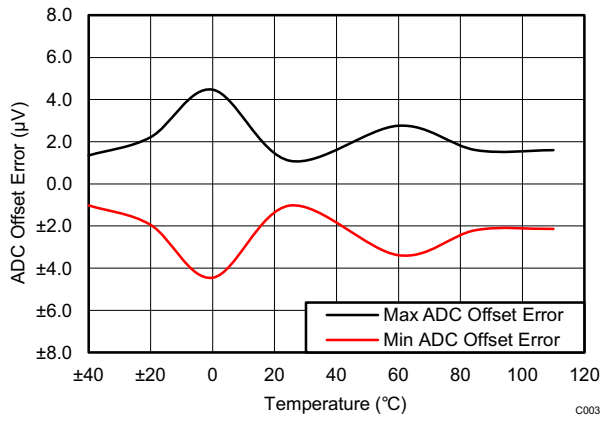


图 7-3. ADC Offset Error vs. Temperature

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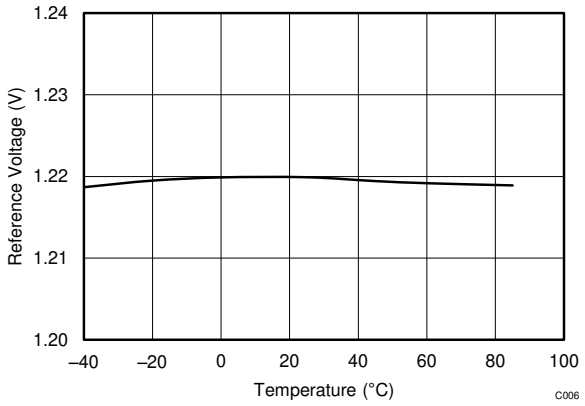


图 7-4. Reference Voltage vs. Temperature

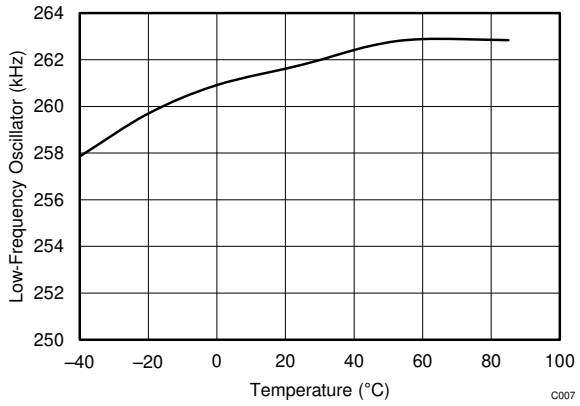


图 7-5. Low-Frequency Oscillator vs. Temperature

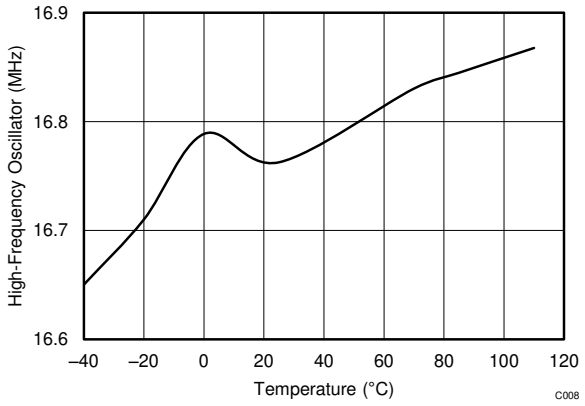
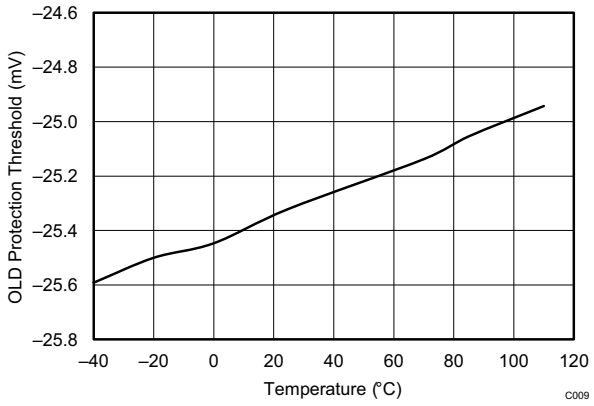
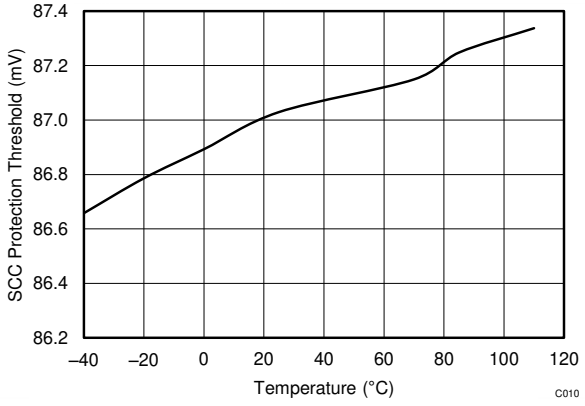


图 7-6. High-Frequency Oscillator vs. Temperature



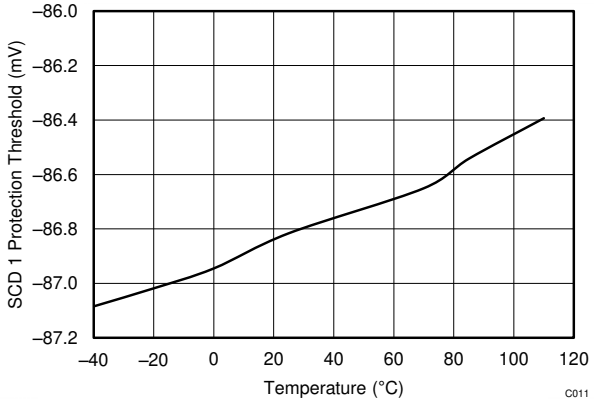
Threshold setting is –25 mV.

图 7-7. Overcurrent Discharge Protection Threshold vs. Temperature



Threshold setting is 88.85 mV.

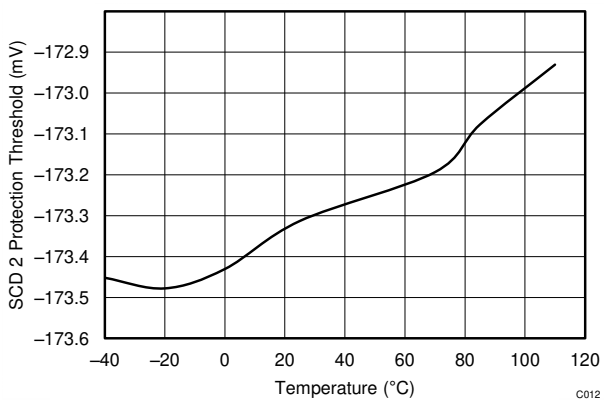
图 7-8. Short Circuit Charge Protection Threshold vs. Temperature



Threshold setting is –88.85 mV.

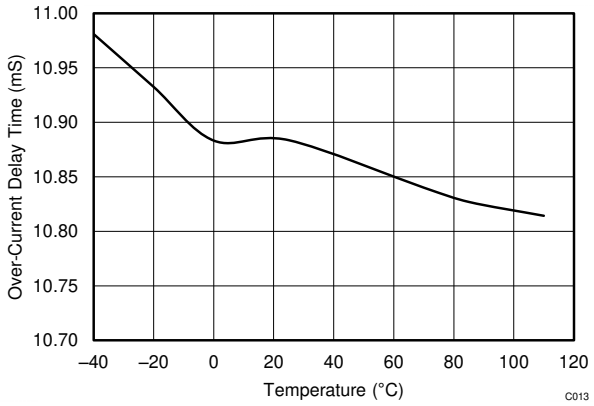
图 7-9. Short Circuit Discharge 1 Protection Threshold vs. Temperature

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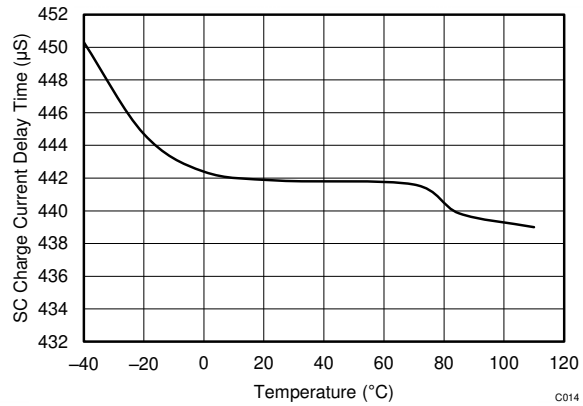
Threshold setting is – 177.7 mV.

图 7-10. Short Circuit Discharge 2 Protection Threshold vs. Temperature



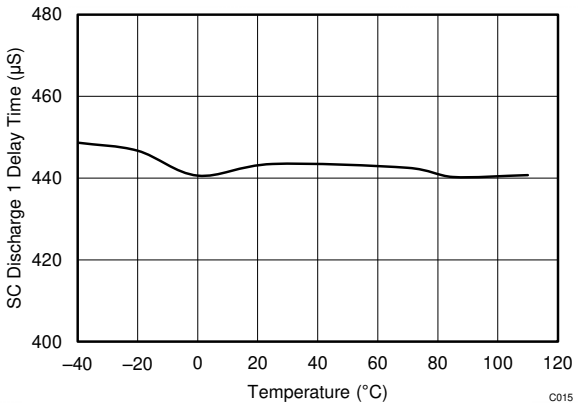
Threshold setting is 11 ms.

图 7-11. Overcurrent Delay Time vs. Temperature



Threshold setting is 465 µs.

图 7-12. Short Circuit Charge Current Delay Time vs. Temperature



Threshold setting is 465 µs (including internal delay).

图 7-13. Short Circuit Discharge 1 Delay Time vs. Temperature

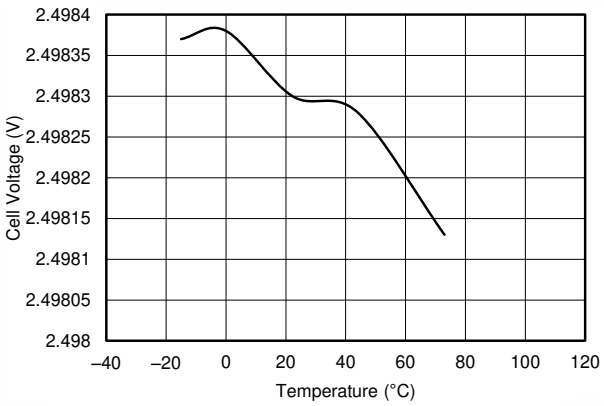
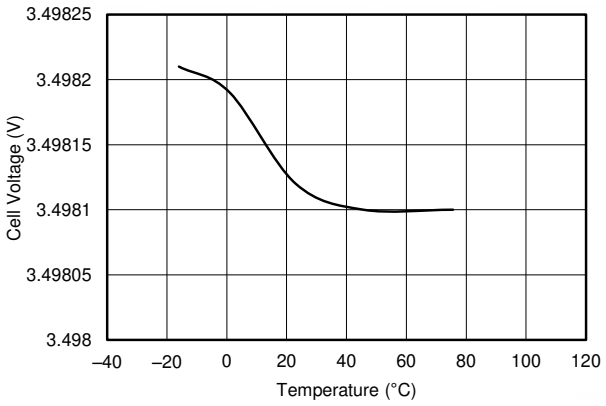


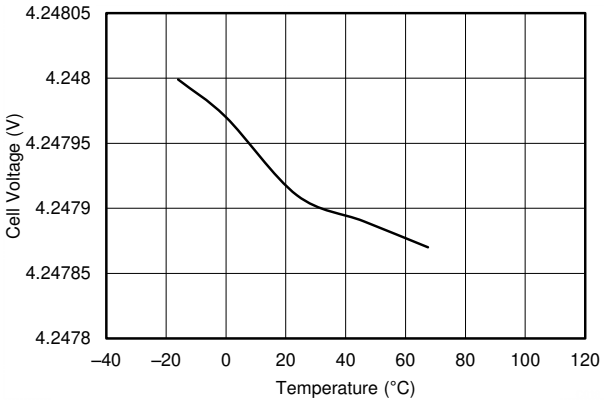
图 7-14. V_{CELL} Measurement at 2.5-V vs. Temperature



This is the V_{CELL} average for single cell.

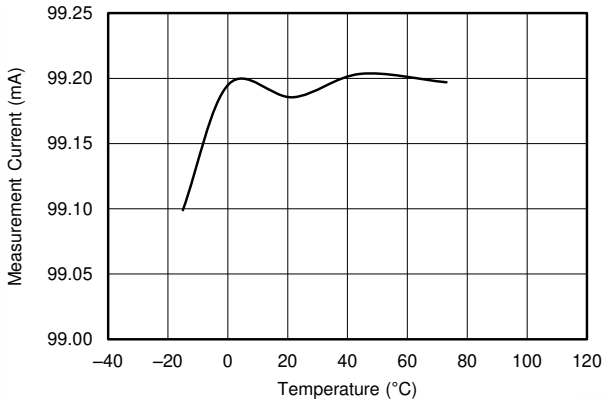
图 7-15. V_{CELL} Measurement at 3.5-V vs. Temperature

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This is the V_{CELL} average for single cell.

图 7-16. V_{CELL} Measurement at 4.25-V vs. Temperature



I_{SET} = 100 mA

图 7-17. I measured vs. Temperature

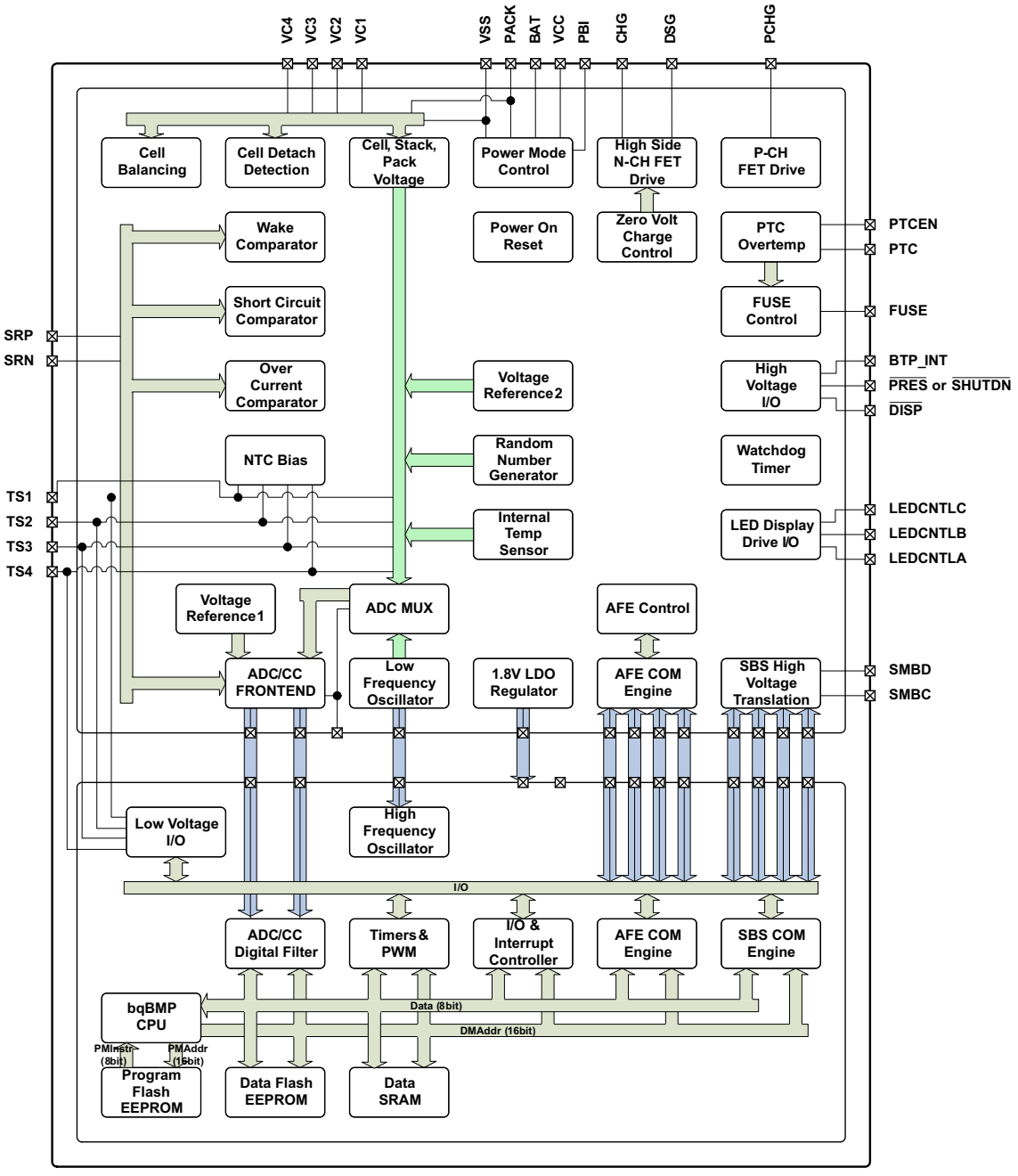
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8 Detailed Description

8.1 Overview

The BQ40Z50-R2 device, incorporating patented Impedance Track™ technology, provides cell balancing while charging or at rest. This fully integrated, single-chip, pack-based solution, including a diagnostic lifetime data monitor and black box recorder, provides a rich array of features for gas gauging, protection, and authentication for 1-series, 2-series, 3-series, and 4-series cell Li-ion and Li-polymer battery packs.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Primary (1st Level) Safety Features

The BQ40Z50-R2 supports a wide range of battery and system protection features that can easily be configured. See the *BQ40Z50-R2 Technical Reference Manual* (SLUUBK0) for detailed descriptions of each protection function.

The primary safety features include:

- Cell Overvoltage Protection
- Cell Undervoltage Protection
- Cell Undervoltage Protection Compensated
- Overcurrent in Charge Protection
- Overcurrent in Discharge Protection
- Overload in Discharge Protection
- Short Circuit in Charge Protection
- Short Circuit in Discharge Protection
- Overtemperature in Charge Protection
- Overtemperature in Discharge Protection
- Undertemperature in Charge Protection
- Undertemperature in Discharge Protection
- Overtemperature FET protection
- Precharge Timeout Protection
- Host Watchdog Timeout Protection
- Fast Charge Timeout Protection
- Overcharge Protection
- Overcharging Voltage Protection
- Overcharging Current Protection
- Over Precharge Current Protection

8.3.2 Secondary (2nd Level) Safety Features

The secondary safety features of the BQ40Z50-R2 can be used to indicate more serious faults via the FUSE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. See the *BQ40Z50-R2 Technical Reference Manual* (SLUUBK0) for detailed descriptions of each protection function.

The secondary safety features provide protection against:

- Safety Overvoltage Permanent Failure
- Safety Undervoltage Permanent Failure
- Safety Overtemperature Permanent Failure
- Safety FET Overtemperature Permanent Failure
- Qmax Imbalance Permanent Failure
- Impedance Imbalance Permanent Failure
- Capacity Degradation Permanent Failure
- Cell Balancing Permanent Failure
- Fuse Failure Permanent Failure
- PTC Permanent Failure
- Voltage Imbalance At Rest Permanent Failure
- Voltage Imbalance Active Permanent Failure
- Charge FET Permanent Failure
- Discharge FET Permanent Failure
- AFE Register Permanent Failure
- AFE Communication Permanent Failure

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- Second Level Protector Permanent Failure
- Instruction Flash Checksum Permanent Failure
- Open Cell Connection Permanent Failure
- Data Flash Permanent Failure
- Open Thermistor Permanent Failure

8.3.3 Charge Control Features

The BQ40Z50-R2 charge control features include:

- Supports JEITA temperature ranges. Reports charging voltage and charging current according to the active temperature range
- Handles more complex charging profiles. Allows for splitting the standard temperature range into two sub-ranges and allows for varying the charging current according to the cell voltage
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts
- Reduces the charge difference of the battery cells in a fully charged state of the battery pack gradually using a voltage-based cell balancing algorithm during charging. A voltage threshold can be set up for cell balancing to be active. This prevents fully charged cells from overcharging and causing excessive degradation and also increases the usable pack energy by preventing premature charge termination.
- Supports precharging/0-volt charging
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicates charge status via charge and discharge alarms

8.3.4 Gas Gauging

The BQ40Z50-R2 uses the Impedance Track algorithm to measure and calculate the available capacity in battery cells. The BQ40Z50-R2 accumulates a measure of charge and discharge currents and compensates the charge current measurement for the temperature and state-of-charge of the battery. The BQ40Z50-R2 estimates self-discharge of the battery and also adjusts the self-discharge estimation based on temperature. The device also has TURBO Mode 2.0 support, which enables the BQ40Z50-R2 to provide the necessary data for the MCU to determine what level of peak power consumption can be applied without causing a system reset or transient battery voltage level spike to trigger termination flags. See the *BQ40Z50-R2 Technical Reference Manual* (SLUUBK0) for further details.

8.3.5 Configuration

8.3.5.1 Oscillator Function

The BQ40Z50-R2 fully integrates the system oscillators and does not require any external components to support this feature.

8.3.5.2 System Present Operation

The BQ40Z50-R2 checks the $\overline{\text{PRES}}$ pin periodically (1 s). If $\overline{\text{PRES}}$ input is pulled to ground by the external system, the BQ40Z50-R2 detects this as system present.

8.3.5.3 Emergency Shutdown

For battery maintenance, the emergency shutdown feature enables a push button action connecting the $\overline{\text{SHUTDN}}$ pin to shut down an embedded battery pack system before removing the battery. A high-to-low transition of the $\overline{\text{SHUTDN}}$ pin signals the BQ40Z50-R2 to turn off the CHG and DSG FETs, disconnecting the power from the system to safely remove the battery pack. The CHG and DSG FETs can be turned on again by another high-to-low transition detected by the $\overline{\text{SHUTDN}}$ pin or when a data flash configurable timeout is reached.

8.3.5.4 1-Series, 2-Series, 3-Series, or 4-Series Cell Configuration

In a 1-series cell configuration, VC4 is shorted to VC, VC2, and VC1. In a 2-series cell configuration, VC4 is shorted to VC3 and VC2. In a 3-series cell configuration, VC4 is shorted to VC3.

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8.3.5.5 Cell Balancing

The device supports cell balancing by bypassing the current of each cell during charging or at rest. If the device's internal bypass is used, up to 10 mA can be bypassed and multiple cells can be bypassed at the same time. Higher cell balance current can be achieved by using an external cell balancing circuit. In external cell balancing mode, only one cell at a time can be balanced.

The cell balancing algorithm determines the amount of charge needed to be bypassed to balance the capacity of all cells.

8.3.6 Battery Parameter Measurements

8.3.6.1 Charge and Discharge Counting

The BQ40Z50-R2 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage and temperature measurement.

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SRP and SRN terminals. The integrating ADC measures bipolar signals from –0.1 V to 0.1 V. The BQ40Z50-R2 detects charge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is positive, and discharge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is negative. The BQ40Z50-R2 continuously integrates the signal over time, using an internal counter. The fundamental rate of the counter is 0.26 nVh.

8.3.7 Battery Trip Point (BTP)

Required for WIN8 OS, the battery trip point (BTP) feature indicates when the RSOC of a battery pack has depleted to a certain value set in a DF register. This feature enables a host to program two capacity-based thresholds that govern the triggering of a BTP interrupt on the BTP_INT pin, and the setting or clearing of the *OperationStatus[BTP_INT]* on the basis of *RemainingCapacity()*.

An internal weak pullup is applied when the BTP feature is active. Depending on the system design, an external pullup may be required to put on the BTP_INT pin. See 节 *7.12* for details.

8.3.8 Lifetime Data Logging Features

The BQ40Z50-R2 offers lifetime data logging for several critical battery parameters. The following parameters are updated every 10 hours if a difference is detected between values in RAM and data flash:

- Maximum and Minimum Cell Voltages
- Maximum Delta Cell Voltage
- Maximum Charge Current
- Maximum Discharge Current
- Maximum Average Discharge Current
- Maximum Average Discharge Power
- Maximum and Minimum Cell Temperature
- Maximum Delta Cell Temperature
- Maximum and Minimum Internal Sensor Temperature
- Maximum FET Temperature
- Number of Safety Events Occurrences and the Last Cycle of the Occurrence
- Number of Valid Charge Termination and the Last Cycle of the Valid Charge Termination
- Number of Qmax and Ra Updates and the Last Cycle of the Qmax and Ra Updates
- Number of Shutdown Events
- Cell Balancing Time for Each Cell

  (This data is updated every 2 hours if a difference is detected.)
- Total FW Runtime and Time Spent in Each Temperature Range

  (This data is updated every 2 hours if a difference is detected.)

8.3.9 Authentication

The BQ40Z50-R2 supports authentication by the host using SHA-1.

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8.3.10 LED Display

The BQ40Z50-R2 can drive a 3-, 4-, or 5- segment LED display for remaining capacity indication and/or a permanent fail (PF) error code indication.

8.3.11 IATA Support

The BQ40Z50-R2 supports IATA with several new commands and procedures. See the *BQ40Z50-R2 Technical Reference Manual* (SLUUBK0) for further details.

8.3.12 Voltage

The BQ40Z50-R2 updates the individual series cell voltages at 0.25-s intervals. The internal ADC of the BQ40Z50-R2 measures the voltage, and scales and calibrates it appropriately. This data is also used to calculate the impedance of the cell for the Impedance Track gas gauging.

8.3.13 Current

The BQ40Z50-R2 uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a 1-mΩ to 3-mΩ typ. sense resistor.

8.3.14 Temperature

The BQ40Z50-R2 has an internal temperature sensor and inputs for four external temperature sensors. All five temperature sensor options can be individually enabled and configured for cell or FET temperature usage. Two configurable thermistor models are provided to allow the monitoring of cell temperature in addition to FET temperature, which use a different thermistor profile.

8.3.15 Communications

The BQ40Z50-R2 uses SMBus v1.1 with MASTER mode and packet error checking (PEC) options per the SBS specification.

8.3.15.1 SMBus On and Off State

The BQ40Z50-R2 detects an SMBus off state when SMBC and SMBD are low for two or more seconds. Clearing this state requires that either SMBC or SMBD transition high. The communication bus will resume activity within 1 ms.

8.3.15.2 SBS Commands

See the *BQ40Z50-R2 Technical Reference Manual* (SLUUBK0) for further details.

8.4 Device Functional Modes

The BQ40Z50-R2 supports three power modes to reduce power consumption:

- In NORMAL mode, the BQ40Z50-R2 performs measurements, calculations, protection decisions, and data updates in 250-ms intervals. Between these intervals, the BQ40Z50-R2 is in a reduced power stage.
- In SLEEP mode, the BQ40Z50-R2 performs measurements, calculations, protection decisions, and data updates in adjustable time intervals. Between these intervals, the BQ40Z50-R2 is in a reduced power stage. The BQ40Z50-R2 has a wake function that enables exit from SLEEP mode when current flow or failure is detected.
- In SHUTDOWN mode, the BQ40Z50-R2 is completely disabled.

See the *BQ40Z50-R2 Technical Reference Manual* (SLUUBK0) for further details.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The BQ40Z50-R2 is a gas gauge with primary protection support, and can be used with 1-series to 4-series Li-ion/Li-polymer battery packs. To implement and design a comprehensive set of parameters for a specific battery pack, users need the Battery Management Studio (BQSTUDIO) graphical user-interface tool installed on a PC during development. The firmware installed on the BQSTUDIO tool has default values for this product, which are summarized in the *BQ40Z50-R2 Technical Reference Manual* (SLUUBK0). Using the BQSTUDIO tool, these default values can be changed to cater to specific application requirements during development once the system parameters, such as fault trigger thresholds for protection, enable/disable of certain features for operation, configuration of cells, chemistry that best matches the cell used, and more are known. This data is referred to as the "golden image."

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9.2 Typical Applications

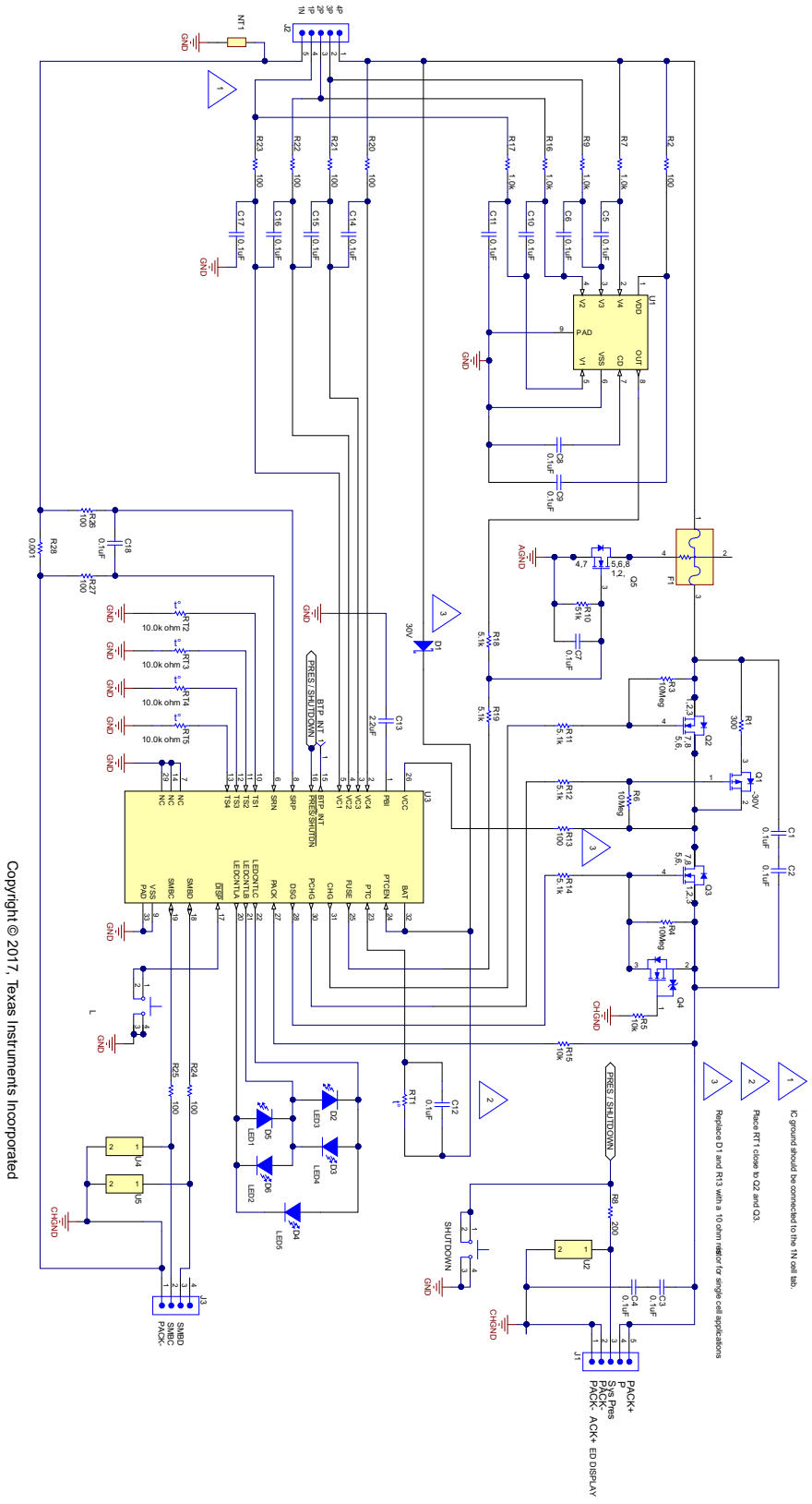


图 9-1. Application Schematic

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9.2.1 Design Requirements

表 9-1 shows the default settings for the main parameters. Use the BQSTUDIO tool to update the settings to meet the specific application or battery pack configuration requirements.

The device should be calibrated before any gauging test. Follow the procedures on the BQSTUDIO **Calibration** page to calibrate the device, and use the information on the BQSTUDIO **Chemistry** page to update the match chemistry profile to the device.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE
Cell Configuration	3s1p (3-series with 1 parallel)(1)
Design Capacity	4400 mAh
Device Chemistry	1210 ($LiCoO_2$/graphitized carbon)
Cell Overvoltage at Standard Temperature	4300 mV
Cell Undervoltage	2500 mV
Shutdown Voltage	2300 mV
Overcurrent in CHARGE Mode	6000 mA
Overcurrent in DISCHARGE Mode	– 6000 mA
Short Circuit in CHARGE Mode	0.1 V/Rsense across SRP, SRN
Short Circuit in DISCHARGE Mode	0.1 V/Rsense across SRP, SRN
Safety Overvoltage	4500 mV
Cell Balancing	Disabled
Internal and External Temperature Sensor	External temperature sensor is used.
Undertemperature Charging	0°C
Undertemperature Discharging	0°C
BROADCAST Mode	Disabled
Battery Trip Point (BTP) with active high interrupt	Disabled

(1) When using the device the first time and if a 1-s or 2-s battery pack is used, then a charger or power supply should be connected to the PACK+ terminal to prevent device shutdown. Then update the cell configuration (see the *BQ40Z50-R2 Technical Reference Manual* [SLUUBK0] for details) before removing the charger connection.

9.2.2 Detailed Design Procedure

9.2.2.1 High-Current Path

The high-current path begins at the PACK+ terminal of the battery pack. As charge current travels through the pack, it finds its way through protection FETs, a chemical fuse, the Li-ion cells and cell connections, and the sense resistor, and then returns to the PACK – terminal (see 图 9-2). In addition, some components are placed across the PACK+ and PACK – terminals to reduce effects from electrostatic discharge.

9.2.2.1.1 Protection FETs

Select the N-channel charge and discharge FETs for a given application. Most portable battery applications are a good match for the CSD17308Q3. The TI CSD17308Q3 is a 47A, 30-V device with Rds(on) of 8.2 mΩ when the gate drive voltage is 8 V.

If a precharge FET is used, R1 is calculated to limit the precharge current to the desired rate. Be sure to account for the power dissipation of the series resistor. The precharge current is limited to ($V_{CHARGER}$ – V_{BAT})/R1 and maximum power dissipation is ($V_{charger}$ – V_{bat})^2/R1.

The gates of all protection FETs are pulled to the source with a high-value resistor between the gate and source to ensure they are turned off if the gate drive is open.

Capacitors C1 and C2 help protect the FETs during an ESD event. Using two devices ensures normal operation if one becomes shorted. To have good ESD protection, the copper trace inductance of the capacitor leads must

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be designed to be as short and wide as possible. Ensure that the voltage ratings of both C1 and C2 are adequate to hold off the applied voltage if one of the capacitors becomes shorted.

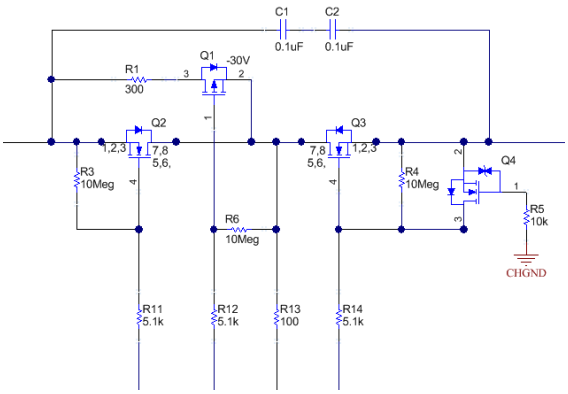


图 9-2. BQ40Z50-R2 Protection FETs

9.2.2.1.2 Chemical Fuse

The chemical fuse (Dexerials, Uchihashi, and so on) is ignited under command from either the bq294700 secondary voltage protection IC or from the FUSE pin of the gas gauge. Either of these events applies a positive voltage to the gate of Q5, shown in 图 9-3, which then sinks current from the third terminal of the fuse, causing it to ignite and open permanently.

It is important to carefully review the fuse specifications and match the required ignition current to that available from the N-channel FET. Ensure that the proper voltage, current, and Rds(on) ratings are used for this device. The fuse control circuit is discussed in detail in *节 9.2.2.2.5*.

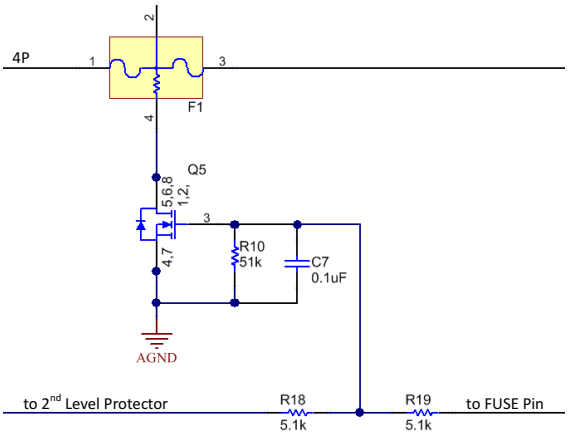


图 9-3. FUSE Circuit

9.2.2.1.3 Li-Ion Cell Connections

For cell connections, it is important to remember that high current flows through the top and bottom connections; therefore, the voltage sense leads at these points must be made with a Kelvin connection to avoid any errors due to a drop in the high-current copper trace. The location marked 4P in 图 9-4 indicates the Kelvin connection of the most positive battery node. The connection marked 1N is equally important. The VC5 pin (a ground reference for cell voltage measurement), which is in the older generation devices, is not in the BQ40Z50-R2 device. Therefore, the single-point connection at 1N to the low-current ground is needed to avoid an unwanted voltage drop through long traces while the gas gauge is measuring the bottom cell voltage.

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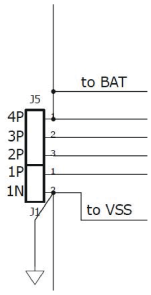


图 9-4. Li-Ion Cell Connections

9.2.2.1.4 Sense Resistor

As with the cell connections, the quality of the Kelvin connections at the sense resistor is critical. The sense resistor must have a temperature coefficient no greater than 50 ppm in order to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short-circuit ranges of the BQ40Z50-R2 device. Select the smallest value possible to minimize the negative voltage generated on the BQ40Z50-R2 V_{SS} node(s) during a short circuit. This pin has an absolute minimum of –0.3 V. Parallel resistors can be used as long as good Kelvin sensing is ensured. The device is designed to support a 1-mΩ to 3-mΩ sense resistor.

The BQ40Z50-R2 ground scheme is different from that of the older generation devices. In previous devices, the device ground (or low current ground) is connected to the SRN side of the R_{SENSE} resistor pad. In the BQ40Z50-R2 device, however, it connects the low-current ground on the SRP side of the R_{SENSE} resistor pad close to the battery 1N terminal (see 节 9.2.2.1.3). This is because the BQ40Z50-R2 device has one less VC pin (a ground reference pin VC5) compared to the previous devices. The pin was removed and was internally combined to SRP.

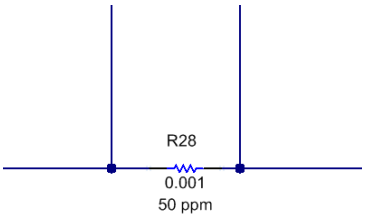


图 9-5. Sense Resistor

9.2.2.1.5 ESD Mitigation

A pair of series 0.1-μF ceramic capacitors is placed across the PACK+ and PACK– terminals to help in the mitigation of external electrostatic discharges. The two devices in series ensure continued operation of the pack if one of the capacitors becomes shorted.

Optionally, a tranzorb such as the SMBJ2A can be placed across the terminals to further improve ESD immunity.

9.2.2.2 Gas Gauge Circuit

The gas gauge circuit includes the BQ40Z50-R2 and its peripheral components. These components are divided into the following groups: differential low-pass filter, PBI, system present, SMBus communication, fuse circuit, and LED.

9.2.2.2.1 Coulomb-Counting Interface

The BQ40Z50-R2 uses an integrating delta-sigma ADC for current measurements. Add a 100-Ω resistor from the sense resistor to the SRP and SRN inputs of the device. Place a 0.1-μF (C18) filter capacitor across the SRP and SRN inputs.

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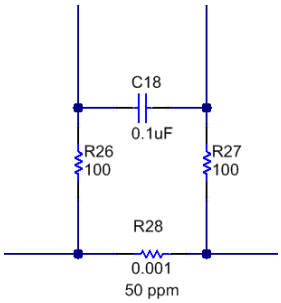


图 9-6. Differential Filter

9.2.2.2.2 Power Supply Decoupling and PBI

The BQ40Z50-R2 device has an internal LDO that is internally compensated and does not require an external decoupling capacitor.

The PBI pin is used as a power supply backup input pin, providing power during brief transient power outages. A standard 2.2-µF ceramic capacitor is connected from the PBI pin to ground, as shown in 图 9-7.

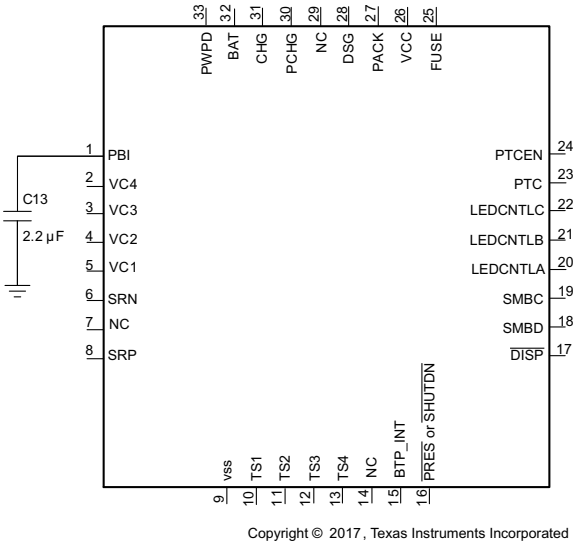


图 9-7. Power Supply Decoupling

9.2.2.2.3 System Present

The system present signal informs the gas gauge whether the pack is installed into or removed from the system. In the host system, this pin is grounded. The $\overline{\text{PRES}}$ pin of the BQ40Z50-R2 device is occasionally sampled to test for system present. In ACTIVE mode, the $\overline{\text{PRES}}$ pin is pulsed every 250 ms for a duration of 5 ms (RHOEN is on), and just before it is turned off, the state of the $\overline{\text{PRES}}$ pin is checked to see if it is low or high. The average of the four measurements is used to determine if the $\overline{\text{PRES}}$ is asserted or not. In SLEEP mode, the $\overline{\text{PRES}}$ pin is pulsed every "Sleep Voltage Time," and the state of the $\overline{\text{PRES}}$ pin is determined. A resistor can be used to pull the signal low and the resistance must be 20 kΩ or lower to ensure that the test pulse is lower than the V_{IL} limit. The pullup current source is typically 10 µA to 20 µA. When the $\overline{\text{PRES}}$ pin is not pulsed, the $\overline{\text{PRES}}$ pin is tied internally to VSS (RHOUT is on), and any pullup on the $\overline{\text{PRES}}$ pin will cause a battery drain when not charging. Refer to the $\overline{\text{PRES}}$ pin diagram in

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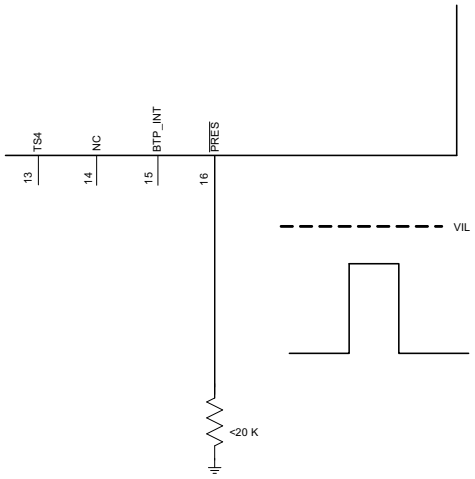


图 9-8. System Present Pull-Down Resistor

Because the System Present signal is part of the pack connector interface to the outside world, it must be protected from external electrostatic discharge events. The $\overline{\text{PRES}}$ pin has integrated ESD protection to 2 kV. External protection can be added to support higher ESD protection requirements. The TPD1E10B06 single-channel ESD protection diode (U2) can protect the input up to 30 kV, and the R8 reduces the holding current to release the internal SCR in the event that it triggers.

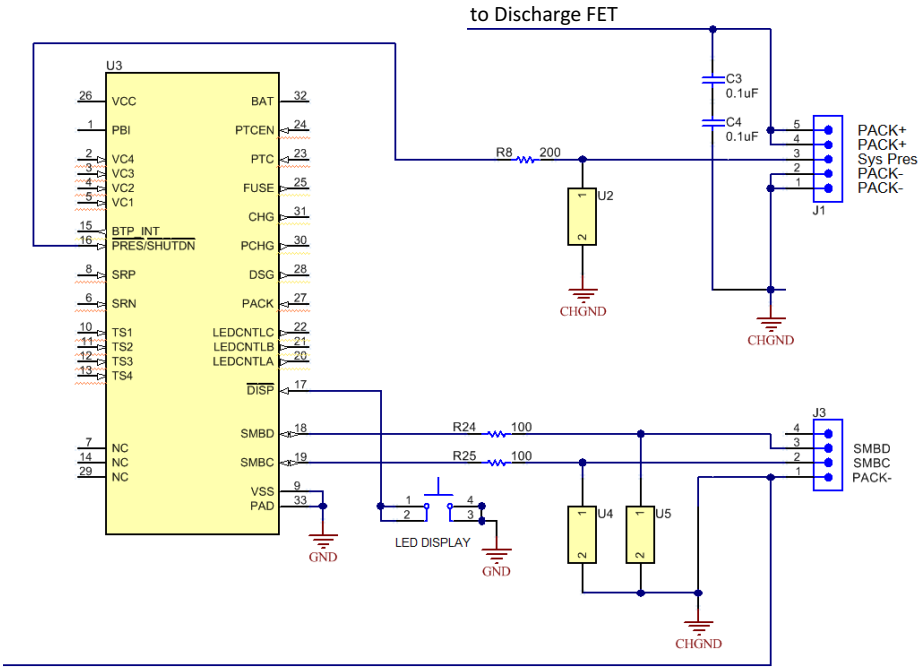


图 9-9. System Present ESD and Short Protection

9.2.2.2.4 SMBus Communication

The SMBus clock and data pins have integrated high-voltage ESD protection circuits; however, adding TPD1E10B06 ESD protection diodes (U4 and U5) and series resistors (R24 and R25) provides more robust ESD performance.

The SMBus clock and data lines have internal pulldown. When the gas gauge senses that both lines are low (such as during removal of the pack), the device performs auto-offset calibration and then goes into SLEEP mode to conserve power.

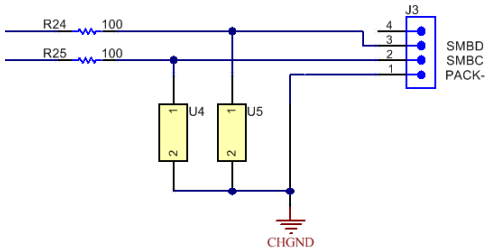


图 9-10. ESD Protection for SMBus Communication

9.2.2.2.5 FUSE Circuitry

The FUSE pin of the BQ40Z50-R2 device is designed to ignite the chemical fuse if one of the various safety criteria is violated. The FUSE pin also monitors the state of the secondary-voltage protection IC. Q5 ignites the chemical fuse when its gate is high. The 7-V output of the bq294700 is divided by R18 and R19, which provides adequate gate drive for Q5 while guarding against excessive back current into the bq294700 if the FUSE signal is high.

Using C7 is generally a good practice, especially for RFI immunity. C7 may be removed, if desired, because the chemical fuse is a comparatively slow device and is not affected by any sub-microsecond glitches that come from the FUSE output during the cell connection process.

If the AFEFUSE output is not used, it should be connected to VSS.

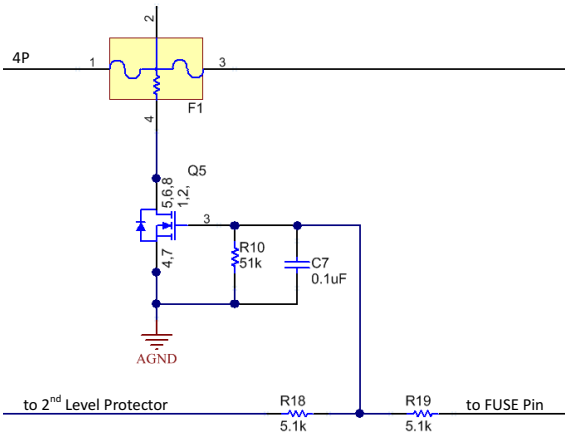


图 9-11. FUSE Circuit

When the BQ40Z50-R2 device is commanded to ignite the chemical fuse, the FUSE pin activates to give a typical 8-V output. The new design makes it possible to use a higher Vgs FET for Q5. This improves the robustness of the system, as well as widens the choices for Q5.

9.2.2.3 Secondary-Current Protection

The BQ40Z50-R2 device provides secondary overcurrent and short-circuit protection, cell balancing, cell voltage multiplexing, and voltage translation. The following section examines cell and battery inputs, pack and FET control, temperature output, and cell balancing.

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9.2.2.3.1 Cell and Battery Inputs

Each cell input is conditioned with a simple RC filter, which provides ESD protection during cell connect and acts to filter unwanted voltage transients. The resistor value allows some trade-off for cell balancing versus safety protection.

The integrated cell balancing FETs enable the AFE to bypass cell current around a given cell or numerous cells, effectively balancing the entire battery stack. External series resistors placed between the cell connections and the VCx I/O pins set the balancing current magnitude. The internal FETs provide a 200-Ω resistance (2 V < VDS < 4 V). Series input resistors between 100 Ω and 300 Ω are recommended for effective cell balancing.

The BAT input uses a diode (D1) to isolate and decouple it from the cells in the event of a transient dip in voltage caused by a short-circuit event.

Also, as described in 节 *9.2.2.1*, the top and bottom nodes of the cells must be sensed at the battery connections with a Kelvin connection to prevent voltage sensing errors caused by a drop in the high-current PCB copper.

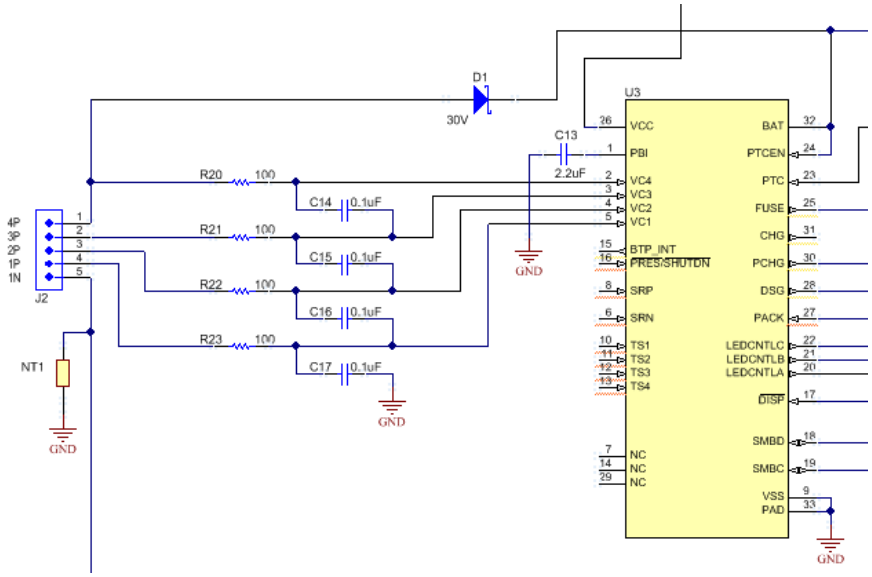


图 9-12. Cell and BAT Inputs

9.2.2.3.2 External Cell Balancing

Internal cell balancing can only support up to 10 mA. External cell balancing is provided as another option for faster cell balancing. For details, refer to the application note, *Fast Cell Balancing Using External MOSFET* (SLUA420).

9.2.2.3.3 PACK and FET Control

The PACK and V_{CC} inputs provide power to the BQ40Z50-R2 device from the charger. The PACK input also provides a method to measure and detect the presence of a charger. The PACK input uses a 10-kΩ resistor; whereas, the V_{CC} input uses an internal diode to guard against input transients and prevent a misoperation of the gate driver during short-circuit events.

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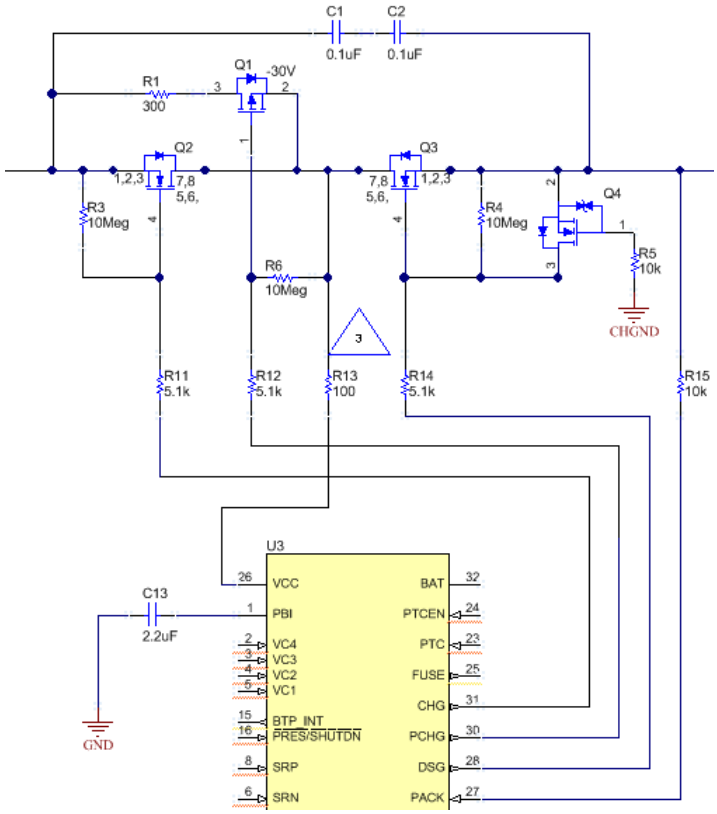


图 9-13. BQ40Z50-R2 PACK and FET Control

The N-channel charge and discharge FETs are controlled with 5.1-kΩ series gate resistors, which provide a switching time constant of a few microseconds. The 10-MΩ resistors ensure that the FETs are off in the event of an open connection to the FET drivers. Q4 is provided to protect the discharge FET (Q3) in the event of a reverse-connected charger. Without Q4, Q3 can be driven into its linear region and suffer severe damage if the PACK+ input becomes slightly negative.

Q4 turns on in that case to protect Q3 by shorting its gate to source. To use the simple ground gate circuit, the FET must have a low gate turn-on threshold. If it is desired to use a more standard device, such as the 2N7002 as the reference schematic, the gate should be biased up to 3.3 V with a high-value resistor. The BQ40Z50-R2 device has the capability to provide a current-limited charging path typically used for low battery voltage or low temperature charging. The BQ40Z50-R2 device uses an external P-channel, precharge FET controlled by PCHG.

9.2.2.3.4 Temperature Output

For the BQ40Z50-R2 device, TS1, TS2, TS3, and TS4 provide thermistor drive-under program control. Each pin can be enabled with an integrated 18-kΩ (typical) linearization pullup resistor to support the use of a 10-kΩ at 25°C (103) NTC external thermistor, such as a Mitsubishi BN35-3H103. The reference design includes four 10-kΩ thermistors: RT2, RT3, RT4, and RT5. The BQ40Z50-R2 device supports up to four external thermistors. Connect unused thermistor pins to V_{SS}.

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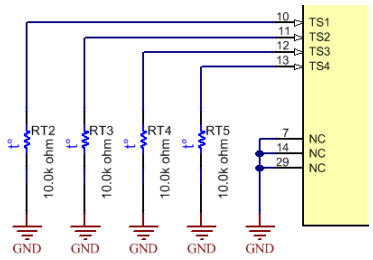


图 9-14. Thermistor Drive

9.2.2.3.5 LEDs

Three LED control outputs provide constant current sinks for the driving external LEDs. These outputs are configured to provide voltage and control for up to five LEDs. No external bias voltage is required. Unused LEDCNTL pins can remain open or they can be connected to V_{SS}. The $\overline{DISP}$ pin should be connected to V_{SS} if the LED feature is not used.

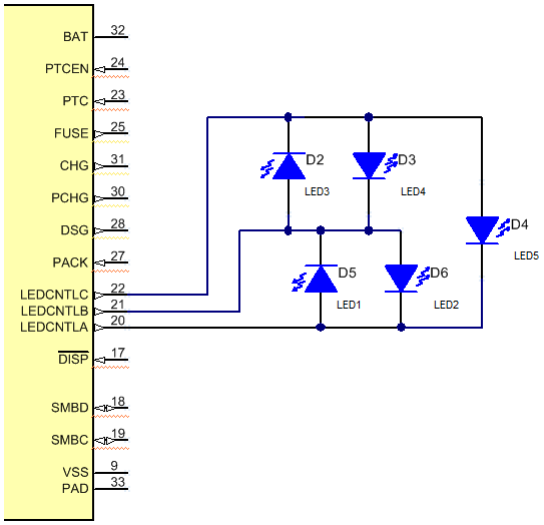


图 9-15. LEDs

9.2.2.3.6 Safety PTC Thermistor

The BQ40Z50-R2 device provides support for a safety PTC thermistor. The PTC thermistor is connected between the PTC and BAT pins. It can be placed close to the CHG/DSG FETs to monitor the temperature. The PTC pin monitors the voltage at the pin and will trip if the thermistor resistance exceeds the defined threshold. A PTC fault is one of the permanent failure modes. It can only be cleared by a POR.

To disable, connect PTC and PTCEN to VSS.

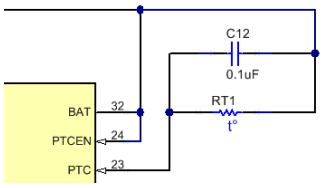
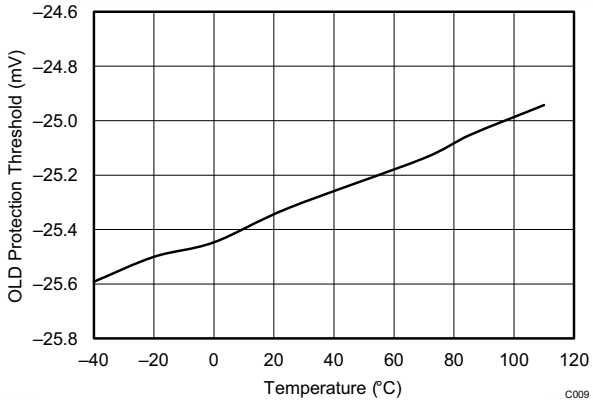


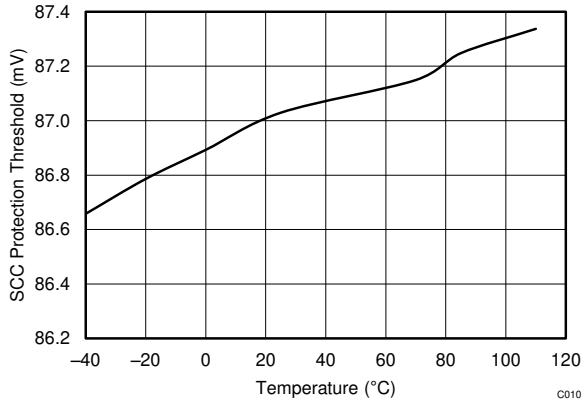
图 9-16. PTC Thermistor

9.2.3 Application Curves



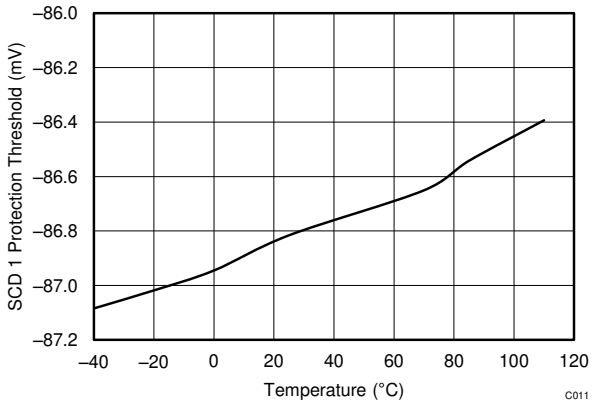
Threshold setting is – 25 mV.

图 9-17. Overcurrent Discharge Protection Threshold vs. Temperature



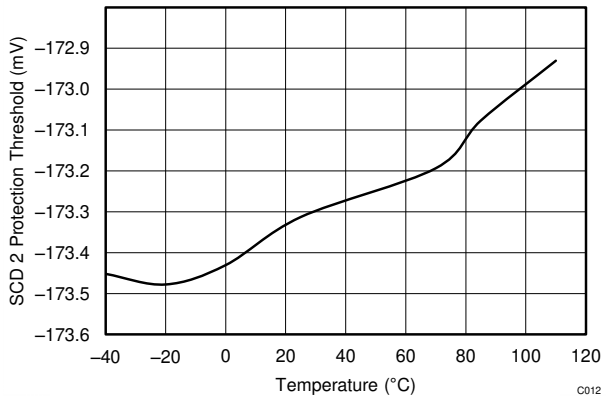
Threshold setting is 88.85 mV.

图 9-18. Short Circuit Charge Protection Threshold vs. Temperature



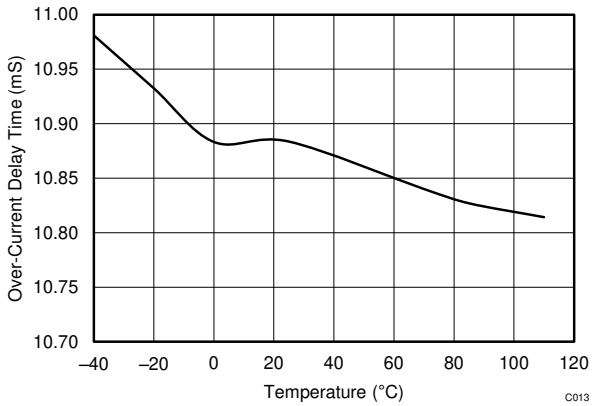
Threshold setting is – 88.85 mV.

图 9-19. Short Circuit Discharge 1 Protection Threshold vs. Temperature



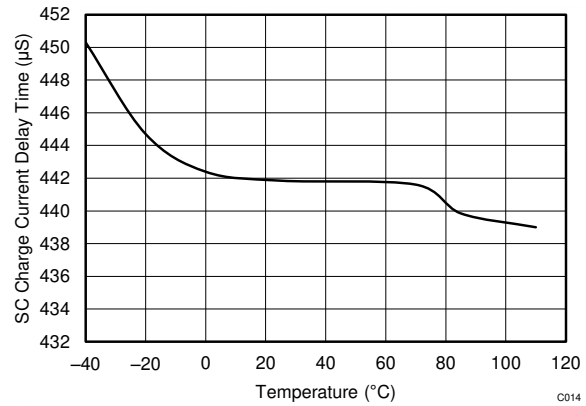
Threshold setting is – 177.7 mV.

图 9-20. Short Circuit Discharge 2 Protection Threshold vs. Temperature



Threshold setting is 11 ms.

图 9-21. Overcurrent Delay Time vs. Temperature



Threshold setting is 465 µs.

图 9-22. Short Circuit Charge Current Delay Time vs. Temperature

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10 Power Supply Recommendations

The device manages its supply voltage dynamically according to the operation conditions. Normally, the BAT input is the primary power source to the device. The BAT pin should be connected to the positive termination of the battery stack. The input voltage for the BAT pin ranges from 2.2 V to 26 V.

The VCC pin is the secondary power input, which activates when the BAT voltage falls below minimum V_{CC}. This enables the device to source power from a charger (if present) connected to the PACK pin. The VCC pin should be connected to the common drain of the CHG and DSG FETs. The charger input should be connected to the PACK pin.

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11 Layout

11.1 Layout Guidelines

A battery fuel gauge circuit board is a challenging environment due to the fundamental incompatibility of high-current traces and ultra-low current semiconductor devices. The best way to protect against unwanted trace-to-trace coupling is with a component placement, such as that shown in 图 11-1, where the high-current section is on the opposite side of the board from the electronic devices. Clearly, this is not possible in many situations due to mechanical constraints. Still, every attempt should be made to route high-current traces away from signal traces, which enter the BQ40Z50-R2 directly. IC references and registers can be disturbed and in rare cases damaged due to magnetic and capacitive coupling from the high-current path.

Note

During surge current and ESD events, the high-current traces appear inductive and can couple unwanted noise into sensitive nodes of the gas gauge electronics, as illustrated in 图 11-2.

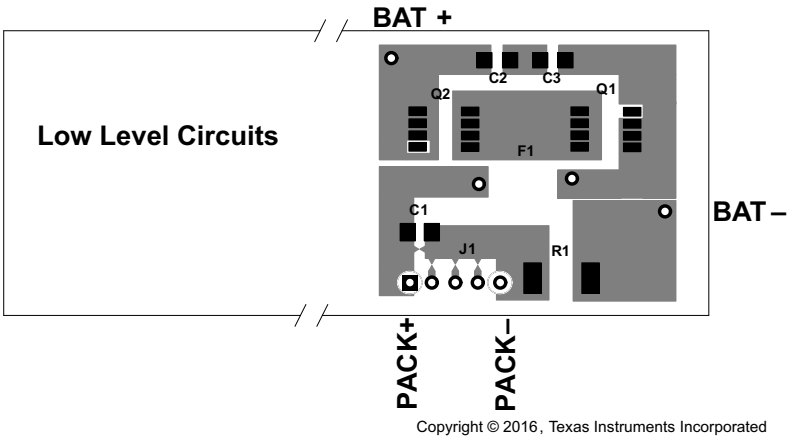


图 11-1. Separating High- and Low-Current Sections Provides an Advantage in Noise Immunity

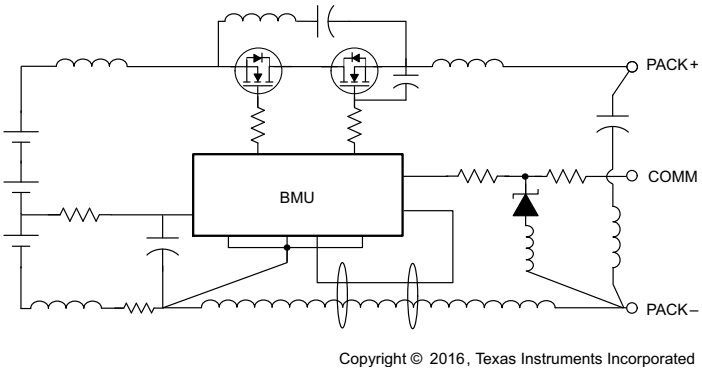


图 11-2. Avoid Close Spacing Between High-Current and Low-Level Signal Lines

Kelvin voltage sensing is extremely important in order to accurately measure current and top and bottom cell voltages. Place all filter components as close as possible to the device. Route the traces from the sense resistor in parallel to the filter circuit. Adding a ground plane around the filter network can add additional noise immunity. 图 11-3 and 图 11-4 demonstrate correct Kelvin current sensing.

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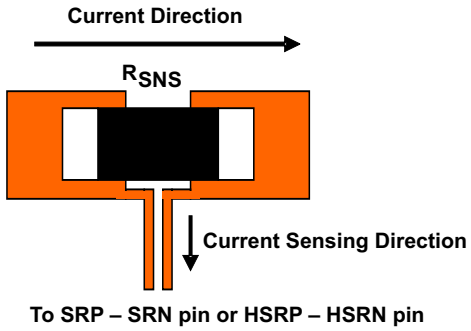


图 11-3. Sensing Resistor PCB Layout

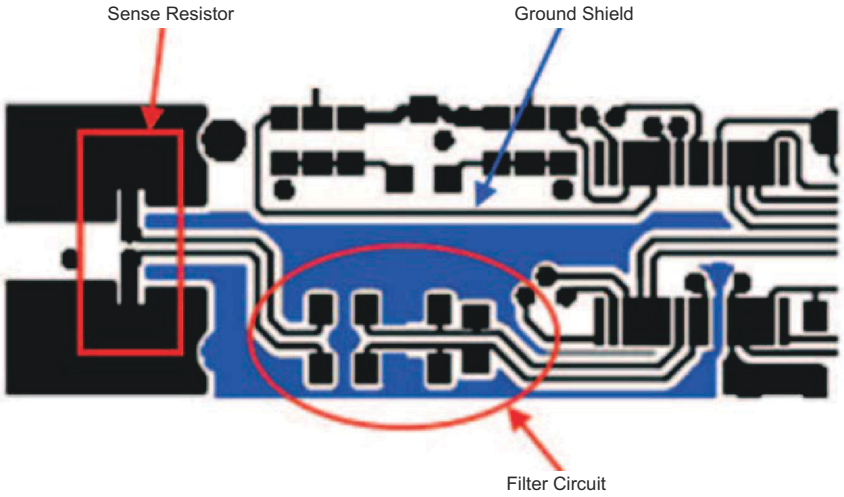
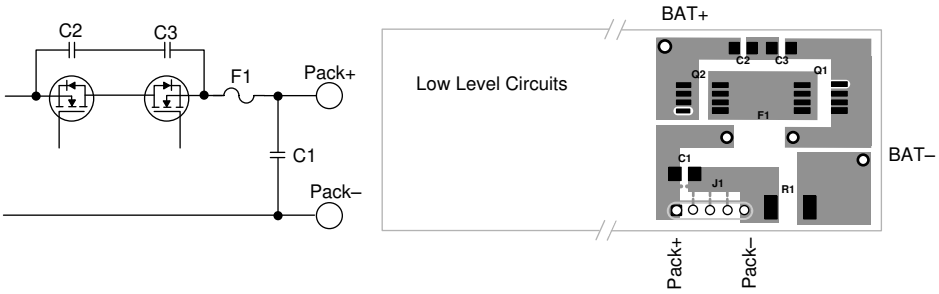


图 11-4. Sense Resistor, Ground Shield, and Filter Circuit Layout

11.1.1 Protector FET Bypass and Pack Terminal Bypass Capacitors

Use wide copper traces to lower the inductance of the bypass capacitor circuit. 图 11-5 shows an example layout, demonstrating this technique.



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图 11-5. Use Wide Copper Traces to Lower the Inductance of Bypass Capacitors C1, C2, and C3

11.1.2 ESD Spark Gap

Protect SMBus clock, data, and other communication lines from ESD with a spark gap at the connector. The pattern in 图 11-6 is recommended, with 0.2-mm spacing between the points.

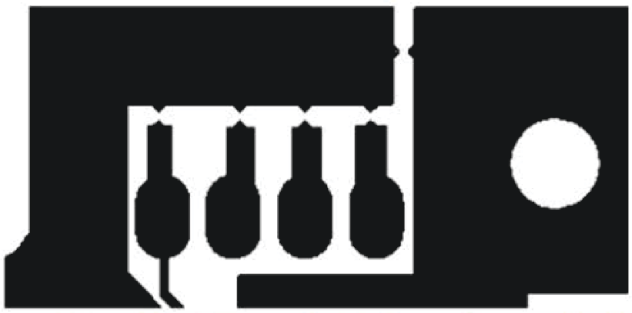


图 11-6. Recommended Spark-Gap Pattern Helps Protect Communication Lines from ESD

11.2 Layout Example

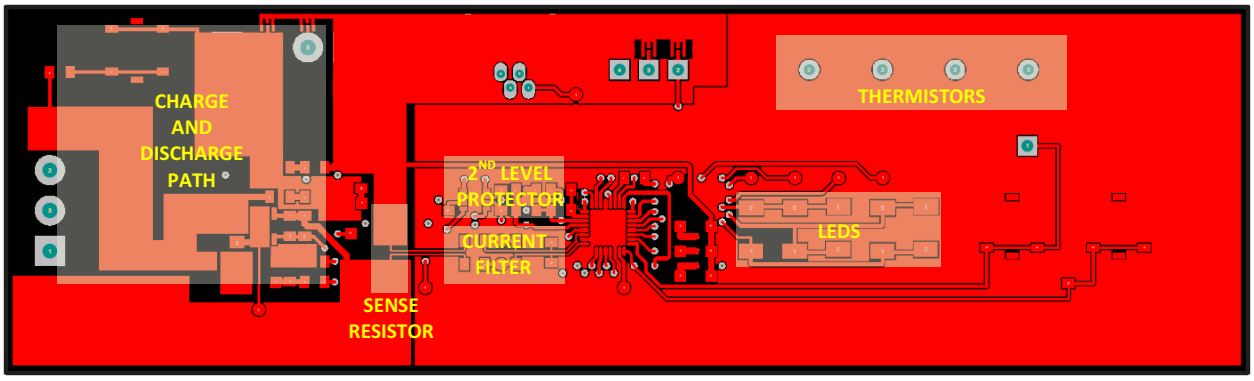


图 11-7. Top Layer

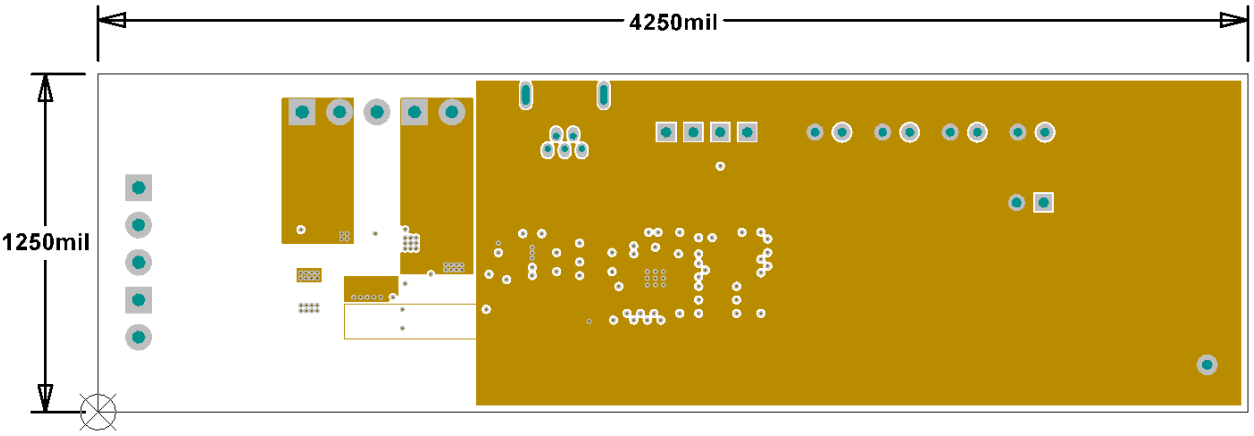


图 11-8. Internal Layer 1

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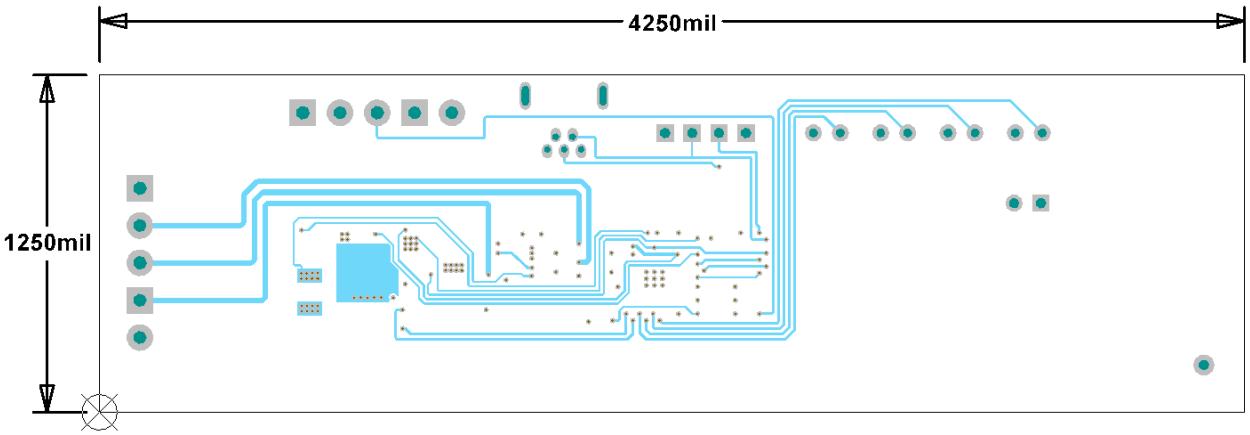


图 11-9. Internal Layer 2

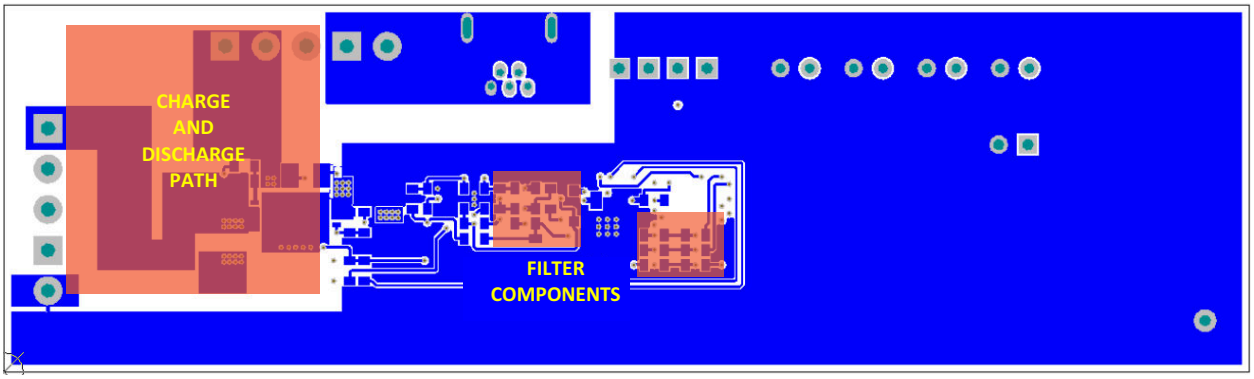


图 11-10. Bottom Layer

12 Device and Documentation Support

12.1 第三方产品免责声明

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following from the BQ40Z50-R2 product page on TI.com:

- *BQ40Z50-R2 Technical Reference Manual* (SLUUBK0)
- *BQ40Z50EVM Li-Ion Battery Pack Manager Evaluation Module User's Guide* (SLUUAV7)

12.2.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on ***Alert me*** to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 支持资源

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ40Z50RSMR-R2	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	BQ40Z50
BQ40Z50RSMR-R2.A	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ40Z50
BQ40Z50RSMR-R2.B	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ40Z50
BQ40Z50RSMR-R2G4	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ40Z50
BQ40Z50RSMR-R2G4.A	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ40Z50
BQ40Z50RSMT-R2	Active	Production	VQFN (RSM) | 32	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	BQ40Z50
BQ40Z50RSMT-R2.A	Active	Production	VQFN (RSM) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ40Z50

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

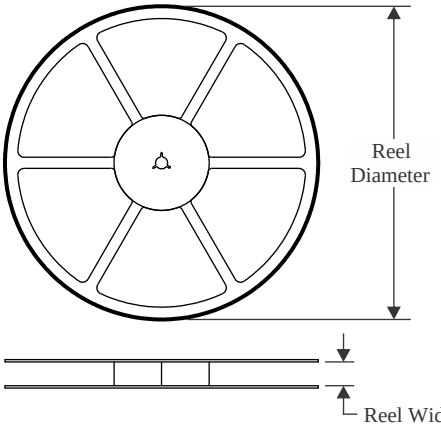
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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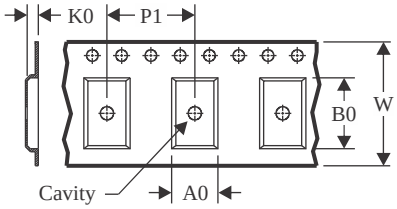
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

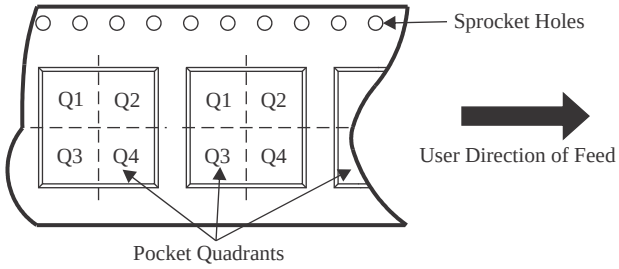


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

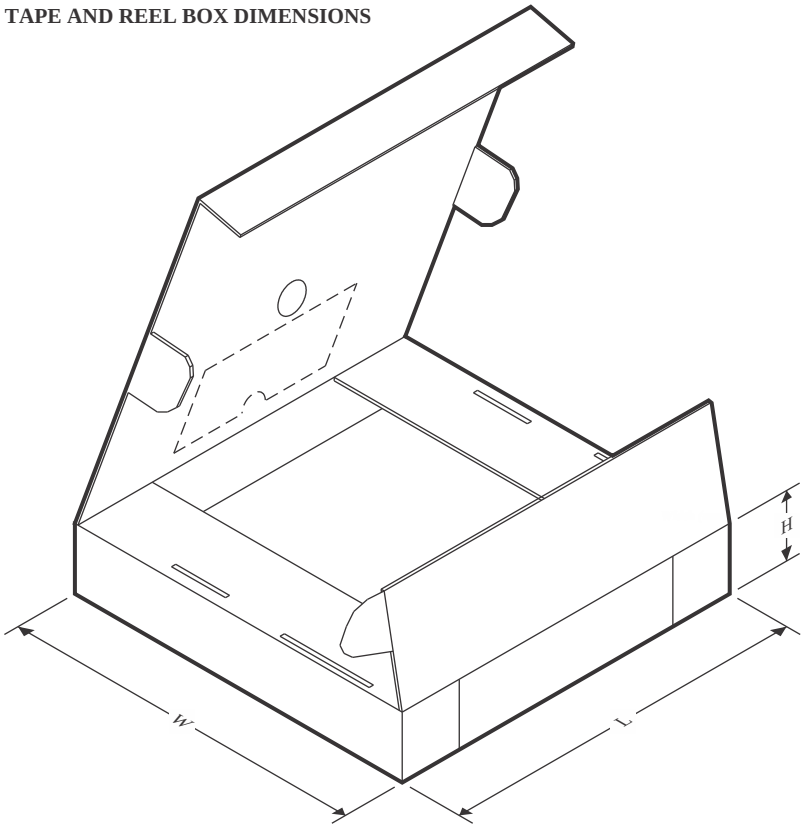
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ40Z50RSMR-R2	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ40Z50RSMR-R2	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ40Z50RSMR-R2G4	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ40Z50RSMT-R2	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ40Z50RSMT-R2	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ40Z50RSMR-R2	VQFN	RSM	32	3000	367.0	367.0	35.0
BQ40Z50RSMR-R2	VQFN	RSM	32	3000	346.0	346.0	33.0
BQ40Z50RSMR-R2G4	VQFN	RSM	32	3000	367.0	367.0	35.0
BQ40Z50RSMT-R2	VQFN	RSM	32	250	210.0	185.0	35.0
BQ40Z50RSMT-R2	VQFN	RSM	32	250	182.0	182.0	20.0

GENERIC PACKAGE VIEW

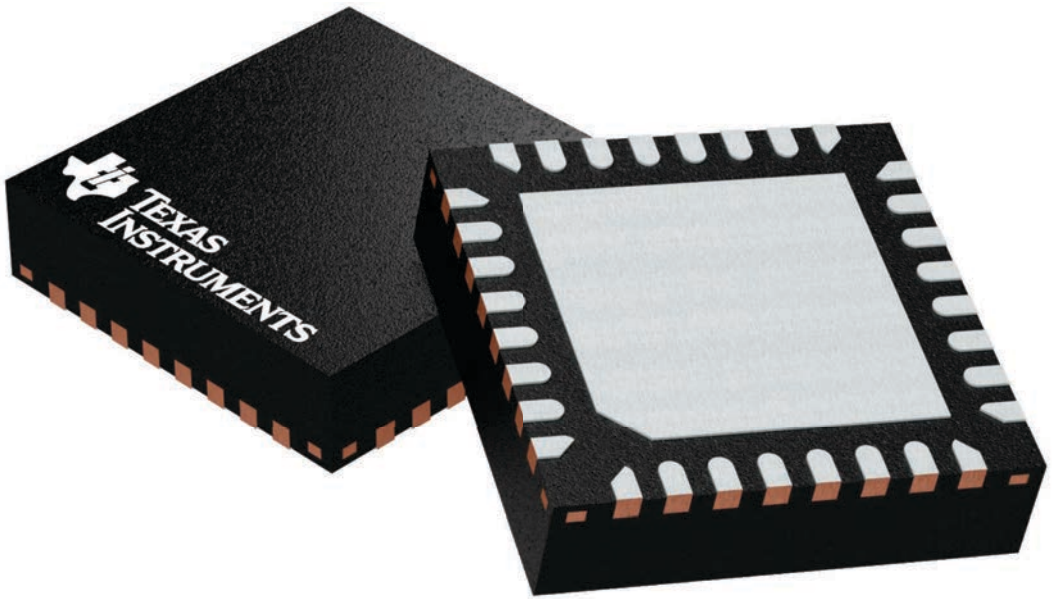
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



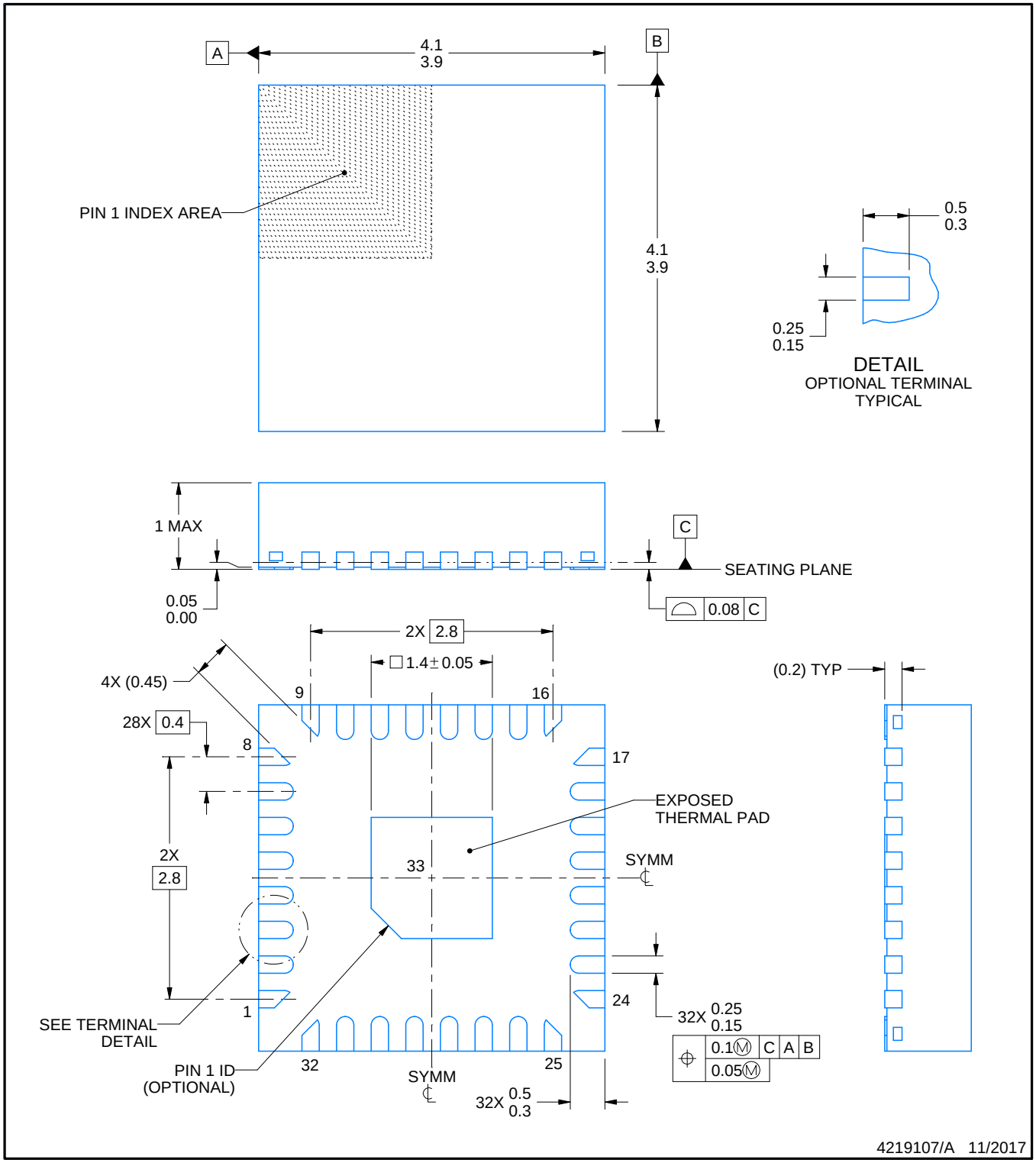
4224982/A

PACKAGE OUTLINE

RSM0032A

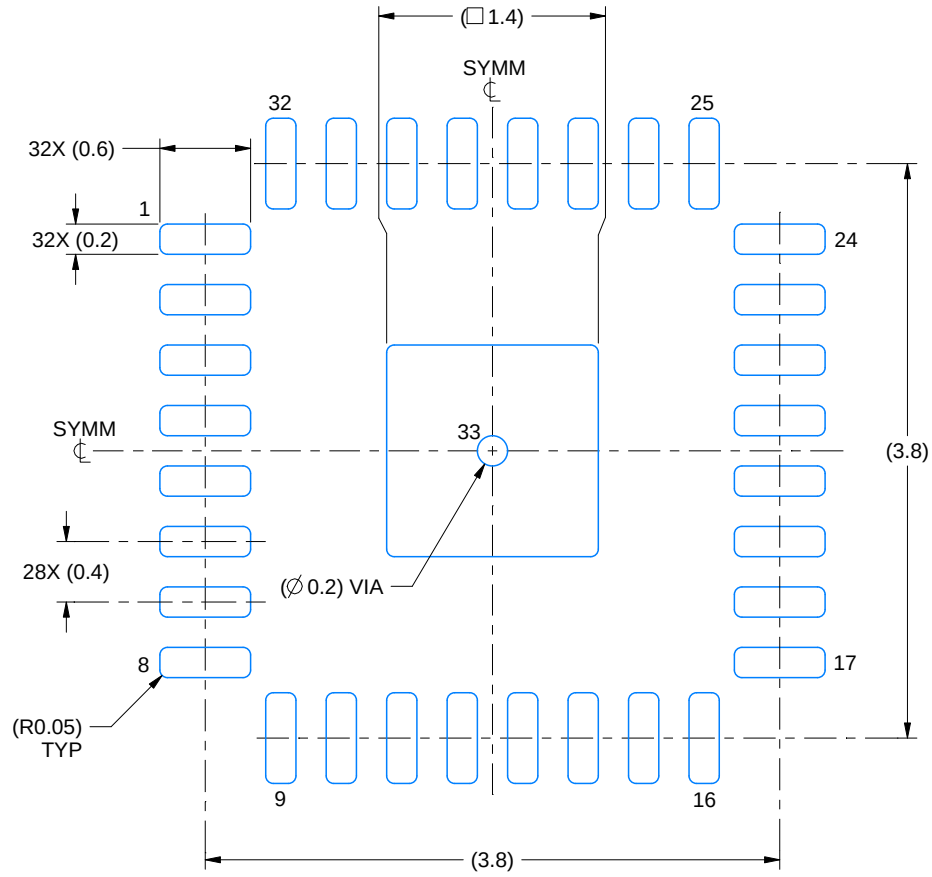
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

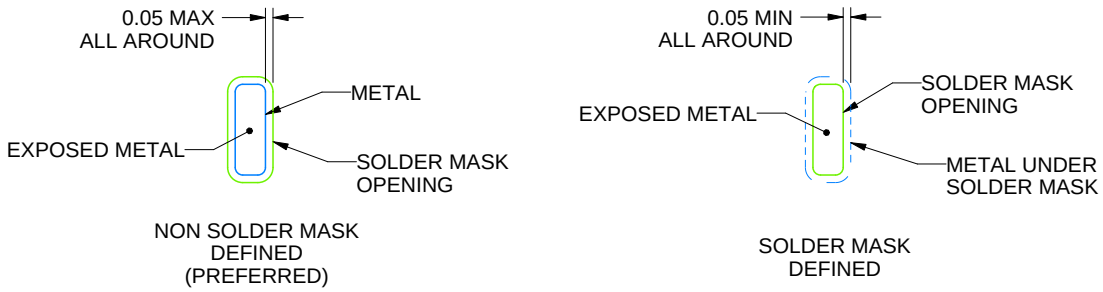


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

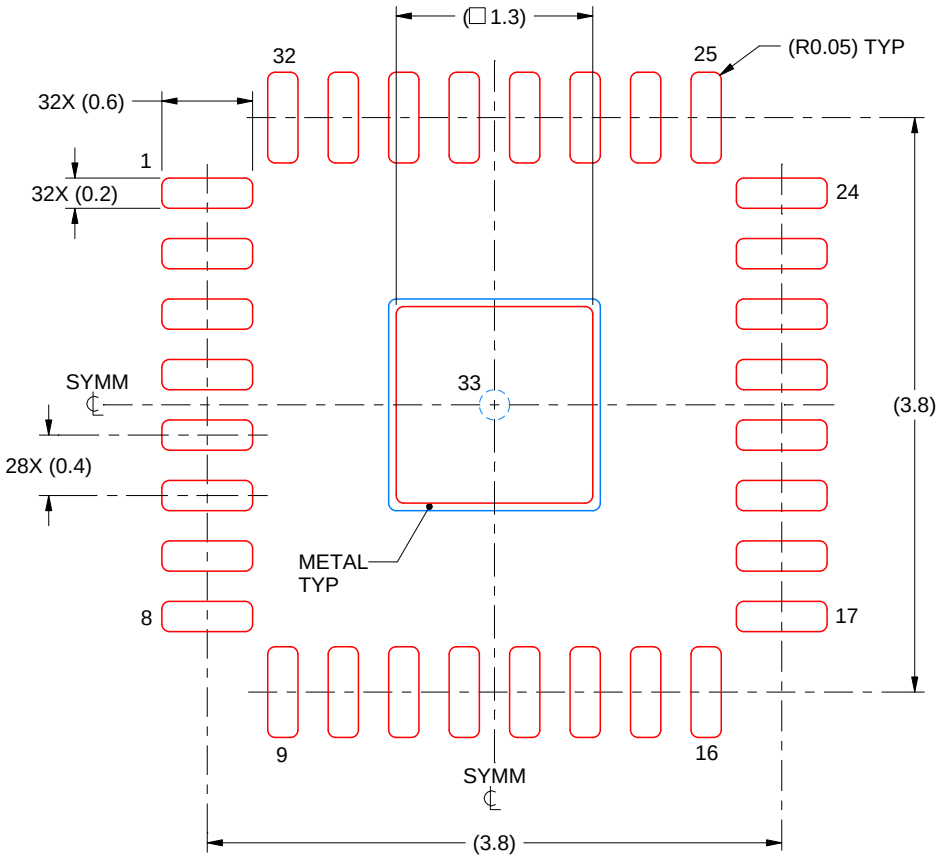


SOLDER MASK DETAILS

4219107/A 11/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219107/A 11/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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