

针对无线电源联盟 (WPC) TX A5 或 A11 的低系统成本，无线电源控制器

查询样片: bq500212A

特性

- 针对发射端应用的已经验证，经 **Qi** 认证的超值解决方案
- 针对全部 **WPC1.1 5V** 解决方案的最少器件数量
- 符合无线电源联盟 **(WPC1.1)** 类型 **A5** 或 **A11** 发送器技术规范的 **5V** 运行
- 完全 **WPC** 兼容，其中包括经改进的外来物体检测 **(FOD)** 方法
- 允许使用 **X7R** 类型谐振电容器以减少成本
- 针对 **USB** 和受限源运行的 **Dynamic Power Limiting™**
- 数字解调减少了组件
- 充电状态和故障状态的发光二极管 **(LED)** 指示
- 低待机和高效率

应用范围

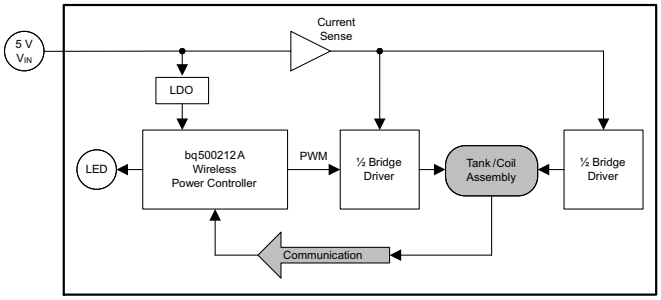
- 无线电源联盟 **(WPC1.1)** 兼容无线充电器，用于：
  - 经 **Qi** 认证的智能手机和其它手持设备
  - 汽车和其它车辆配件
- **TI** 无线充电解决方案的更多信息，请见**www.ti.com/wirelesspower**

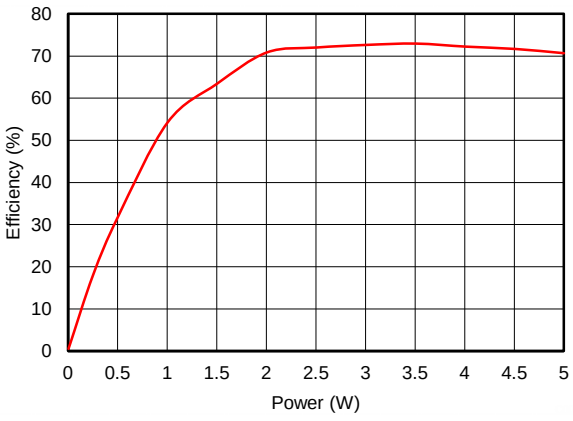
说明

bq500212A 是一款经 Qi 认证的超值解决方案，此解决方案集成了控制到单个 WPC1.1 兼容接收器无线电源传输所需的全部功能。 它与 WPC1.1 兼容，并且被设计成用于 5V 系统的无线电源联盟类型 A5 或 A11 发射器。 bq500212A *询问* 周围环境以寻找将被供电的 WPC 兼容器件，安全使用器件，接收来自被供电器件的数据包通信并根据 WPC1.1 技术规范管理此电源传输。 为了最大限度地增加无线电源控制应用中的灵活性， Dynamic Power Limiting™ (DPL) 成为 bq500212A 的特性。 Dynamic Power Limiting™ 通过无缝优化受限输入电源上可用功率的用量提高用户体验。 通过持续监控已建立的电源传输的效率，bq500212A 支持针对以往产品的外来物体检测 (FOD) 和增强性寄生金属检测 (PMOD)，从而防止由于在无线电源传输场中错误放置金属物体而导致的电源丢失。 如果在电源传输期间发生任何异常情况，bq500212A 对其进行处理并提供指示器输出。 综合状态和故障监视特性可实现一个低成本但是稳健耐用的，经 Qi 认证的无线电源系统设计。

bq500212A 采用 48 引脚，7mm x 7mm 四方扁平无引线 (QFN) 封装。

系统图和效率与系统输出功率间的关系





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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

OPERATING TEMPERATURE RANGE, T_A	ORDERABLE PART NUMBER	PIN COUNT	SUPPLY	PACKAGE	TOP SIDE MARKING
-40°C to 110°C	BQ500212ARGZR	48 pin	Reel of 2500	QFN	BQ500212A
	BQ500212ARGZT	48 pin	Reel of 250	QFN	BQ500212A

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

	VALUE		UNIT
	MIN	MAX	
Voltage applied at V33D to GND	–0.3	3.6	V
Voltage applied at V33A to GND	–0.3	3.6	
Voltage applied to any pin (2)	–0.3	3.6	
Storage temperature, T_{STG}	–40	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to GND.

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V	Supply voltage during operation, V33D, V33A	3.0	3.3	3.6	V
T_A	Operating free-air temperature range	–40		110	°C
T_J	Junction temperature			110	

THERMAL INFORMATION

THERMAL METRIC(1)		bq500212A RGZ 48 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	28.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	14.2	
θ_{JB}	Junction-to-board thermal resistance(4)	5.4	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.2	
ψ_{JB}	Junction-to-board characterization parameter(6)	5.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	1.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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ELECTRICAL CHARACTERISTICS

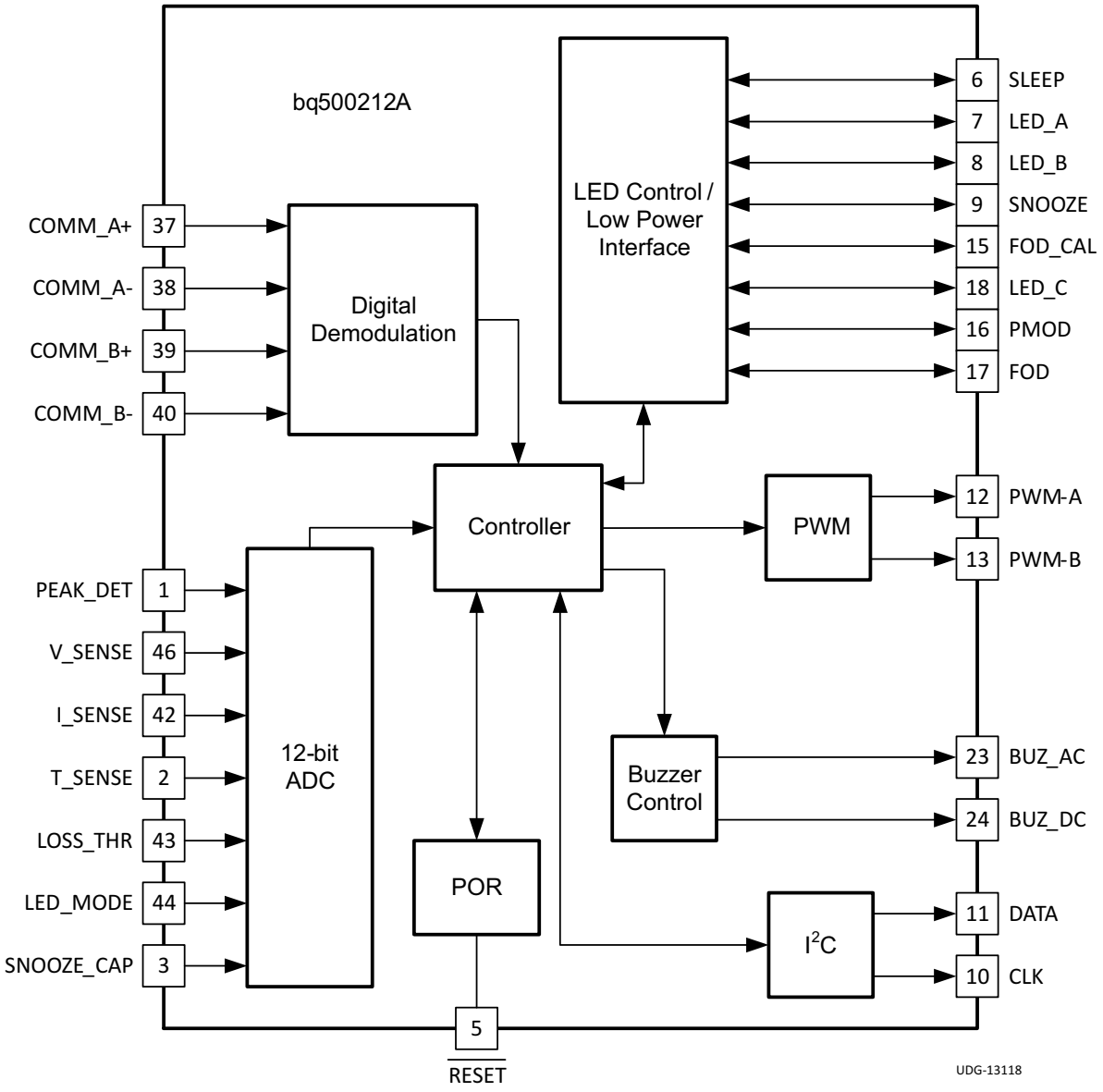
over operating free-air temperature range (unless otherwise noted)

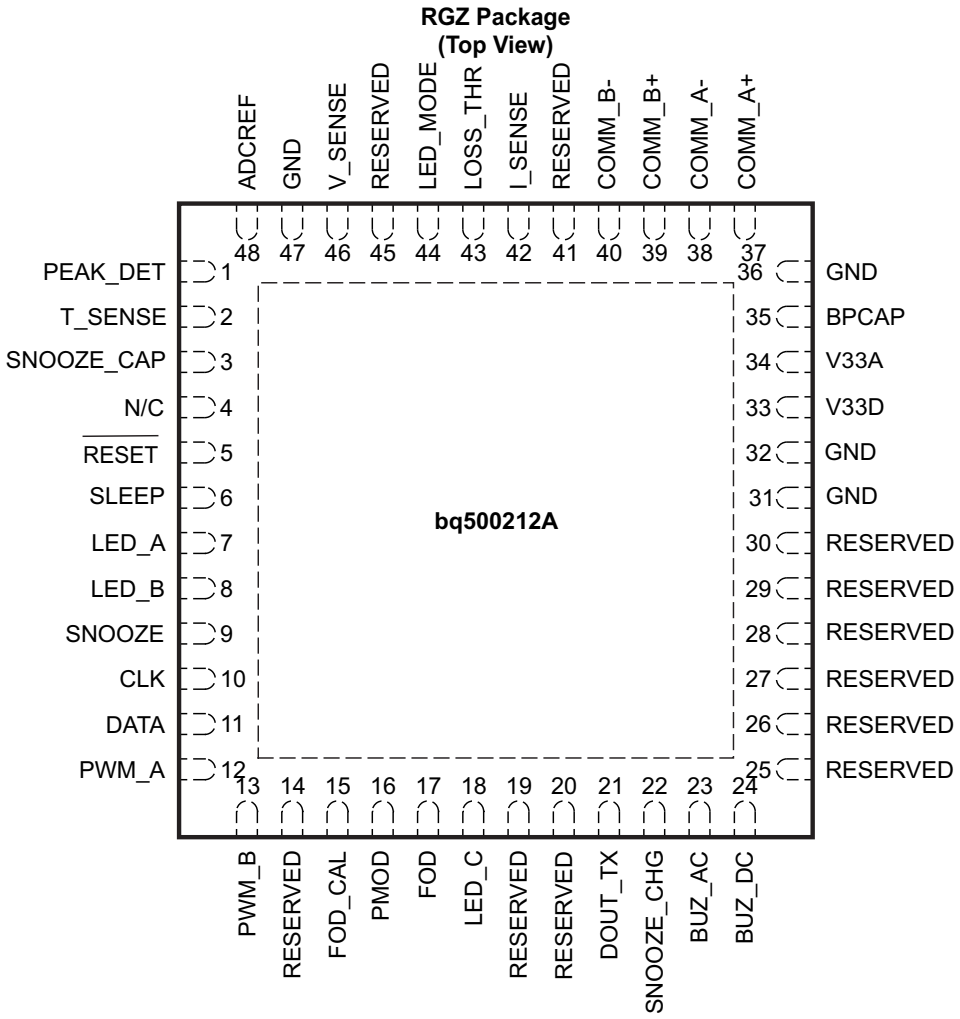
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{V33A}	Supply current	V33A = 3.3 V		8	15	mA
I_{V33D}		V33D = 3.3 V		44	55	
I_{TOTAL}		V33D = V33A = 3.3 V		52	60	
INTERNAL REGULATOR CONTROLLER INPUTS/OUTPUTS						
V33	3.3-V linear regulator	Emitter of NPN transistor	3.25	3.3	3.6	V
V33FB	3.3-V linear regulator feedback			4	4.6	
I_{V33FB}	Series pass base drive	V_{IN} = 12 V; current into V33FB pin		10		mA
Beta	Series NPN pass device		40			
EXTERNALLY SUPPLIED 3.3 V POWER						
V33D	Digital 3.3-V power	T_A = 25°C	3		3.6	V
V33A	Analog 3.3-V power	T_A = 25°C	3		3.6	
V33Slew	V33 slew rate	V33 slew rate between 2.3 V and 2.9 V, V33A = V33D	0.25			V/ms
DIGITAL DEMODULATION INPUTS COMM_A+, COMM_A-, COMM_B+, COMM_B-						
V_{bias}	COMM+ Bias Voltage			1.5		V
COMM+, COMM-	Modulation voltage digital resolution			1		mV
R_{EA}	Input impedance	Ground reference	0.5	1.5	3	MΩ
I_{OFFSET}	Input offset current	1-kΩ source impedance	–5		5	µA
ANALOG INPUTS V_SENSE, I_SENSE, T_SENSE, LED_MODE, LOSS_THR, SNOOZE_CAP, PWR_UP						
V_{ADDR_OPEN}	Voltage indicating open pin	LED_MODE open	2.37			V
V_{ADDR_SHORT}	Voltage indicating pin shorted to GND	LED_MODE shorted to ground			0.36	
V_{ADC_RANGE}	Measurement range for voltage monitoring	ALL ANALOG INPUTS	0		2.5	
INL	ADC integral nonlinearity		-2.5		2.5	mV
R_{IN}	Input impedance	Ground reference	8			MΩ
C_{IN}	Input capacitance				10	pF
DIGITAL INPUTS/OUTPUTS						
V_{OL}	Low-level output voltage	I_{OL} = 6 mA , V33D = 3 V			DGND1 + 0.25	V
V_{OH}	High-level output voltage	I_{OH} = -6 mA , V33D = 3 V	V33D - 0.6V			
V_{IH}	High-level input voltage	V33D = 3V	2.1		3.6	
V_{IL}	Low-level input voltage	V33D = 3.5 V			1.4	
I_{OH}(MAX)	Output high source current				4	mA
I_{OL}(MAX)	Output low sink current				4	
SYSTEM PERFORMANCE						
V_{RESET}	Voltage where device comes out of reset	V33D Pin			2.4	V
t_{RESET}	Pulse width needed for reset	$\overline{RESET}$ pin	2			µs
f_{SW}	Switching Frequency		112		205	kHz

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DEVICE INFORMATION

Functional Block Diagram





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PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NO.	NAME		
1	PEAK_DET	I	Connected to peak detect circuit. Protects from coil overvoltage event.
2	T_SENSE	I	Sensor Input. Device shuts down when below 1 V for longer than 150ms. If not used, keep above 1 V by connecting to the 3.3-V supply.
3	SNOOZE_CAP	I	Connected to interval timing capacitor
4	N/C	I	Not used. Can be left open. Can also be tied to GND and flooded with copper to improve GND plane.
5	$\overline{\text{RESET}}$	I	Device reset. Use a 10-kΩ to 100-kΩ pull-up resistor to the 3.3-V supply.
6	SLEEP	O	Connected to 5 s interval circuit
7	LED_A	I	Connect to an LED via 470-Ω resistor for status indication.
8	LED_B	I	Connect to an LED via 470-Ω resistor for status indication.
9	SNOOZE	O	Connected to 500ms ping interval circuit
10	CLK	I/O	10-kΩ pull-up resistor to 3.3-V supply. For factory use only.
11	DATA	I/O	10-kΩ pull-up resistor to 3.3-V supply. For factory use only.
12	PWM_A	O	PWM Output A, controls one half of the full bridge in a phase-shifted full bridge. Switching deadtimes must be externally generated.
13	PWM_B	O	PWM Output B, controls other half of the full bridge in a phase-shifted full bridge. Switching deadtimes must be externally generated.
14	RESERVED	O	Reserved. Leave open.
15	FOD_CAL	O	FOD Calibration pin. It controls the FOD calibration setting at startup.
16	PMOD	O	Set the threshold used to detect a PMOD condition by connecting, via resistor, to pin 43. Leave open to disable PMOD.
17	FOD	O	Set the threshold used to detect an FOD condition by connecting, via resistor, to pin 43. Leave open to disable FOD.
18	LED_C	O	Connect to an LED via 470-Ω resistor for status indication.
19	RESERVED	O	Reserved, leave this pin open.
20	RESERVED	I	Reserved, connect to GND.
21	DOUT_TX	I	Not used. Leave this pin open.
22	SNOOZE_CHG	I	Connected to interval timing capacitor.
23	BUZ_AC	O	AC Buzzer Output. Outputs a 400-ms, 4-kHz AC pulse when charging begins.
24	BUZ_DC	O	DC Buzzer Output. Outputs a 400-ms DC pulse when charging begins. This could also be connected to an LED via 470-Ω resistor.
25	RESERVED	I/O	Not used, leave this pin open.
26	RESERVED	I/O	Not used, leave this pin open.
27	RESERVED	I/O	Reserved, leave this pin open.
28	RESERVED	I/O	Reserved, leave this pin open.
29	RESERVED	I/O	Reserved, leave this pin open.
30	RESERVED	I/O	Reserved, leave this pin open.
31	GND	I/O	Reserved, connect to GND.

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PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
32	GND	—	GND.
33	V33D	—	Digital core 3.3-V supply. Be sure to decouple with bypass capacitors as close to the part as possible.
34	V33A	—	Analog 3.3-V Supply. This pin can be derived from V33D supply, decouple with 10-Ω resistor and additional bypass capacitors
35	BPCAP	—	Bypass capacitor for internal 1.8-V core regulator. Connect bypass capacitor to GND.
36	GND	—	GND.
37	COMM_A+	I	Digital demodulation non-inverting input A, connect parallel to input B+.
38	COMM_A-	I	Digital demodulation inverting input A, connect parallel to input B-.
39	COMM_B+	I	Digital demodulation non-inverting input B, connect parallel to input A+.
40	COMM_B-	I	Digital demodulation inverting input B, connect parallel to input A-.
41	RESERVED	O	Reserved, leave this pin open.
42	I_SENSE	I	Transmitter input current, used for efficiency calculations. Use 20-mΩ sense resistor and A=50 gain current sense amplifier.
43	LOSS_THR	I	Input to program FOD/PMOD thresholds and FOD_CAL correction.
44	LED_MODE	I	Input to select from four LED modes.
45	RESERVED	I	Connect to V33D (3.3 V).
46	V_SENSE	I	Transmitter input voltage, used for efficiency calculations. Use 76.8-kΩ to 10-kΩ divider to minimize quiescent current.
47	GND	—	GND.
48	ADCREF	I	External Reference Voltage Input. Connect this input to GND.
49	EPAD	—	Flood with copper GND plane and stitch vias to PCB internal GND plane.

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Principles of Operation

Fundamentals

The principle of wireless power transfer is simply an open cored transformer consisting of primary and secondary coils and associated electronics. The primary coil and electronics are also referred to as the transmitter, and the secondary side the receiver. The transmitter coil and electronics are typically built into a charger pad. The receiver coil and electronics are typically built into a portable device, such as a cell-phone.

When the receiver coil is positioned on the transmitter coil, magnetic coupling occurs when the transmitter coil is driven. The flux is coupled into the secondary coil which induces a voltage, current flows, it is rectified and power can be transferred quite effectively to a load - wirelessly. Power transfer can be managed via any of various familiar closed-loop control schemes.

Wireless Power Consortium (WPC)

The Wireless Power Consortium (WPC) is an international group of companies from diverse industries. The WPC standard was developed to facilitate cross compatibility of compliant transmitters and receivers. The standard defines the physical parameters and the communication protocol to be used in wireless power. For more information, go to www.wirelesspowerconsortium.com.

Power Transfer

Power transfer depends on coil coupling. Coupling is dependant on the distance between coils, alignment, coil dimensions, coil materials, number of turns, magnetic shielding, impedance matching, frequency and duty cycle.

Most importantly, the receiver and transmitter coils must be aligned for best coupling and efficient power transfer. The closer the space between the coils, the better the coupling, but the practical distance is set to be less than 5 mm (as defined within the WPC Specification) to account for housing and interface surfaces.

Shielding is added as a backing to both the transmitter and receiver coils to direct the magnetic field to the coupled zone. Magnetic fields outside the coupled zone do not transfer power. Thus, shielding also serves to contain the fields to avoid coupling to other adjacent system components.

Regulation can be achieved by controlling any one of the coil coupling parameters. For WPC compatibility, the transmitter coils and capacitance are specified and the resonant frequency point is fixed at 100 kHz. Power transfer is regulated by changing the operating frequency between 110 kHz to 205 kHz. The higher the frequency, the further from resonance and the lower the power. Duty cycle remains constant at 50% throughout the power band and is reduced only once 205 kHz is reached.

The WPC standard describes the dimension and materials of the coils. It also has information on tuning the coils to resonance. The value of the inductor and resonant capacitor are critical to proper operation and system efficiency.

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Communication

Communication within the WPC is from the receiver to the transmitter, where the receiver tells the transmitter to send power and how much. In order to regulate, the receiver must communicate with the transmitter whether to increase or decrease frequency. The receiver monitors the rectifier output and using Amplitude Modulation (AM), sends packets of information to the transmitter. A packet is comprised of a preamble, a header, the actual message and a checksum, as defined by the WPC standard.

The receiver sends a packet by modulating an impedance network. This AM signal reflects back as a change in the voltage amplitude on the transmitter coil. The signal is demodulated and decoded by the transmitter side electronics and the frequency of its coil drive output is adjusted to close the regulation loop. The bq500212A features internal digital demodulation circuitry.

The modulated impedance network on the receiver can either be resistive or capacitive. Figure 1 shows the resistive modulation approach, where a resistor is periodically added to the load and also shows the resulting change in resonant curve which causes the amplitude change in the transmitter voltage indicated by the two operating points at the same frequency. Figure 2 shows the capacitive modulation approach, where a capacitor is periodically added to the load and also shows the resulting amplitude change in the transmitter voltage.

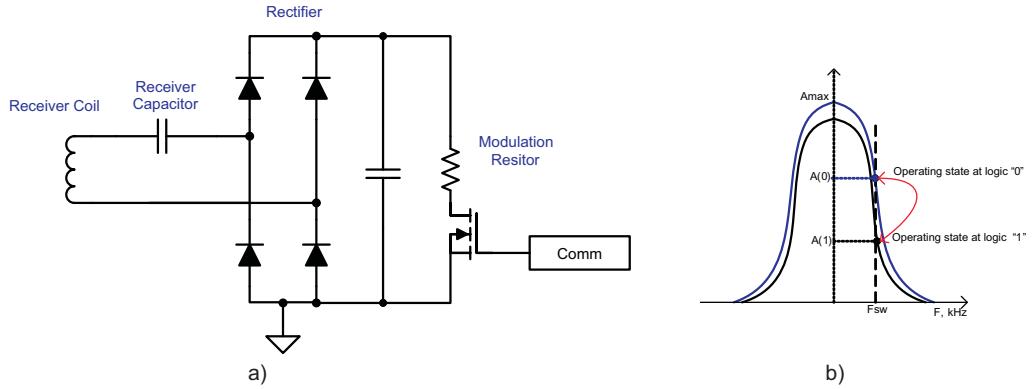


Figure 1. Receiver Resistive Modulation Circuit

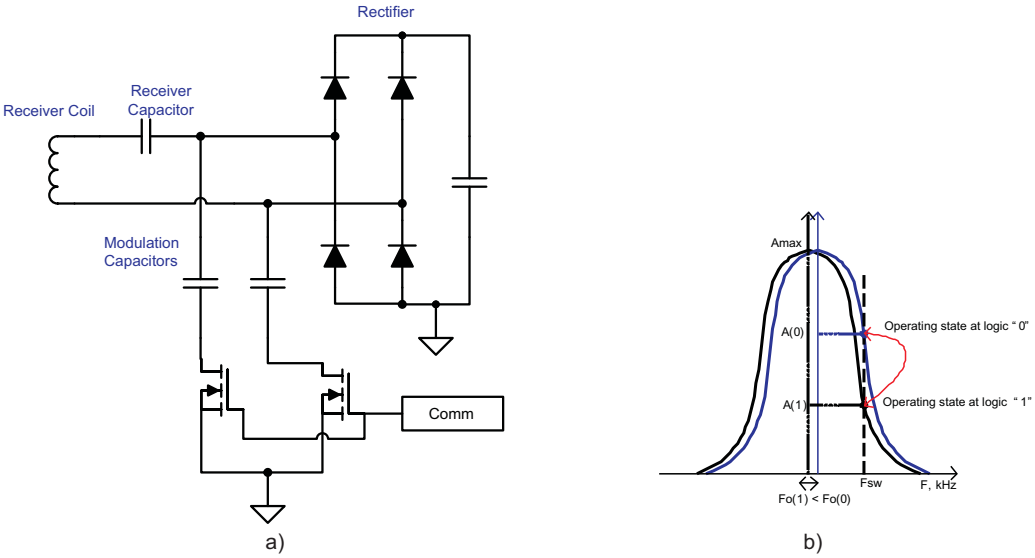


Figure 2. Receiver Capacitive Modulation Circuit

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Application Information

Coils and Matching Capacitors

The coil and matching capacitor selection for the transmitter has been established by WPC standard. These values are fixed and cannot be changed on the transmitter side.

An up to date list of available and compatible A5 or A11 transmitter coils can be found here (Texas Instruments Literature Number SLUA649):

Capacitor selection is critical to proper system operation. A total capacitance value of 400 nF is required in the resonant tank. A 400-nF capacitor is not a standard value and therefore several must be combined in parallel. It is recommended to use 4 x 100nF, as these are very commonly available.

NOTE

A total capacitance value of 400 nF/50 V is required in the resonant tank to achieve a 100-kHz resonance frequency.

To achieve the 400nF total capacitance in the resonant tank, the bq500212A sensitive demodulation circuitry allows the use of three (3) lower cost 100nF/X7R type capacitors in parallel with one (1) high quality 100nF/C0G type, thereby reducing system cost from competitive solutions requiring four C0G types.

The capacitors chosen must be rated for 50 V operation. Use quality capacitors from reputable vendors such as KEMET, MURATA or TDK.

Dynamic Power Limiting™

Dynamic Power Limiting™ (DPL) allows operation from a 5-V supply with limited current capability (such as a USB port). When the input voltage is observed drooping, the output power is dynamically limited to reduce the load and provides margin relative to the supply's capability.

Anytime the DPL control loop is regulating the operating point of the transmitter, the LED will indicate that DPL is active. The LED color and flashing pattern are determined by the LED Table. If the receiver sends a Control Error Packet (CEP) with a negative value, (for example, to reduce power to the load), the WPTX in DPL mode will respond to this CEP via the normal WPC control loop.

NOTE

The power limit indication depends on the LED_MODE selected.

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Option Select Pins

Several pins on the bq500212A are allocated to programming the FOD and PMOD Loss Threshold and the LED mode of the device. At power up, a bias current is applied to pins LED_MODE and LOSS_THR and the resulting voltage measured in order to identify the value of the attached programming resistor. The values of the operating parameters set by these pins are determined using Table 2. For LED_MODE, the selected bin determines the LED behavior based on Table 1; for the LOSS_THR, the selected bin sets a threshold used for parasitic metal object detection (see Parasitic Metal Detection (PMOD) and Foreign Object Detection (FOD) section). Table 1.

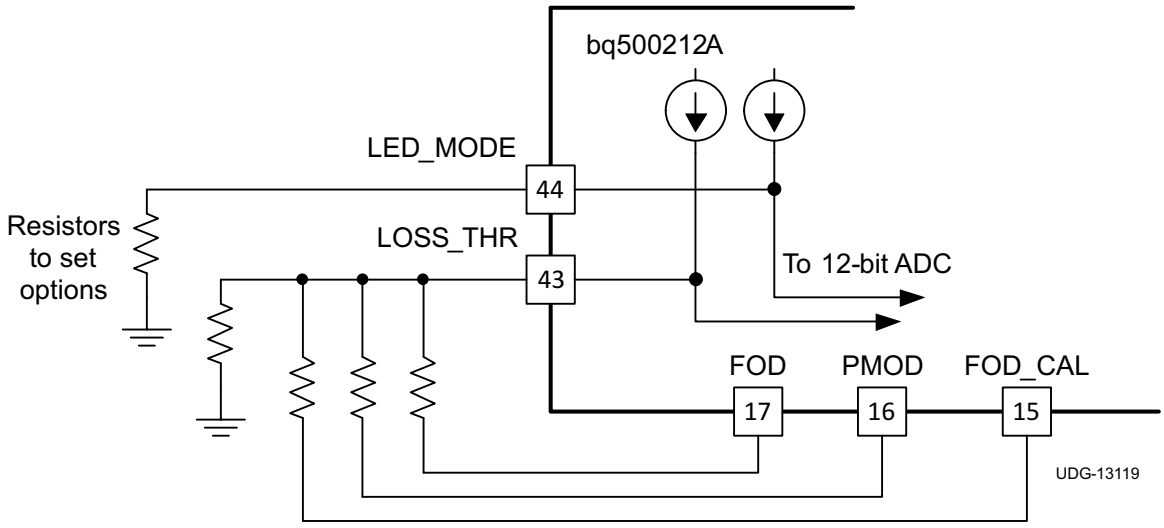


Figure 3. Option Select Pin Programming

LED Indication Modes

The bq500212A can directly drive up to three (3) LED outputs (pin 7, pin 8 and pin 18) through a simple current limit resistor (typically 470 Ω), based on the mode selected. The current limit resistors can be individually adjusted to tune or match the brightness of the LEDs. Do not exceed the maximum output current rating of the device. The resistor in Figure 3 connected to pin 44 and GND selects the desired LED indication scheme in Table 1.

- LED modes permit the use of one to three indicator LED's. Amber in the 2-LED mode is obtained by turning on both the green and red.
- LEDs can be turned on solid or configured to blink either slow (approx. 1.6s period) or fast (approx. 400ms period).
- Except in modes 2 and 9, the charge complete state is only maintained for 5 seconds after which it reverts to idle. This permits the processor to sleep in order to reduce standby power consumption. In other modes, external logic, such as a flip-flop, may be implemented to maintain the charge complete indication if desired.

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Table 1. LED Modes

LED CONTROL OPTION	LED SELECTION RESISTOR	DESCRIPTION	LED	OPERATIONAL STATES					
				STANDBY	POWER TRANSFER	CHARGE COMPLETE	FAULT	DYNAMIC POWER LIMITING™	FOD Warning
X	< 36.5 kΩ	Reserved, do not use	LED1, green	-	-	-	-	-	-
			LED2, red						
			LED3, amber						
1	42.2 kΩ	Choice number 1	LED1, green	Off	Blink slow	On	Off	Blink slow	Off
			LED2, red	Off	Off	Off	On	Blink slow	Blink fast
			LED3, amber	-	-	-	-	-	-
2	48.7 kΩ	Choice number 2	LED1, green	On	Blink slow	On	Off	Blink slow	Off
			LED2, red	On	Off	Off	On	Blink slow	Blink fast
			LED3, amber	-	-	-	-	-	-
3	56.2 kΩ	Choice number 3	LED1, green	Off	On	Off	Blink fast	On	On
			LED2, red	-	-	-	-	-	-
			LED3, amber	-	-	-	-	-	-
4	64.9 kΩ	Choice number 4	LED1, green	Off	On	Off	Off	Off	Off
			LED2, red	Off	Off	Off	On	Blink slow	Blink fast
			LED3, amber	-	-	-	-	-	-
5	75 kΩ	Choice number 5	LED1, green	Off	Off	On	Off	Off	Off
			LED2, red	Off	On	Off	Off	On	On
			LED3, amber	Off	Off	Off	Blink slow	Off	Off
6	86.6 kΩ	Choice number 6	LED1, green	Off	Blink slow	On	Off	Off	Off
			LED2, red	Off	Off	Off	On	Off	Blink fast
			LED3, amber	Off	Off	Off	Off	Blink Slow	Off
7	100 kΩ	Choice number 7	LED1, green	Off	Blink slow	Off	Off	Off	Off
			LED2, red	Off	Off	On	Off	Off	Off
			LED3, amber	Off	Off	Off	On	Blink slow	Blink fast
8	115 kΩ	Choice number 8	LED1, green	Off	Off	On	Blink slow	Off	Off
			LED2, red	Off	On	Off	Blink slow	On	On
			LED3, amber	-	-	-	-	-	-
9	133 kΩ	Choice number 9	LED1, green	Off	Blink slow	On	Off	Blink slow	Off
			LED2, red	Off	Off	Off	On	Blink slow	Blink fast
			LED3, amber	-	-	-	-	-	-
10	154 kΩ	Choice number 10	LED1, green	Off	On	Off	Blink fast	Blink slow	On
			LED2, red	Off	Off	On	Off	Off	Off
			LED3, amber	-	-	-	-	-	-

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Parasitic Metal Object Detect (PMOD), Foreign Object Detection (FOD) and FOD Calibration

The bq500212A supports improved FOD (WPC1.1) and enhanced PMOD (WPC 1.0) features. Continuously monitoring input power, known losses, and the value of power reported by the RX device being charged, the bq500212A can estimate how much power is unaccounted for and presumed lost due to metal objects placed in the wireless power transfer path. If this unexpected loss exceeds the threshold set by the FOD or PMOD resistors, a fault is indicated and power transfer is halted. Whether the FOD or the PMOD algorithm is used is determined by the ID packet of the receiver being charged.

As the default, both PMOD and FOD resistors should set a threshold of 400 mW (selected by 56.2-kΩ resistors from FOD (pin 17) and PMOD(pin16) to LOSS_THR (pin43)). 400 mW has been empirically determined using standard WPC FOD test objects (disc, ring and foil). Some tuning might be required as every system will be slightly different. This tuning is best done by trial and error, use the set resistor values given in the table to increase or decrease the loss threshold and retry the system with the standard test objects. The ultimate goal of the FOD feature is safety; to protect misplaced metal objects from becoming hot. Reducing the loss threshold and making the system too sensitive will lead to false trips and a bad user experience. Find the balance which best suits the application.

If the application requires disabling one function or the other (or both), it is possible by leaving the respective FOD/PMOD pin open. For example, to selectively disable the PMOD function, PMOD (pin16) should be left open.

NOTE

Disabling FOD results in a TX solution that is not WPC compliant.

Resistors of 1% tolerance should be used for a reliable selection of the desired threshold.

The FOD and PMOD resistors (pin17 and pin16) program the permitted power loss for the FOD and PMOD algorithms respectively. The FOD_CAL resistor (pin15), can be used to compensate for any load dependent effect on the power loss. Using a calibrated test receiver with no foreign objects present, the FOD_CAL resistor should be selected such that the calculated loss across the load range is substantially constant (within ~100 mW). After correcting for the load dependence, the FOD and PMOD thresholds should be re-set above the resulting average by approximately 400 mW in order for the transmitter to satisfy the WPC requirements on tolerated heating. Please contact TI for more information about setting appropriate FOD, PMOD, and FOD_CAL resistor values for your design.

Table 2. Option Select Bins

BIN NUMBER	RESISTANCE (kΩ)	LOSS THRESHOLD (mW)
0	<36.5	250
1	42.2	300
2	48.7	350
3	56.2	400
4	64.9	450
5	75.0	500
6	86.6	550
7	100	600
8	115	650
9	133	700
10	154	750
11	178	800
12	205	850
13	>237	Feature Disabled

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Shut Down via External Thermal Sensor or Trigger

Typical applications of the bq500212A will not require additional thermal protection. This shutdown feature is provided for enhanced applications and is not only limited to thermal shutdown. The key parameter is the 1.0 V threshold on pin 2. Voltage below 1.0 V on pin 2 for longer than 150ms causes the device to shutdown.

The application of thermal monitoring via a Negative Temperature Coefficient (NTC) sensor, for example, is straightforward. The NTC forms the lower leg of a temperature dependant voltage divider. The NTC leads are connected to the bq500212A device, pin 2 and GND. The threshold on pin 2 is set to 1.0 V, below which the system shuts down and a fault is indicated (depending on LED mode chosen).

To implement this feature follow these steps:

1) Consult the NTC datasheet and find the resistence vs temperature curve.

2) Determine the actual temperature where the NTC will be placed by using a thermal probe.

3) Read the NTC resistance at that temperature in the NTC datasheet, that is R_NTC.

4) Use the following formula to determine the upper leg resistor (R_Setpoint):

$$R_Setpoint = 2.3 \times R_NTC \quad (1)$$

The system will restore normal operation after approximately five minutes or if the receiver is removed. If the feature is not used, this pin must be pulled high.

NOTE

Pin 2 must always be terminated, else erratic behavior may result.

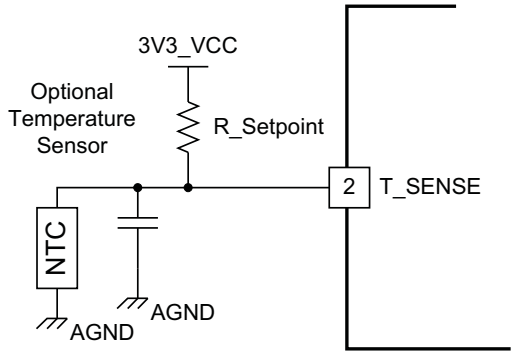


Figure 4. Negative Temperature Coefficient (NTC) Application

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Fault Handling and Indication

The following table provides approximate durations for the time before a retry is attempted for End Power Transfer (EPT) packets and fault events. Precise timing may be affected by external components, or shortened by receiver removal. The LED mode selected determines how the LED indicates the condition or fault.

CONDITION	DURATION (before retry)	HANDLING
EPT-00	Immediate	Unknown
EPT-01	5 seconds	Charge complete
EPT-02	Infinite	Internal fault
EPT-03	5 minutes	Over temperature
EPT-04	Immediate	Over voltage
EPT-05	Immediate	Over current
EPT-06	Infinite	Battery failure
EPT-07	Not applicable	Reconfiguration
EPT-08	Immediate	No response
OC (over current)	1 minute	
NTC (external sensor)	5 minutes	
PMOD/FOD warning	12 seconds	10 seconds LED only, 2 seconds LED + buzzer
PMOD/FOD	5 minutes	

Power Transfer Start Signal

The bq500212A features two signal outputs to indicate that power transfer has begun. Pin 23 outputs a 400-ms duration, 4-kHz square wave for driving low cost AC type ceramic buzzers. Pin 24 outputs logic high, also for 400 ms, which is suitable for DC type buzzers with built-in tone generators, or as a trigger for any type of customized indication scheme. If not used, these pins can be left open.

Power-On Reset

The bq500212A has an integrated Power-On Reset (POR) circuit which monitors the supply voltage and handles the correct device startup sequence. Additional supply voltage supervisor or reset circuits are not needed.

External Reset, $\overline{\text{RESET}}$ Pin

The bq500212A can be forced into a reset state by an external circuit connected to the $\overline{\text{RESET}}$ pin. A logic low voltage on this pin holds the device in reset. For normal operation, this pin is pulled up to 3.3 V_{CC} with a 10-kΩ pull-up resistor.

Low Power Mode

During standby, when nothing is on the transmitter pad, the bq500212A pings the surrounding environment at fixed intervals. The ping interval can be adjusted; the component values selected for the SNOOZE circuit determine this interval between pings. The choice of the ping interval effects two quantities: the idle efficiency of the system, and the time required to detect the presence of a receiver when it is placed on the pad. A trade off should be made which balances low power (longest ping interval) with good user experience (quick detection through short ping interval) while still meeting the WPC requirement for detection within 0.5 seconds.

The system power consumption is approximately 300 mW during an active ping, which lasts approximately 90 ms, and 40 mW for the balance of the cycle. A weighted average can thus be used to estimate the overall system's idle consumption:

If T_ping is the interval between pings in ms, P_idle in mW is approximately:

$$(40 \times (T_ping - 90) + 300 \times 90)/T_ping \quad (2)$$

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Trickle Charge and CS100

The WPC specification provides an End-of-Power Transfer message (EPT–01) to indicate charge complete. Upon receipt of the charge complete message, the bq500212A will change the LED indication. The exact indication depends on the LED_MODE chosen.

In some battery charging applications there is a benefit to continue the charging process in trickle-charge mode to top off the battery. There are several information packets in the WPC specification related to the levels of battery charge (Charge Status). The bq500212A uses these commands to enable top-off charging. The bq500212A changes the LED indication to reflect charge complete when a Charge Status message is 100% received, but unlike the response to an EPT, it will not halt power transfer while the LED is solid green. The mobile device can use a CS100 packet to enable trickle charge mode.

If the reported charge status drops below 90% normal, charging indication will be resumed.

Current Monitoring Requirements

The bq500212A is WPC1.1 ready. In order to enable the FOD or PMOD features, current monitoring circuitry must be provided in the application design.

For proper scaling of the current monitor signal, the current sense resistor should be 20 mΩ and the current shunt amplifier should have a gain of 50, such as the INA199A1. For FOD accuracy, the current sense resistor must be a quality component with 1% tolerance, at least 1/4-Watt rating, and a temperature stability of ±200 PPM. Proper current sensing techniques in the application hardware should also be observed.

If WPC compliance is not required current monitoring can be omitted. Connect the I_SENSE pin (pin 42) to GND.

All Unused Pins

All unused pins can be left open unless otherwise indicated. Pin 4 can be tied to GND and flooded with copper to improve ground shielding. Please refer to the pin definition table for further explanations.

Design Checklist for WPC1.1 Compliance with the bq500212A

- Coil and capacitor selection matches the A5/A11 specification.
- Total 400-nF resonant capacitor requirement is composed of: (3 x 100nF/X7R) + (1 x 100nF/C0G) types.
- Precision current sense amp used, such as the INA199A1. This is required for accurate FOD operation.
- Current shunt resistor 1% and <200 PPM. This is required for accurate FOD operation.

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APPLICATION INFORMATION

Overview

The application schematic for the transmitter with reduced standby power is shown in Figure 5.

CAUTION

Please check the bq500212A product page for the most up-to-date application schematic and list of materials package before starting a new design.

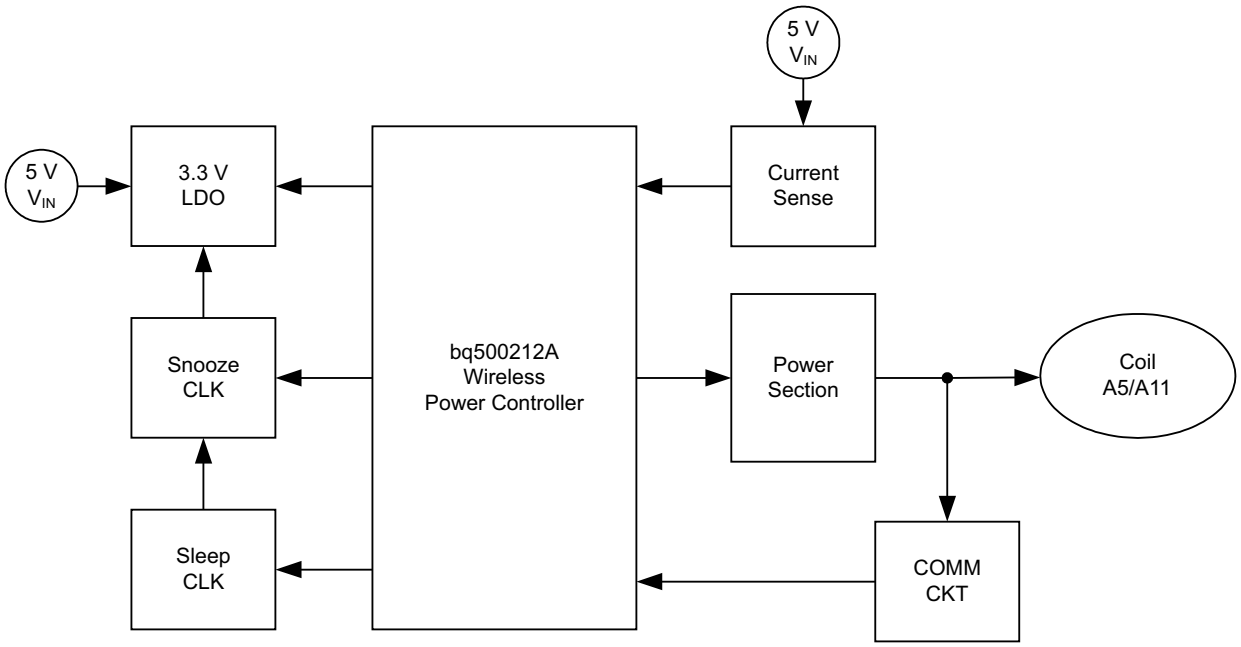


Figure 5. bq50012A Block Diagram

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Input Regulator

The bq500212A requires 3.3 VDC to operate. A buck regulator or a linear regulator can be used to step down from the 5-V system input. Either choice is fully WPC compatible, the decision lies in the user's requirements with respect to cost or efficiency.

For lowest cost the TLV70033 linear regulator is recommended.

Power Train

The bq500212A drives a phase-shifted full bridge. This is essentially twin half bridges and the choice of driver devices is quite simple; a pair of CSD97376 Integrated Power Stages are used. Other combinations using discrete driver and MOSFETs can work and system performance with regards to efficiency and EMI emissions will vary. Any alternate MOSFETs chosen must be fully saturated at the 5-V system gate drive voltage available and be sure to pay attention whether or not to use gate resistors; some tuning might be required.

PCB Layout

A good PCB layout is critical to proper system operation and due care should be taken. There are many references on proper PCB layout techniques.

Generally speaking, the system layout will require a 4-layer PCB layout, although a 2-layer PCB layout can be achieved. A proven and recommended approach to the layer stack-up has been:

- Layer 1, component placement and as much ground plane as possible.
- Layer 2, clean ground.
- Layer 3, finish routing.
- Layer 4, clean ground.

Thus, the circuitry is virtually sandwiched between grounds. This minimizes EMI noise emissions and also provides a noise free voltage reference plane for device operation.

Keep as much copper as possible. Make sure the bq500212A GND pins and the power pad have a continuous flood connection to the ground plane. The power pad should also be stitched to the ground plane, which also acts as a heat sink for the bq500212A. A good GND reference is necessary for proper bq500212A operation, such as analog-digital conversion, clock stability and best overall EMI performance.

Separate the analog ground plane from the power ground plane and use only one tie point to connect grounds. Having several tie points defeats the purpose of separating the grounds.

The COMM return signal from the resonant tank should be routed as a differential pair. This is intended to reduce stray noise induction. The frequencies of concern warrant low-noise analog signaling techniques, such as differential routing and shielding, but the COMM signal lines do not need to be impedance matched.

Typically a single chip controller solution with integrated power FET and synchronous rectifier will be used. To create a tight loop, pull in the buck inductor and power loop as close as possible. Likewise, the power-train, full-bridge components should be pulled together as tight as possible. See the bq500212AEVM-550, bqTESLA Wireless Power TX EVM User's Guide (Texas Instruments Literature Number SLVU536) for layout examples.

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References

1. *Building a Wireless Power Transmitter*, Application Report, (Texas Instruments Literature Number, SLUA635)
2. *Technology*, Wireless Power Consortium, www.wirelesspowerconsortium.com
3. *An Introduction to the Wireless Power Consortium Standard and TI's Compliant Solutions*, (Johns Bill, Texas Instruments)
4. *Integrated Wireless Power Supply Receiver, Qi (Wireless Power Consortium)*, BQ51013 Datasheet, (Texas Instruments Literature Number, SLUSAY6)

REVISION HISTORY

Changes from Original (July) to Revision A **Page**

- Changed 将销售状态从产品预览改为生产数据。 1

Changes from Revision A (August, 2013) to Revision B **Page**

- Changed 在整个文档内将 WPC1 改为 WPC1.1 1

Changes from Revision B (November 2013) to Revision C **Page**

- Changed RGZ pin package. 6
- Changed PIN 45 pin description. 8
- Changed bq50012A Schematic to bq50012A Block Diagram. 18

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ500212ARGZR	NRND	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 0	BQ500212A
BQ500212ARGZR.A	NRND	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 0	BQ500212A
BQ500212ARGZR.B	NRND	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 0	BQ500212A
BQ500212ARGZT	NRND	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 0	BQ500212A
BQ500212ARGZT.A	NRND	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 0	BQ500212A
BQ500212ARGZT.B	NRND	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 0	BQ500212A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

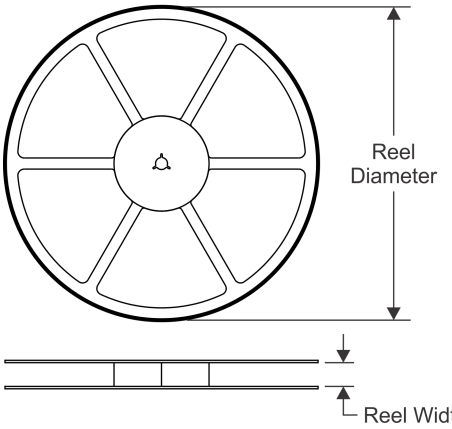
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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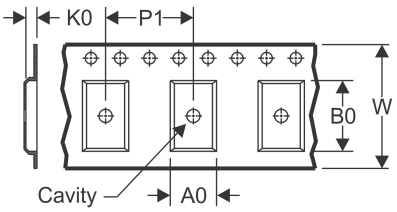
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

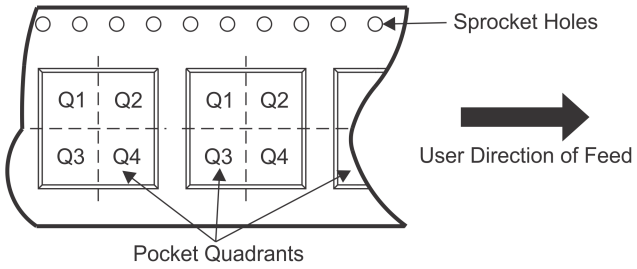


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

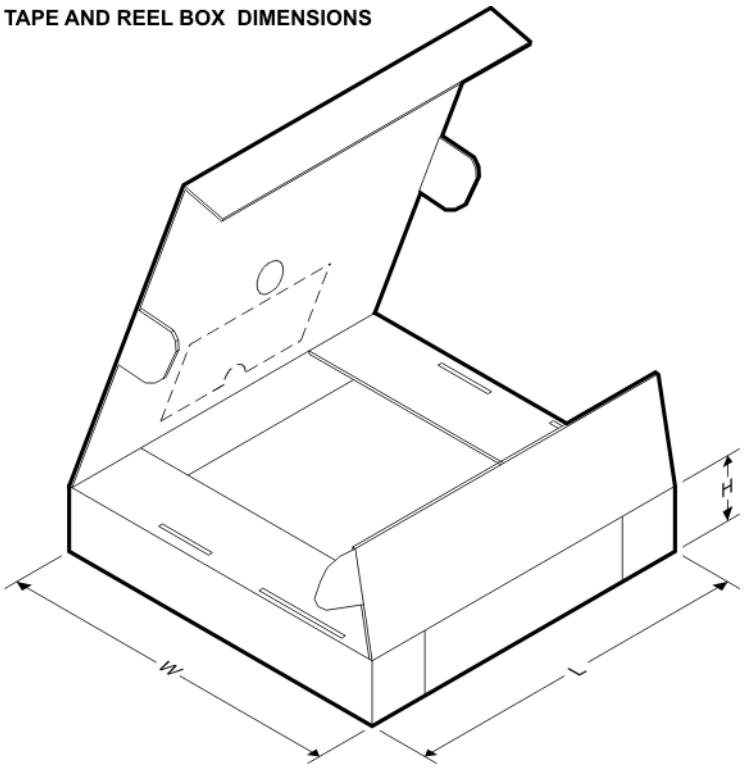
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ500212ARGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
BQ500212ARGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ500212ARGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
BQ500212ARGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

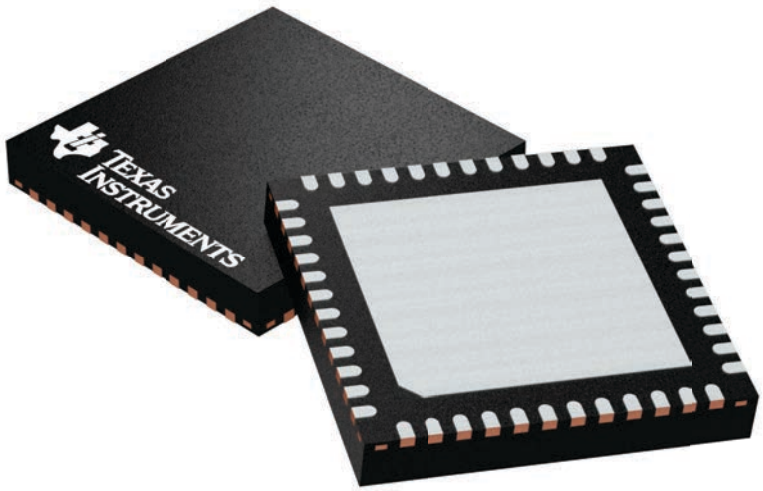
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

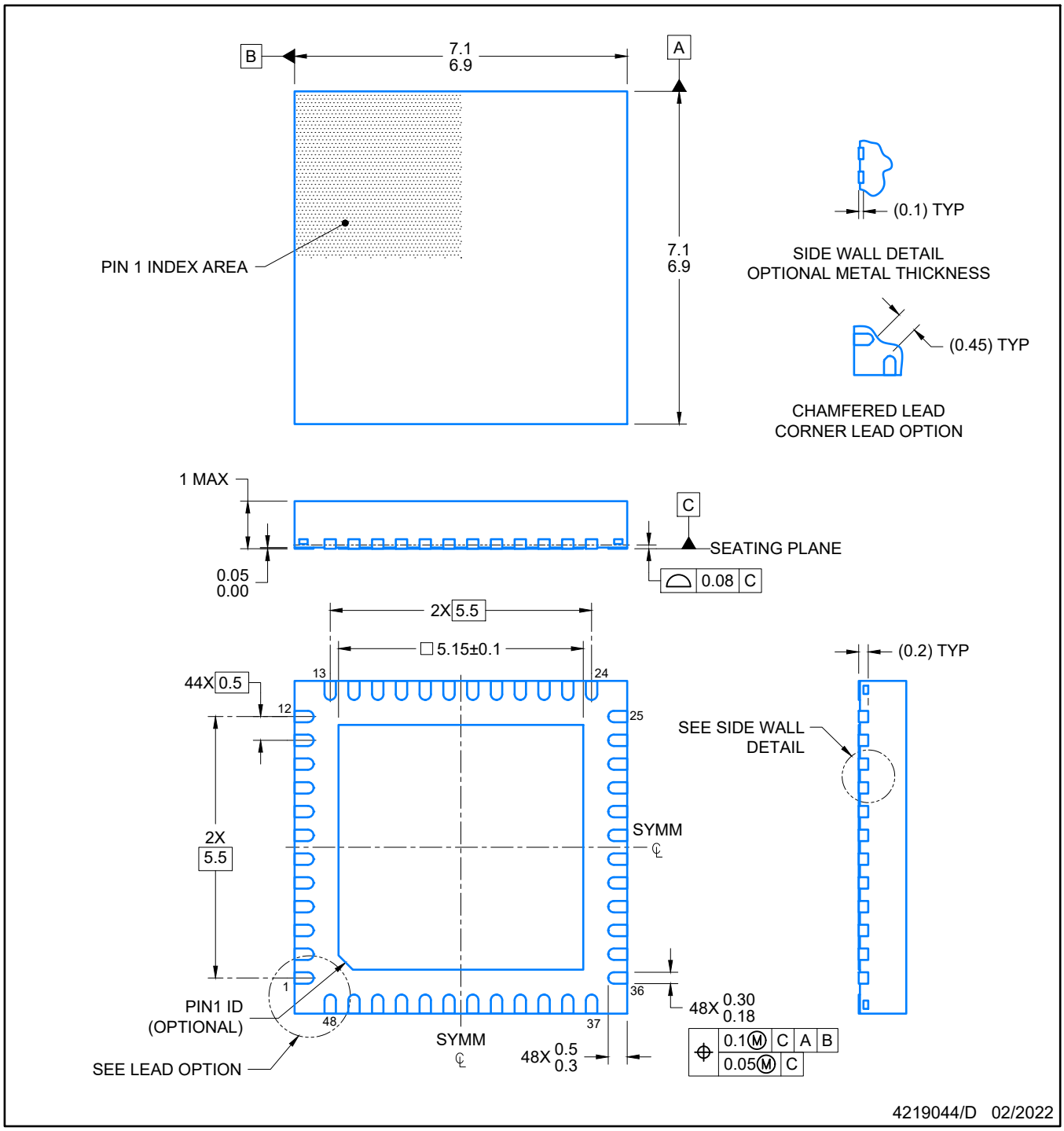
PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

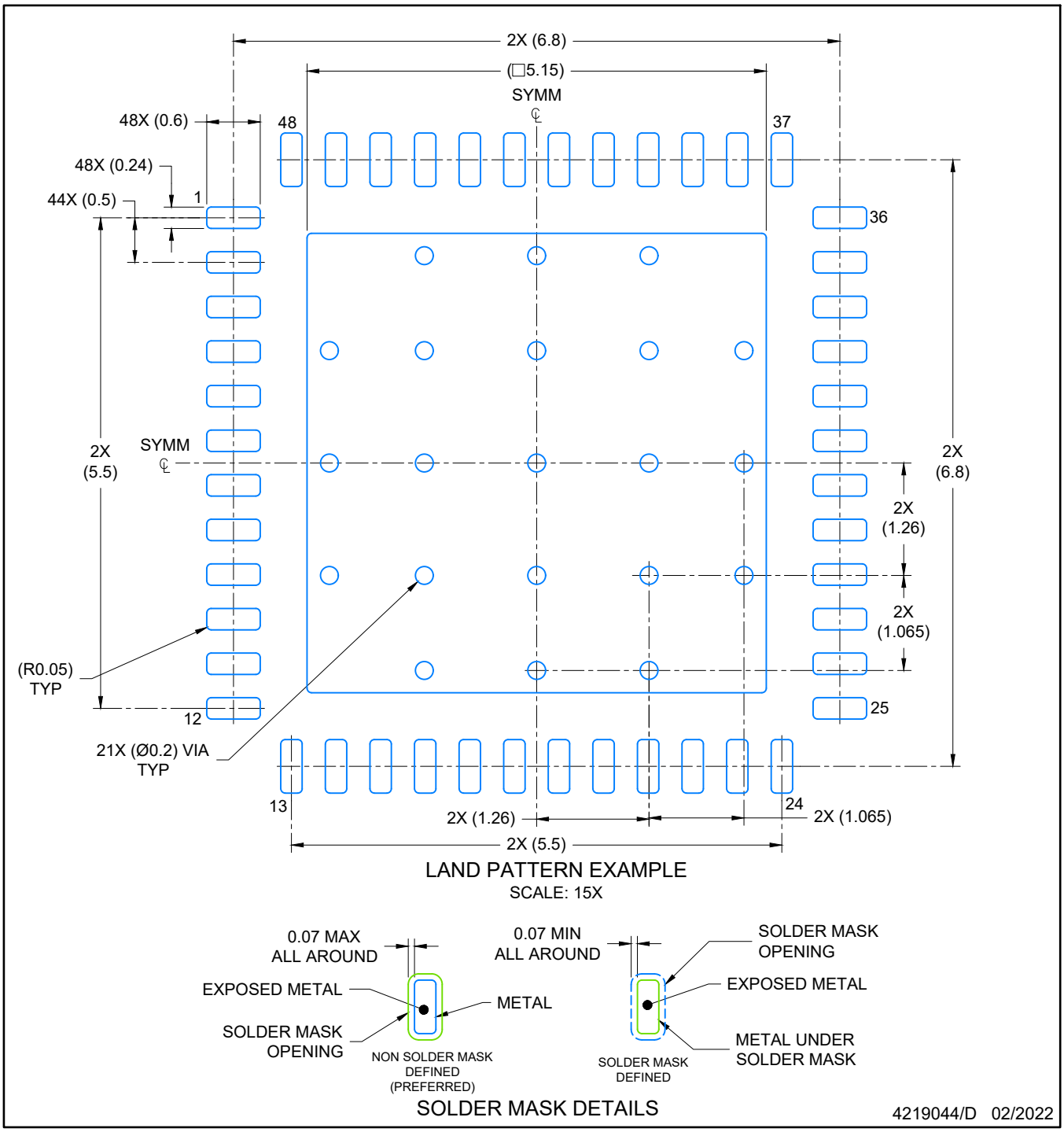
4224671/A

PLASTIC QUADFLAT PACK- NO LEAD



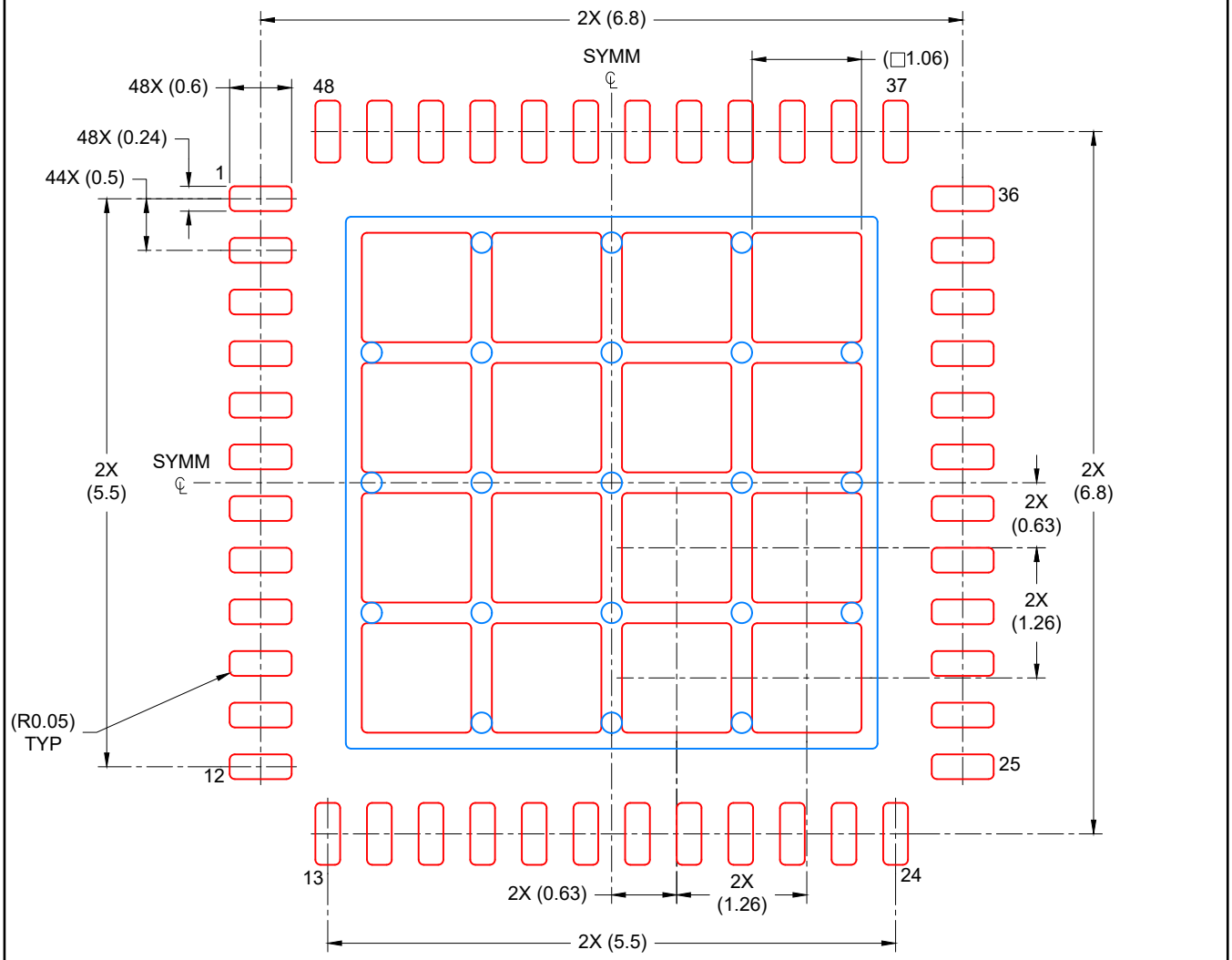
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

4219044/D 02/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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