集成型无线电源接收器，符合 Qi （无线电源联盟）标准

查询样品: bq51013A, bq51014

特性

- 支持 **5-V** 稳压电源的集成型无线电源接收器解决方案
  - **93%** 的整体峰值 **AC-DC** 效率
  - 完全同步整流器
  - 符合 **WPC v1.0** 标准的通信控制
  - 输出电压调节
  - **RX** 线圈与 **5-V DC** 输出电压之间仅需的 **IC**
- 针对经改进的负载瞬态响应的*动态整流器控制*
- 针对输出功率任一范围上已优化的性能的*动态性能调节*
- 针对高水平负载电流噪声期间稳健通信的*自适应通信限制*
- 支持 **20-V** 最大输入
- 低功耗耗散整流器过压钳位 **(V_{OVP} = 15 V)**
- 热关断
- 用于温度监控、充电完成和故障主机控制的多功能负温度系数热敏电阻 **(NTC)** 和控制引脚
- 独立数字控制器
- 用于充电状态 **100% (CS100)** 支持的可编程终止引脚
- 采用 **1.9 x 3mm** 晶圆级芯片规模封装 **(DSBG)** 或 **4.5 x 3.5mm** 四方扁平无引线 **(QFN)** 封装

应用范围

- 符合 **WPC** 标准的接收器
- 手机与智能电话
- 耳机
- 数码摄像机
- 便携式媒体播放器
- 手持式设备

说明

bq5101x 是一款适用于便携式应用无线电源传输的集成型高级接收器 IC， 此器件不但提供 AC/DC 电源转换，同时还集成符合 Qi v1.0 通信协议标准所需的数字控制功能。 bq5101x 与 bq500210 发送器控制器相结合，可为无线电源解决方案实现完整的非接触式电源传输系统。 通过使用近场感应电能传输，嵌入在便携式器件中的接收器线圈可通过相互耦合的电感器接受发送器线圈发出的电能。 来自接收器线圈的 AC 信号此后经过整流和调节，可用作系统关闭电子产品 (down-system electronics) 的电源。 全局反馈通过仅次于发送器的机制建立，以通过反散射调制稳定电源传输过程。 通过使用支持高达 5 W 应用的 Qi v1.0 通信协议来建立这个反馈。

该器件集成了一个低阻抗完全同步整流器、低压降稳压器、数字控制、和精确电压与电流环路。 整个功率级（整流器与 LDO）均采用低电阻 NMOS FET 技术以确保高效率与低功率耗散。

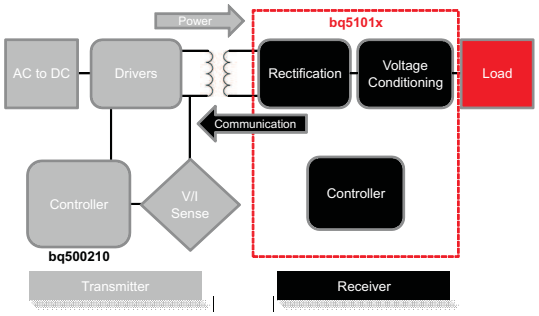


图 **1.** 无线电源联盟（**WPC** 或者 **Qi**）感应电源系统

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

Part NO	Marking	Function	Package	Ordering Number (Tape and Reel)	Quantity
bq51013A	bq51013A	5V Regulated Power Supply	DSBGA-YFP	bq51013AYFPR	3000
				bq51013AYFPT	250
			QFN-RHL	bq51013ARHLR	3000
				bq51013ARHLT	250
bq51014	bq51014	5V Regulated Power Supply	DSBGA-YFP	bq51014YFPR	3000
				bq51014YFPT	250

AVAILABLE OPTIONS

Device	Function	WPC Version	$V_{RECT-OVP}$	$V_{OUT-(REG)}$	Over Current Shutdown	AD-OVP	Termination (CS100)	Communication Current Limit(1) (2)
bq51013A	5V Power Supply	v1.0	15V	5V	Disabled	Disabled	Disabled	Tracking + 1s Hold-Off
bq51014	5V Power Supply	v1.0	15V	5V	Enabled	12.5V	Enabled	Tracking + 1s Hold-Off

(1) Enabled if EN2 is low and disabled if EN2 is high
(2) Communication current limit is disabled for 1 second at startup

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	PIN	VALUES		UNITS
		MIN	MAX	
Input Voltage	AC1, AC2, RECT, COM1, COM2, OUT, $\overline{CHG}$, CLAMP1, CLAMP2	-0.3	20	V
	AD, $\overline{AD\text{-}EN}$	-0.3	30	V
	BOOT1, BOOT2	-0.3	26	V
	EN1, EN2, TERM, FOD, TS-CTRL, ILIM	-0.3	7	V
Input Current	AC1, AC2		2	A(RMS)
Output Current	OUT		1.5	A
Output Sink Current	$\overline{CHG}$		15	mA
	COM1, COM2		1	A
Junction temperature, T_J		-40	150	°C
Storage temperature, T_{STG}		-65	150	°C
ESD Rating (HBM) (100pF, 1.5KΩ)	All	2		kV

(1) All voltages are with respect to the VSS terminal, unless otherwise noted.
(2) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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THERMAL INFORMATION

THERMAL METRIC(1)		RHL	YFP	UNITS
		20 PiNS	28 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	37.7	58.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	35.5	0.2	
θ_{JB}	Junction-to-board thermal resistance	13.6	9.1	
ψ_{JT}	Junction-to-top characterization parameter	0.5	1.4	
ψ_{JB}	Junction-to-board characterization parameter	13.5	8.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.7	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	PINS	MIN	MAX	UNITS
Input voltage range, V_{IN}	RECT	4	10	V
Input current, I_{IN}	RECT		1.5	A
Output current, I_{OUT}	OUT		1.5	A
Sink current, $I_{\overline{AD\text{-}EN}}$	$\overline{AD\text{-}EN}$		1	mA
COMM sink current, I_{COMM}	COMM		500	mA
Junction Temperature, T_J		0	125	ºC

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TYPICAL APPLICATION SCHEMATICS

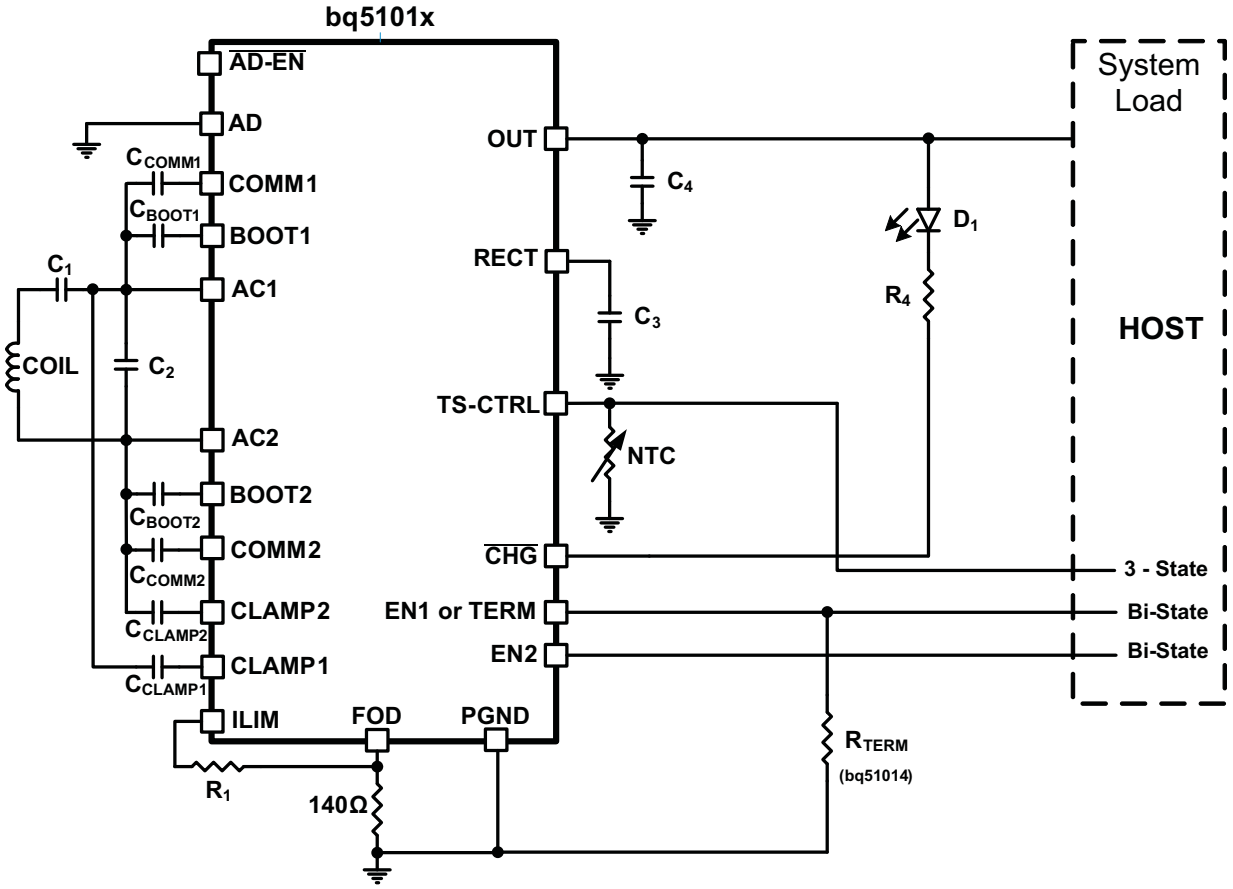


Figure 2. bq5101x Used as a Wireless Power Receiver and Power Supply for System Loads

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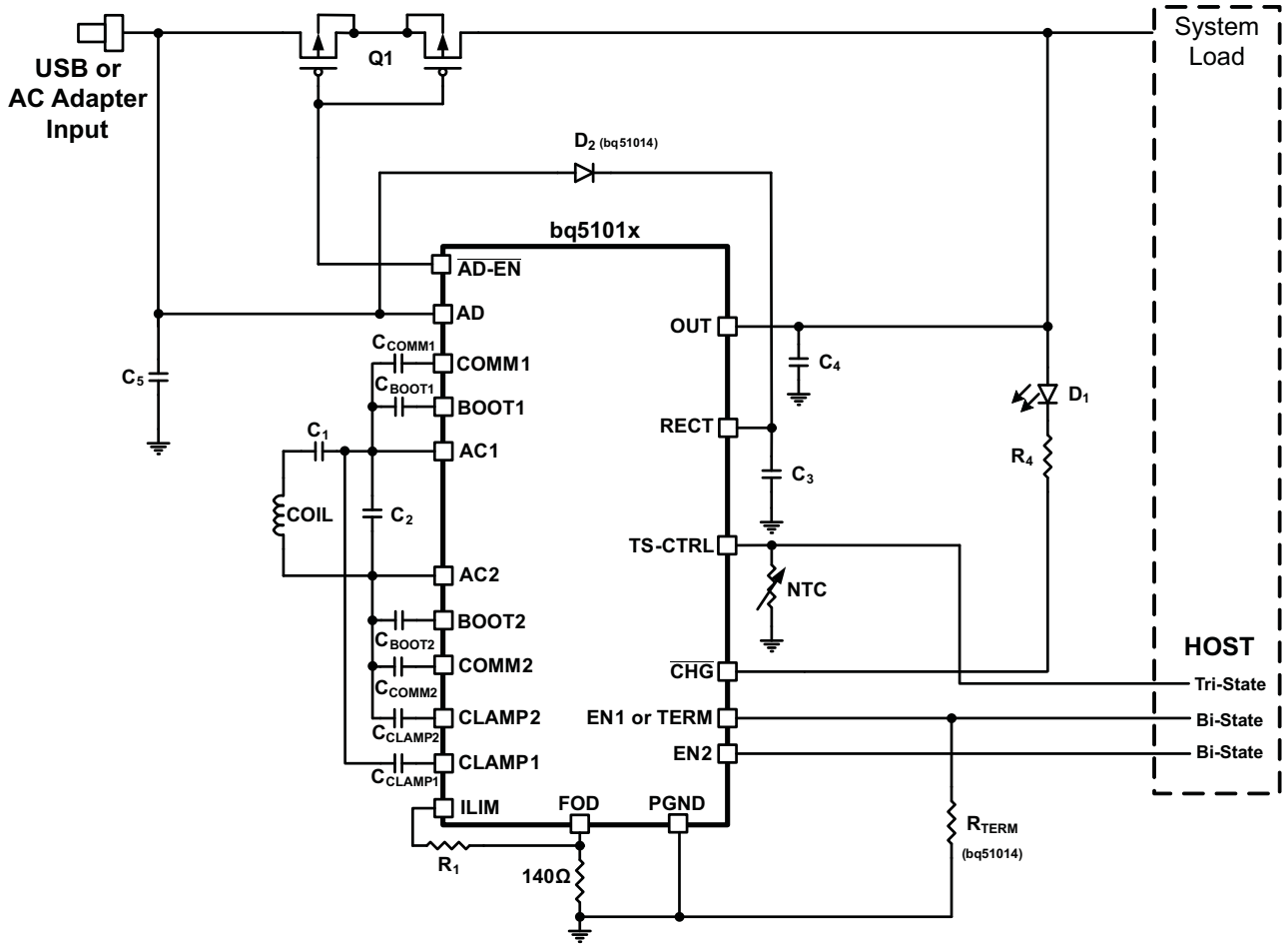


Figure 3. bq5101x Used as a Wireless Power Receiver and Power Supply for System Loads With Adapter Power-Path Multiplexing

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ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, 0°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO	Undervoltage lock-out	V_{RECT}: 0V → 3V	2.6	2.7	2.8	V
V_{HYS}	Hysteresis on UVLO	V_{RECT}: 3V → 2V		250		mV
	Hysteresis on OVP	V_{RECT}: 16V → 5V		150		mV
V_{RECT}	Input overvoltage threshold	V_{RECT}: 5V → 16V	14.5	15	15.5	V
$V_{RECT-REG}$	Dynamic V_{RECT} Threshold 1	I_{LOAD} < 0.1 x I_{ILIM} (I_{LOAD} rising)		7.08		V
	Dynamic V_{RECT} Threshold 2	0.1 x I_{ILIM} < I_{LOAD} < 0.2 x I_{ILIM} (I_{LOAD} rising)		6.28		
	Dynamic V_{RECT} Threshold 3	0.2 x I_{ILIM} < I_{LOAD} < 0.4 x I_{ILIM} (I_{LOAD} rising)		5.53		
	Dynamic V_{RECT} Threshold 4	I_{LOAD} > 0.4 x I_{ILIM} (I_{LOAD} rising)		5.11		
I_{LOAD}	I_{LOAD} Hysteresis for dynamic V_{RECT} thresholds as a % of I_{ILIM}	I_{LOAD} falling		4%		
$V_{RECT-DPM}$	Rectifier undervoltage protection, restricts I_{OUT} at $V_{RECT-DPM}$		3	3.1	3.2	V
$V_{RECT-REV}$	Rectifier reverse voltage protection at the output	$V_{RECT-REV}$ = V_{OUT} - V_{RECT}, V_{OUT} = 10V		8	9	V
Quiescent Current						
I_{RECT}	Active chip quiescent current consumption from RECT	I_{LOAD} = 0 mA, 0°C ≤ T_J ≤ 85°C		8	10	mA
		I_{LOAD} = 300 mA, 0°C ≤ T_J ≤ 85°C		2	3.0	mA
I_{OUT}	Quiescent current at the output when wireless power is disabled (Standby)	V_{OUT} = 5 V, 0°C ≤ T_J ≤ 85°C		20	35	µA
I_{LIM} Short Circuit						
R_{ILIM}	Highest value of I_{LIM} resistor considered a fault (short). Monitored for I_{OUT} > 100 mA	R_{ILIM}: 200Ω → 50Ω. I_{OUT} latches off, cycle power to reset			120	Ω
t_{DGL}	Deglitch time transition from I_{LIM} short to I_{OUT} disable			1		ms
I_{LIM_SC}	$I_{LIM-SHORT,OK}$ enables the I_{LIM} short comparator when I_{OUT} is greater than this value	I_{LOAD}: 0 → 20 0mA	120	145	165	mA
	Hysteresis for $I_{LIM-SHORT,OK}$ comparator	I_{LOAD}: 0 → 200 mA		30		mA
I_{OUT}	Maximum output current limit, C_L	Maximum I_{LOAD} that will be delivered for 1 ms when I_{LIM} is shorted			2.4	A
OUTPUT						
$V_{OUT-REG}$	Regulated output voltage	I_{LOAD} = 1000 mA	4.85	4.95	5	V
		I_{LOAD} = 10 mA	4.95	5	5.05	
K_{ILIM}	Current programming factor for hardware short circuit protection	R_{LIM} = K_{ILIM} / I_{ILIM}, where I_{ILIM} is the hardware current limit. I_{OUT} = 1 A	280	300	320	AΩ
K_{IMAX}	Current programming factor for the nominal operating current	I_{IMAX} = K_{IMAX} / R_{LIM} where I_{MAX} is the maximum normal operating current. I_{OUT} = 1 A	230	250	270	AΩ
I_{OUT}	Current limit programming range				1500	mA
I_{COMM}	Current limit during WPC communication	I_{OUT} > 300 mA		I_{OUT} + 50		mA
		I_{OUT} < 300 mA	365	390	420	mA
t_{HOLD}	Hold off time for the communication current limit during startup			1		s

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, 0°C to 125°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
TERMINATION (Charge Status 100%) – bq51014 ONLY							
K_{TERM}	Programmable termination factor as a percentage of I_{MAX}		R_{TERM} = %I_{MAX} x K_{TERM}	160	200	240	Ω/%
I_{TERM}	High termination current threshold calculation		$I_{TERM-HI} = (R_{TERM} / K_{TERM}) \times 0.01 \times I_{MAX}$, where $I_{MAX} = K_{IMAX} / R_{ILIM}$				
	Low termination current threshold				25		mA
	Constant current at the TERM pin to bias the termination resistor		V_{TERM} = 0 V	48	51	54	µA
t_{TERM}	High termination threshold deglitch		$I_{TERM-LOW} < I_{OUT} < I_{TERM-HI}$		180		sec
	High termination threshold deglitch		$I_{OUT} < I_{TERM-LOW}$		7		sec
TS / CTRL							
V_{TS}	Internal TS Bias Voltage		$I_{TS-Bias}$ < 100 µA (periodically driven see $t_{TS-CTRL}$)	2	2.2	2.4	V
V_{COLD}	Rising threshold		V_{TS}: 50% → 60%	56.5	58.7	60.8	%$V_{TS-Bias}$
	Falling hysteresis		V_{TS}: 60% → 50%		1		
V_{HOT}	Falling threshold		V_{TS}: 20% → 15%	18.5	19.6	20.7	
	Rising hysteresis		V_{TS}: 15% → 20%		1		
V_{CTRL}	CTRL pin threshold for a high		$V_{TS/CTRL}$: 50 → 150mV	80	100	130	mV
	CTRL pin threshold for a low		$V_{TS/CTRL}$: 150 → 50mV	50	80	100	mV
$t_{TS-CTRL}$	Time VTS-Bias is active when TS measurements occur		Synchronous to the communication period		24		ms
t_{TS}	Deglitch time for all TS comparators				10		ms
R_{TS}	Pull-up resistor for the NTC network. Pulled up to the voltage bias			18	20	22	kΩ
THERMAL PROTECTION							
T_J	Thermal shutdown temperature				155		°C
	Thermal shutdown hysteresis				20		°C
OUTPUT LOGIC LEVELS ON $\overline{WPG}$							
V_{OL}	Open drain $\overline{WPG}$ pin		I_{SINK} = 5 mA			500	mV
I_{OFF}	$\overline{WPG}$ leakage current when disabled		$V_{\overline{CHG}}$ = 20 V			1	µA
COMM PIN							
$R_{DS(ON)}$	COM1 and COM2		V_{RECT} = 2.6 V		1.5		Ω
f_{COMM}	Signaling frequency on COMM pin				2.00		Kb/s
I_{OFF}	Comm pin leakage current		V_{COM1} = 20 V, V_{COM2} = 20 V			1	µA
CLAMP PIN							
$R_{DS(ON)}$	Clamp1 and Clamp2				1		Ω
Adapter Enable							
$V_{\overline{AD-EN}}$	V_{AD} Rising threshold voltage. EN-UVLO		V_{AD} 0 → 5 V	3.5	3.6	3.8	V
	$V_{\overline{AD-EN}}$ hysteresis, EN-HYS		V_{AD} 5 → 0 V		400		mV
I_{AD}	Input leakage current		V_{RECT} = 0V, V_{AD} = 5V			60	µA
V_{AD-OVP}	Adapter mode OVP threshold rising edge	bq51014	V_{AD} 10 → 15 V	12	12.5	13	V
	V_{AD-OVP} hysteresis		V_{AD} 15 → 10 V		0.5		V
R_{AD}	Pull-up resistance from $\overline{AD-EN}$ to OUT when adapter mode is disabled and V_{OUT} > V_{AD}, EN-OUT		V_{AD} = 0, V_{OUT} = 5		200	350	Ω
V_{AD}	Voltage difference between V_{AD} and $V_{\overline{AD-EN}}$ when adapter mode is enabled, EN-ON		V_{AD} = 5 V, 0°C ≤ T_J ≤ 85°C	3	4.5	5	V

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ELECTRICAL CHARACTERISTICS (continued)

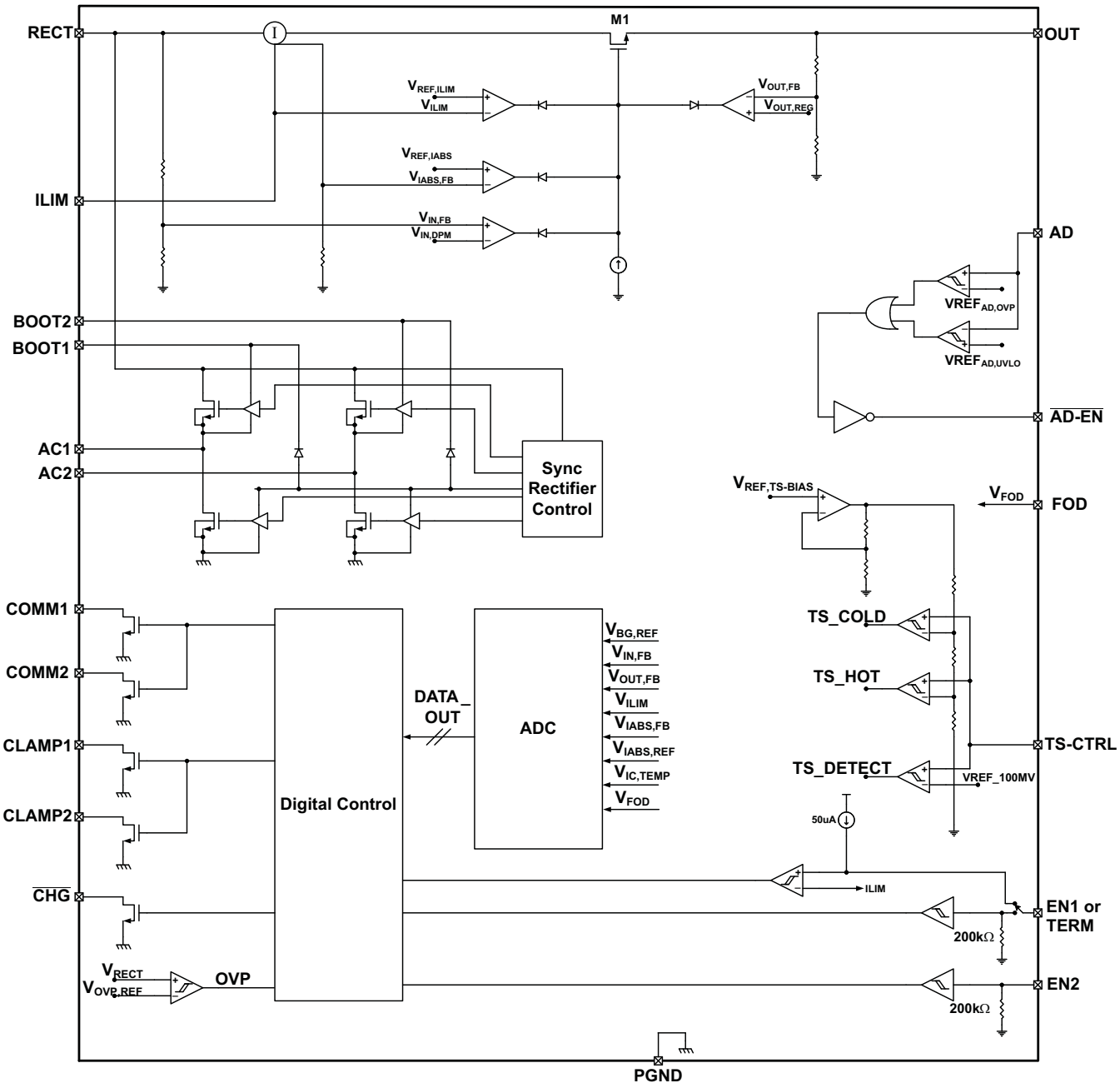
over operating free-air temperature range, 0°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Synchronous Rectifier						
I_{OUT}	I_{OUT} at which the synchronous rectifier enters half synchronous mode, SYNC_EN	I_{LOAD} 200 → 0 mA	80	100	125	mA
	Hysteresis for $I_{OUT,RECT-EN}$ (full-synchronous mode enabled)	I_{LOAD} 0 → 200 mA		25		mA
$V_{HS-DIODE}$	High-side diode drop when the rectifier is in half synchronous mode	$I_{AC-VRECT}$ = 250 mA and T_J = 25°C		0.7		V
EN1 and EN2						
V_{IL}	Input low threshold for EN1 and EN2				0.4	V
V_{IH}	Input high threshold for EN1 and EN2		1.3			V
R_{PD}	EN1 and EN2 pull down resistance			200		kΩ
ADC (WPC Related Measurements and Coefficients)						
P_{RECT}	Rectified power accuracy as a percentage of output power	0W – 5W of rectified power		±6		%

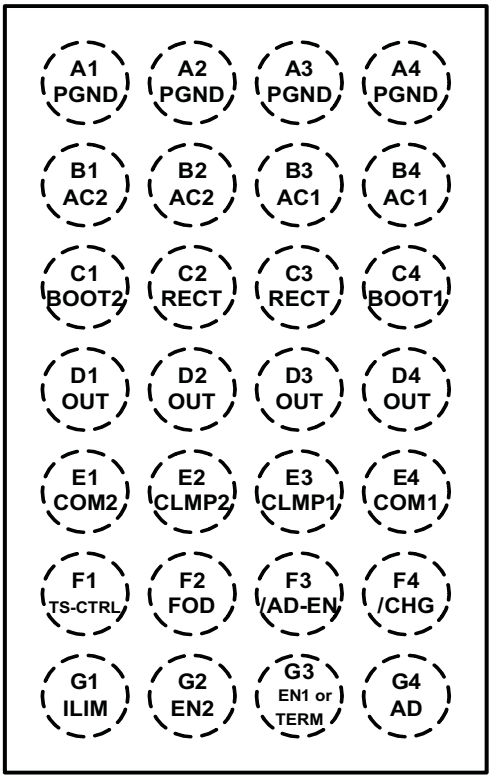
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DEVICE INFORMATION

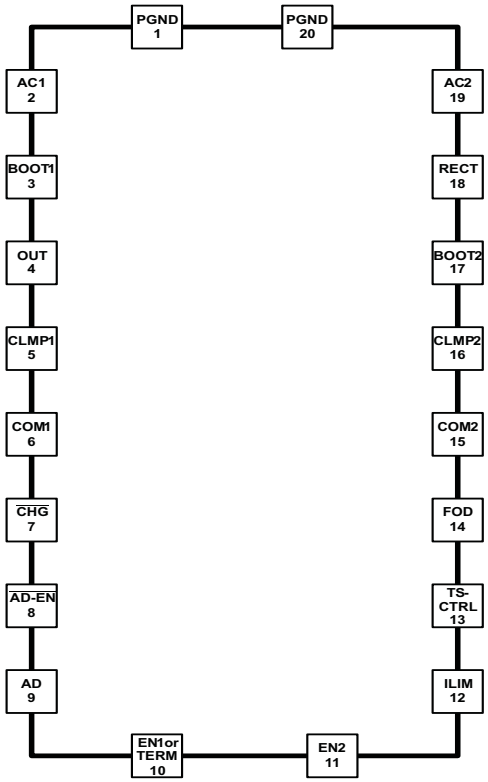
SIMPLIFIED BLOCK DIAGRAM



YFP Package
(TOP VIEW)



RHL Package
(TOP VIEW)



PIN FUNCTIONS

NAME	YFP	RHL	I/O	DESCRIPTION
AC1	B3, B4	2	I	AC input from receiver coil antenna.
AC2	B1, B2	19	I	
BOOT1	C4	3	O	Bootstrap capacitors for driving the high-side FETs of the synchronous rectifier. Connect a 10 nF ceramic capacitor from BOOT1 to AC1 and from BOOT2 to AC2.
BOOT2	C1	17	O	
RECT	C2, C3	18	O	Filter capacitor for the internal synchronous rectifier. Connect a ceramic capacitor to PGND. Depending on the power levels, the value may be 4.7 µF to 22 µF.
OUT	D1, D2, D3, D4	4	O	Output pin, delivers power to the load.
COM1	E4	6	O	Open-drain output used to communicate with primary by varying reflected impedance. Connect through a capacitor to either AC1 or AC2 for capacitive load modulation (COM2 must be connected to the alternate AC1 or AC2 pin). For resistive modulation connect COM1 and COM2 to RECT via a single resistor; connect through separate capacitors for capacitive load modulation.
COM2	E1	15	O	Open-drain output used to communicate with primary by varying reflected impedance. Connect through a capacitor to either AC1 or AC2 for capacitive load modulation (COM1 must be connected to the alternate AC1 or AC2 pin). For resistive modulation connect COM1 and COM2 to RECT via a single resistor; connect through separate capacitors for capacitive load modulation.
CLMP2	E2	16	O	Open drain FETs which are utilized for a non-power dissipative over-voltage AC clamp protection. When the RECT voltage goes above 15 V, both switches will be turned on and the capacitors will act as a low impedance to protect the IC from damage. If used, Clamp1 is required to be connected to AC1, and Clamp2 is required to be connected to AC2 via 0.47µF capacitors.
CLMP1	E3	5	O	
PGND	A1, A2, A3, A4	1, 20		Power ground

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PIN FUNCTIONS (continued)

NAME	YFP	RHL	I/O	DESCRIPTION
ILIM	G1	12	I/O	Programming pin for the over current limit. Connect external resistor to VSS. Size R_{ILIM} with the following equation: R_{ILIM} = 250 / I_{MAX} where IMAX is the expected maximum output current of the wireless power supply. The hardware current limit (IILIM) will be 20% greater than IMAX or 1.2 x 1_{MAX}. If the supply is meant to operate in current limit use R_{ILIM} = 300 / I_{ILIM} R_{ILIM} = R1 + 140
AD	G4	9	I	Connect this pin to the wired adapter input. When a voltage is applied to this pin wireless charging is disabled and AD_EN is driven low. Connect to GND through a 1 µF capacitor. If unused, capacitor is not required and should be grounded directly. For the bq51014, there is an OVP protection of 12.5 V. If the AD voltage is greater than 12.5 V, wireless charging will remain active.
$\overline{\text{AD-EN}}$	F3	8	O	Push-pull driver for external PFET connecting AD and OUT. This node is pulled to the higher of OUT and AD when turning off the external FET. This voltage tracks approximately 4 V below AD when voltage is present at AD and provides a regulated VSG bias for the external FET. Float this pin if unused.
TS-CTRL	F1	13	I	Must be connected to ground via a resistor. If an NTC function is not desired connect to GND with a 10 kΩ resistor. As a CTRL pin pull to ground to send end power transfer (EPT) fault to the transmitter or pull-up to an internal rail (i.e. 1.8 V) to send EPT termination to the transmitter. Note that a 3-state driver should be used to interface this pin (see the 3-state Driver section for further description)
EN1	G3	10	I	Inputs that allow user to enable/disable wireless and wired charging <EN1 EN2>: <00> wireless charging is enabled unless AD voltage > 3.6 V <01> Dynamic communication current limit disabled <10> $\overline{\text{AD-EN}}$ pulled low, wireless charging disabled <11> wired and wireless charging disabled.
EN2	G2	11	I	
TERM	G3	10	I	Input that allows allows the upper termination threshold ($I_{TERM-HI}$) to be programmable. K_{TERM} = 200 Ω/%. Set the termination threshold by applying the following equation R_{TERM} = %I_{MAX} x K_{TERM} where %IMAX is the desired percentage of the maximum output current when termination should occur (i.e. 10% of 1 A = 0.1 mA)
FOD	F2	14	O	Input for the rectified power measurement. Connect to GND with a 140 Ω resistor
$\overline{\text{CHG}}$	F4	7	O	Open-drain output – active when output current is being delivered to the load (i.e. when the output of the supply is enabled).

TYPICAL CHARACTERISTICS

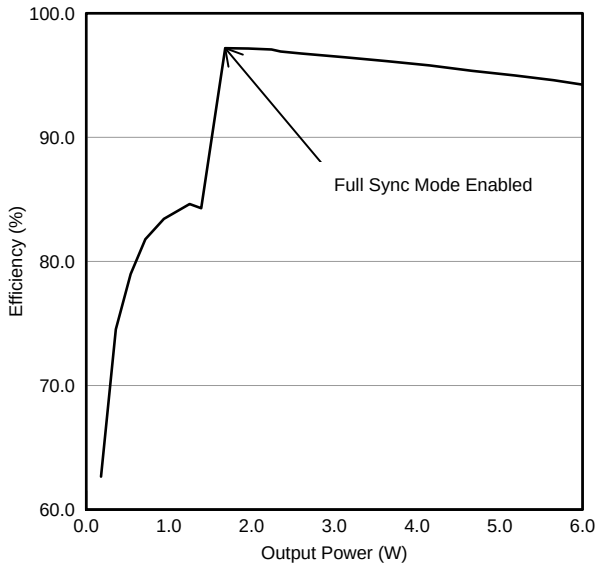


Figure 4. Rectifier Efficiency

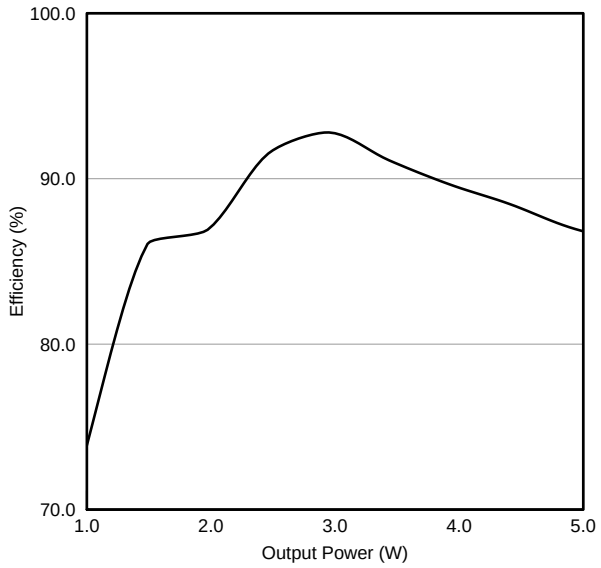


Figure 5. IC Efficiency from AC Input to DC Output

TYPICAL CHARACTERISTICS (continued)

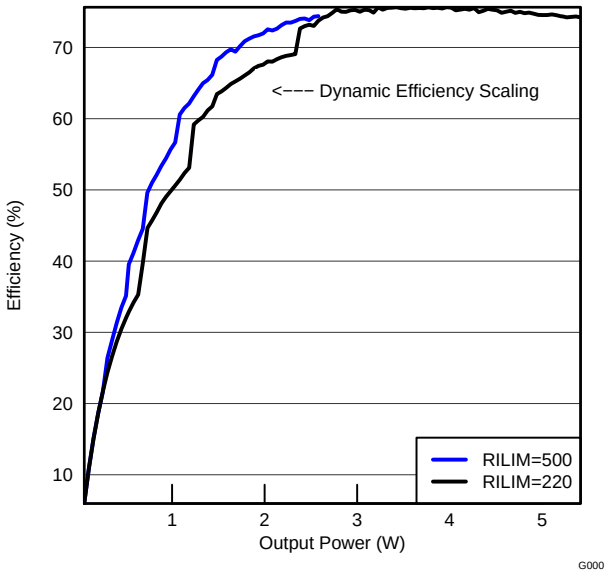


Figure 6. Light Load Efficiency Improvement due to Dynamic Efficiency Scaling Feature(1)

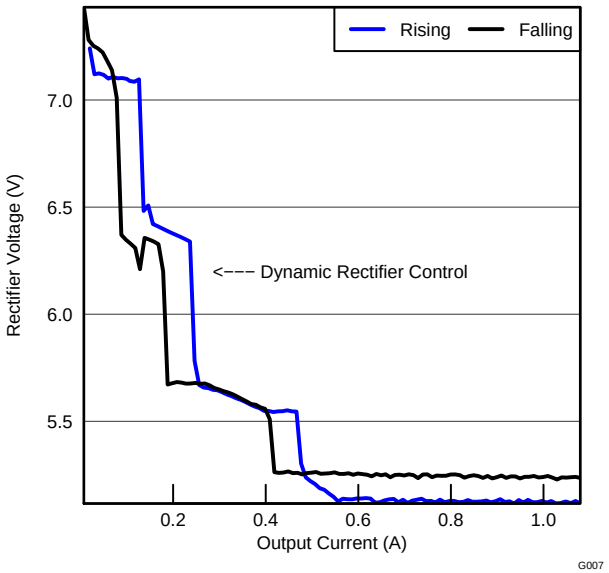


Figure 7. V_{RECT} vs. I_{LOAD}at R_{ILIM} = 220Ω

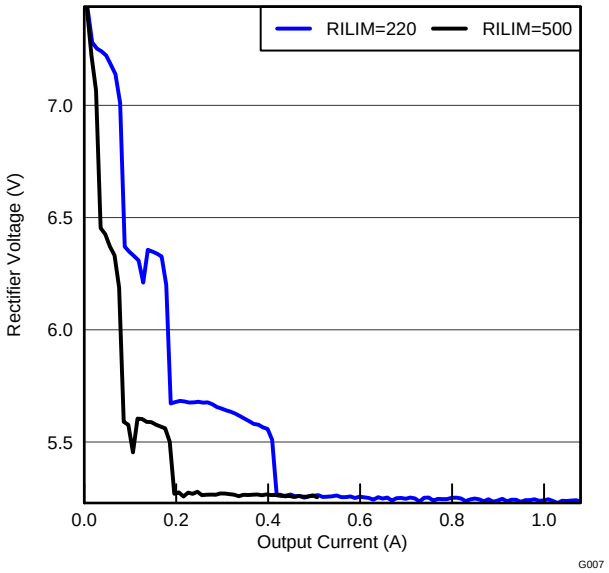


Figure 8. V_{RECT} vs. I_{LOAD} at R_{ILIM} = 220 Ω and 500 Ω

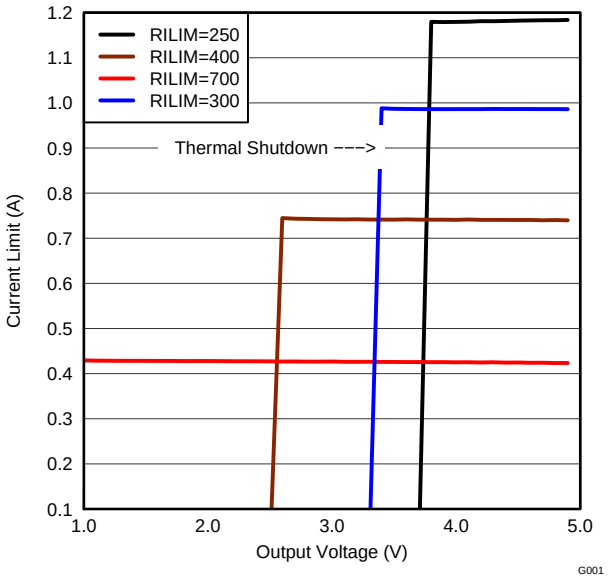


Figure 9. V_{OUT} Sweep (I-V Curve)(2)

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TYPICAL CHARACTERISTICS (continued)

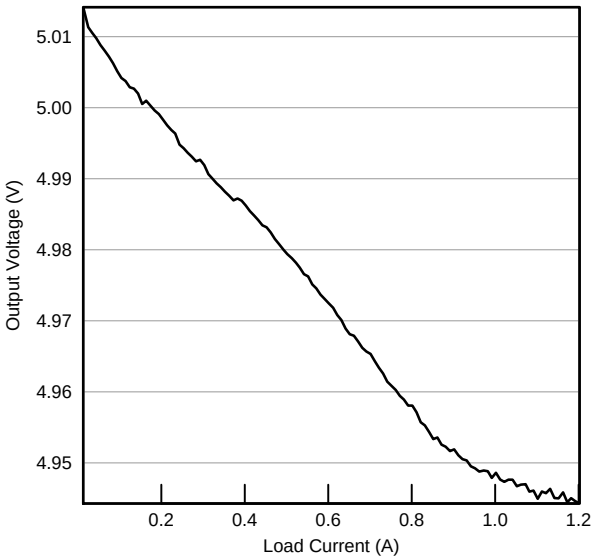


Figure 10. I_{LOAD} Sweep (I-V Curve)

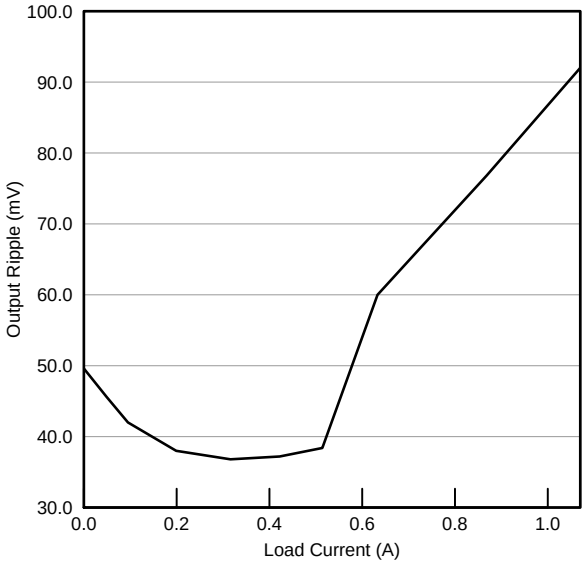


Figure 11. Output Ripple vs. I_{LOAD} (C_{OUT} = 1µF)

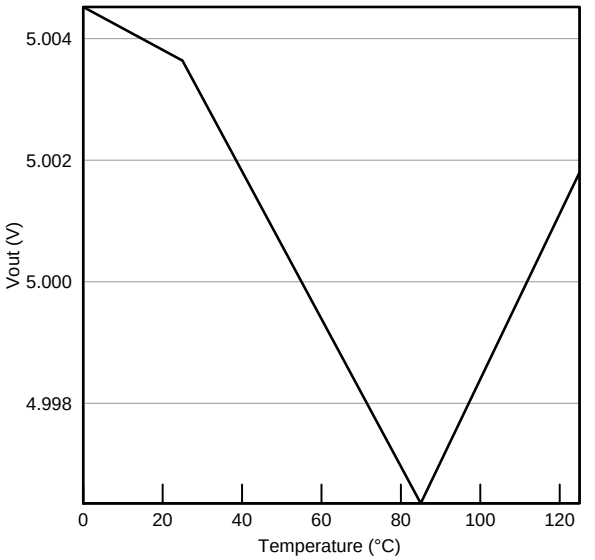


Figure 12. V_{OUT} vs Temperature

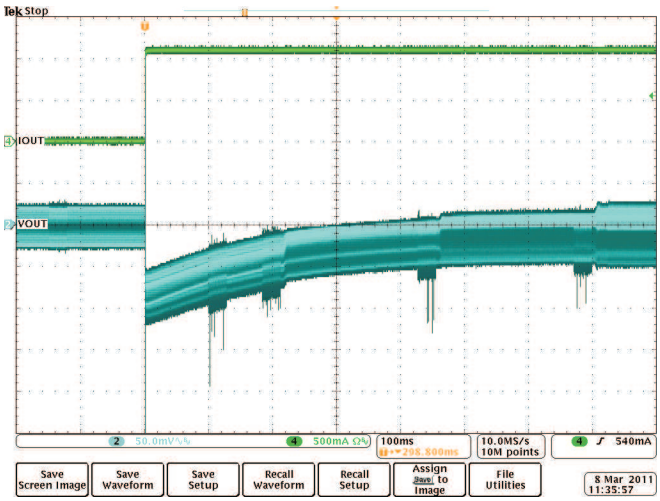


Figure 13. 1A Instantaneous Load Step(3)

TYPICAL CHARACTERISTICS (continued)

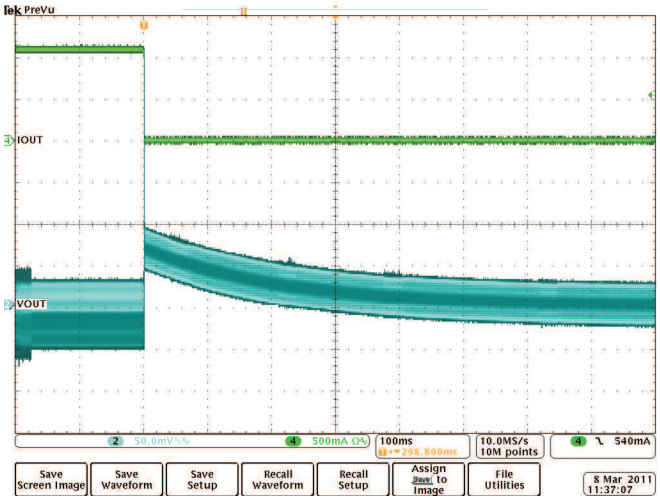


Figure 14. 1A Instantaneous Load Dump(3)

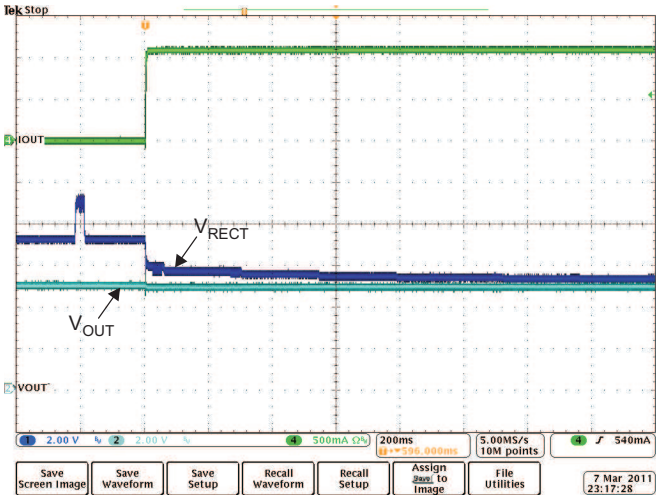


Figure 15. 1A Load Step Full System Response

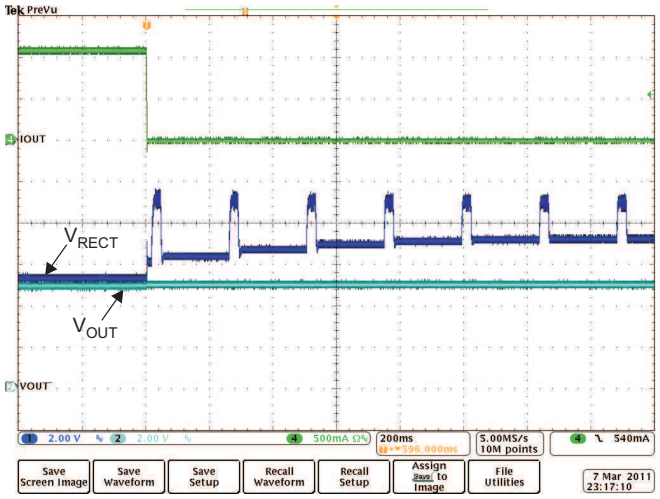


Figure 16. 1A Load Dump Full System Response

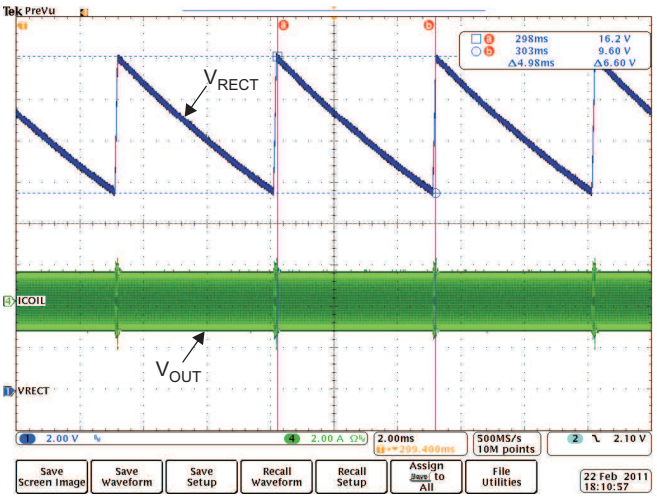


Figure 17. Rectifier Overvoltage Clamp (f_{op} = 110kHz)

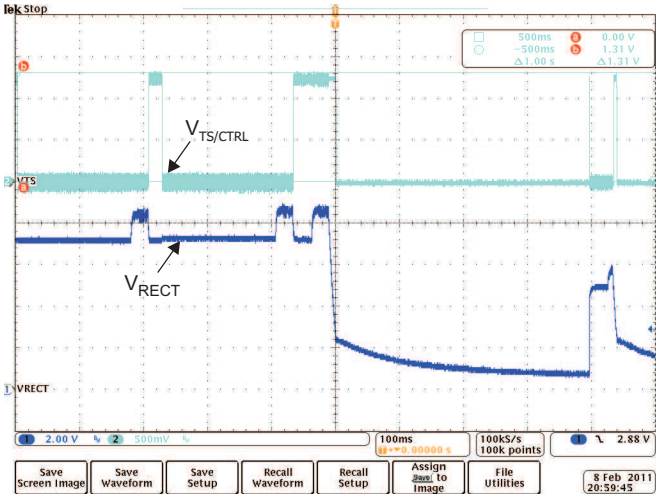


Figure 18. TS Fault

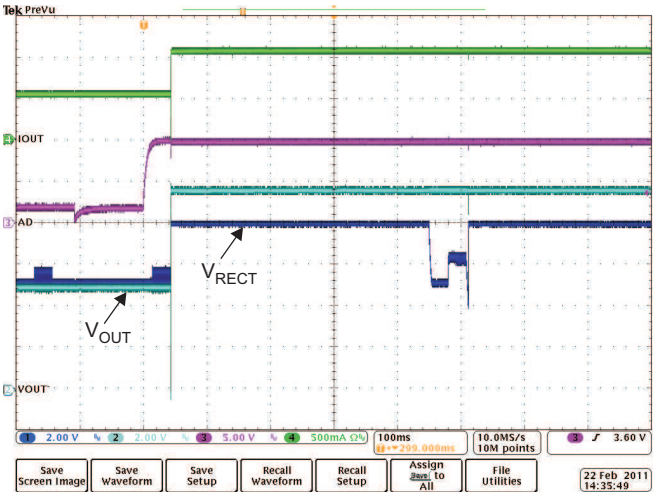


Figure 19. Adapter Insertion (V_{AD} = 10V)

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TYPICAL CHARACTERISTICS (continued)

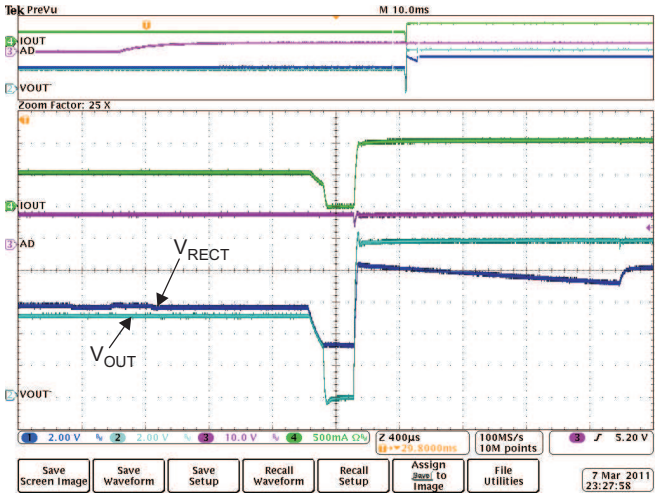


Figure 20. Adapter Insertion (V_{AD} = 10V) Illustrating Break-Before-Make Operation

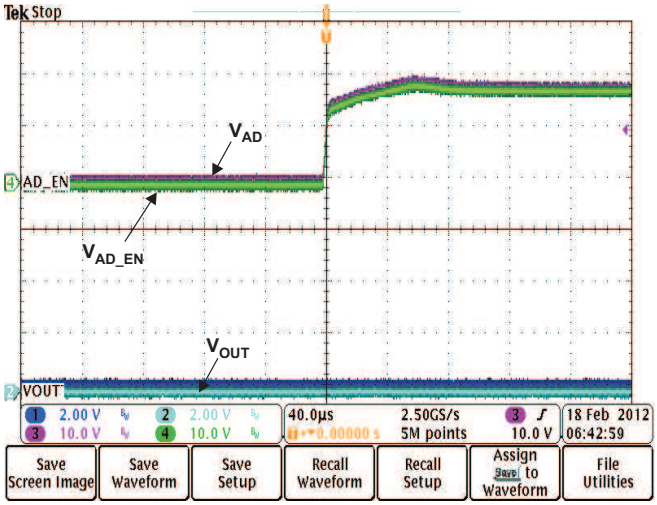


Figure 21. 20V adapter Insertion with AD OVP Enabled (bq51014) and Wireless Power not Present

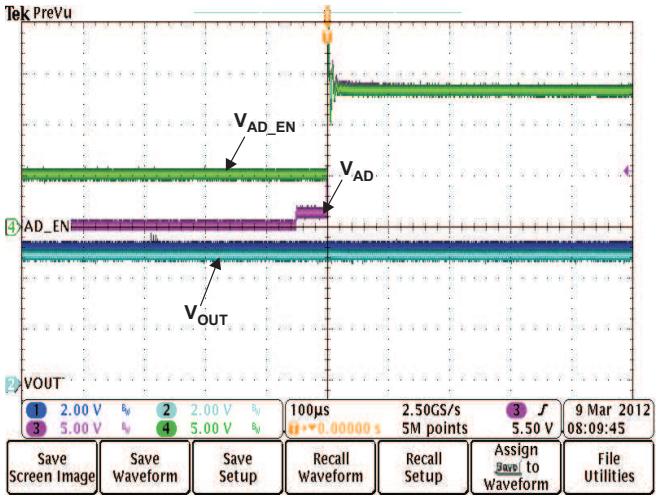


Figure 22. AD OVP Condition While Wireless Charging is Active (bq51014)

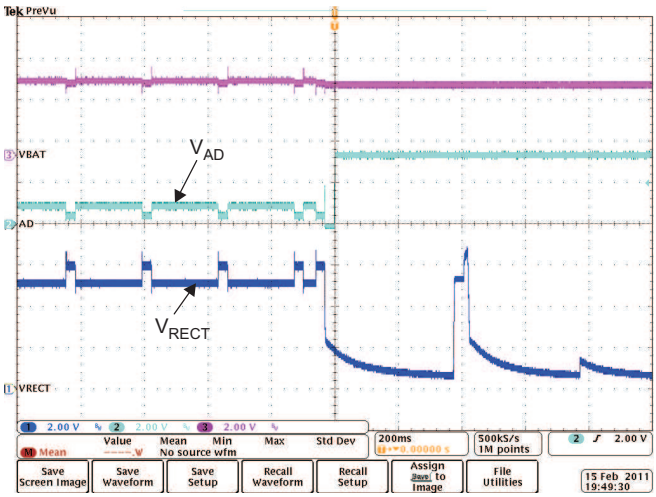


Figure 23. On the Go Enabled (V_{OTG} = 3.5V)(4)

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TYPICAL CHARACTERISTICS (continued)

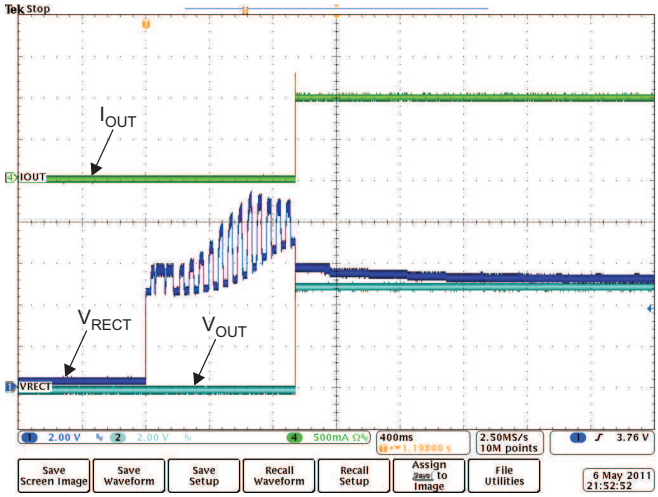


Figure 24. bq5101x Typical Startup with a 1A System Load

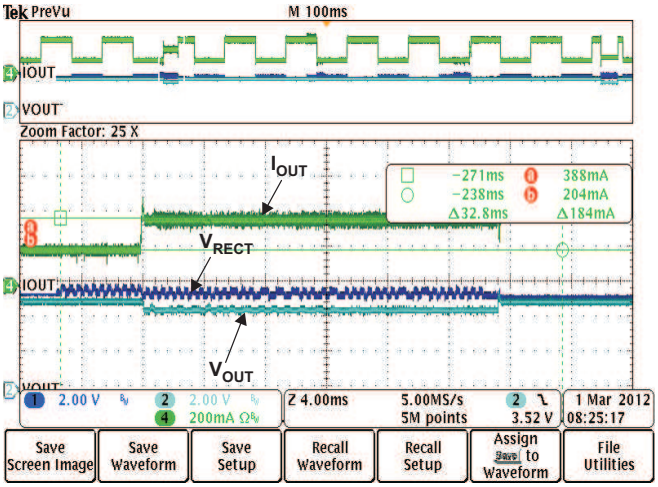


Figure 25. Adaptive Communication Limit Event Where the 400 mA Current Limit is Enabled (I_{OUT-DC} < 300 mA)

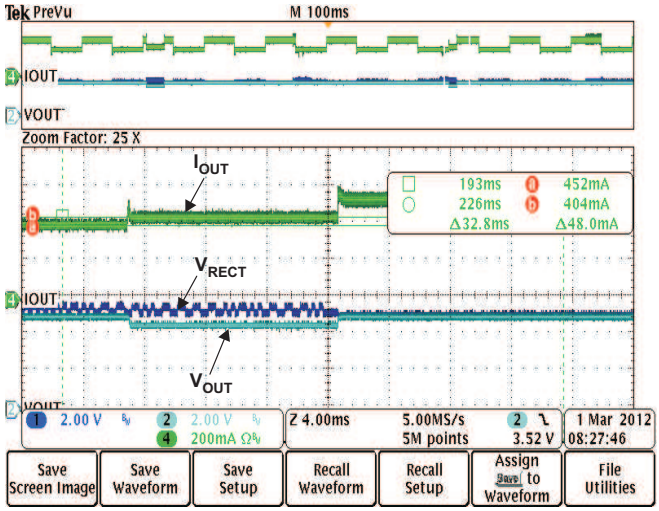


Figure 26. Adaptive Communication Limit Event Where the Current Limit is I_{OUT} + 50 mA (I_{OUT-DC} > 300 mA)

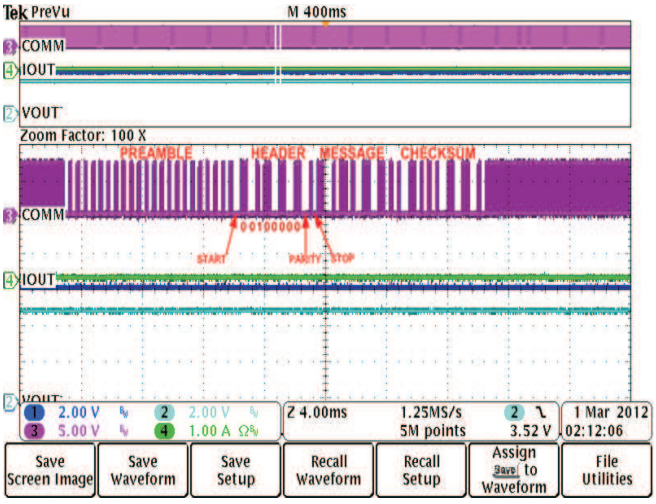


Figure 27. Rx Communication Packet Structure

(1) Efficiency measured from DC input to the transmitter to DC output of the receiver. Transmitter was the bq500210 EVM. Measurement subject to change if an alternate transmitter is used.

(2) Curves illustrates the resulting I_{LIM} current by sweeping the output voltage at different R_{ILIM} settings. ILIM current collapses due to the increasing power dissipation as the voltage at the output is decreased—thermal shutdown is occurring.

(3) Total droop experienced at the output is dependent on receiver coil design. The output impedance must be low enough at that particular operating frequency in order to not collapse the rectifier below 5V.

(4) On the go mode is enabled by driving EN1 high. In this test the external PMOS is connected between the output of the bq5101x IC and the AD pin; therefore, any voltage source on the output is supplied to the AD pin.

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PRINCIPLE OF OPERATION

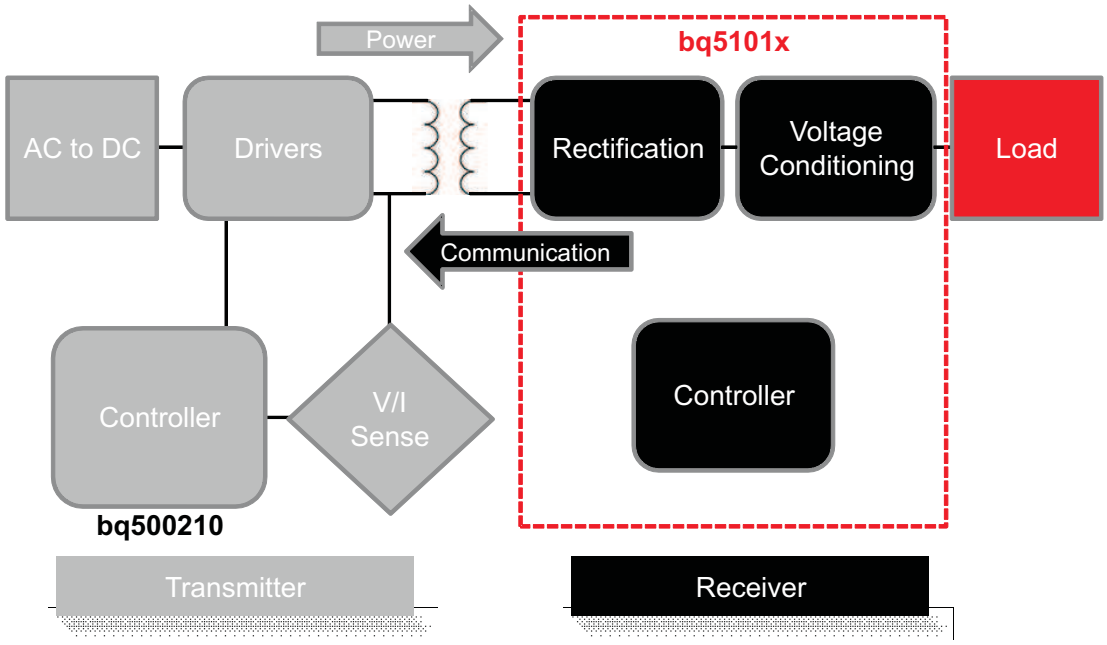


Figure 28. WPC Wireless Power System Indicating the Functional Integration of the bq5101x

A Brief Description of the Wireless System:

A wireless system consists of a charging pad (transmitter or primary) and the secondary-side equipment (receiver or secondary). There is a coil in the charging pad and in the secondary equipment which are magnetically coupled to each other when the secondary is placed on the primary. Power is then transferred from the transmitter to the receiver via coupled inductors (e.g. an air-core transformer). Controlling the amount of power transferred is achieved by sending feedback (error signal) communication to the primary (e.g. to increase or decrease power).

The receiver communicates with the transmitter by changing the load seen by the transmitter. This load variation results in a change in the transmitter coil current, which is measured and interpreted by a processor in the charging pad. The communication is digital - packets are transferred from the receiver to the transmitter. Differential Bi-phase encoding is used for the packets. The bit rate is 2-kbps.

Various types of communication packets have been defined. These include identification and authentication packets, error packets, control packets, end power packets, and power usage packets.

The transmitter coil stays powered off most of the time. It occasionally wakes up to see if a receiver is present. When a receiver authenticates itself to the transmitter, the transmiter will remain powered on. The receiver maintains full control over the power transfer using communication packets.

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Using the bq5101x as a Wireless Power Supply: (See Figure 3)

Figure 3 is the schematic of a system which uses the bq5101x as power supply while power multiplexing the wired (adapter) port.

When the system shown in Figure 3 is placed on the charging pad, the receiver coil is inductively coupled to the magnetic flux generated by the coil in the charging pad which consequently induces a voltage in the receiver coil. The internal synchronous rectifier feeds this voltage to the RECT pin which has the filter capacitor C3.

The bq5101x identifies and authenticates itself to the primary using the COM pins by switching on and off the COM FETs and hence switching in and out C_{COMM}. If the authentication is successful, the transmitter will remain powered on. The bq5101x measures the voltage at the RECT pin, calculates the difference between the actual voltage and the desired voltage $V_{RECT-REG}$, (threshold 1 at no load) and sends back error packets to the primary. This process goes on until the input voltage settles at $V_{RECT-REG}$. During a load transient, the dynamic rectifier algorithm will set the targets specified by $V_{RECT-REG}$ thresholds 1, 2, 3, and 4. This algorithm is termed Dynamic Rectifier Control and is used to enhance the transient response of the power supply.

During power-up, the LDO is held off until the $V_{RECT-REG}$ threshold 1 converges. The voltage control loop ensures that the output voltage is maintained at $V_{OUT-REG}$ to power the system. The bq5101x meanwhile continues to monitor the input voltage, and maintains sending error packets to the primary every 250ms. If a large transient occurs, the feedback to the primary speeds up to every 32ms in order to converge on an operating point in less time.

Details of a Qi Wireless Power System and bq5101x Power Transfer Flow Diagrams

The bq5101x family integrates a fully compliant WPC v1.0 communication algorithm in order to streamline receiver designs (no extra software development required). Other unique algorithms such has Dynamic Rectifier Control are also integrated to provide best in class system performance. This section provides a high level overview of these features by illustrating the wireless power transfer flow diagram from startup to active operation.

During startup operation, the wireless power receiver must comply with proper handshaking to be granted a power contract from the Tx. The Tx will initiate the hand shake by providing an extended digital ping. If an Rx is present on the Tx surface, the Rx will then provide the signal strength, configuration and identification packets to the Tx (see volume 1 of the WPC specification for details on each packet). These are the first three packets sent to the Tx. The only exception is if there is a true shutdown condition on the EN1/EN2, AD, or TS-CTRL pins where the Rx will shut down the Tx immediately. See Table 4 for details. Once the Tx has successfully received the signal strength, configuration and identification packets, the Rx will be granted a power contract and is then allowed to control the operating point of the power transfer. With the use of the bq5101x Dynamic Rectifier Control algorithm, the Rx will inform the Tx to adjust the rectifier voltage above 7 V prior to enabling the output supply. This method enhances the transient performance during system startup. See Figure 29 for the startup flow diagram details.

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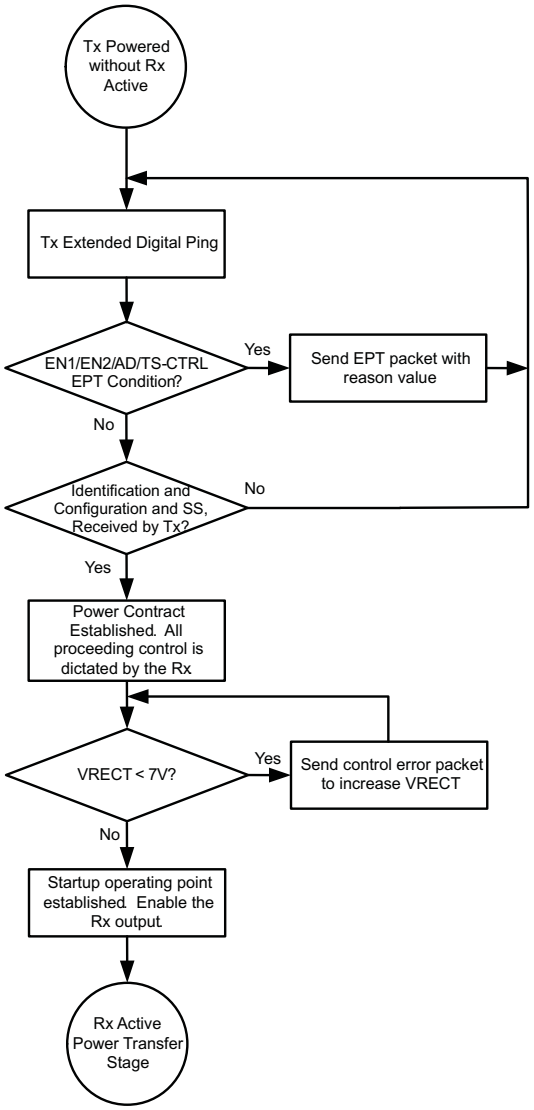


Figure 29. Wireless Power Startup Flow Diagram

Once the startup procedure has been established, the Rx will enter the active power transfer stage. This is considered the “main loop” of operation. The Dynamic Rectifier Control algorithm will determine the rectifier voltage target based on a percentage of the maximum output current level setting (set by K_{IMAX} and the ILIM resistance to GND). The Rx will send control error packets in order to converge on these targets. As the output current changes, the rectifier voltage target will dynamically change. As a note, the feedback loop of the WPC system is relatively slow where it can take up to 90 ms to converge on a new rectifier voltage target. It should be understood that the instantaneous transient response of the system is open loop and dependent on the Rx coil output impedance at that operating point. More details on this will be covered in the section Receiver Coil Load-Line Analysis. The “main loop” will also determine if any conditions in Table 4 are true in order to discontinue power transfer. See Figure 30 which illustrates the active power transfer loop.

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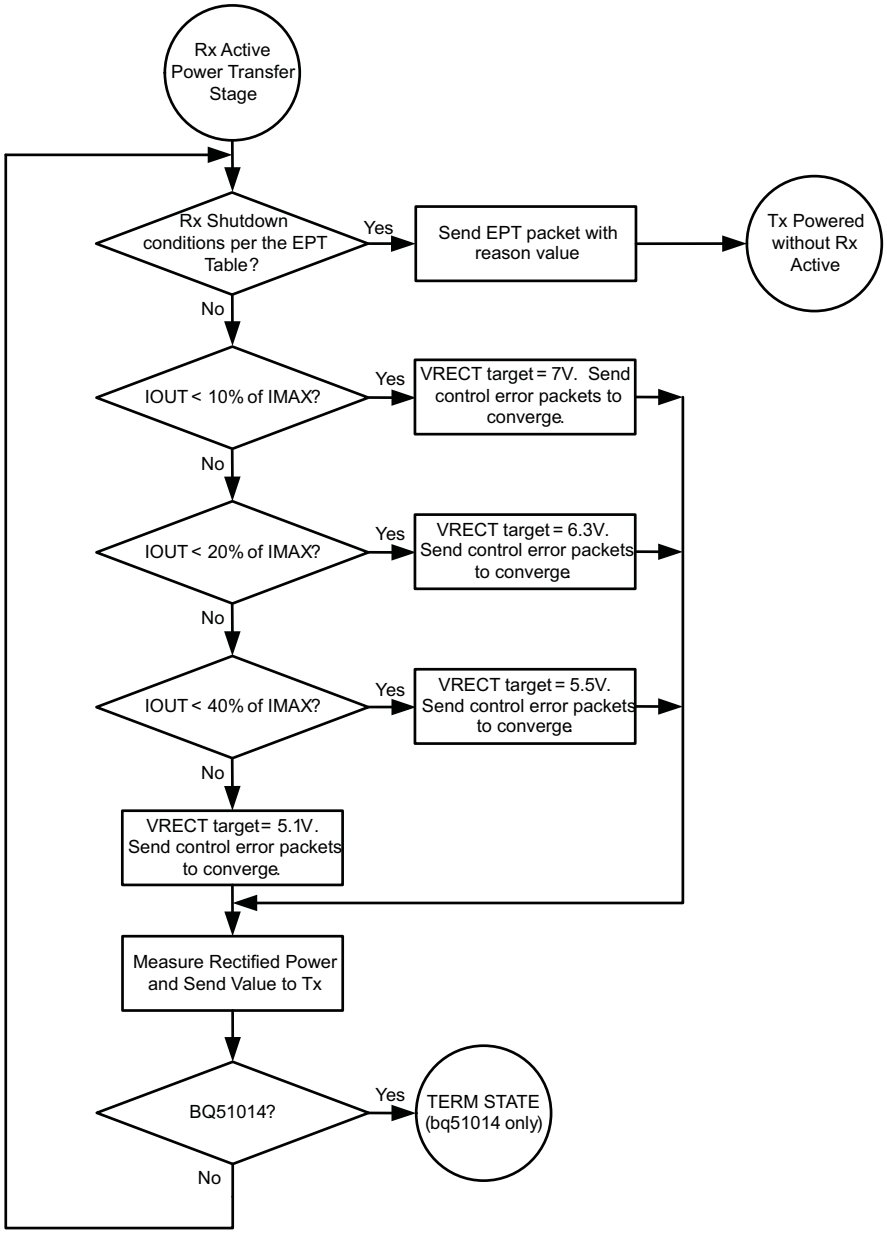


Figure 30. Active Power Transfer Flow Diagram

Another requirement of the WPC v1.0 specification is to send the measured rectifier power. This entitles the Rx to determine the rectifier voltage and output current in order to report this to the Tx as a percentage of the maximum output power. This is also handled in the active power transfer loop.

If the device is a bq51014, a special state called the “TERM STATE” is enabled in the active power transfer loop. This state is used to determine the level of the output current versus the programmed level of termination current (set by the K_{TERM} factor and R_{TERM} resistor). The primary purpose of this feature is to determine if the charge status is 100% based on the output current from the Rx. In a condition where the mobile device battery is fully charged, a low system current (output current from Rx) signature can be determined. This current level (signature) is set by the end system designer and is termed $I_{TERM-HI}$. In addition to this current level, there is a no-load termination current level termed $I_{TERM-LO}$ which is fixed at 40 mA. For the high termination condition to be

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true, the output current must be between $I_{TERM-HI}$ and $I_{TERM-LO}$ for approximately 180s. Once this condition is true, the Rx will send charge status of 100% to the Tx. The Tx can then illustrate that the mobile device has been fully charged (100% charged). If the output current remains below $I_{TERM-LO}$ for ~7s then the charge status of 100% is immediately sent. This condition can occur if the mobile device is put into a low standby mode after the battery is fully charged. See Figure 31 for the flow diagram of the "TERM STATE".

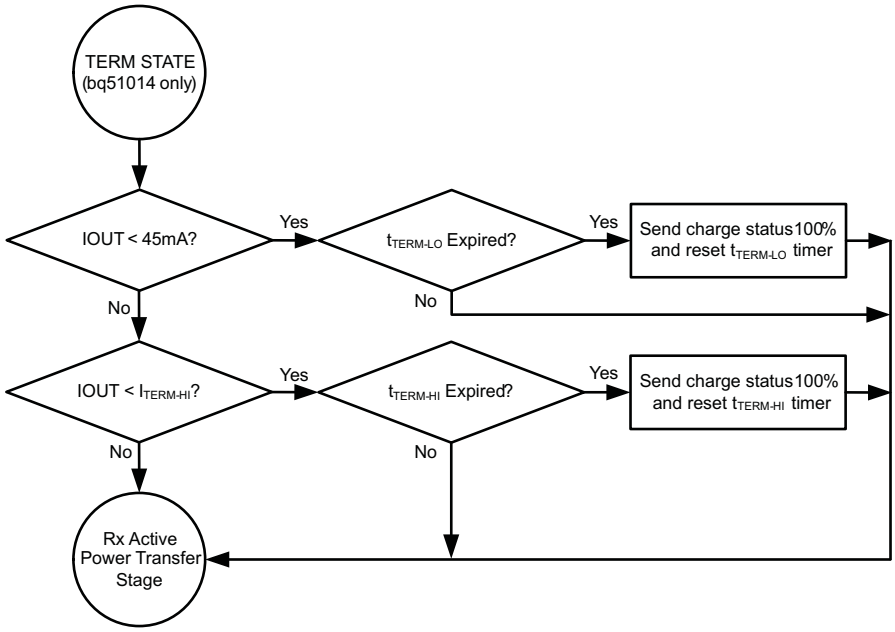


Figure 31. TERM STATE Flow Diagram for the bq51014 Only

Dynamic Rectifier Control

The Dynamic Rectifier Control algorithm offers the end system designer optimal transient response for a given max output current setting. This is achieved by providing enough voltage headroom across the internal regulator at light loads in order to maintain regulation during a load transient. The WPC system has a relatively slow global feedback loop where it can take up to 90 ms to converge on a new rectifier voltage target. Therefore, a transient response is dependent on the loosely coupled transformers output impedance profile. The Dynamic Rectifier Control allows for a 2 V change in rectified voltage before the transient response will be observed at the output of the internal regulator (output of the bq5101x). A 1-A application allows up to a 2 Ω output impedance. The Dynamic Rectifier Control behavior is illustrated in Figure 7 where R_{ILIM} is set to 220 Ω.

Dynamic Efficiency Scaling

The Dynamic Efficiency Scaling feature allows for the loss characteristics of the bq5101x to be scaled based on the maximum expected output power in the end application. This effectively optimizes the efficiency for each application. This feature is achieved by scaling the loss of the internal LDO based on a percentage of the maximum output current. Note that the maximum output current is set by the K_{IMAX} term and the R_{ILIM} resistance (where $R_{ILIM} = K_{IMAX} / I_{MAX}$). The flow diagram show in Figure 30 illustrates how the rectifier is dynamically controlled (*Dynamic Rectifier Control*) based on a fixed percentage of the I_{MAX} setting. The below table summarizes how the rectifier behavior is dynamically adjusted based on two different R_{ILIM} settings.

Table 1.

Output Current Percentage	R_{ILIM} = 500Ω I_{MAX} = 0.5A	R_{ILIM} = 220 Ω I_{MAX} = 1.14 A	V_{RECT}
0 to 10%	0 A to 0.05 A	0 A to 0.114 A	7.08 V
10 to 20%	0.05 A to 0.1A	0.114 A to 0.227 A	6.28 V
20 to 40%	0.1 A to 0.2 A	0.227 A to 0.454 A	5.53 V
>40%	> 0.2 A	> 0.454 A	5.11 V

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Figure 8 illustrates the shift in the *Dynamic Rectifier Controll* behavior based on the two different R_{ILIM} settings. With the rectifier voltage (V_{RECT}) being the input to the internal LDO, this adjustment in the *Dynamic Rectifier Control* thresholds will dynamically adjust the power dissipation across the LDO where:

$$P_{DIS} = \left(V_{RECT} - V_{OUT}\right) \times I_{OUT} \quad (1)$$

Figure 6 illustrates how the system efficiency is improved due to the *Dynamic Efficiency Scaling* feature. Note that this feature balances efficiency with optimal system transient response.

R_{ILIM} Calculations

The bq5101x includes a means of providing hardware overcurrent protection by means of an analog current regulation loop. The hardware current limit provides an extra level of safety by clamping the maximum allowable output current (e.g. a current compliance). The R_{ILIM} resistor size also set the thresholds for the dynamic rectifier levels and thus providing efficiency tuning per each application's maximum system current. The calculation for the total R_{ILIM} resistance is as follows:

$$R_{ILIM} = \frac{250}{I_{MAX}}$$
$$I_{ILIM} = 1.2 \times I_{MAX} = \frac{300}{R_{ILIM}}$$
$$R_{ILIM} = R_1 + 140 \quad (2)$$

Where I_{MAX} is the expected maximum output current during normal operation and I_{ILIM} is the hardware over current limit. When referring to the application diagram shown in Figure 2, R_{ILIM} is the sum of 140 and the R_1 resistance (e.g. the total resistance from the ILIM pin to GND).

Termination Calculations (bq51014 only)

The bq51014 includes a programmable upper termination threshold. This pin can be used to send the charge status 100% packet (CS100) to the transmitter in order to indicate a full charge status. The header for this packet is 0x05. Note that this packet does not turn off the transmitter and is only used as an informative indication of the mobile device's charge status. The upper termination threshold is calculated using Equation 3:

$$R_{TERM} = 200 \times \%I_{MAX}$$
$$\%I_{MAX} = \frac{I_{TERM-HI}}{I_{MAX}} \times 100$$
$$I_{MAX} = \frac{250}{R_{ILIM}} \quad (3)$$

The 200 constant is specified in the datasheet as K_{TERM}. The upper termination threshold is set as a percentage of the I_{IMAX} setting. For example, if the ILIM resistance is set to 250 Ω the I_{IMAX} current will be 1A (250 ÷ 250). If the upper termination threshold is desired to be 100 mA, this would be 10% of I_{IMAX}. The R_{TERM} resistor would then equal 2kΩ (200 x 10).

When the output current is in between $I_{TERM-HI}$ and $I_{TERM-LO}$, the CS100 packet is sent approximately every 3 min. When the output current is below $I_{TERM-LO}$, the CS100 packet is sent approximately every 7 seconds. The output current must remain in one of the termination conditions for that specific amount of time for the first CS100 packet to be sent (deglitch). See Figure 32 for details:

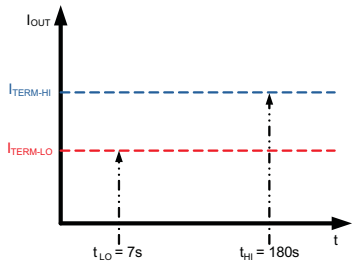


Figure 32. Termination Deglitch Timings for the CS100 Packet

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Input Overvoltage

If the input voltage suddenly increases in potential (e.g. a change in position of the equipment on the charging pad), the voltage-control loop inside the bq5101x becomes active, and prevents the output from going beyond $V_{OUT-REG}$. The receiver then starts sending back error packets to the transmitter every 30ms until the input voltage comes back to the $V_{RECT-REG}$ target, and then maintains the error communication every 250ms.

If the input voltage increases in potential beyond V_{OVP}, the IC switches off the LDO and communicates to the primary to bring the voltage back to $V_{RECT-REG}$. In addition, a proprietary voltage protection circuit is activated by means of C_{CLAMP1} and C_{CLAMP2} that protects the IC from voltages beyond the maximum rating of the IC (e.g. 20V).

Adapter Enable Functionality and EN1/EN2 Control

Figure 3 is an example application that shows the bq5101x used as a wireless power receiver that can power mutliplex between wired or wireless power for the down-system electronics. In the default operating mode pins EN1 and EN2 are low, which activates the adapter enable functionality. In this mode, if an adapter is not present the AD pin will be low, and $\overline{\text{AD-EN}}$ pin will be pulled to the higher of the OUT and AD pins so that the PMOS between OUT and AD will be turned off. If an adapter is plugged in and the voltage at the AD pin goes above 3.6V then wireless charging is disabled and the $\overline{\text{AD-EN}}$ pin will be pulled approximately 4V below the AD pin to connect AD to the secondary charger. The difference between AD and AD-EN is regulated to a maximum of 7V to ensure the V_{GS} of the external PMOS is protected.

The EN1 and EN2 pins include internal 200kΩ pull-down resistors, so that if these pins are not connected bq5101x defaults to $\overline{\text{AD-EN}}$ control mode. However, these pins can be pulled high to enable other operating modes as described in Table 2:

Table 2.

EN1	EN2	Result
0	0	Adapter control enabled. If adapter is present then secondary charger is powered by adapter, otherwise wireless charging is enabled when wireless power is available. Communication current limit is enabled.
0	1	Disables communication current limit.
1	0	$\overline{\text{AD-EN}}$ is pulled low, whether or not adapter voltage is present. This feature can be used, e.g., for USB OTG applications.
1	1	Adapter and wireless charging are disabled, i.e., power will never be delivered by the OUT pin in this mode.

Table 3.

EN1	EN2	Wireless Power	Wired Power	OTG Mode	Adaptive Communication Limit	EPT Termination
0	0	Enabled	Priority(1)	Disabled	Enabled	Not Sent to Tx
0	1	Enabled	Priority(1)	Disabled	Disabled	Not Sent to Tx
1	0	Disabled	Enabled	Enabled(2)	N/A	Sent to Tx
1	1	Disabled	Disabled	Disabled	N/A	Sent to Tx

(1) If both wired and wireless power are present, wired power is given priority.
(2) Allows for a boost-back supply to be driven from the output terminal of the Rx to the adapter port via the external back-to-back PMOS FET.

As described in Table 2, pulling EN2 high disables the adapter mode and only allows wireless charging. In this mode the adapter voltage will always be blocked from the OUT pin. An application example where this mode is useful is when USB power is present at AD, but the USB is in suspend mode so that no power can be taken from the USB supply. Pulling EN1 high enables the off-chip PMOS regardless of the presence of a voltage. This function can be used in USB OTG mode to allow a charger connected to the OUT pin to power the AD pin. Finally, pulling both EN1 and EN2 high disables both wired and wireless charging.

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NOTE

It is required to connect a back-to-back PMOS between AD and OUT so that voltage is blocked in both directions. Also, when AD mode is enabled no load can be pulled from the RECT pin as this could cause an internal device overvoltage in bq5101x.

End Power Transfer Packet (WPC Header 0x02)

The WPC allows for a special command for the receiver to terminate power transfer from the trasmitter termed End Power Transfer (EPT) packet. Table 4 specifies the v1.0 Reasons columb and their responding data field value. The Condition column corresponds to the values sent by the bq5101x for a given reason.

Table 4.

Reason	Value	Condition
Unknown	0x00	AD > 3.6V
Charge Complete	0x01	TS/CTRL = 1, or EN1 = 1, or <EN1 EN2> = <11>
Internal Fault	0x02	T_J > 150°C or R_{ILIM} < 100Ω
Over Temperature	0x03	TS < V_{HOT}, TS > V_{COLD}, or TS/CTRL < 100mV
Over Voltage	0x04	Not Sent
Over Current	0x05	I_{OUT} > 90% of I_{LIM} (bq51014 only)
Battery Failure	0x06	Not Sent
Reconfigure	0x07	Not Sent
No Response	0x08	VRECT target doesn't converge

Over Current Shutdown (bq51014)

The bq51014 includes an over current shutdown feature where the Rx sends an end power transfer packet to the Tx when the output current reaches 100% of the I_{ILIM} setting or 120% of the I_{IMAX} setting. The Tx will shut down as soon as the end power transfer packet is received which discontinues power transfer. This feature disallows the Rx from operating in a current limit situation in order to protect from down system shorts or failures.

Status Outputs

bq5101x has one status output, $\overline{CHG}$. This output is an open-drain NMOS device that is rated to 20V. The open-drain FET connected to the $\overline{CHG}$ pin will be turned on whenever the output of the power supply is enabled. Please note, the output of the power supply will not be enabled if the $V_{RECT-REG}$ does not converge at the no-load target voltage.

WPC Communication Scheme

The WPC communication uses a modulation technique termed “back-scatter modulation” where the receiver coil is dynamically loaded in order to provide amplitude modulation of the transmitters coil voltage and current. This scheme is possible due to the fundamental behavior between two loosely coupled inductors (e.g. between the Tx and Rx coil). This type of modulation can be accomplished by switching in and out a resistor at the output of the rectifier, or by switching in and out a capacitor across the AC1/AC2 net. Figure 33 shows how to implement resistive modulation.

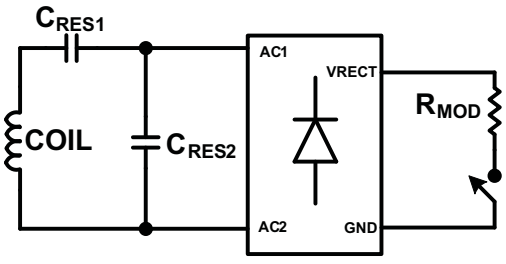


Figure 33. Resistive Modulation

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Figure 34 Shows how to implement capacitive modulation.

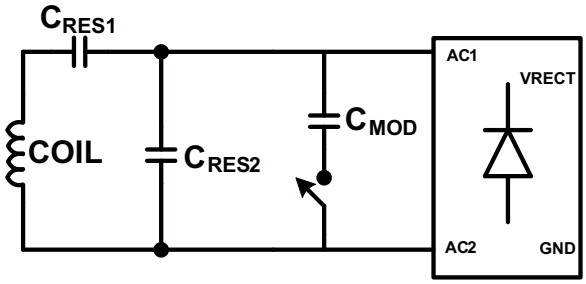


Figure 34. Capacitive Modulation

The amplitude change in Tx coil voltage or current can be detected by the transmitters decoder. The resulting signal observed by the Tx is shown in Figure 35.

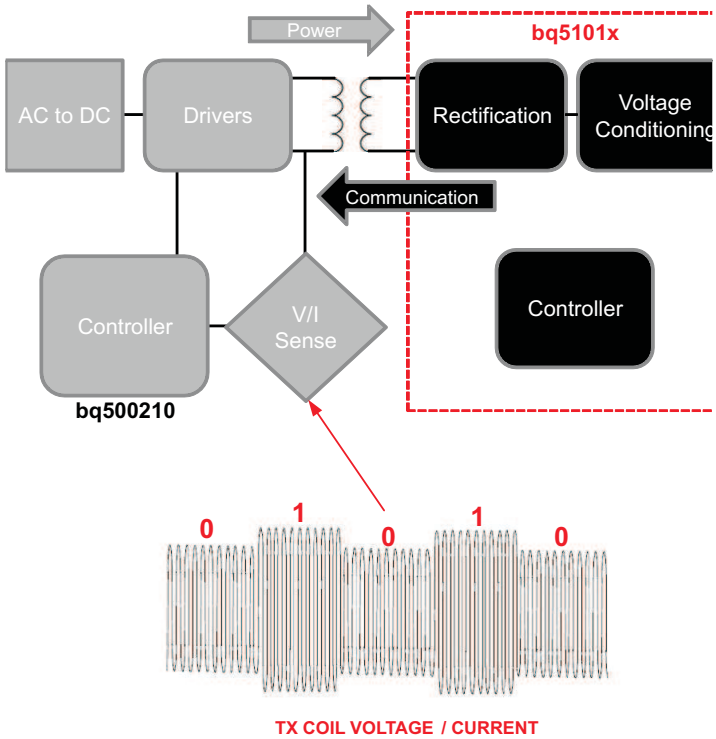


Figure 35.

The WPC protocol uses a differential bi-phase encoding scheme to modulate the data bits onto the Tx coil voltage/current. Each data bit is aligned at a full period of 0.5 ms (t_{CLK}) or 2 kHz. An encoded ONE results in two transitions during the bit period and an encoded ZERO results in a single transition. See Figure 36 for an example of the differential bi-phase encoding.

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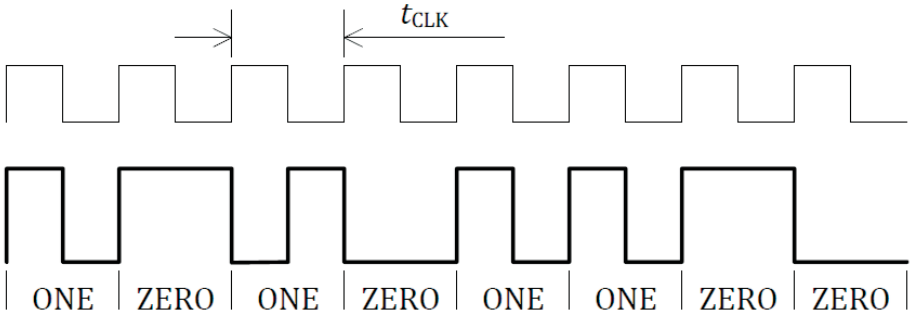


Figure 36. Differential Bi-phase Encoding Scheme (WPC volume 1: Low Power, Part 1 Interface Definition)

The bits are sent LSB first and use an 11-bit asynchronous serial format for each portion of the packet. This includes one start bit, n-data bytes, a parity bit, and a single stop bit. The start bit is always ZERO and the parity bit is odd. The stop bit is always ONE. Figure 37 shows the details of the asynchronous serial format.

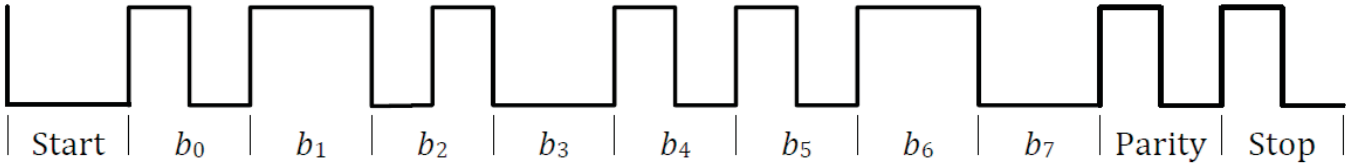


Figure 37. Asynchronous Serial Formatting (WPC volume 1: Low Power, Part 1 Interface Definition)

Each packet format is organized as shown in Figure 38.



Figure 38. Packet Format (WPC volume 1: Low Power, Part 1 Interface Definition)

Figure 27 above shows an example waveform of the receiver sending a rectified power packet (header 0x04).

Communication Modulator

bq5101x provides two identical, integrated communication FETs which are connected to the pins COM1 and COM2. These FETs are used for modulating the secondary load current which allows bq5101x to communicate error control and configuration information to the transmitter. Figure 39 below shows how the COMM pins can be used for resistive load modulation. Each COMM pin can handle at most a 24Ω communication resistor. Therefore, if a COMM resistor between 12Ω and 24Ω is required COM1 and COM2 pins must be connected in parallel. bq5101x does not support a COMM resistor less than 12Ω.

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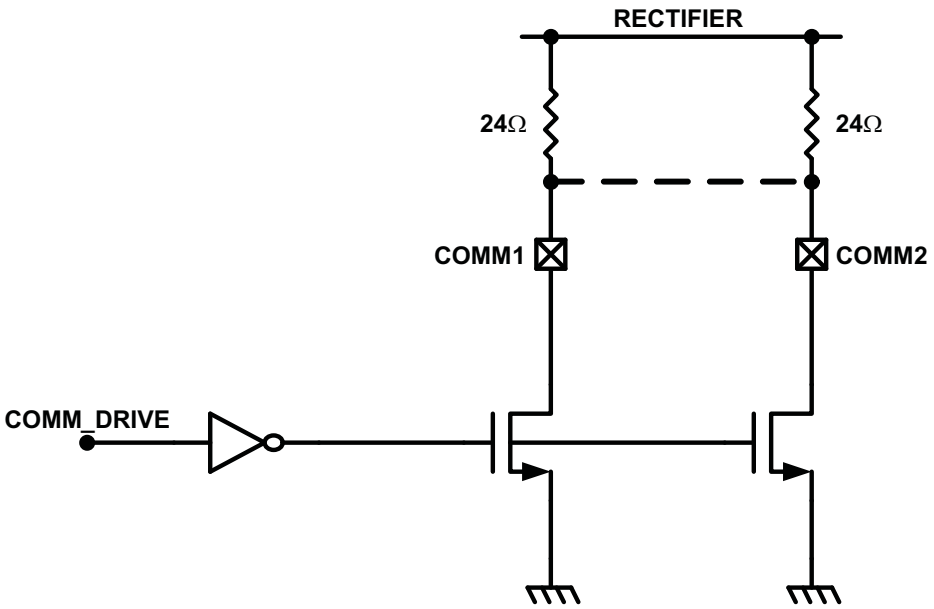


Figure 39. Resistive Load Modulation

In addition to resistive load modulation, the bq5101x is also capable of capacitive load modulation as shown in Figure 40 below. In this case, a capacitor is connected from COM1 to AC1 and from COM2 to AC2. When the COMM switches are closed there is effectively a 22 nF capacitor connected between AC1 and AC2. Connecting a capacitor in between AC1 and AC2 modulates the impedance seen by the coil, which will be reflected in the primary as a change in current.

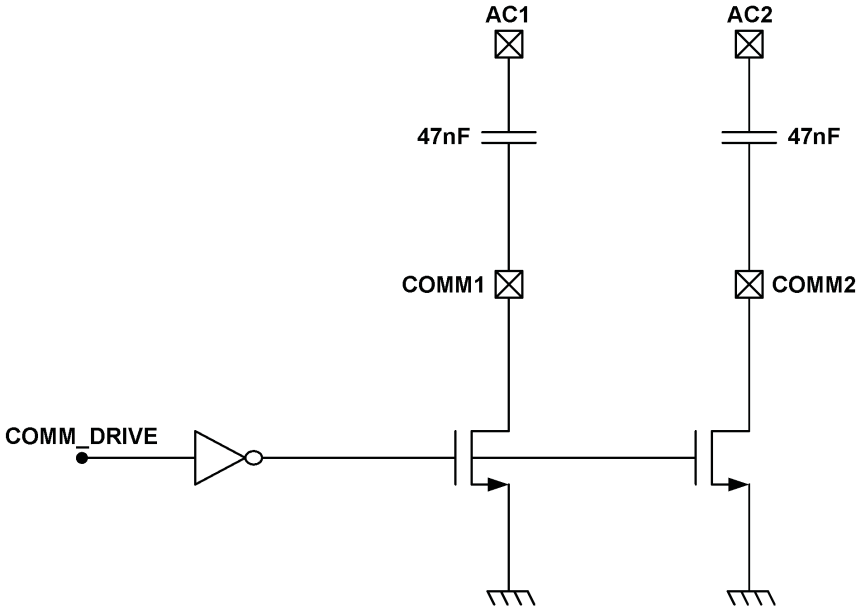


Figure 40. Capacitive Load Modulation

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Adaptive Communication Limit

The Qi communication channel is established via backscatter modulation as described in the previous sections. This type of modulation takes advantage of the loosely coupled inductor relationship between the Rx and Tx coil. Essentially the switching in-and-out of the communication capacitor or resistor adds a transient load to the Rx coil in order to modulate the Tx coil voltage/current waveform (amplitude modulation). The consequence of this technique is that a load transient (load current noise) from the mobile device has the same signature. In order to provide noise immunity to the communication channel, the output load transients must be isolated from the Rx coil. The proprietary feature *Adaptive Communication Limit* achieves this by dynamically adjusting the current limit of the regulator. When the regulator is put in current limit, any load transients will be offloaded to the battery in the system.

Note that this requires the battery charger IC to have input voltage regulation (weak adapter mode). The output of the Rx appears as a weak supply if a transient occurs above the current limit of the regulator.

The Adaptive Communication Limit feature has two current limit modes and is detailed in the table below:

Table 5.

I_{OUT}	Communication Current Limit
< 300 mA	Fixed 400 mA
> 300 mA	I_{OUT} + 50 mA

The first mode is illustrated in Figure 25. In this plot, an output load pulse of 300 mA is periodically introduced on a DC current level of 200 mA. Therefore, the 400 mA current limit is enabled. The pulses on V_{RECT} indicate that a communication packet event is occurring. When the output load pulse occurs, the regulator limits the pulse to a constant 400 mA and; therefore, preserves communication. Note that V_{OUT} drops to 4.5 V instead of GND. A charger IC with an input voltage regulation set to 4.5 V allows this to occur by offloading the load transient support to the mobile device's battery

The second mode is illustrated in Figure 26. In this plot, an output pulse of 200 mA is periodically introduced on a DC current level of 400 mA. Therefore, the tracking current mode (I_{OUT} + 50 mA) is enabled. In this mode the bq5101x measures the active output current and sets the regulators current limit 50 mA above this measurement. When the load pulse occurs during a communication packet event, the output current is regulated to 450 mA. As the communication packet event has finished the output load is allowed to increase. Note that during the time the regulator is in current limit V_{OUT} is reduced to 4.5 V and 5 V when not in current limit.

Synchronous Rectification

The bq5101x provides an integrated, self-driven synchronous rectifier that enables high-efficiency AC to DC power conversion. The rectifier consists of an all NMOS H-Bridge driver where the backgates of the diodes are configured to be the rectifier when the synchronous rectifier is disabled. During the initial startup of the WPC system the synchronous rectifier is not enabled. At this operating point, the DC rectifier voltage is provided by the diode rectifier. Once V_{RECT} is greater than UVLO, half synchronous mode will be enabled until the load current surpasses 120 mA. Above 120 mA the full synchronous rectifier stays enabled until the load current drops back below 100 mA where half synchronous mode is enabled instead.

Temperature Sense Resistor Network (TS)

bq5101x includes a ratiometric external temperature sense function. The temperature sense function has two ratiometric thresholds which represent a hot and cold condition. An external temperature sensor is recommended in order to provide safe operating conditions for the receiver product. This pin is best used for monitoring the surface that can be exposed to the end user (e.g. place the NTC resistor closest to the user).

Figure 41 allows for any NTC resistor to be used with the given V_{HOT} and V_{COLD} thresholds.

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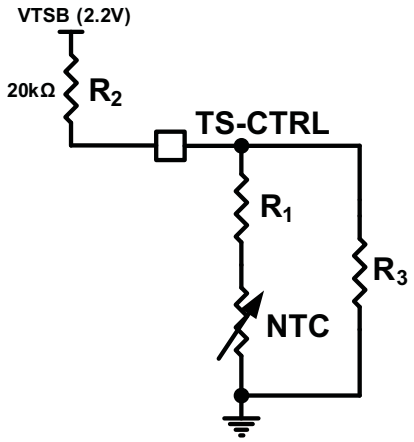


Figure 41. NTC Circuit Used for Safe Operation of the Wireless Receiver Power Supply

The resistors R_1 and R_3 can be solved by resolving the system of equations at the desired temperature thresholds. The two equations are:

$$\%V_{COLD} = \frac{\left(\frac{R_3\left(R_{NTC}|_{TCOLD} + R_1\right)}{R_3 + \left(R_{NTC}|_{TCOLD} + R_1\right)}\right)}{\left(\frac{R_3\left(R_{NTC}|_{TCOLD} + R_1\right)}{R_3 + \left(R_{NTC}|_{TCOLD} + R_1\right)}\right) + R2} \times 100$$

$$\%V_{HOT} = \frac{\left(\frac{R_3\left(R_{NTC}|_{THOT} + R_1\right)}{R_3 + \left(R_{NTC}|_{THOT} + R_1\right)}\right)}{\left(\frac{R_3\left(R_{NTC}|_{THOT} + R_1\right)}{R_3 + \left(R_{NTC}|_{THOT} + R_1\right)}\right) + R2} \times 100 \quad (4)$$

Where:

$$R_{NTC}|_{TCOLD} = R_o e^{\beta\left(1/T_{COLD} - 1/T_o\right)}$$

$$R_{NTC}|_{THOT} = R_o e^{\beta\left(1/T_{HOT} - 1/T_o\right)} \quad (5)$$

where, T_{COLD} and T_{HOT} are the desired temperature thresholds in degrees Kelvin. R_O is the nominal resistance and β is the temperature coefficient of the NTC resistor. R_O is fixed at 20 kΩ. An example solution is provided:

- R1 = 4.23kΩ
- R3 = 66.8kΩ

where the chosen parameters are:

- $\%V_{HOT}$ = 19.6%
- $\%V_{COLD}$ = 58.7%
- T_{COLD} = –10°C
- T_{HOT} = 100°C
- β = 3380
- R_O = 10kΩ

The plot of the percent V_{TSB} vs. temperature is shown in Figure 42:

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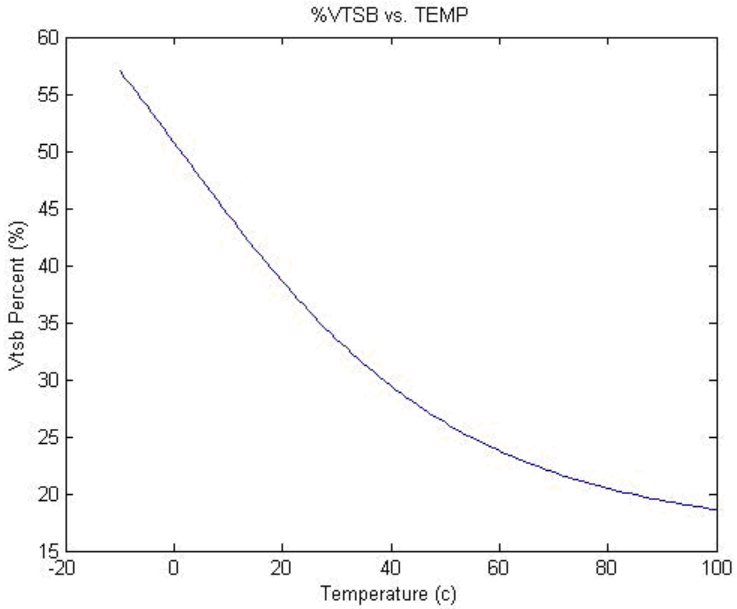


Figure 42. Example Solution for an NTC resistor with R_O = 10KΩ and β = 4500

Figure 43 illustrates the periodic biasing scheme used for measuring the TS state. The TS_READ signal enables the TS bias voltage for 24ms. During this period the TS comparators are read (each comparator has a 10 ms deglitch) and appropriate action is taken based on the temperature measurement. After this 24ms period has elapsed, the TS_READ signal goes low, which causes the TS-Bias pin to become high impedance. During the next 35ms (priority packet period) or 235ms (standard packet period), the TS voltage is monitored and compared to 100mV. If the TS voltage is greater than 100mV then a secondary device is driving the TS/CTRL pin and a CTRL = '1' is detected.

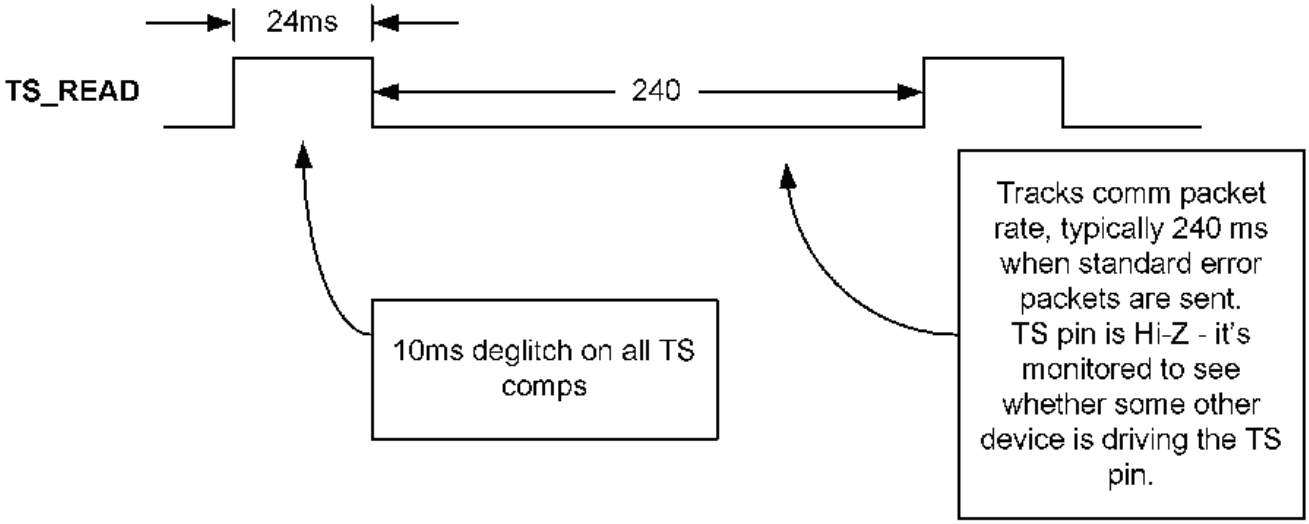


Figure 43. Timing Diagram for TS Detection Circuit

3-state Driver Recommendations for the TS-CTRL Pin

The TS-CTRL pin offers three functions with one 3-state driver interface

1. NTC temperature monitoring,
2. Fault indication,

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3. Charge done indication

A 3-state driver can be implemented with the circuit in Figure 44 and the use of two GPIO connections.

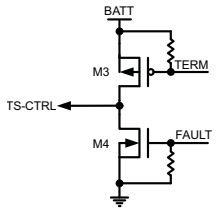


Figure 44. 3-state Driver for TS-CTRL

Note that the signals “TERM” and “FAULT” are given by two GPIO’s. The truth table for this circuit is found in Table 6:

Table 6.

TERM	FAULT	F (Result)
1	0	Z (Normal Mode)
0	0	Charge Complete
1	1	System Fault

The default setting is TERM = 1 and FAULT = 0. In this condition, the TS-CTRL net is high impedance (hi-z) and; therefore, the NTC is function is allowed to operate. When the TS-CTRL pin is pulled to GND by setting FAULT = 1, the Rx is shutdown with the indication of a fault. When the TS-CTRL pin is pulled to the battery by setting TERM = 1, the Rx is shutdown with the indication of a charge complete condition. Therefore, the host controller can indicate whether the Rx is system is turning off due to a fault or due to a charge complete condition.

Thermal Protection

The bq5101x includes a thermal shutdown protection. If the die temperature reaches T_J(OFF), the LDO is shut off to prevent any further power dissipation.

Series and Parallel Resonant Capacitor Selection

Shown in Figure 2, the capacitors C1 (series) and C2 (parallel) make up the dual resonant circuit with the receiver coil. These two capacitors must be sized correctly per the WPC v1.0 specification. Figure 45 illustrates the equivalent circuit of the dual resonant circuit:

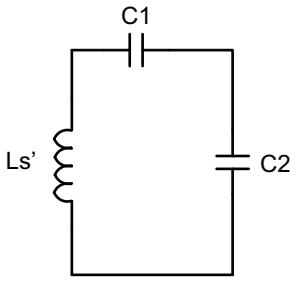


Figure 45. Dual Resonant Circuit with the Receiver Coil

Section 4.2 (Power Receiver Design Requirements) in volume 1 of the WPC v1.0 specification highlights in detail the sizing requirements. To summarize, the receiver designer will be required take inductance measurements with a fixed test fixture. The test fixture is shown in Figure 46:

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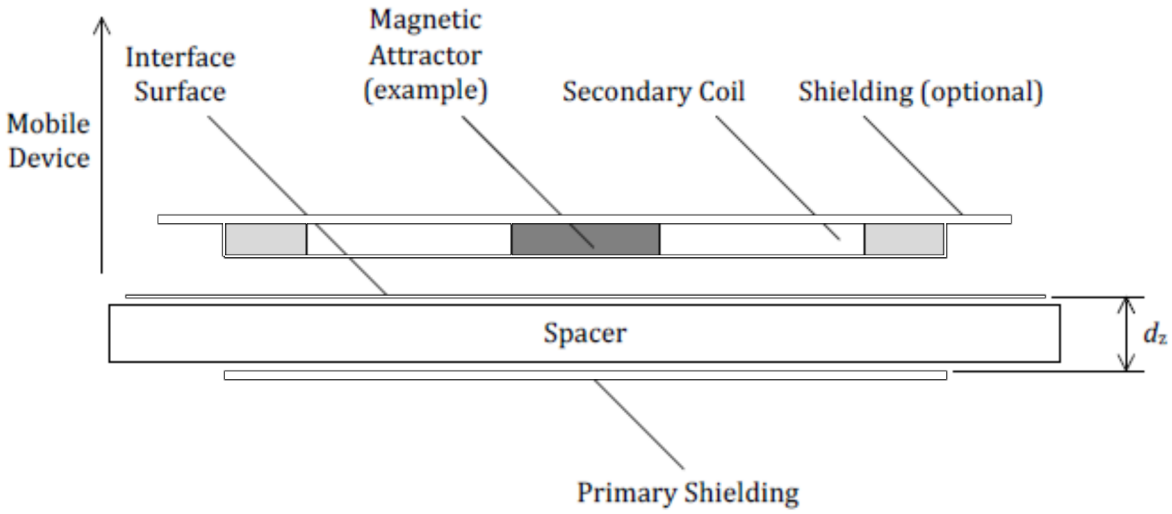


Figure 46. WPC v1.0 Receiver Coil Test Fixture for the Inductance Measurement Ls' (copied from System Description Wireless Power Transfer, volume 1: Low Power, Part 1 Interface Definition, Version 1.0.1, Figure 4-4)

The primary shield is to be 50 mm x 50 mm x 1 mm of Ferrite material PC44 from TDK Corp. The gap d_Z is to be 3.4 mm. The receiver coil, as it will be placed in the final system (e.g. the back cover and battery must be included if the system calls for this), is to be placed on top of this surface and the inductance is to be measured at 1-V RMS and a frequency of 100 kHz. This measurement is termed Ls'. The same measurement is to be repeated without the test fixture shown in Figure 11. This measurement is termed Ls or the free-space inductance. Each capacitor can then be calculated using Equation 6:

$$C_1 = \left[\left(f_S \cdot 2\pi \right)^2 \cdot L'_S \right]^{-1}$$

$$C_2 = \left[\left(f_D \cdot 2\pi \right)^2 \cdot L_S - \frac{1}{C_1} \right]^{-1} \quad (6)$$

Where f_S is 100 kHz +5/-10% and f_D is 1 MHz ±10%. C1 must be chosen first prior to calculating C2.

The quality factor must be greater than 77 and can be determined by Equation 7:

$$Q = \frac{2\pi \cdot f_D \cdot L_S}{R} \quad (7)$$

where R is the DC resistance of the receiver coil. All other constants are defined above.

Receiver Coil Load-Line Analysis

When choosing a receiver coil, it is recommend to analyze the transformer characteristics between the primary coil and receiver coil via load-line analysis. This will capture two important conditions in the WPC system:

1. Operating point characteristics in the closed loop of the WPC system.
2. Instantaneous transient response prior to the convergence of the new operating point.

An example test configuration for conducting this analysis is shown in Figure 47:

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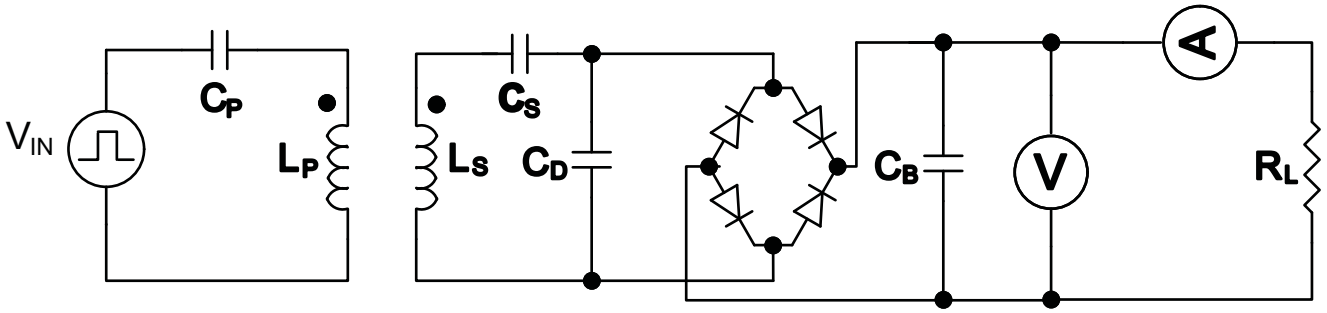


Figure 47. Load-Line Analysis Test Bench

Where:

- V_{IN} is a square-wave power source that should have a peak-to-peak operation of 19V.
- C_P is the primary series resonant capacitor (i.e. 100 nF for Type A1 coil).
- L_P is the primary coil of interest (i.e. Type A1).
- L_S is the secondary coil of interest.
- C_S is the series resonant capacitor chosen for the receiver coil under test.
- C_D is the parallel resonant capacitor chosen for the receiver coil under test.
- C_B is the bulk capacitor of the diode bridge (voltage rating should be at least 25 V and capacitance value of at least 10µ F)
- V is a Kelvin connected voltage meter
- A is a series ammeter
- R_L is the load of interest

It is recommended that the diode bridge be constructed of Schottky diodes.

The test procedure is as follows

- Supply a 19V AC signal to L_P starting at a frequency of 210 kHz
- Measure the resulting rectified voltage from no load to the expected full load
- Repeat the above steps for lower frequencies (stopping at 110 kHz)

An example load-line analysis is shown in Figure 48:

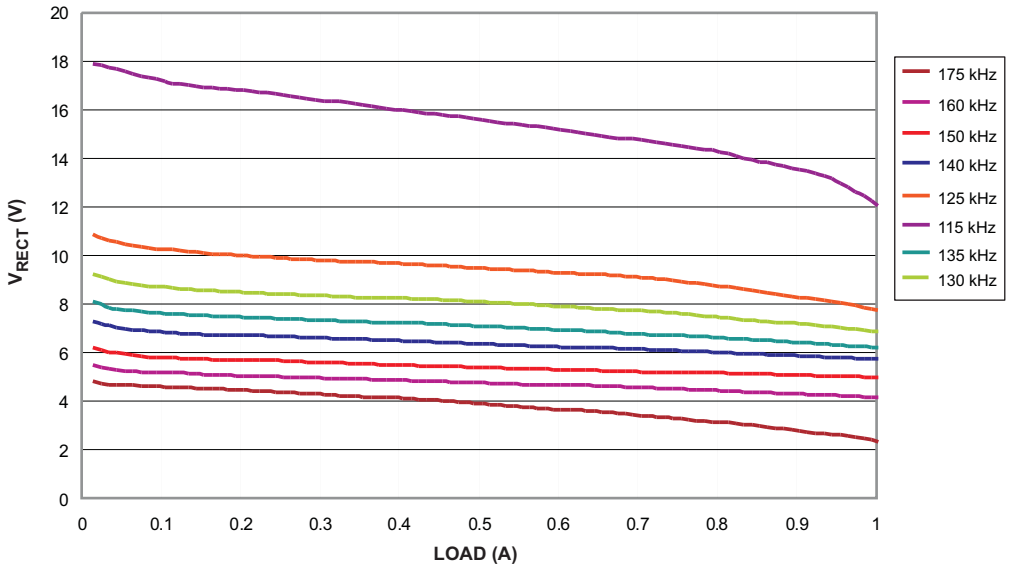


Figure 48. Example Load-Line Results

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What this plot conveys about the operating point is that a specific load and rectifier target condition consequently results in a specific operating frequency (for the type A1 TX). For example, at 1 A the dynamic rectifier target is 5.15 V. Therefore, the operating frequency will be between 150kHz and 160kHz in the above example. This is an acceptable operating point. If the operating point ever falls outside the WPC frequency range (110kHz – 205kHz), the system will never converge and will become unstable.

In regards to transient analysis, there are two major points of interest:

1. Rectifier voltage at the ping frequency (175kHz).
2. Rectifier voltage droop from no load to full load at the constant operating point.

In this example, the ping voltage will be approximately 5 V. This is above the UVLO of the bq5101x and; therefore, startup in the WPC system can be ensured. If the voltage is near or below the UVLO at this frequency, then startup in the WPC system may not occur.

If the max load step is 1 A, the droop in this example will be Approximately1V with a voltage at 1 A of Approximately 5.5 V (140 kHz load-line). To analyze the droop locate the load-line that starts at 7 V at no-load. Follow this load-line to the max load expected and take the difference between the 7V no-load voltage and the full-load voltage at that constant frequency. Ensure that the full-load voltage at this constant frequency is above 5V. If it descends below 5V, the output of the power supply will also droop to this level. This type of transient response analysis is necessary due to the slow feedback response of the WPC system. This simulates the step response prior to the WPC system adjusting the operating point.

NOTE

Coupling between the primary and secondary coils will worsen with misalignment of the secondary coil. Therefore, it is recommended to re-analyze the load-lines at multiple misalignments to determine where, in planar space, the receiver will discontinue operation.

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Recommended Rx coils can be found in Table 7:

Table 7.

Manufacturer	Part Number	Dimensions	Ls	Ls'	Output Current Range	Application
TDK	WR-483250-15M2-G	48 x 32mm	10.4 µH	12 µH(1)	50-1000 mA	General 5V Power Supply
TDK	WR-383250-17M2-G	38 x 32mm	11.1 µH	12.3 µH(1)	50-1000 mA	Space limited 5V Power Supply
Vishay	IWAS-4832FF-50	48 x 32mm	10.8 µH	12.5 µH(1)	50-1000 mA	General 5V Power Supply
Mingstar	312-00012	48 x 32mm	10.8 µH	12.9 µH(1)	50-1000 mA	General 5V power Supply
Mingstar	312-00015	28 x 14mm	36.5 µH	45 µH(2)	150-1000 mA	Space limited 5V Power Supply

(1) Ls' measurements conducted with a standard battery behind the Rx coil assembly. This measurement is subject to change based on different battery sizes, placements, and casing material.
(2) Battery not present behind the Rx coil assembly. Subject to drop in inductance depending on the placement of the battery.

It is recommended that all inductance measurements are repeated in the designers specific system as there are many influence on the final measurements.

Package Summary

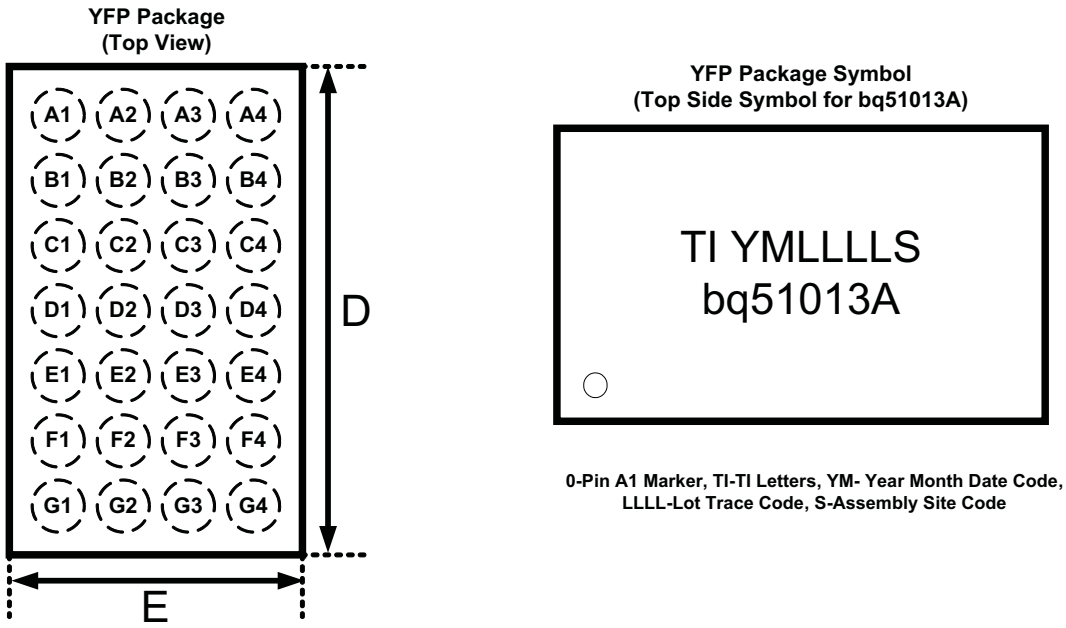


Figure 49. Chip Scale Packaging Dimensions

- D = 3.0mm ± 0.035mm
- E = 1.88mm ± 0.035mm

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REVISION HISTORY

Changes from Original (March 2012) to Revision A	Page
• Deleted $V_{RECT-TRACK}$ from the Electrical Characteristics table	6

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ51013ARHLR	Active	Production	VQFN (RHL) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BQ51013A
BQ51013ARHLR.A	Active	Production	VQFN (RHL) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BQ51013A
BQ51013ARHLR.B	Active	Production	VQFN (RHL) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BQ51013A
BQ51013ARHLT	Active	Production	VQFN (RHL) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BQ51013A
BQ51013ARHLT.A	Active	Production	VQFN (RHL) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BQ51013A
BQ51013ARHLT.B	Active	Production	VQFN (RHL) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BQ51013A
BQ51013AYFPR	Active	Production	DSBGA (YFP) | 28	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51013A
BQ51013AYFPR.A	Active	Production	DSBGA (YFP) | 28	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51013A
BQ51013AYFPR.B	Active	Production	DSBGA (YFP) | 28	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51013A
BQ51013AYFPT	Active	Production	DSBGA (YFP) | 28	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51013A
BQ51013AYFPT.A	Active	Production	DSBGA (YFP) | 28	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51013A
BQ51013AYFPT.B	Active	Production	DSBGA (YFP) | 28	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51013A
BQ51014YFPR	NRND	Production	DSBGA (YFP) | 28	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51014
BQ51014YFPR.A	NRND	Production	DSBGA (YFP) | 28	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51014
BQ51014YFPR.B	NRND	Production	DSBGA (YFP) | 28	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51014
BQ51014YFPT	NRND	Production	DSBGA (YFP) | 28	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51014
BQ51014YFPT.A	NRND	Production	DSBGA (YFP) | 28	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51014
BQ51014YFPT.B	NRND	Production	DSBGA (YFP) | 28	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51014

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

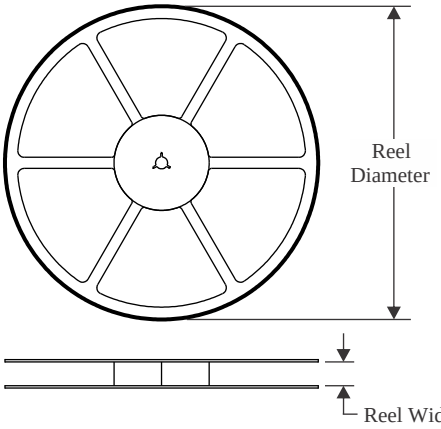
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

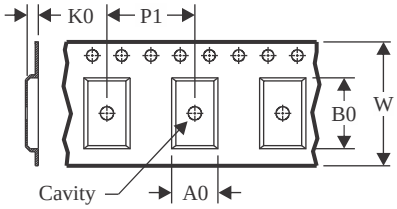
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

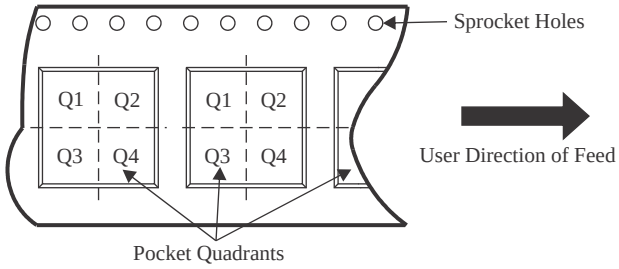


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

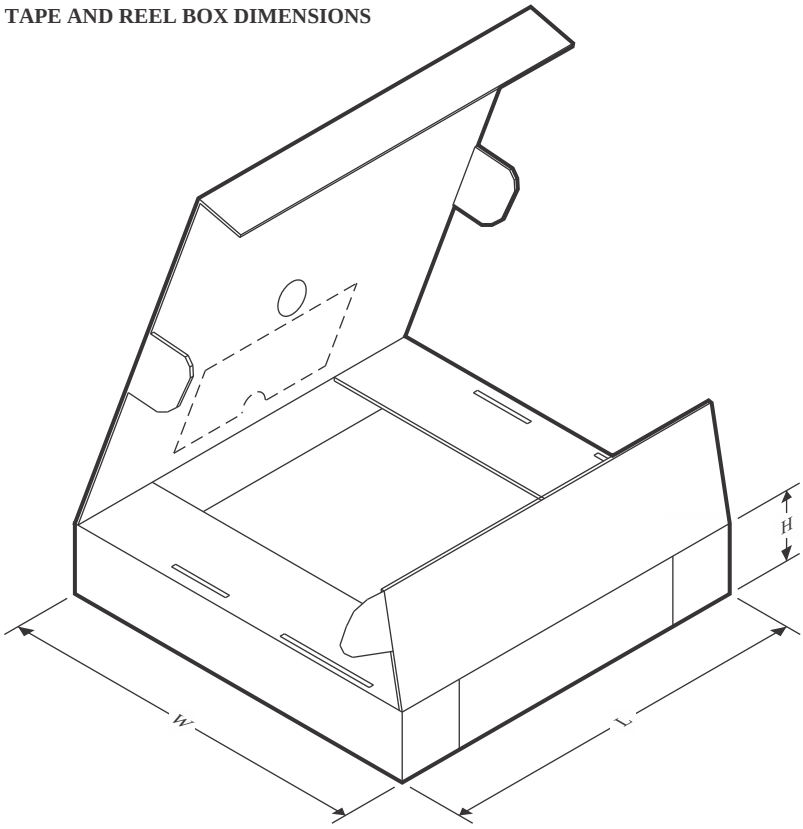
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ51013ARHLR	VQFN	RHL	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
BQ51013ARHLT	VQFN	RHL	20	250	180.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
BQ51013AYFPR	DSBGA	YFP	28	3000	180.0	8.4	2.0	3.13	0.6	4.0	8.0	Q1
BQ51013AYFPT	DSBGA	YFP	28	250	180.0	8.4	2.0	3.13	0.6	4.0	8.0	Q1
BQ51014YFPR	DSBGA	YFP	28	3000	180.0	8.4	2.0	3.13	0.6	4.0	8.0	Q1
BQ51014YFPT	DSBGA	YFP	28	250	180.0	8.4	2.0	3.13	0.6	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

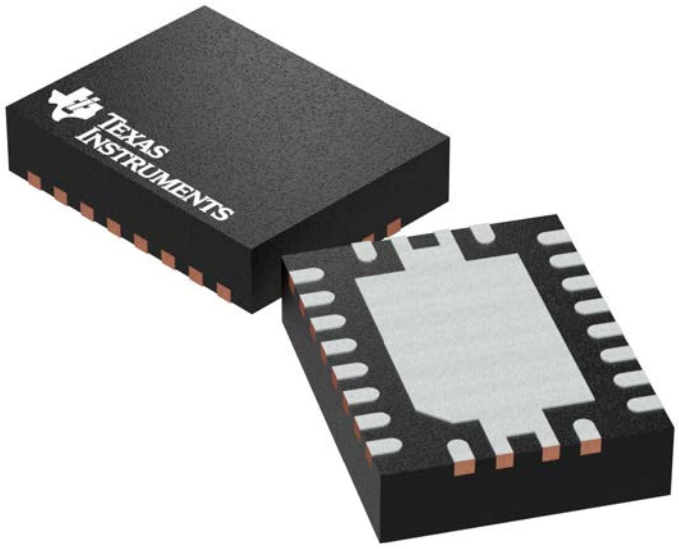
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ51013ARHLR	VQFN	RHL	20	3000	346.0	346.0	33.0
BQ51013ARHLT	VQFN	RHL	20	250	210.0	185.0	35.0
BQ51013AYFPR	DSBGA	YFP	28	3000	182.0	182.0	20.0
BQ51013AYFPT	DSBGA	YFP	28	250	182.0	182.0	20.0
BQ51014YFPR	DSBGA	YFP	28	3000	182.0	182.0	20.0
BQ51014YFPT	DSBGA	YFP	28	250	182.0	182.0	20.0

RHL 20

VQFN - 1 mm max height

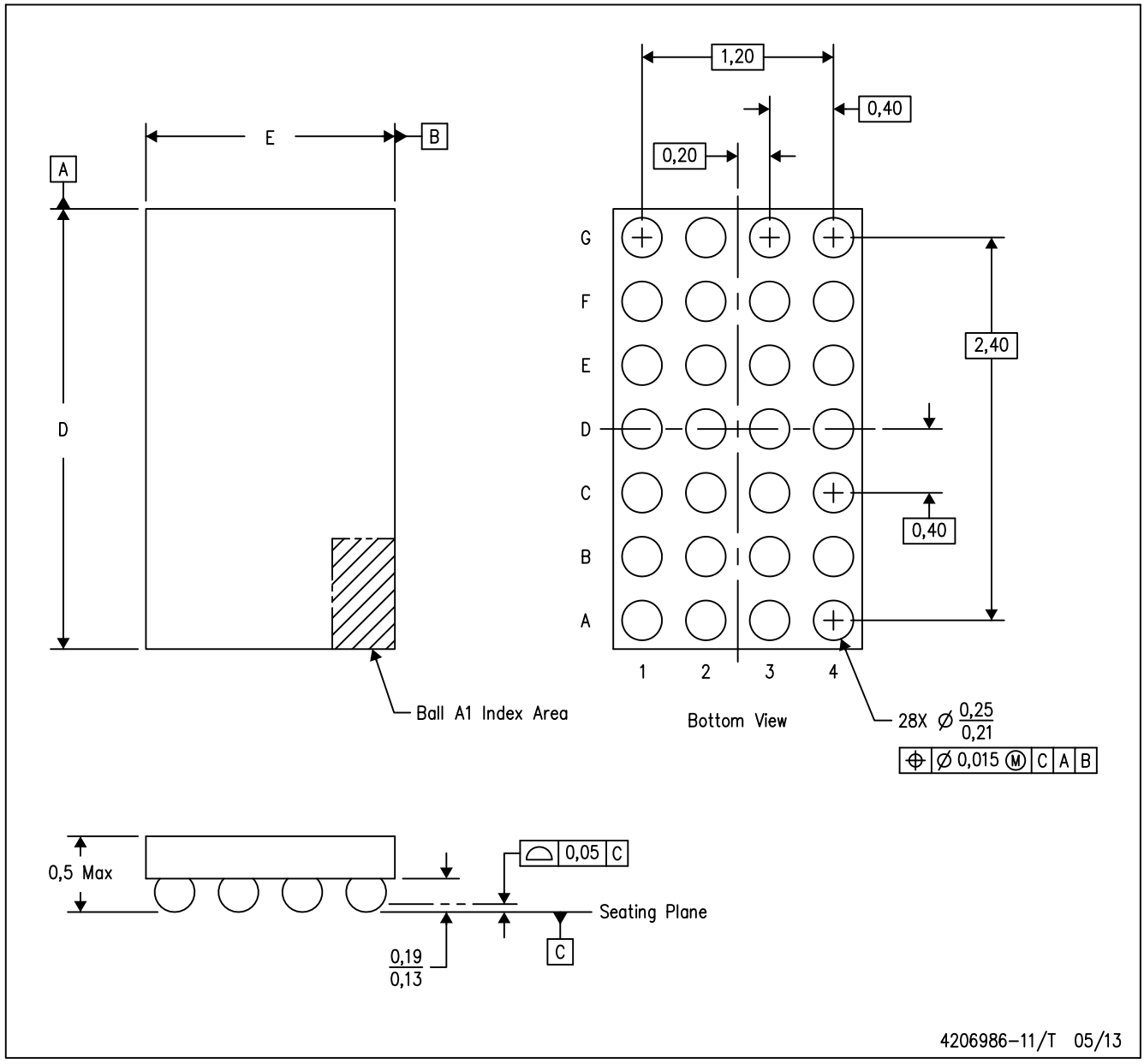
PLASTIC QUAD FLATPACK - NO LEAD

3.5 x 4.5 mm, 0.5 mm pitch



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

YFP (R–XBGA–N28) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments

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