BUF16821-Q1 可编程伽马电压生成器和 具有集成型 2 组存储器的 VCOM 校准器
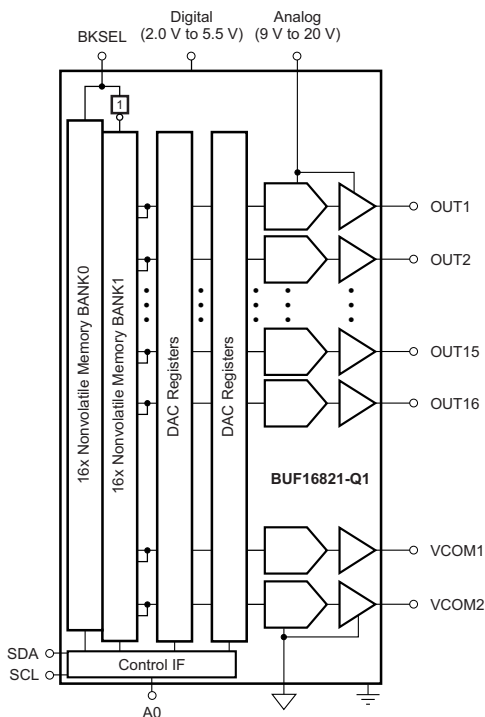
1 特性

- 具有符合 AEC-Q100 标准的以下结果：
  - 温度等级 3：-40℃ 至 85℃
  - 人体模型 (HBM) 静电放电 (ESD) 分类等级 2
  - 充电器件模型 (CDM) ESD 分类等级 C4B
- 16 通道 P 伽马，2 通道 P-VCOM，10 位分辨率
- 16x 可重写非易失性存储器
- 两个独立的引脚可选存储器组
- 轨至轨输出：
  - 300mV（最小值）电源轨摆幅 (10mA)
  - > 300mA（最大值）I_{OUT}
- 电源电压：9V 至 20V
- 数字电源：2V 至 5.5V
- I²C™ 接口：支持 400kHz 和 2.7MHz

2 应用范围

TFT-LCD 基准驱动器

功能方框图

3 说明

BUF16821-Q1 提供 16 条可编程伽马通道，以及两个可编程 VCOM 通道。 最终的伽马和 VCOM 值可被存储在片上、非易失性存储器中。 为了应对编程错误时或使液晶显示屏 (LCD) 面板重新开始工作，此器件支持多达 16 个对片上存储器的写操作。

此器件具有两个独立的存储器组，可实现两个不同伽马曲线的同时存储，从而使伽马曲线之间的切换更加便捷。 所有伽马和 VCOM 通道提供一个轨到轨输出，此输出在 10mA 负载时，通常在任一电源轨的 150mV 内摆动。 可使用一个 I²C 接口对所有通道进行编程，这个接口支持高达 400kHz 的标准运行，以及高达 2.7MHz 的高速数据传输。

此器件使用德州仪器 (TI) 专有的、最先进的高压 CMOS 工艺制造。 这一工艺提供高达 20V 的高密度逻辑和高电源电压运行。此器件采用带散热片薄型小外形尺寸 (HTSSOP)-28 PowerPAD™ 封装，并且在 -40℃ 至 +85℃ 的温度范围内额定运行。

器件信息[1]

产品型号	封装	封装尺寸（标称值）
BUF16821-Q1	HTSSOP (28)	9.70mm x 4.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

目录

4 修订历史记录

日期	修订版本	注释
2014 年 5 月	*	最初发布。

Related Products

FEATURES	DEVICE
22-channel gamma correction buffer	BUF22821
12-channel gamma correction buffer	BUF12800
18-, 20-channel programmable buffer, 10-bit, VCOM	BUF20800
18-, 20-channel programmable buffer with memory	BUF20820
Programmable VCOM driver	BUF01900
18-V supply, traditional gamma buffers	BUF11704
22-V supply, traditional gamma buffers	BUF11705

5 Pin Configuration and Functions

PWP Package
HTSSOP-28
(Top View)

Left Pin	#		#	Right Pin
VCOM2	1		28	VCOM1
OUT1	2		27	OUT16
OUT2	3		26	OUT15
OUT3	4		25	OUT14
OUT4	5		24	GNDA[1]
OUT5	6		23	VS
OUT6	7	PowerPAD Lead-Frame Die Pad Exposed on Underside (must connect to GNDA and GNDD)	22	OUT13
GNDA[1]	8		21	OUT12
VS	9		20	OUT11
OUT7	10		19	OUT10
OUT8	11		18	GNDD[1]
OUT9	12		17	BKSEL
VSD	13		16	A0
SCL	14		15	SDA

(1) GNDA and GNDD must be connected together.

Pin Functions

PIN		DESCRIPTION
NO.	NAME	
1	VCOM2	VCOM channel 2
2	OUT1	DAC output 1
3	OUT2	DAC output 2
4	OUT3	DAC output 3
5	OUT4	DAC output 4
6	OUT5	DAC output 5
7	OUT6	DAC output 6
8	GNDA	Analog ground; must be connected to digital ground (GNDD).
9	VS	VS connected to analog supply
10	OUT7	DAC output 7
11	OUT8	DAC output 8
12	OUT9	DAC output 9
13	VSD	Digital supply; connect to logic supply
14	SCL	Serial clock input; open-drain, connect to pull-up resistor.
15	SDA	Serial data I/O; open-drain, connect to pull-up resistor.
16	A0	A0 address pin for I2C address; connect to either logic 1 or logic 0; refer to Table 2.
17	BKSEL	Selects memory bank 0 or 1; connect to either logic 1 to select bank 1 or logic 0 to select bank 0.
18	GNDD	Digital ground; must be connected to analog ground at the BUF16821-Q1.
19	OUT10	DAC output 10
20	OUT11	DAC output 11
21	OUT12	DAC output 12
22	OUT13	DAC output 13
23	VS	VS connected to analog supply
24	GNDA	Analog ground; must be connected to digital ground (GNDD).
25	OUT14	DAC output 14
26	OUT15	DAC output 15
27	OUT16	DAC output 16
28	VCOM1	VCOM channel 1

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_S	Supply voltage			22	V
DVDD	Digital power supply (VSD pin)			6	V
	Digital input pins	SCL, SDA, AO, BKSEL: voltage	−0.5	6	V
		SCL, SDA, AO, BKSEL: current		±10	mA
	Output pins, OUT1 through OUT16, VCOM1 and VCOM2[2]		(V−) − 0.5	(V+) + 0.5	V
	Output short-circuit[3]		Continuous		
	Ambient operating temperature		−40	95	°C
T_J	Junction temperature			125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See the *Output Protection* section.
(3) Short-circuit to ground, one amplifier per package.

6.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			−65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]		−2000	2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 14, 15, and 28)	−750	750	
			Other pins	−500	500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage	9.0	18.0	20.0	V
DVDD	Digital power supply (VSD pin)	2.0	3.3	5.5	V

6.4 Thermal Information

THERMAL METRIC[1]		BUF16821-Q1 PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	17.4	
ψ_{JT}	Junction-to-top characterization parameter	0.7	
ψ_{JB}	Junction-to-board characterization parameter	17.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_A = 25°C, V_S = 18 V, V_{SD} = 2 V, R_L = 1.5 kΩ connected to ground, and C_L = 200 pF, unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG GAMMA BUFFER CHANNELS						
	Reset value	Code 512		9		V
	OUT 1–16 output swing: high	Code = 1023, sourcing 10 mA, T_A = –40°C to 85°C	17.7	17.85		V
	OUT 1–16 output swing: low	Code = 0, sinking 10 mA, T_A = –40°C to 85°C		0.07	0.3	V
	VCOM1, 2 output swing: high	Code = 1023, sourcing 100 mA, T_A = –40°C to 85°C	13	16.2		V
	VCOM1, 2 output swing: low	Code = 0, sinking 100 mA, T_A = –40°C to 85°C		0.6	2	V
	Continuous output current[1]			30		mA
	Output accuracy			±20	±50	mV
	Output accuracy over temperature	Code 512, T_A = –40°C to 85°C		±25		µV/°C
INL	Integral nonlinearity			0.3		LSB
DNL	Differential nonlinearity			0.3		LSB
$\Delta V_{O(\Delta IO)}$	Load regulation, 10 mA	Code 512 or V_{CC} / 2, I_{OUT} = 5-mA to –5-mA step		0.5	1.5	mV/mA
OTP MEMORY						
	Number of OTP write cycles				16	Cycles
	Memory retention			100		Years
ANALOG POWER SUPPLY						
	Operating range		9		20	V
$I_{CC(tot)}$	Total analog supply current	Outputs at reset values, no load		12	14	mA
	$I_{CC(tot)}$ over temperature	T_A = –40°C to 85°C			18	mA
DIGITAL						
V_{IH}	Logic 1 high input voltage		0.7 × V_{SD}			V
V_{IL}	Logic 0 low input voltage				0.3 × V_{SD}	V
V_{OL}	Logic 0 low output voltage	I_{SINK} = 3 mA		0.15	0.4	V
	Input leakage			±0.01	±10	µA
f_{CLK}	Clock frequency	Standard, fast mode, T_A = –40°C to 85°C			400	kHz
		High-speed mode, T_A = –40°C to 85°C			2.7	MHz
DIGITAL POWER SUPPLY						
DVDD	Digital power supply (VSD pin)		2.0		5.5	V
I_{SD}	Digital supply current[1]	Outputs at reset values, no load, two-wire bus inactive		115	150	µA
	I_{SD} over temperature	T_A = –40°C to 85°C		115		µA
TEMPERATURE RANGE						
	Specified range		–40		85	°C
	Operating range	Junction temperature < 125°C	–40		95	°C
	Storage range		–65		150	°C
$R_{\theta JA}$	Thermal resistance, HTSSOP-28[1][2]			40		°C/W

(1) Observe maximum power dissipation.
(2) Thermal pad is attached to the printed circuit board (PCB), 0-lfm airflow, and 76-mm × 76-mm copper area.

6.6 Timing Requirements

	PARAMETER	FAST MODE		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	0.001	0.4	0.001	2.7	MHz
$t_{(BUF)}$	Bus free time between stop and start conditions	1300		230		ns
$t_{(HDSTA)}$	Hold time after repeated start condition. After this period, the first clock is generated.	600		230		ns
$t_{(SUSTA)}$	Repeated start condition setup time	600		230		ns
$t_{(SUSTO)}$	Stop condition setup time	600		230		ns
$t_{(HDDAT)}$	Data hold time	20	900	20	130	ns
$t_{(SUDAT)}$	Data setup time	100		20		ns
$t_{(LOW)}$	SCL clock low period	1300		230		ns
$t_{(HIGH)}$	SCL clock high period	600		60		ns
$t_{R(SDA)}$, $t_{F(SDA)}$	Data rise and fall time		300		80	ns
$t_{R(SCL)}$, $t_{F(SCL)}$	Clock rise and fall time		300		40	ns
t_R	Clock and data rise time for SCLK ≤ 100 kHz		1000			ns

Figure 1. Timing Requirements Diagram

6.7 Typical Characteristics

At T_A = 25°C, V_S = 18 V, V_{SD} = 2 V, R_L = 1.5 kΩ connected to ground, and C_L = 200 pF, unless otherwise noted.
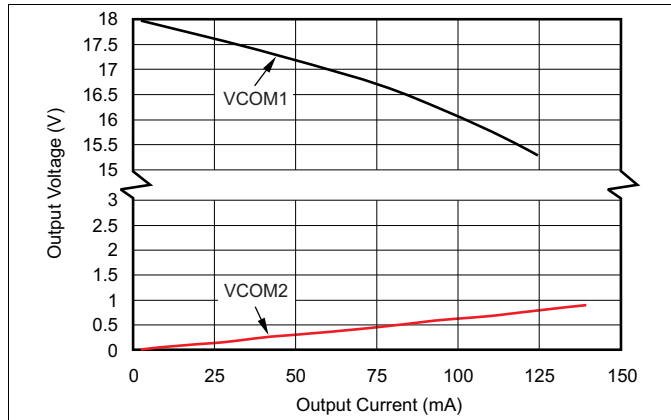

**Figure 2. Output Voltage vs Output Current
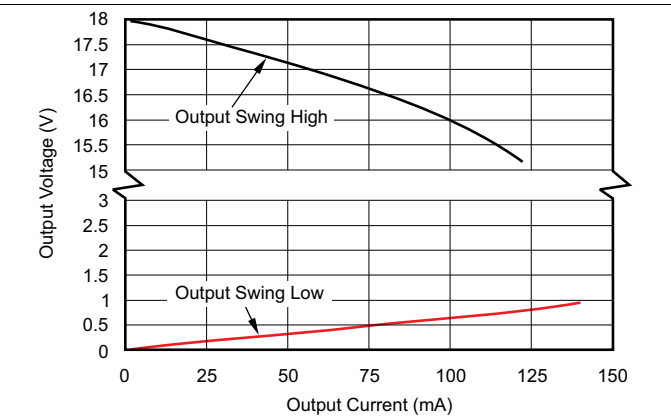(VCOM1 and VCOM2)**

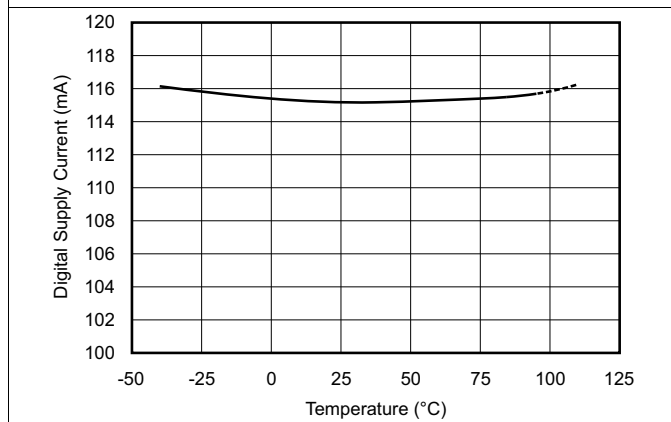**Figure 3. Output Voltage vs Output Current
(Channels 1–16)**

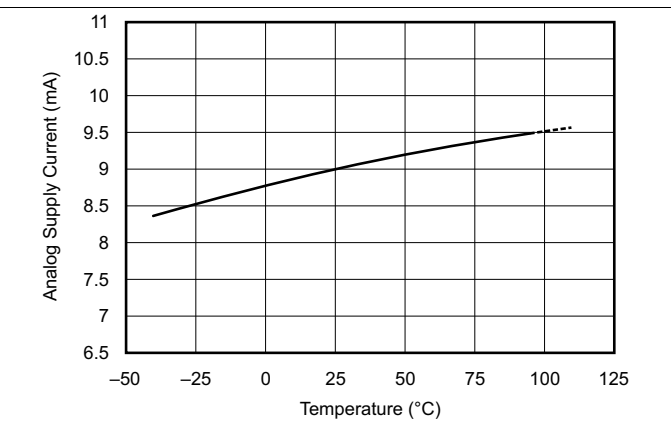**Figure 4. Digital Supply Current vs Temperature**

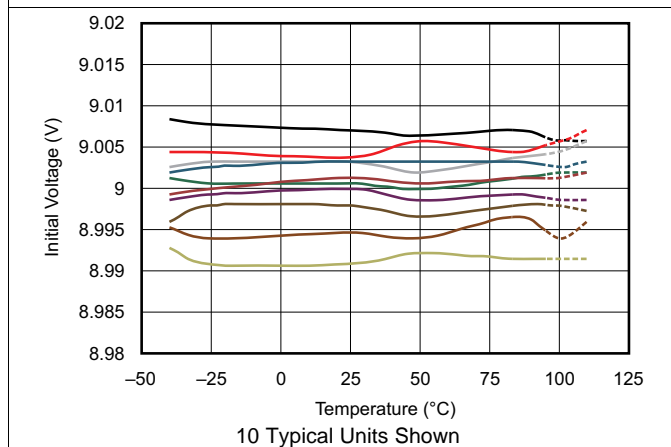**Figure 5. Analog Supply Current vs Temperature**

Figure 6. Output Voltage vs Temperature
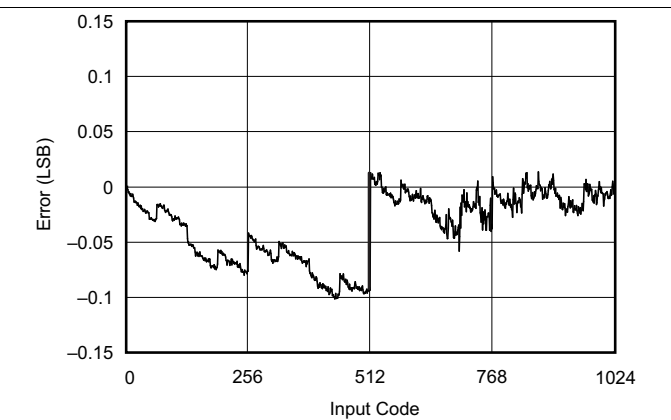

Figure 7. Differential Linearity Error

Typical Characteristics (continued)

At T_A = 25°C, V_S = 18 V, V_{SD} = 2 V, R_L = 1.5 kΩ connected to ground, and C_L = 200 pF, unless otherwise noted.

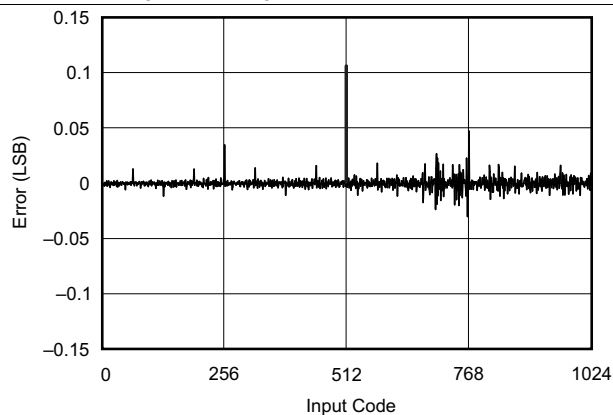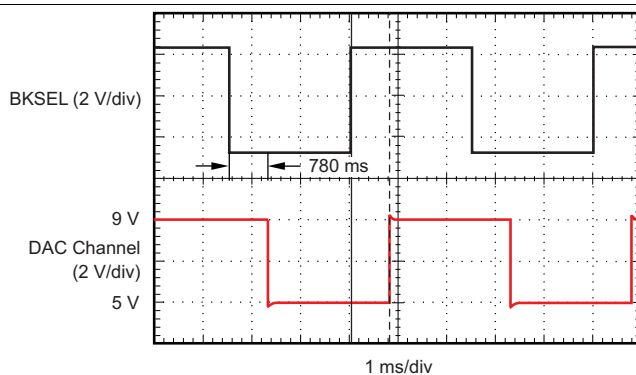**Figure 8. Integral Linearity Error**

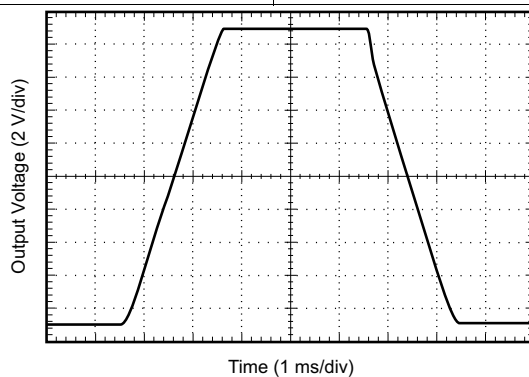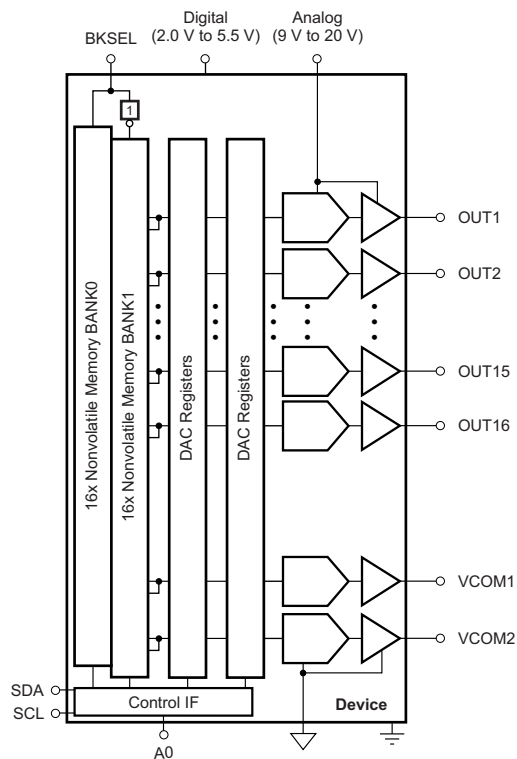**Figure 9. BKSEL Switching Time Delay**

Figure 10. Large-Signal Step Response

7 Detailed Description

7.1 Overview

The BUF16821-Q1 programmable voltage reference allows fast and easy adjustment of 16 programmable gamma reference outputs and two VCOM outputs, each with 10-bit resolution. The device is programmed through a high-speed, I^{2}C interface. The final gamma and VCOM values can be stored in the onboard, nonvolatile memory. To allow for programming errors or liquid crystal display (LCD) panel rework, the device supports up to 16 write operations to the onboard memory. The device has two separate memory banks, allowing simultaneous storage of two different gamma curves to facilitate dynamic switching between gamma curves. Figure 19 illustrates a typical configuration of the device.

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Two-Wire Bus Overview

The device communicates over an industry-standard, two-wire interface to receive data in slave mode. This standard uses a two-wire, open-drain interface that supports multiple devices on a single bus. Bus lines are driven to a logic low level only. The device that initiates the communication is called a *master*, and the devices controlled by the master are *slaves*. The master generates the serial clock on the clock signal line (SCL), controls the bus access, and generates the start and stop conditions.

To address a specific device, the master initiates a start condition by pulling the data signal line (SDA) from a high to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte on the SCL rising edge, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an acknowledge and pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a start or stop condition.

Feature Description (continued)

When all data are transferred, the master generates a stop condition, indicated by pulling SDA from low to high while SCL is high. The device can act only as a slave device and therefore never drives SCL. SCL is an input only for the BUF16821-Q1.

7.3.2 Data Rates

The two-wire bus operates in one of three speed modes:
- Standard: allows a clock frequency of up to 100 kHz;
- Fast: allows a clock frequency of up to 400 kHz; and
- High-speed mode (also called Hs mode): allows a clock frequency of up to 2.7 MHz.

The device is fully compatible with all three modes. No special action is required to use the device in standard or fast modes, but high-speed mode must be activated. To activate high-speed mode, send a special address byte of 00001 xxx, with SCL ≤ 400 kHz, following the start condition; where *xxx* are bits unique to the Hs-capable master, which can be any value. This byte is called the Hs master code. Table 1 provides a reference for the high-speed mode command code. (Note that this configuration is different from normal address bytes—the low bit does not indicate read or write status.) The device responds to the high-speed command regardless of the value of these last three bits. The device does not acknowledge this byte; the communication protocol prohibits acknowledgment of the Hs master code. Upon receiving a master code, the device switches on its Hs mode filters, and communicates at up to 2.7 MHz. Additional high-speed transfers may be initiated without resending the Hs mode byte by generating a repeat start without a stop. The device switches out of Hs mode with the next stop condition.

Table 1. Quick-Reference of Command Codes

COMMAND	CODE
General-call reset	Address byte of 00h followed by a data byte of 06h.
High-speed mode	00001xxx, with SCL ≤ 400 kHz; where *xxx* are bits unique to the Hs-capable master. This byte is called the Hs master code.

7.3.3 General-Call Reset and Power-Up

The device responds to a general-call reset, which is an address byte of 00h (0000 0000) followed by a data byte of 06h (0000 0110). The device acknowledges both bytes. Table 1 provides a reference for the general-call reset command code. Upon receiving a general-call reset, the device performs a full internal reset, as though it was powered off and then on. The device always acknowledges the general-call address byte of 00h (0000 0000), but does not acknowledge any general-call data bytes other than 06h (0000 0110).

The device automatically performs a reset when powered up. As part of the reset, the device is configured for all outputs to change to the last programmed nonvolatile memory values, or 1000000000 if the nonvolatile memory values are not programmed.

7.3.4 Output Voltage

The buffer output values are determined by the analog supply voltage (V_S) and the decimal value of the binary input code used to program that buffer. The value is calculated using Equation 1:

$$V_{OUT} = V_S \times \left(\frac{CODE_{10}}{1024} \right)$$

(1)

The device outputs are capable of a full-scale voltage output change in typically 5 µs; no intermediate steps are required.

7.3.5 Updating the DAC Output Voltages

Updating the digital-to-analog converter (DAC) and the VCOM **register** is not the same as updating the DAC and VCOM **output voltage** because the device features a double-buffered register structure. There are two methods for updating the DAC and VCOM output voltages.

Method 1: Method 1 is used when the DAC and VCOM output voltage are desired to change immediately after writing to a DAC register. For each write transaction, the master sets data bit 15 to a 1. The DAC and VCOM output voltage update occurs after receiving the 16th data bit for the currently-written register.

Method 2: Method 2 is used when all DAC and VCOM output voltages are desired to change at the same time. First, the master writes to the desired DAC and VCOM channels with data bit 15 a 0. Then, when writing the last desired DAC and VCOM channel, the master sets data bit 15 to a 1. All DAC and VCOM channels are updated at the same time after receiving the 16th data bit.

7.3.6 DIE_ID and DIE_REV Registers

The user can verify the presence of the BUF16821-Q1 in the system by reading from address 111101. When read at this address, the BUF16821-Q1A returns *0101100100100111* and the BUF16821-Q1B returns *0101100100100100*.

The user can also determine the die revision of the device by reading from register 111100. The device returns *0000000000000000* when a RevA die is present. RevB is designated by *0000000000000001*, and so on.

7.3.7 Read and Write Operations

Read and write operations can be done for a single DAC and VCOM or for multiple DACs and VCOMs. Writing to a DAC and VCOM register differs from writing to the nonvolatile memory. Bits D15–D14 of the most significant byte of data determine if data are written to the DAC and VCOM register or the nonvolatile memory.

7.3.7.1 Read and Write: DAC and VCOM Register (Volatile Memory)

The device is able to read from a single DAC and VCOM, or multiple DACs and VCOMs, or write to the register of a single DAC and VCOM, or multiple DACs and VCOMs in a single communication transaction. The DAC pointer addresses begin with 000000 (which corresponds to OUT1) through 001111 (which corresponds to OUT16). Addresses 010010 and 010011 are VCOM1 and VCOM2, respectively.

Write commands are performed by setting the read and write bit low. Setting the read or write bit high performs a read transaction.

7.3.7.2 Writing: DAC and VCOM Register (Volatile Memory)

To write to a single DAC and VCOM register:
1. Send a start condition on the bus.
2. Send the device address and read and write bit = low. The device acknowledges this byte.
3. Send a DAC and VCOM pointer address byte. Set bit D7 = 0 and D6 = 0. Bits D5–D0 are the DAC and VCOM address. Although the device acknowledges 000000 through 010111, data are stored and returned only from these addresses:
   – 000000 through 001111
   – 010010 through 010011
   The device returns *0000* for reads from 010000 through 010001, and 010100 through 010111. See Table 4 for valid DAC and VCOM addresses.
4. Send two bytes of data for the specified register. Begin by sending the most significant byte first (bits D15–D8, of which only bits D9 and D8 are used, and bits D15–D14 must not be 01), followed by the least significant byte (bits D7–D0). The register is updated after receiving the second byte.
5. Send a stop or start condition on the bus.

The device acknowledges each data byte. If the master terminates communication early by sending a stop or start condition on the bus, the specified register is not updated. Updating the DAC and VCOM register is not the same as updating the DAC and VCOM output voltage; see the *Updating the DAC Output Voltages* section.

The process of updating multiple DAC and VCOM registers begins the same as when updating a single register. However, instead of sending a stop condition after writing the addressed register, the master continues to send data for the next register. The device automatically and sequentially steps through subsequent registers as additional data are sent. The process continues until all desired registers are updated or a stop or start condition is sent.

To write to multiple DAC and VCOM registers:

1. Send a start condition on the bus.
2. Send the device address and read or write bit = low. The device acknowledges this byte.
3. Send either the OUT1 pointer address byte to start at the first DAC, or send the pointer address byte for whichever DAC and VCOM is the first in the sequence of DACs and VCOMs to be updated. The device begins with this DAC and VCOM and steps through subsequent DACs and VCOMs in sequential order.
4. Send the bytes of data; begin by sending the most significant byte (bits D15–D8, of which only bits D9 and D8 have meaning, and bits D15–D14 must not be 01), followed by the least significant byte (bits D7–D0). The first two bytes are for the DAC and VCOM addressed in the previous step. The DAC and VCOM register is automatically updated after receiving the second byte. The next two bytes are for the following DAC and VCOM. That DAC and VCOM register is updated after receiving the fourth byte. This process continues until the registers of all following DACs and VCOMs are updated. The device continues to accept data for a total of 18 DACs; however, the two data sets following the 16th data set are meaningless. The 19th and 20th data sets apply to VCOM1 and VCOM2. The write disable bit cannot be accessed using this method. This bit must be written to using *the write to a single DAC register* procedure.
5. Send a stop or start condition on the bus.

The device acknowledges each byte. To terminate communication, send a stop or start condition on the bus. Only DAC registers that have received both bytes of data are updated.

7.3.7.3 Reading: DAC, VCOM, Other Register (Volatile Memory)

Reading a register returns the data stored in that DAC, VCOM, other register.

To read a single DAC, VCOM, other register:

1. Send a start condition on the bus.
2. Send the device address and read or write bit = low. The device acknowledges this byte.
3. Send the DAC, VCOM, other pointer address byte. Set bit D7 = 0 and D6 = 0; bits D5–D0 are the DAC, VCOM, other address. Note that the device stores and returns data only from these addresses:
   – 000000 through 001111
   – 010010
   – 010011
   – 111100 through 111111
   The device returns *0000* for reads from 010000 and 010001, and 010100 through 010111. See Table 4 for valid DAC, VCOM, other addresses.
4. Send a start or stop and start condition.
5. Send the correct device address and read or write bit = high. The device acknowledges this byte.
6. Receive two bytes of data. These bytes are for the specified register. The most significant byte (bits D15–D8) is received first; next is the least significant byte (bits D7–D0). In the case of DAC and VCOM channels, bits D15–D10 have no meaning.
7. Acknowledge after receiving the first byte.
8. Send a stop or start condition on the bus or do not acknowledge the second byte to end the read transaction.

Communication may be terminated by sending a premature stop or start condition on the bus, or by not acknowledging.

To read multiple registers:

1. Send a start condition on the bus.
2. Send the device address and read or write bit = low. The device acknowledges this byte.
3. Send either the OUT1 pointer address byte to start at the first DAC, or send the pointer address byte for whichever register is the first in the sequence of DACs and VCOMs to be read. The device begins with this DAC and VCOM and steps through subsequent DACs and VCOMs in sequential order.
4. Send a start or stop and start condition on the bus.
5. Send the correct device address and read or write bit = high. The device acknowledges this byte.

6. Receive two bytes of data. These bytes are for the specified DAC and VCOM. The first received byte is the most significant byte (bits D15–D8; only bits D9 and D8 have meaning), next is the least significant byte (bits D7–D0).

7. Acknowledge after receiving each byte of data.

8. When all desired DACs are read, send a stop or start condition on the bus.

Communication may be terminated by sending a premature stop or start condition on the bus, or by not sending the acknowledge bit. Reading the DieID, DieRev, and MaxBank registers is not supported in this mode of operation (these values must be read using the single register read method).

7.3.7.4 Write: Nonvolatile Memory for the DAC Register

The device is able to write to the nonvolatile memory of a single DAC and VCOM in a single communication transaction. In contrast to the BUF20820, writing to multiple nonvolatile memory words in a single transaction is not supported. Valid DAC and VCOM pointer addresses begin with 000000 (which corresponds to OUT1) through 001111 (which corresponds to OUT16). Addresses 010010 and 010011 are VCOM1 and VCOM2, respectively.

When programming the nonvolatile memory, the analog supply voltage must be between 9 V and 20 V. Write commands are performed by setting the read or write bit low.

To write to a single nonvolatile register:

1. Send a start condition on the bus.

2. Send the device address and read or write bit = low. The device acknowledges this byte. Although the device acknowledges 000000 through 010111, data are stored and returned only from these addresses:
   – 000000 through 001111
   – 010010 and 010011
   The device returns *0000* for reads from 010000 through 010001, and 010100 through 010111. See Table 4 for DAC and VCOM addresses.

3. Send a DAC and VCOM pointer address byte. Set bit D7 = 0 and D6 = 0. Bits D5–D0 are the DAC and VCOM address.

4. Send two bytes of data for the nonvolatile register of the specified DAC and VCOM. Begin by sending the most significant byte first (bits D15–D8, of which only bits D9 and D8 are data bits, and bits D15–D14 must be 01), followed by the least significant byte (bits D7–D0). The register is updated after receiving the second byte.

5. Send a stop condition on the bus.

The device acknowledges each data byte. If the master terminates communication early by sending a stop or start condition on the bus, the specified nonvolatile register is not updated. Writing a nonvolatile register also updates the DAC and VCOM register and output voltage.

The DAC and VCOM register and DAC and VCOM output voltage are updated immediately, while the programming of the nonvolatile memory takes up to 250 µs. When a nonvolatile register write command is issued, no communication with the device should take place for at least 250 µs. Writing or reading over the serial interface while the nonvolatile memory is being written jeopardizes the integrity of the data being stored.

7.3.7.5 Read: Nonvolatile Memory for the DAC Register

To read the data present in nonvolatile register for a particular DAC and VCOM channel, the master must first issue a general acquire command, or a single acquire command with the appropriate DAC and VCOM channel chosen. This action updates both the DAC and VCOM registers and DAC and VCOM output voltages. The master may then read from the appropriate DAC and VCOM register as described earlier.
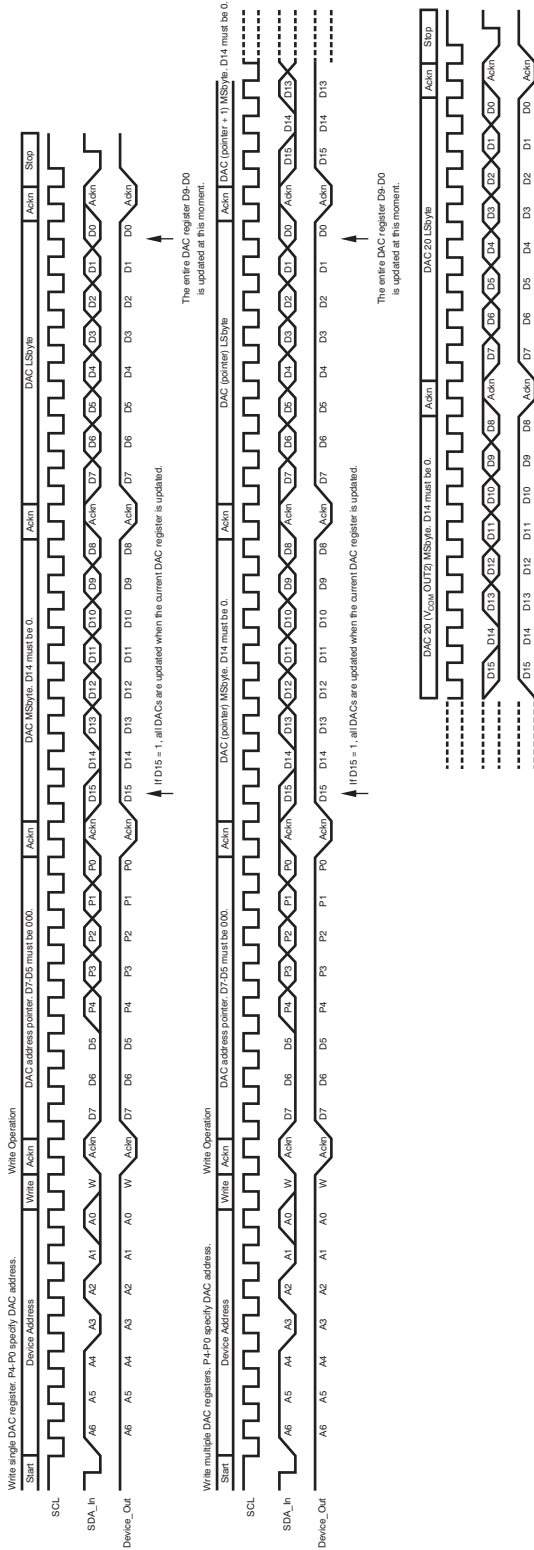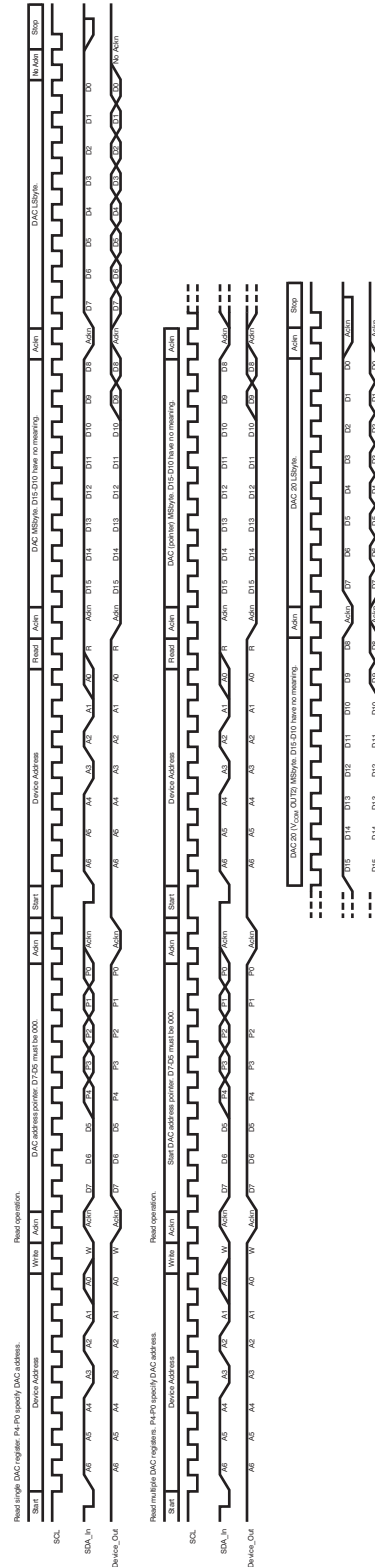
Figure 11. Write DAC Register Timing
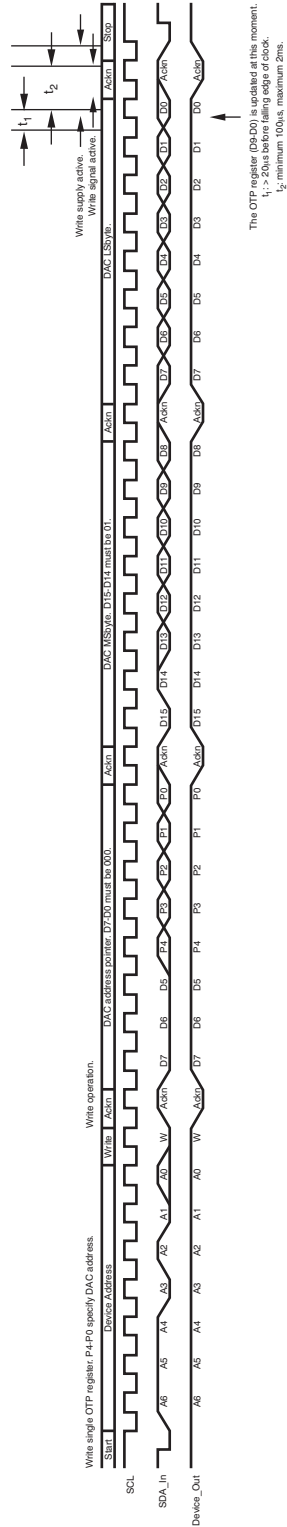
Figure 12. Read Register Timing

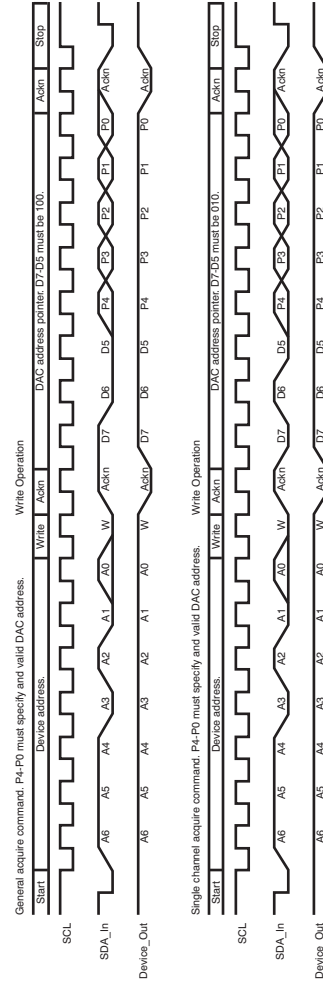**Figure 13. Write Nonvolatile Register Timing**
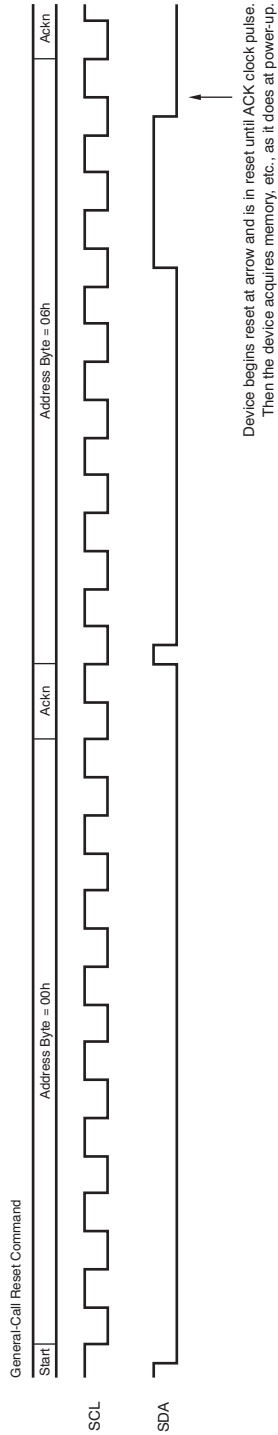

Figure 14. Acquire Operation Timing

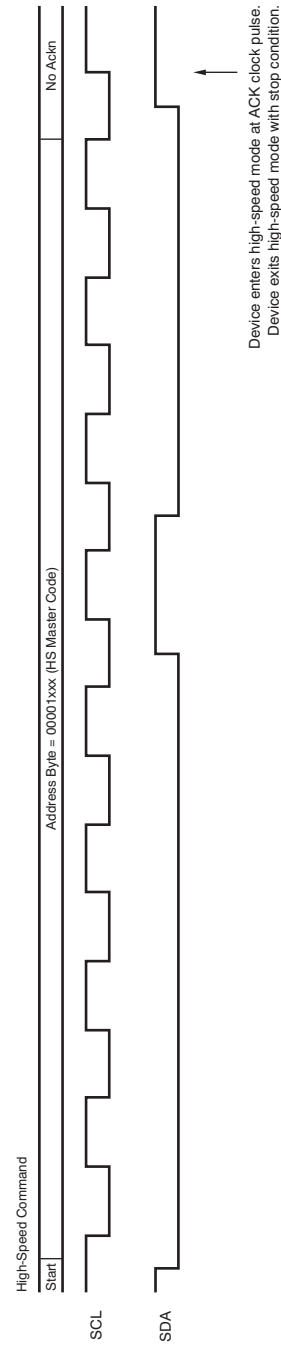**Figure 15. General-Call Reset Timing**

Figure 16. High-Speed Mode Timing

7.3.8 Output Protection

The device output stages can safely source and sink the current levels indicated in Figure 2 and Figure 3. However, there are other modes where precautions must be taken to prevent the output stages from being damaged by excessive current flow. The outputs (OUT1 through OUT16, VCOM1 and VCOM2) include electrostatic discharge (ESD) protection diodes, as shown in Figure 17. Normally, these diodes do not conduct and are passive during typical device operation. Unusual operating conditions can occur where the diodes may conduct, potentially subjecting them to high, even damaging current levels. These conditions are most likely to occur when a voltage applied to an output exceeds (V_S) + 0.5 V, or drops below GND – 0.5 V.

One common scenario where this condition can occur is when the output pin is connected to a sufficiently large capacitor and the device power-supply source (V_S) is suddenly removed. Removing the power-supply source allows the capacitor to discharge through the current-steering diodes. The energy released during the high current flow period causes the power dissipation limits of the diode to be exceeded. Protection against the high current flow may be provided by placing current-limiting resistors in series with the output; see Figure 19. Select a resistor value that restricts the current level to the maximum rating for the particular pin.
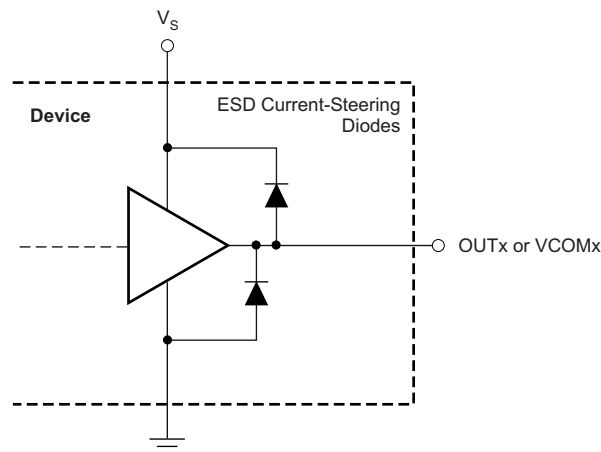

Figure 17. Output Pins ESD Protection Current-Steering Diodes

7.4 Device Functional Modes

7.4.1 End-User Selected Gamma Control

The device is well-suited for providing two levels of gamma control by using the BKSEL pin because the device has two banks of nonvolatile memory, as shown in Figure 18. When the state of the BKSEL pin changes, the device updates all 18 programmable buffer outputs simultaneously after 750 µs (±80 µs).

To update all 18 programmable output voltages simultaneously via hardware, toggle the BKSEL pin to switch between gamma curve 0 (stored in Bank0) and gamma curve 1 (stored in Bank1).

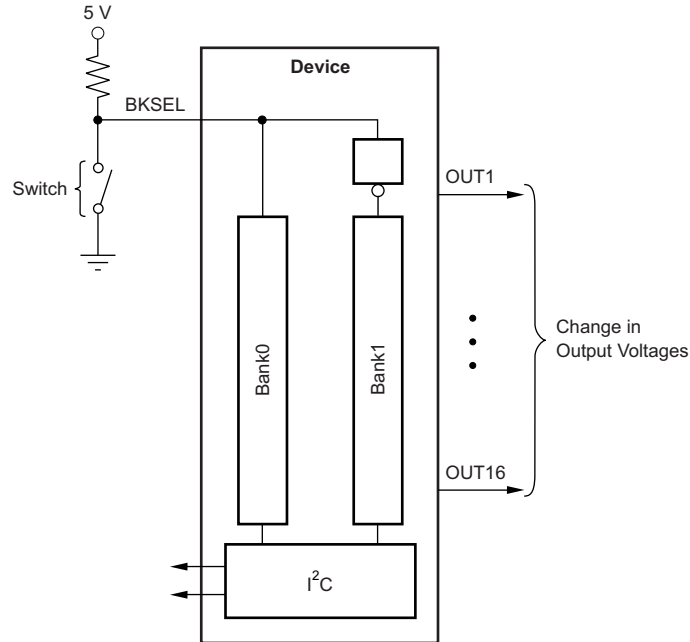All DAC and VCOM registers and output voltages are updated simultaneously after approximately 750 µs.

Figure 18. Gamma Control

7.4.2 Dynamic Gamma Control

Dynamic gamma control is a technique used to improve the picture quality in LCD television applications. This technique typically requires switching gamma curves between frames. Using the BKSEL pin to switch between two gamma curves does not often provide good results because of the 750 µs required to transfer the data from the nonvolatile memory to the DAC register. However, dynamic gamma control can still be accomplished by storing two gamma curves in an external electrically erasable programmable read-only memory (EEPROM) and writing directly to the DAC register (volatile).

The double register input structure saves programming time by allowing updated DAC values to be pre-stored into the first register bank. Storage of this data can occur while a picture is still being displayed. Because the data are only stored into the first register bank, the DAC and VCOM output values remain unchanged—the display is unaffected. At the beginning or the end of a picture frame, the DAC and VCOM outputs (and therefore, the gamma voltages) can be quickly updated by writing a 1 in bit 15 of any DAC and VCOM register. For details on the operation of the double register input structure, see the *Updating the DAC Output Voltages* section.

To update all 18 programmable output voltages simultaneously via software, perform the following actions:

STEP 1: Write to registers 1–18 with bit 15 always 0.

STEP 2: Write any DAC and VCOM register a second time with identical data. Make sure that bit 15 is set to 1. All DAC and VCOM channels are updated simultaneously after receiving the last bit of data.

7.5 Programming

7.5.1 Addressing the Device

The device address 111010x, where *x* is the state of the A0 pin. When the A0 pin is low, the device acknowledges on address 74h (1110100). If the A0 pin is high, the device acknowledges on address 75h (1110101). Table 2 shows the A0 pin settings and device address options.

Other valid addresses are possible through a simple mask change. Contact your TI representative for information.

Table 2. Quick-Reference of Device Addresses

DEVICE, COMPONENT (Device Address)	ADDRESS
A0 pin is low (device acknowledges on address 74h)	1110100
A0 pin is high (device acknowledges on address 75h)	1110101

(1) RC combination optional; see the *Output Protection* section.

(2) GNDA and GNDD must be connected together.

Figure 19. Typical Application Configuration

7.5.2 Nonvolatile Memory

7.5.2.1 BKSEL Pin

The device has 16x rewrite capability of the nonvolatile memory. Additionally, the device is capable of storing two distinct gamma curves in two different nonvolatile memory banks, each of which has 16x rewrite capability. One of the two available banks is selected using the external input pin, BKSEL. When this pin is low, Bank0 is selected; when this pin is high, Bank1 is selected.

When the BKSEL pin changes state, the device acquires the last programmed DAC and VCOM values from the nonvolatile memory associated with this newly chosen bank. At power-up, the state of the BKSEL pin determines which memory bank is selected.

The I^{2}C master can also update (acquire) the DAC registers with the last programmed nonvolatile memory values using software control. The bank to be acquired depends on the state of BKSEL.

7.5.2.2 General Acquire Command

A general acquire command is used to update all registers and DAC and VCOM outputs to the last programmed values stored in nonvolatile memory. A single-channel acquire command updates only the register and DAC and VCOM output of the DAC and VCOM corresponding to the DAC and VCOM address used in the single-channel acquire command.

These are the steps of the sequence to initiate a general channel acquire:
1. Be sure BKSEL is in its desired state and is stable for at least 1 ms.
2. Send a start condition on the bus.
3. Send the appropriate device address (based on A0) and the read or write bit = low. The device acknowledges this byte.
4. Send a DAC and VCOM pointer address byte. Set bit D7 = 1 and D6 = 0. Bits D5–D0 are any valid DAC and VCOM address. Although the device acknowledges 000000 through 010111, data are stored and returned only from these addresses:
   – 000000 through 001111
   – 010010 and 010011
   The device returns *0000* for reads from 010000 and 010001, and 010100 through 010111. See Table 4 for valid DAC and VCOM addresses.
5. Send a stop condition on the bus.

Approximately 750 µs (±80 µs) after issuing this command, all DAC and VCOM registers and DAC and VCOM output voltages change to the respective, appropriate nonvolatile memory values.

7.5.2.3 Single-Channel Acquire Command

These are the steps to initiate a single-channel acquire:
1. Be sure BKSEL is in its desired state and is stable for at least 1 ms.
2. Send a start condition on the bus.
3. Send the device address (based on A0) and read or write bit = low. The device acknowledges this byte.
4. Send a DAC and VCOM pointer address byte using the DAC and VCOM address corresponding to the output and register to update with the OTP memory value. Set bit D7 = 0 and D6 = 1. Bits D5–D0 are the DAC and VCOM address. Although the device acknowledges 000000 through 010111, data are stored and returned only from these addresses:
   – 000000 through 001111
   – 010010 and 010011
   The device returns *0000* reads from 010000 and 010001, and 010100 through 010111. See Table 4 for valid DAC and VCOM addresses.
5. Send a stop condition on the bus.

Approximately 36 µs (±4 µs) after issuing this command, the specified DAC and VCOM register and DAC and VCOM output voltage change to the appropriate OTP memory value.

7.5.2.4 MaxBank

The device can provide the user with the number of times the nonvolatile memory of a particular DAC and VCOM channel nonvolatile memory is written to for the current memory bank. This information is provided by reading the register at pointer address 111111.

There are two ways to update the MaxBank register:

1. After initiating a single acquire command, the device updates the MaxBank register with a code corresponding to how many times that particular channel memory is written to.
2. Following a general acquire command, the device updates the MaxBank register with a code corresponding to the maximum number of times the most used channel (OUT1–16 and VCOMs) is written to.

MaxBank is a read-only register and is only updated by performing a general- or single-channel acquire.

Table 3 shows the relationship between the number of times the nonvolatile memory is programmed and the corresponding state of the MaxBank Register.

Table 3. MaxBank Details

NUMBER OF TIMES WRITTEN TO	RETURNS CODE
0	0000
1	0000
2	0001
3	0010
4	0011
5	0100
6	0101
7	0110
8	0111
9	1000
10	1001
11	1010
12	1011
13	1100
14	1101
15	1110
16	1111

7.5.2.5 Parity Error Correction

The device provides single-bit parity error correction for data stored in the nonvolatile memory to provide increased reliability of the nonvolatile memory. If a single bit of nonvolatile memory for a channel fails, the device corrects for the failure and updates the appropriate DAC with the intended value when its memory is acquired.

If more than one bit of nonvolatile memory for a channel fails, the device does not correct for it, and updates the appropriate DAC and VCOM with the default value of 1000000000.

7.6 Register Maps

Table 4. DAC Register Pointer Addresses

DAC REGISTER	POINTER ADDRESS
OUT1	000000
OUT2	000001
OUT3	000010
OUT4	000011
OUT5	000100
OUT6	000101
OUT7	000110
OUT8	000111
OUT9	001000
OUT10	001001
OUT11	001010
OUT12	001011
OUT13	001100
OUT14	001101
OUT15	001110
OUT16	001111
VCOM1	010010
VCOM2	010011
OTHER REGISTER	**POINTER ADDRESS**
Die_Rev	111100
Die_ID	111101
MaxBank	111111

8 Application and Implementation

8.1 Application Information

The BUF16821-Q1 is a multichannel programmable voltage reference. Featuring 16 programmable gamma reference outputs and two programmable VCOM outputs, the device is designed to interface between timing controllers and source drivers commonly used in LCD displays.

8.2 Typical Application

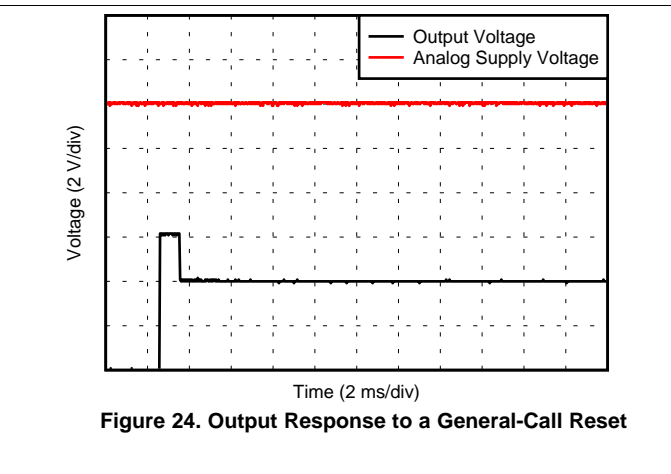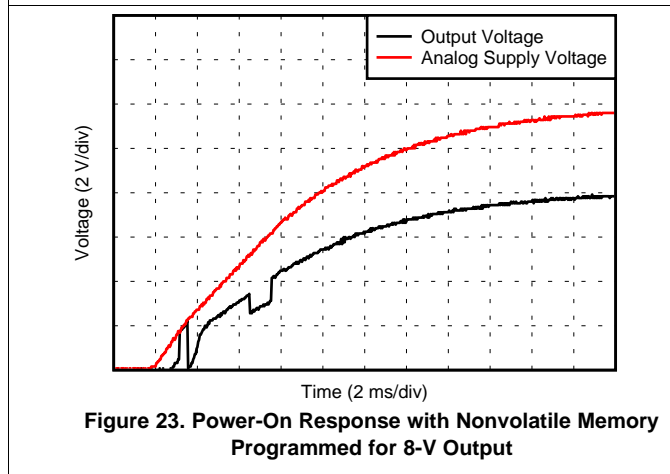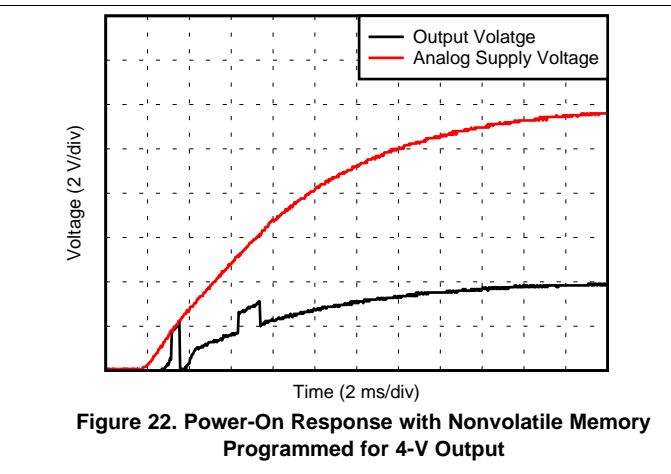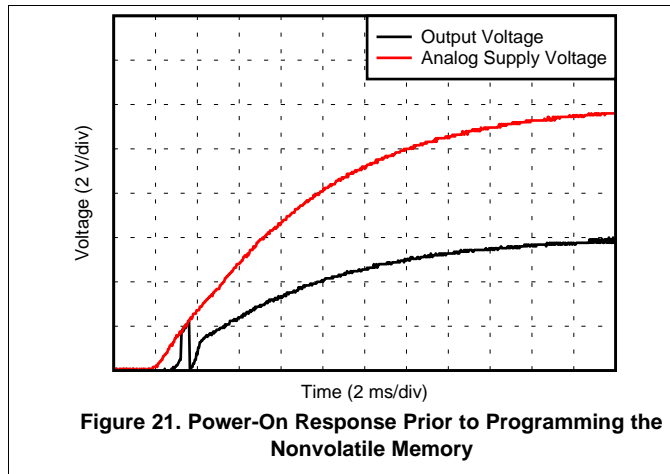**Figure 20. Gamma Control Block Diagram**

8.2.1 Design Requirements

If the nonvolatile memory has never been programmed, the BUF16821-Q1 outputs defaults to V_S / 2 following power-up. Refer to the *Power Supply Recommendations* section for proper power-supply sequencing requirements. Figure 21 shows the typical output response when the analog power supply (V_S) ramps to its desired value. When the analog supply is below 2 V, the outputs follow the analog supply voltage. After the analog supply voltage (V_S) exceeds approximately 2 V, the outputs begin to track at V_S / 2. This sequence is illustrated in Figure 21.

If the nonvolatile memory is pre-programmed, the device outputs ramp to their pre-programmed values. Figure 22 and Figure 23 illustrate the power-up behavior of the device pre-programmed to a 4-V and 8-V output voltage, respectively. Note that when the analog power supply voltage (V_S) exceeds approximately 5 V, the device performs an automatic read of the nonvolatile memory, acquiring the pre-programmed values to ensure the proper output value when the analog supply voltage ramps to its final value. During the nonvolatile memory acquire operation, the output tracks at V_S / 2 for approximately 1 ms. This sequence is illustrated in Figure 22 and Figure 23 . Note that the minimum valid analog supply voltage, V_S, is specified as 9 V. Below this value the outputs should not be considered valid.

Figure 24 illustrates the device output response to a general-call reset. During the internal reset, the output momentarily tracks at V_S / 2 while the nonvolatile memory values are acquired. Following the reset, the output returns to the pre-programmed value.

8.2.2 Detailed Design Procedure

Proper power-supply bypassing is required when using the BUF16821-Q1. TI recommends connecting a 10-µF capacitor in parallel with a 100-nF capacitor at each analog supply pin (pins 9 and 23), as illustrated in Figure 19. Similarly, connecting a 1-µF capacitor in parallel with a 100-nF capacitor at the digital supply pin (pin 13) is also recommended. However, adding more than 200-pF capacitance at any gamma or VCOM output is not recommended; see the *Output Protection* section.

Typical Application (continued)

8.2.3 Application Curves

Figure 21. Power-On Response Prior to Programming the Nonvolatile Memory

Figure 22. Power-On Response with Nonvolatile Memory Programmed for 4-V Output

Figure 23. Power-On Response with Nonvolatile Memory Programmed for 8-V Output

Figure 24. Output Response to a General-Call Reset

9 Power Supply Recommendations

The device can be powered using an analog supply voltage from 9 V to 20 V, and a digital supply from 2 V to 5.5 V. The digital supply must be applied before the analog supply to avoid excessive current and power consumption, or possibly even damage to the device if left connected only to the analog supply for extended periods of time.

10 Layout

10.1 Layout Guidelines

10.1.1 General PowerPAD Design Considerations

The device is available in a thermally-enhanced PowerPAD package. This package is constructed using a downset leadframe upon which the die is mounted; see Figure 25(a) and Figure 25(b). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package; see Figure 25(c). This thermal pad has direct thermal contact with the die; thus, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.
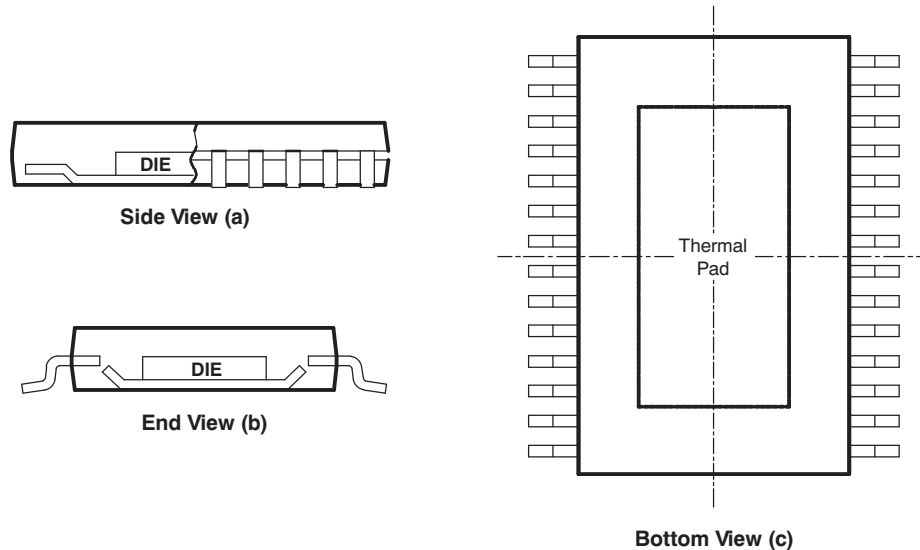

Figure 25. Views of a Thermally-Enhanced PWP Package

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the PowerPAD to the printed circuit board (PCB) is always required, even with applications that have low power dissipation. This technique provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

The PowerPAD must be connected to the most negative supply voltage on the device, GNDA and GNDD.

1. Prepare the PCB with a top-side etch pattern. There should be etching for the leads as well as etch for the thermal pad.
2. Place recommended holes in the area of the thermal pad. Ideal thermal land size and thermal via patterns for the HTSSOP-28 PWP package can be seen in the technical brief, *PowerPAD Thermally-Enhanced Package* (SLMA002), available for download at www.ti.com. These holes should be 13 mils (0.33 mm) in diameter. Keep these holes small, so that solder wicking through the holes is not a problem during reflow. An example thermal land pattern mechanical drawing is attached to the end of this data sheet.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area to help dissipate the heat generated by the device. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. These vias can be larger because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.
4. Connect all holes to the internal plane that is at the same voltage potential as the GND pins.

Layout Guidelines (continued)

5. When connecting these holes to the internal plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This configuration makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the device PowerPAD package should make their connection to the internal plane with a complete connection around the entire circumference of the plated-through hole.

6. The top-side solder mask should leave the pins of the package and the thermal pad area with its twelve holes exposed. The bottom-side solder mask should cover the holes of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.

7. Apply solder paste to the exposed thermal pad area and all device pins.

8. With these preparatory steps in place, simply place the device in position and run the chip through the solder reflow operation as any standard surface-mount component. This preparation results in a properly installed part.

For a given $R_{\theta JA}$ (listed in the Electrical Characteristics), the maximum power dissipation is shown in Figure 26 and calculated by Equation 2:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

where

- P_D = maximum power dissipation (W),
- T_{MAX} = absolute maximum junction temperature (125°C), and
- T_A = free-ambient air temperature (°C). (2)
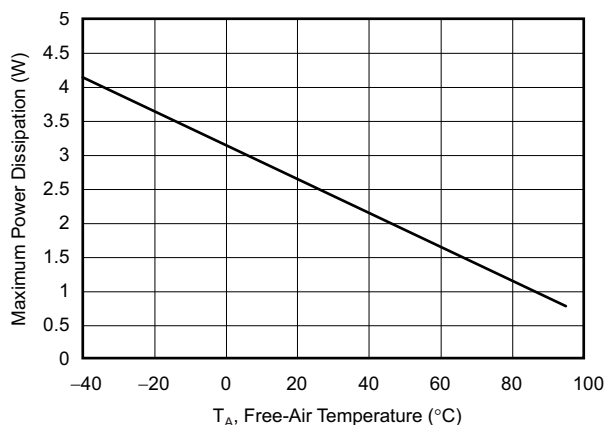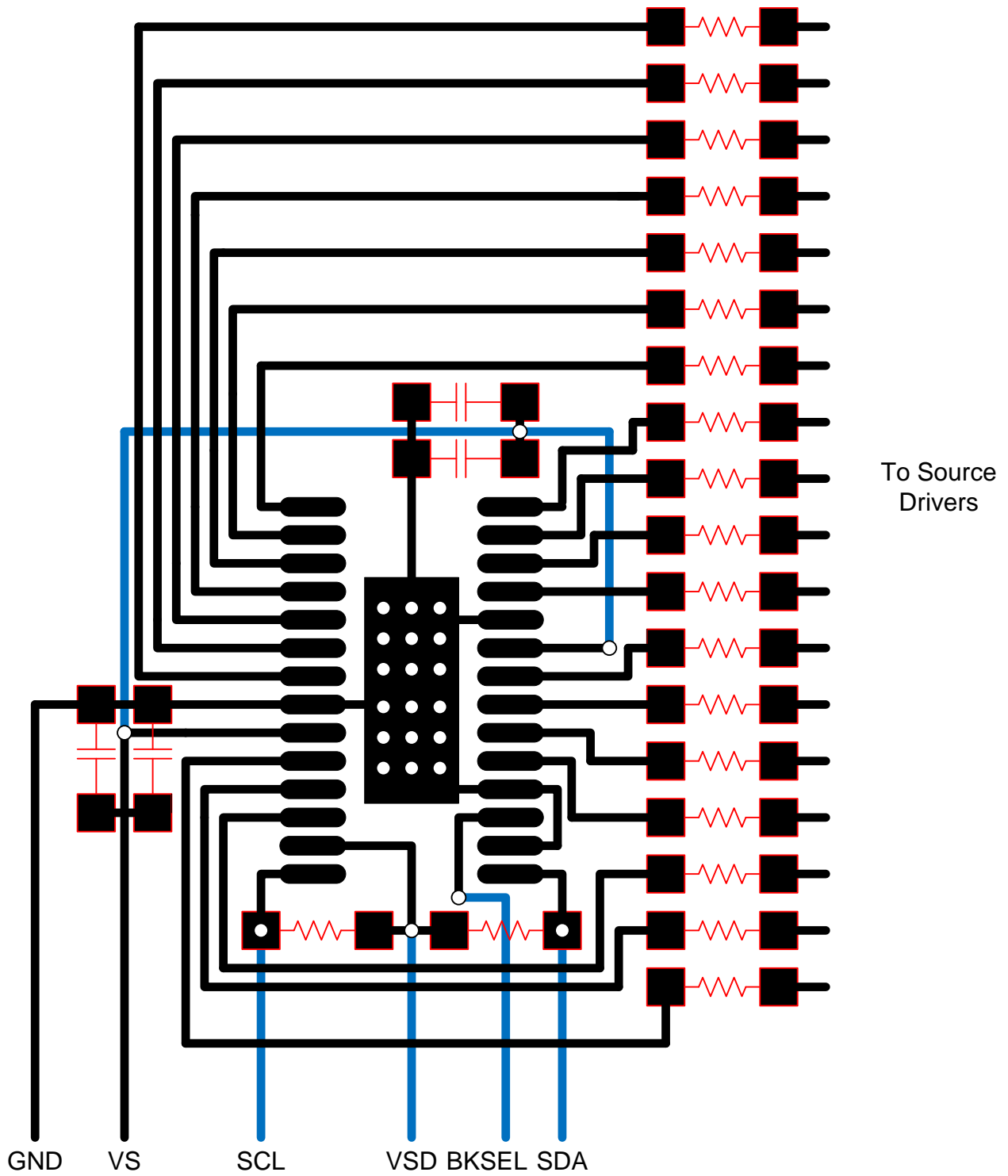

**Figure 26. Maximum Power Dissipation
vs Free-Air Temperature
(With PowerPAD Soldered Down)**

10.2   Layout Example

To Source
Drivers

GND   VS   SCL   VSD BKSEL SDA

To Timing Controller

Figure 27. PCB Layout Example

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

- 《BUF16821EVM-USB 用户指南》，SBOU106
- 《BUF20820 数据表》，SBOS330
- 《*PowerPAD 散热增强型封装*》，SLMA002
- 《*用伽马缓冲器驱动电容负载*》，SBOA134

11.2 Trademarks

PowerPAD is a trademark of Texas Instruments.
I^{2}C is a trademark of NXP Semiconductors.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BUF16821AIPWPRQ1	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B16821Q1
BUF16821AIPWPRQ1.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B16821Q1

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF BUF16821-Q1 :

● Catalog : BUF16821

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

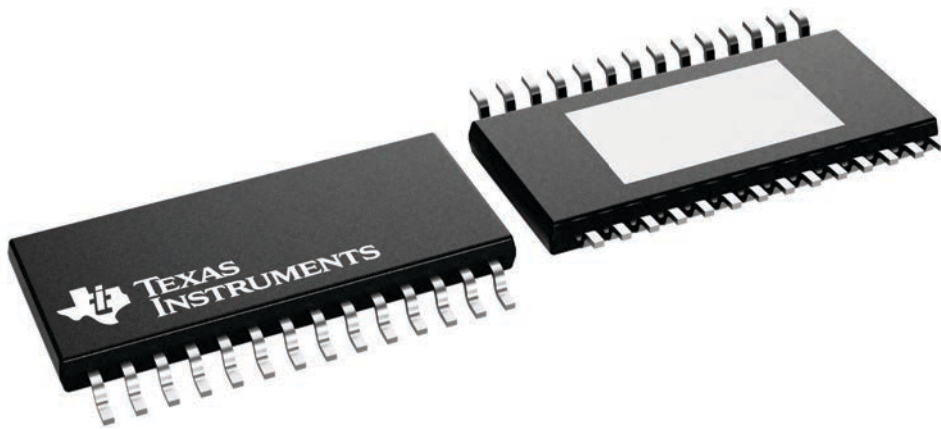**PWP 28**

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224765/B

PWP (R−PDSO−G28)   PowerPAD™ PLASTIC SMALL OUTLINE

4073225−6/I 05/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad
              Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding
              recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
         E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
         E.   Falls within JEDEC MO−153

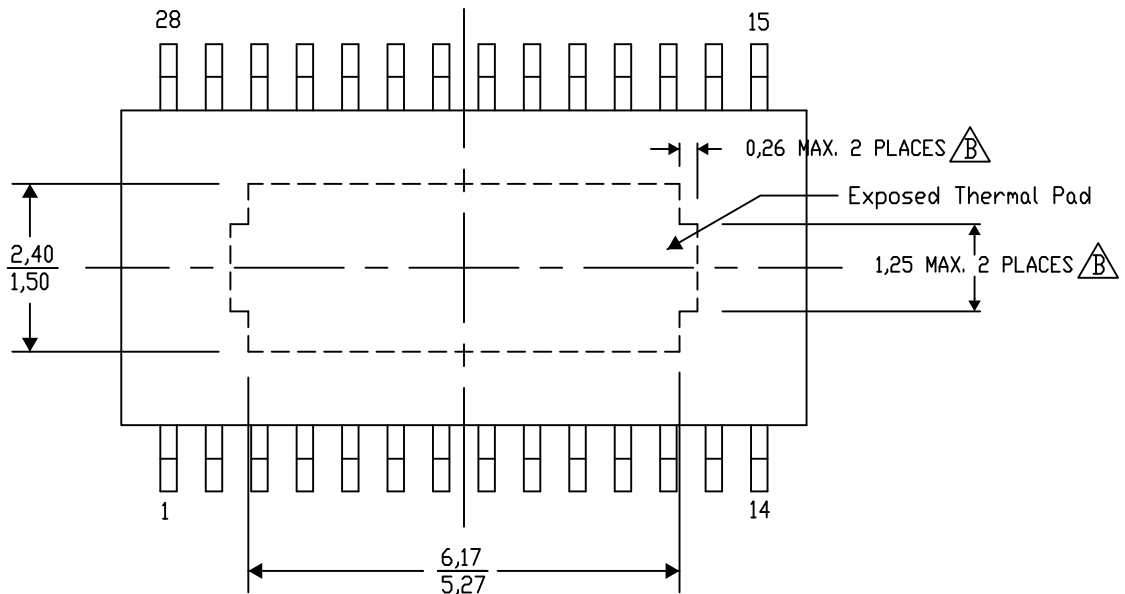**PowerPAD is a trademark of Texas Instruments.**

PWP (R−PDSO−G28)   PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

28   15

0,26 MAX. 2 PLACES /B\

Exposed Thermal Pad

$\dfrac{2,40}{1,50}$

1,25 MAX. 2 PLACES /B\

1   14

$\dfrac{6,17}{5,27}$

Top View

Exposed Thermal Pad Dimensions
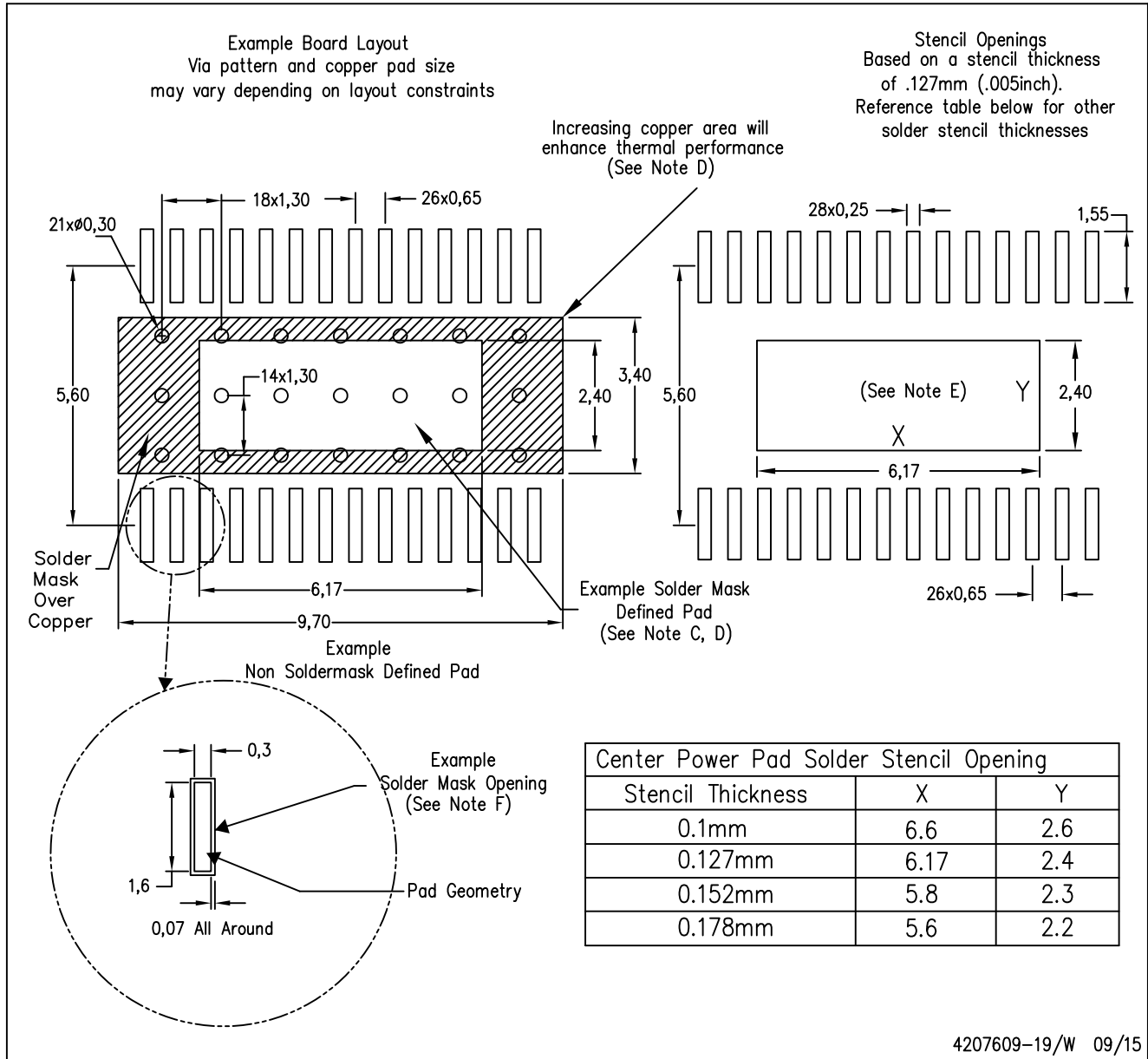
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NOTE: A. All linear dimensions are in millimeters
        /B\ Exposed tie strap features may not be present.

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PWP (R−PDSO−G28) PowerPAD™ PLASTIC SMALL OUTLINE

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
Reference table below for other
solder stencil thicknesses

Increasing copper area will
enhance thermal performance
(See Note D)

18x1,30   26x0,65

21x∅0,30

28x0,25   1,55

14x1,30

3,40
5,60   2,40

(See Note E)   Y   2,40

X

6,17

5,60

6,17

9,70

26x0,65

Example
Non Soldermask Defined Pad

Solder
Mask
Over
Copper

Example Solder Mask
Defined Pad
(See Note C, D)

Example

0,3

Example
Solder Mask Opening
(See Note F)

1,6

Pad Geometry

0,07 All Around

Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.17	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center
   solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad
   Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents
   are available at www.ti.com <http://www.ti.com>. Publication IPC−7351 is recommended for alternate designs.
   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.
   Customers should contact their board assembly site for stencil design recommendations. Example stencil
   design based on a 50% volumetric metal load solder paste. Refer to IPC−7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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