

CC2651P3 具有集成式功率放大器的 SimpleLink™ 单协议 2.4GHz 无线 MCU

1 特性

无线微控制器

- 功能强大的 48 MHz Arm® Cortex®-M4 处理器
- 352KB 闪存程序存储器
- 32KB 超低泄漏 SRAM
- 8KB 缓存 SRAM (也可作为通用 RAM 提供)
- 可编程无线电包括对 2-(G)FSK、4-(G)FSK、MSK、低功耗 *Bluetooth*® 5.2、IEEE 802.15.4 PHY 和 MAC 的支持
- 支持无线升级 (OTA)

低功耗

- MCU 功耗 :
 - 2.91 mA 有源模式, CoreMark®
 - 61 μ A/MHz (运行 CoreMark 时)
 - 0.8 μ A 待机模式, RTC, 32KB RAM
 - 0.1 μ A 关断模式, 引脚唤醒
- 无线电功耗 :
 - RX : 6.4 mA
 - TX : 7.1 mA (在 0 dBm 条件下)
 - TX : 9.5 mA (在 +5 dBm 条件下)
 - TX : 22 mA (在 +10 dBm 条件下)
 - TX : 101 mA (在 +20 dBm 和 7x7 封装条件下)

无线协议支持

- *Zigbee*®
- 低功耗 *Bluetooth*® 5.2
- SimpleLink™ TI 15.4-stack
- 专有系统

高性能无线电

- -104 dBm (在 125 kbps 低功耗 *Bluetooth*® 下)
- 高达 +20 dBm 的输出功率, 具有温度补偿

法规遵从性

- 适用于符合以下标准的系统 :
 - ETSI EN 300 328、EN 300 440 类别 2 和 3
 - FCC CFR47 第 15 部分
 - ARIB STD-T66

MCU 外设

- 数字外设可连接至任何 GPIO
- 四个 32 位或八个 16 位通用计时器
- 12 位 ADC、200 ksps、8 通道
- 8 位 DAC
- 模拟比较器
- UART、SSI、I²C、I²S
- 实时时钟 (RTC)
- 集成温度和电池监控器

安全驱动工具

- AES 128 位加密加速计
- 真随机数发生器 (TRNG)
- 软件开发套件 (SDK) 中提供了其他加密驱动器

开发工具和软件

- [LP-CC2651P3 开发套件](#)
- [SimpleLink™ CC13xx 和 CC26xx 软件开发套件 \(SDK\)](#)
- 用于简单无线电配置的 [SmartRF™ Studio](#)
- [SysConfig](#) 系统配置工具

工作温度范围

- 片上降压直流/直流转换器
- 1.8V 至 3.8V 单电源电压
- -40°C 至 +105°C

封装

- 7mm × 7mm RGZ VQFN48 (26 个 GPIO)
- 5mm × 5mm RKP VQFN40 (18 个 GPIO)
- 符合 RoHS 标准的封装



2 应用

- 2400 至 2500 MHz ISM 和 SRD 系统，¹
接收带宽低至 4kHz
- 楼宇自动化
 - 楼宇安防系统 - 运动检测器、电子智能锁、门窗传感器、车库门系统、网关
 - HVAC - 恒温器、无线环境传感器、HVAC 系统控制器、网关
 - 防火安全系统 - 烟雾和热量探测器、火警控制面板 (FACP)
 - 视频监控 - IP 网络摄像头
 - 升降机和自动扶梯 - 升降机和自动扶梯的电梯主控板

- 工业运输 - 资产跟踪
- 工厂自动化和控制
- 医疗
- 电子销售终端 (EPOS) - 电子货架标签 (ESL)
- 通信设备
 - 有线网络 - 无线 LAN 或 Wi-Fi 接入点、边缘路由器、小型企业路由器
- 个人电子产品
 - 家庭影院和娱乐 - 智能扬声器、智能显示器、机顶盒
 - 可穿戴设备 (非医用) - 智能追踪器、智能服装

3 说明

SimpleLink™ CC2651P3 器件是一款单协议 2.4 GHz 无线微控制器 (MCU)，支持以下协议：[Zigbee®](#)、低功耗 [Bluetooth®5.2](#)、IEEE 802.15.4g、[TI 15.4-Stack](#) (2.4 GHz)。CC2651P3 基于 [Arm® Cortex® M4](#) 主处理器，针对 [电网基础设施](#)、[楼宇自动化](#)、[零售自动化](#)、[个人电子产品](#) 和 [医疗应用](#) 中的低功耗无线通信和高级传感功能进行了优化。

CC2651P3 具有由 [Arm® Cortex® M0](#) 驱动的软件定义无线电，支持多个物理层和射频标准。该器件支持在 2360 MHz 至 2500 MHz 频带内运行。CC2651P3 具有高效的内置 PA，支持 +10 dBm TX (21 mA) 和 +20 dBm TX (101 mA) (7x7 封装)。CC2651P3 接收灵敏度为 -104 dBm (对于 125 kbps 的低功耗 [Bluetooth®](#) 编码 PHY)。

在采用 RTC 并保持 32KB RAM 时，CC2651P3 具有 0.8 μ A 的低待机电流。

许多客户对产品生命周期的要求为 10 至 15 年或者更久，为了达到这一目标，TI 制定了 [产品生命周期政策](#)，对产品的寿命和供货连续性作出承诺。

CC2651P3 器件是 SimpleLink™ MCU 平台的一部分，包括 [Wi-Fi®](#)、低功耗 [Bluetooth®](#)、[Thread](#)、[Zigbee](#)、[Wi-SUN®](#)、[Amazon Sidewalk](#)、[mioty](#)、Sub-1 GHz MCU 和主机 MCU。CC2651P3 是可扩展产品系列 (闪存为 32KB 至 704KB) 的一部分，具有引脚对引脚兼容的封装选项。通用 [SimpleLink™ CC13xx](#) 和 [CC26xx](#) 软件开发套件 (SDK) 及 [SysConfig](#) 系统配置工具支持产品系列中各器件之间的迁移。SDK 随附了丰富的软件栈、应用示例和 SimpleLink™ Academy 培训课程。如需了解更多相关信息，请访问 [无线连接](#)。

器件信息

| 器件型号 ⁽¹⁾ | 封装 | 封装尺寸 (标称值) |
|---------------------|-----------|-----------------|
| CC2651P31T0RGZR | VQFN (48) | 7.00mm × 7.00mm |
| CC2651P31T0RKPR | VQFN (40) | 5.00mm × 5.00mm |

(1) 如需所有可用器件的最新器件、封装和订购信息，请参阅 [节 12](#) 中的“封装选项附录”或访问 [TI 网站](#)。

¹ 请参阅 [射频内核](#)，了解有关支持的协议标准、模块格式和数据速率的更多详细信息。

4 功能方框图

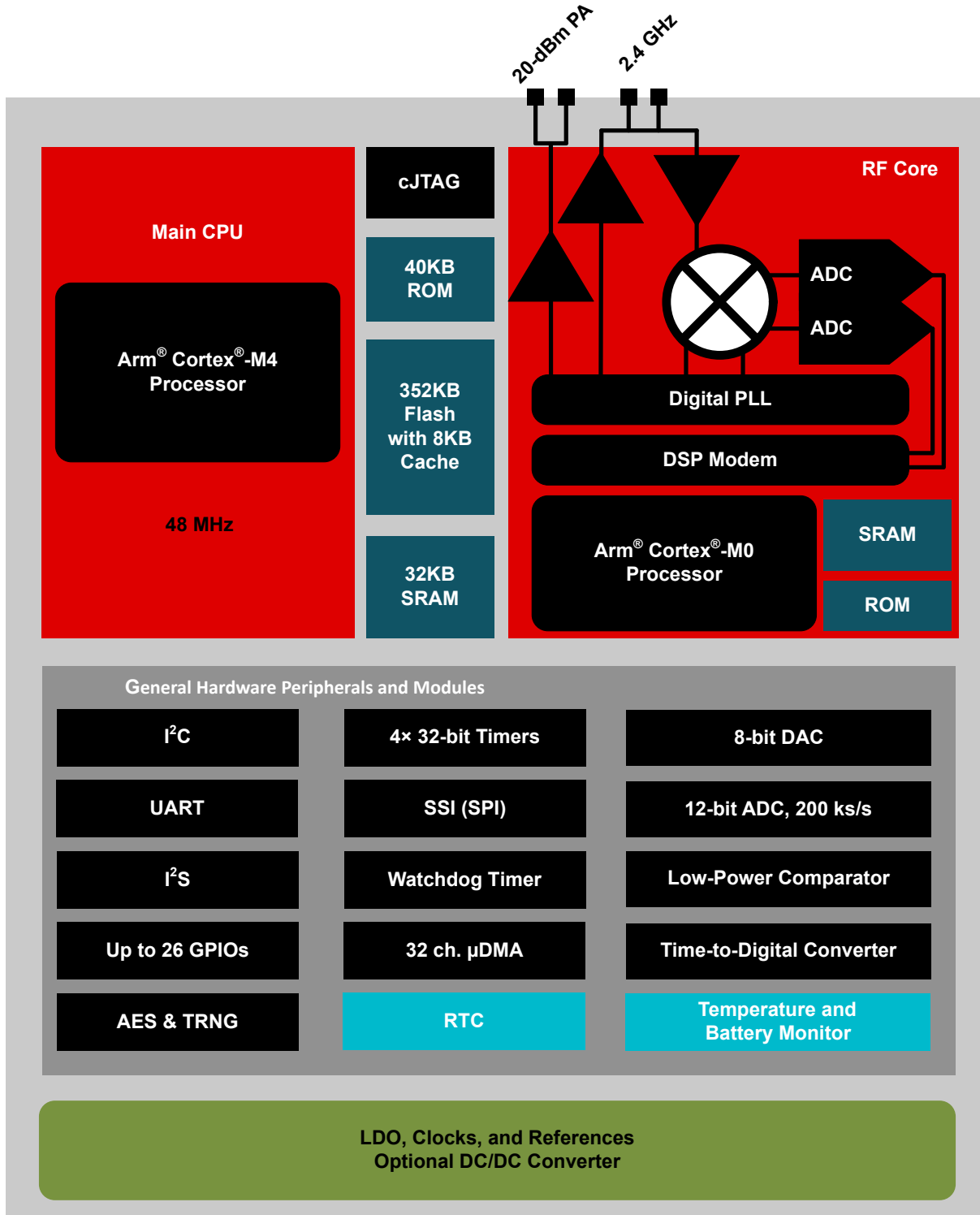


图 4-1. CC2651P3 功能方框图

Table of Contents

| | | | |
|---|-----------|--|-----------|
| 1 特性 | 1 | 8.15 Peripheral Characteristics..... | 25 |
| 2 应用 | 2 | 8.16 Typical Characteristics..... | 31 |
| 3 说明 | 2 | 9 Detailed Description | 39 |
| 4 功能方框图 | 3 | 9.1 Overview..... | 39 |
| 5 Revision History | 4 | 9.2 System CPU..... | 39 |
| 6 Device Comparison | 5 | 9.3 Radio (RF Core)..... | 40 |
| 7 Pin Configuration and Functions | 6 | 9.4 Memory..... | 41 |
| 7.1 Pin Diagram – RGZ Package (Top View)..... | 6 | 9.5 Cryptography..... | 42 |
| 7.2 Signal Descriptions – RGZ Package..... | 7 | 9.6 Timers..... | 43 |
| 7.3 Pin Diagram – RKP Package (Top View)..... | 9 | 9.7 Serial Peripherals and I/O..... | 44 |
| 7.4 Signal Descriptions – RKP Package..... | 9 | 9.8 Battery and Temperature Monitor..... | 44 |
| 7.5 Connections for Unused Pins and Modules..... | 11 | 9.9 μ DMA..... | 44 |
| 8 Specifications | 12 | 9.10 Debug..... | 44 |
| 8.1 Absolute Maximum Ratings..... | 12 | 9.11 Power Management..... | 45 |
| 8.2 ESD Ratings..... | 12 | 9.12 Clock Systems..... | 46 |
| 8.3 Recommended Operating Conditions..... | 12 | 9.13 Network Processor..... | 46 |
| 8.4 Power Supply and Modules..... | 12 | 10 Application, Implementation, and Layout | 47 |
| 8.5 Power Consumption - Power Modes..... | 13 | 10.1 Reference Designs..... | 47 |
| 8.6 Power Consumption - Radio Modes..... | 14 | 11 Device and Documentation Support | 48 |
| 8.7 Nonvolatile (Flash) Memory Characteristics..... | 14 | 11.1 Device Nomenclature..... | 48 |
| 8.8 Thermal Resistance Characteristics..... | 14 | 11.2 Tools and Software..... | 49 |
| 8.9 RF Frequency Bands..... | 15 | 11.3 Documentation Support..... | 51 |
| 8.10 Bluetooth Low Energy - Receive (RX)..... | 16 | 11.4 支持资源..... | 51 |
| 8.11 Bluetooth Low Energy - Transmit (TX)..... | 19 | 11.5 Trademarks..... | 51 |
| 8.12 Zigbee - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - RX..... | 20 | 11.6 Electrostatic Discharge Caution..... | 52 |
| 8.13 Zigbee - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - TX..... | 21 | 11.7 术语表..... | 52 |
| 8.14 Timing and Switching Characteristics..... | 22 | 12 Mechanical, Packaging, and Orderable Information | 53 |

5 Revision History

注：以前版本的页码可能与当前版本的页码不同

| DATE | REVISION | NOTES |
|------------|----------|-----------------|
| March 2022 | * | Initial Release |

6 Device Comparison

| Device | RADIO SUPPORT | | | | | | | | | | | FLASH (KB) | RAM + Cache (KB) | GPIO | PACKAGE SIZE | | | |
|------------|-----------------|--------------|----------------|-------|---------|----------|-------------------|--------|--------|---------------|------------|------------|------------------|-------|--------------------|--------------------|--------------------|--------------------|
| | Sub-1 GHz Prop. | 2.4GHz Prop. | Wireless M-Bus | mioty | WI-SUN® | Sidewalk | Bluetooth® 5.2 LE | ZigBee | Thread | Multiprotocol | +20 dBm PA | | | | 4 X 4 mm VQFN (32) | 5 X 5 mm VQFN (32) | 5 X 5 mm VQFN (40) | 7 X 7 mm VQFN (48) |
| CC1310 | X | | X | X | | | | | | | | 32-128 | 16-20 + 8 | 10-30 | X | X | | X |
| CC1311R3 | X | | X | X | | | | | | | | 352 | 32 + 8 | 22-30 | | | X | X |
| CC1311P3 | X | | X | X | | | | | | | X | 352 | 32 + 8 | 26 | | | | X |
| CC1312R | X | | X | X | X | | | | | | | 352 | 80 + 8 | 30 | | | | X |
| CC1312R7 | X | | X | X | X | X | | | | X | | 704 | 144 + 8 | 30 | | | | X |
| CC1352R | X | X | X | X | X | | X | X | X | X | | 352 | 80 + 8 | 28 | | | | X |
| CC1352P | X | X | X | X | X | | X | X | X | X | X | 352 | 80 + 8 | 26 | | | | X |
| CC1352P7 | X | X | X | X | X | X | X | X | X | X | X | 704 | 144 + 8 | 26 | | | | X |
| CC2640R2F | | | | | | | X | | | | | 128 | 20 + 8 | 10-31 | X | X | | X |
| CC2642R | | | | | | | X | | | | | 352 | 80 + 8 | 31 | | | | X |
| CC2642R-Q1 | | | | | | | X | | | | | 352 | 80 + 8 | 31 | | | | X |
| CC2651R3 | | X | | | | | X | X | | | | 352 | 32 + 8 | 23-31 | | | X | X |
| CC2651P3 | | X | | | | | X | X | | | X | 352 | 32 + 8 | 22-26 | | | X | X |
| CC2652R | | X | | | | | X | X | X | X | | 352 | 80 + 8 | 31 | | | | X |
| CC2652RB | | X | | | | | X | X | X | X | | 352 | 80 + 8 | 31 | | | | X |
| CC2652R7 | | X | | | | | X | X | X | X | | 704 | 144 + 8 | 31 | | | | X |
| CC2652P | | X | | | | | X | X | X | X | X | 352 | 80 + 8 | 26 | | | | X |
| CC2652P7 | | X | | | | | X | X | X | X | X | 704 | 144 + 8 | 26 | | | | X |

7 Pin Configuration and Functions

7.1 Pin Diagram - RGZ Package (Top View)

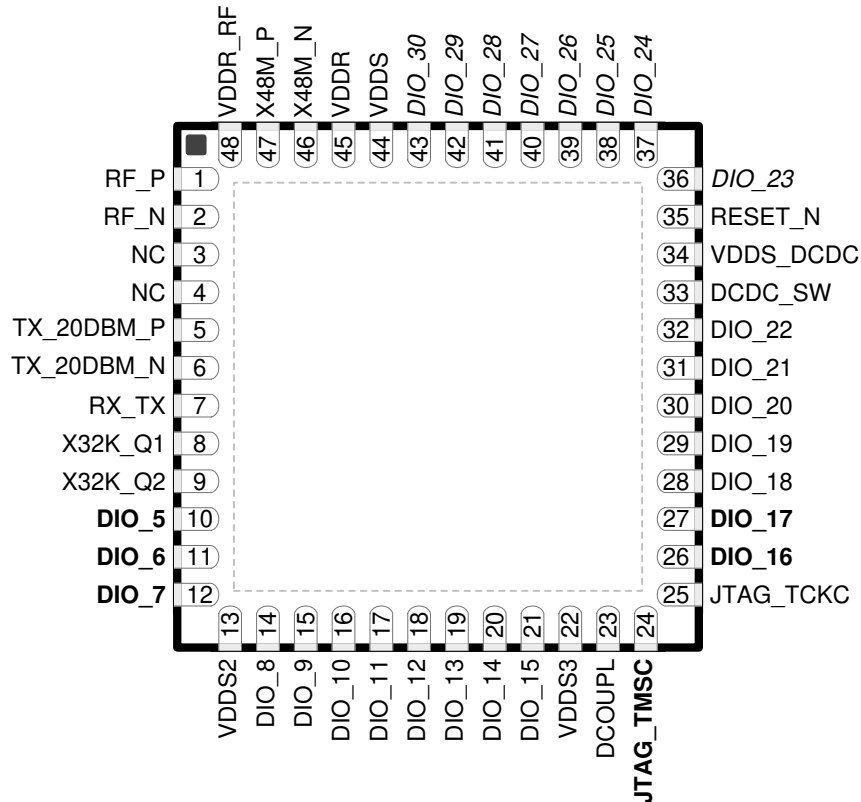


图 7-1. RGZ (7-mm × 7-mm) Pinout, 0.5-mm Pitch (Top View)

The following I/O pins marked in 图 7-1 in **bold** have high-drive capabilities:

- Pin 10, DIO_5
- Pin 11, DIO_6
- Pin 12, DIO_7
- Pin 24, JTAG_TMISC
- Pin 26, DIO_16
- Pin 27, DIO_17

The following I/O pins marked in 图 7-1 in *italics* have analog capabilities:

- Pin 36, DIO_23
- Pin 37, DIO_24
- Pin 38, DIO_25
- Pin 39, DIO_26
- Pin 40, DIO_27
- Pin 41, DIO_28
- Pin 42, DIO_29
- Pin 43, DIO_30

7.2 Signal Descriptions - RGZ Package

表 7-1. Signal Descriptions - RGZ Package

| PIN | | I/O | TYPE | DESCRIPTION |
|-------------|-----|-----|-------------------|---|
| NAME | NO. | | | |
| DCDC_SW | 33 | — | Power | Output from internal DC/DC converter ⁽¹⁾ |
| DCOUP_L | 23 | — | Power | For decoupling of internal 1.27 V regulated digital-supply ⁽²⁾ |
| DIO_5 | 10 | I/O | Digital | GPIO, high-drive capability |
| DIO_6 | 11 | I/O | Digital | GPIO, high-drive capability |
| DIO_7 | 12 | I/O | Digital | GPIO, high-drive capability |
| DIO_8 | 14 | I/O | Digital | GPIO |
| DIO_9 | 15 | I/O | Digital | GPIO |
| DIO_10 | 16 | I/O | Digital | GPIO |
| DIO_11 | 17 | I/O | Digital | GPIO |
| DIO_12 | 18 | I/O | Digital | GPIO |
| DIO_13 | 19 | I/O | Digital | GPIO |
| DIO_14 | 20 | I/O | Digital | GPIO |
| DIO_15 | 21 | I/O | Digital | GPIO |
| DIO_16 | 26 | I/O | Digital | GPIO, JTAG_TDO, high-drive capability |
| DIO_17 | 27 | I/O | Digital | GPIO, JTAG_TDI, high-drive capability |
| DIO_18 | 28 | I/O | Digital | GPIO |
| DIO_19 | 29 | I/O | Digital | GPIO |
| DIO_20 | 30 | I/O | Digital | GPIO |
| DIO_21 | 31 | I/O | Digital | GPIO |
| DIO_22 | 32 | I/O | Digital | GPIO |
| DIO_23 | 36 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_24 | 37 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_25 | 38 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_26 | 39 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_27 | 40 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_28 | 41 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_29 | 42 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_30 | 43 | I/O | Digital or Analog | GPIO, analog capability |
| EGP | — | — | GND | Ground - exposed ground pad ⁽³⁾ |
| JTAG_TM_S_C | 24 | I/O | Digital | JTAG TM_S_C, high-drive capability |
| JTAG_TCK_C | 25 | I | Digital | JTAG TCK_C |
| RESET_N | 35 | I | Digital | Reset, active low. No internal pullup resistor |
| RF_P | 1 | — | RF | Positive RF input signal to LNA during RX Positive RF output signal from PA during TX |
| RF_N | 2 | — | RF | Negative RF input signal to LNA during RX Negative RF output signal from PA during TX |
| RX_TX | 7 | — | RF | Optional bias pin for the RF LNA |
| TX_20DBM_P | 5 | — | RF | Positive high-power TX signal |
| TX_20DBM_N | 6 | — | RF | Negative high-power TX signal |
| VDDR | 45 | — | Power | Internal supply, must be powered from the internal DC/DC converter or the internal LDO ^{(2) (4) (6)} |
| VDDR_RF | 48 | — | Power | Internal supply, must be powered from the internal DC/DC converter or the internal LDO ^{(2) (5) (6)} |
| VDDS | 44 | — | Power | 1.8-V to 3.8-V main chip supply ⁽¹⁾ |

表 7-1. Signal Descriptions - RGZ Package (continued)

| PIN | | I/O | TYPE | DESCRIPTION |
|-----------|-----|-----|--------|--|
| NAME | NO. | | | |
| VDDS2 | 13 | — | Power | 1.8-V to 3.8-V DIO supply ⁽¹⁾ |
| VDDS3 | 22 | — | Power | 1.8-V to 3.8-V DIO supply ⁽¹⁾ |
| VDDS_DCDC | 34 | — | Power | 1.8-V to 3.8-V DC/DC converter supply |
| X48M_N | 46 | — | Analog | 48-MHz crystal oscillator pin 1 |
| X48M_P | 47 | — | Analog | 48-MHz crystal oscillator pin 2 |
| X32K_Q1 | 8 | — | Analog | 32-kHz crystal oscillator pin 1 |
| X32K_Q2 | 9 | — | Analog | 32-kHz crystal oscillator pin 2 |

- (1) For more details, see the device technical reference manual listed in 节 11.3.
- (2) Do not supply external circuitry from this pin.
- (3) EGP is the only ground connection for the device. Good electrical connection to device ground on printed circuit board (PCB) is imperative for proper device operation.
- (4) If internal DC/DC converter is not used, this pin is supplied internally from the main LDO.
- (5) If internal DC/DC converter is not used, this pin must be connected to VDDR for supply from the main LDO.
- (6) Output from internal DC/DC and LDO is trimmed to 1.68 V.

7.3 Pin Diagram - RKP Package (Top View)

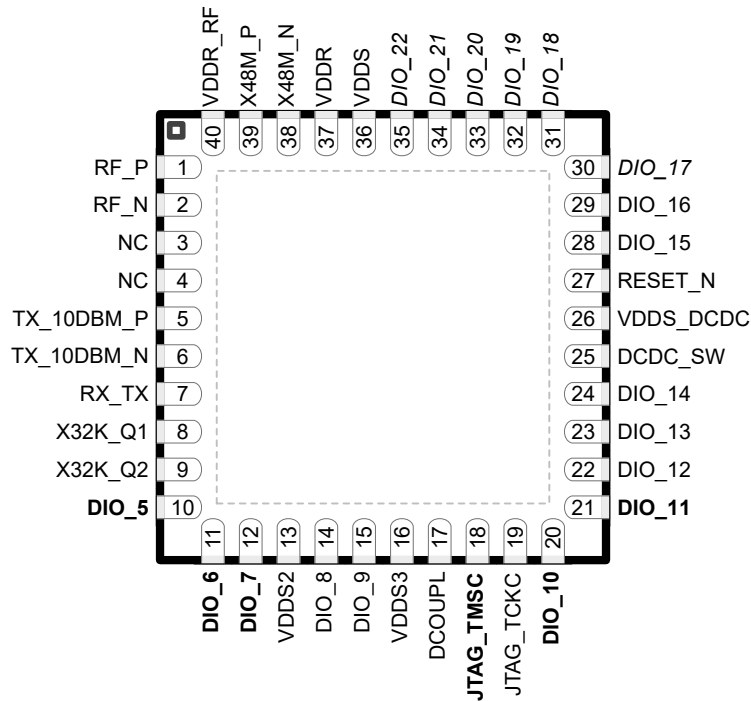


图 7-2. RKP (5-mm × 5-mm) Pinout, 0.4-mm Pitch (Top View)

The following I/O pins marked in 图 7-2 in **bold** have high-drive capabilities:

- Pin 10, DIO_5
- Pin 11, DIO_6
- Pin 12, DIO_7
- Pin 18, JTAG_TMSC
- Pin 20, DIO_10
- Pin 21, DIO_11

The following I/O pins marked in 图 7-2 in *italics* have analog capabilities:

- Pin 28, DIO_15
- Pin 29, DIO_16
- Pin 30, DIO_17
- Pin 31, DIO_18
- Pin 32, DIO_19
- Pin 33, DIO_20
- Pin 34, DIO_21
- Pin 35, DIO_22

7.4 Signal Descriptions - RKP Package

表 7-2. Signal Descriptions - RKP Package

| PIN | | I/O | TYPE | DESCRIPTION |
|---------|-----|-----|---------|---|
| NAME | NO. | | | |
| DCDC_SW | 25 | — | Power | Output from internal DC/DC converter ⁽¹⁾ |
| DCOUPPL | 17 | — | Power | For decoupling of internal 1.27 V regulated digital-supply ⁽²⁾ |
| DIO_5 | 10 | I/O | Digital | GPIO, high-drive capability |
| DIO_6 | 11 | I/O | Digital | GPIO, high-drive capability |

表 7-2. Signal Descriptions - RKP Package (continued)

| PIN | | I/O | TYPE | DESCRIPTION |
|------------|-----|-----|---------|---|
| NAME | NO. | | | |
| DIO_7 | 12 | I/O | Digital | GPIO, high-drive capability |
| DIO_8 | 14 | I/O | Digital | GPIO |
| DIO_9 | 15 | I/O | Digital | GPIO |
| DIO_10 | 20 | I/O | Digital | GPIO, JTAG_TDO, high-drive capability |
| DIO_11 | 21 | I/O | Digital | GPIO, JTAG_TDI, high-drive capability |
| DIO_12 | 22 | I/O | Digital | GPIO |
| DIO_13 | 23 | I/O | Digital | GPIO |
| DIO_14 | 24 | I/O | Digital | GPIO |
| DIO_15 | 28 | I/O | Digital | GPIO, analog capability |
| DIO_16 | 29 | I/O | Digital | GPIO, analog capability |
| DIO_17 | 30 | I/O | Digital | GPIO, analog capability |
| DIO_18 | 31 | I/O | Digital | GPIO, analog capability |
| DIO_19 | 32 | I/O | Digital | GPIO, analog capability |
| DIO_20 | 33 | I/O | Digital | GPIO, analog capability |
| DIO_21 | 34 | I/O | Digital | GPIO, analog capability |
| DIO_22 | 35 | I/O | Digital | GPIO, analog capability |
| EGP | — | — | GND | Ground - exposed ground pad ⁽³⁾ |
| JTAG_TSMC | 18 | I/O | Digital | JTAG TSMC, high-drive capability |
| JTAG_TCKC | 19 | I | Digital | JTAG TCKC |
| RESET_N | 27 | I | Digital | Reset, active low. No internal pullup resistor |
| RF_P | 1 | — | RF | Positive RF input signal to LNA during RX Positive RF output signal from PA during TX |
| RF_N | 2 | — | RF | Negative RF input signal to LNA during RX Negative RF output signal from PA during TX |
| RX_TX | 7 | — | RF | Optional bias pin for the RF LNA |
| TX_20DBM_P | 5 | — | RF | Positive high-power TX signal |
| TX_20DBM_N | 6 | — | RF | Negative high-power TX signal |
| VDDR | 37 | — | Power | Internal supply, must be powered from the internal DC/DC converter or the internal LDO ^{(2) (4) (6)} |
| VDDR_RF | 40 | — | Power | Internal supply, must be powered from the internal DC/DC converter or the internal LDO ^{(2) (5) (6)} |
| VDDS | 36 | — | Power | 1.8-V to 3.8-V main chip supply ⁽¹⁾ |
| VDDS2 | 13 | — | Power | 1.8-V to 3.8-V DIO supply ⁽¹⁾ |
| VDDS3 | 16 | — | Power | 1.8-V to 3.8-V DIO supply ⁽¹⁾ |
| VDDS_DCDC | 26 | — | Power | 1.8-V to 3.8-V DC/DC converter supply |
| X48M_N | 38 | — | Analog | 48-MHz crystal oscillator pin 1 |
| X48M_P | 39 | — | Analog | 48-MHz crystal oscillator pin 2 |
| X32K_Q1 | 8 | — | Analog | 32-kHz crystal oscillator pin 1 |
| X32K_Q2 | 9 | — | Analog | 32-kHz crystal oscillator pin 2 |

(1) For more details, see the device technical reference manual listed in 节 11.3.

(2) Do not supply external circuitry from this pin.

(3) EGP is the only ground connection for the device. Good electrical connection to device ground on printed circuit board (PCB) is imperative for proper device operation.

(4) If internal DC/DC converter is not used, this pin is supplied internally from the main LDO.

(5) If internal DC/DC converter is not used, this pin must be connected to VDDR for supply from the main LDO.

(6) Output from internal DC/DC and LDO is trimmed to 1.68 V.

7.5 Connections for Unused Pins and Modules

表 7-3. Connections for Unused Pins - RGZ Package

| FUNCTION | SIGNAL NAME | PIN NUMBER | ACCEPTABLE PRACTICE ⁽¹⁾ | PREFERRED PRACTICE ⁽¹⁾ |
|--------------------------------|-------------|------------|------------------------------------|-----------------------------------|
| GPIO | DIO_n | 10 - 12 | NC or GND | NC |
| | | 14 - 21 | | |
| | | 26 - 32 | | |
| | | 36 - 43 | | |
| 32.768-kHz crystal | X32K_Q1 | 8 | NC or GND | NC |
| | X32K_Q2 | 9 | | |
| No Connects | NC | 3 - 4 | NC | NC |
| DC/DC converter ⁽²⁾ | DCDC_SW | 33 | NC | NC |
| | VDDS_DCDC | 34 | VDDS | VDDS |

(1) NC = No connect

(2) When the DC/DC converter is not used, the inductor between DCDC_SW and VDDR can be removed. VDDR and VDDR_RF must still be connected and the 22 uF DCDC capacitor must be kept on the VDDR net.

表 7-4. Connection for Unused Pins and Modules - RKP Package

| FUNCTION | SIGNAL NAME | PIN NUMBER | ACCEPTABLE PRACTICE | PREFERRED PRACTICE |
|--------------------|-------------|------------|---------------------|--------------------|
| GPIO | DIO_n | 10-12 | NC or GND | NC |
| | | 14-15 | | |
| | | 20-24 | | |
| | | 28-35 | | |
| 32.768-kHz crystal | X32K_Q1 | 3 | NC or GND | NC |
| | X32K_Q2 | 4 | | |
| No Connects | NC | 3 - 4 | NC | NC |
| DC/DC converter | DCDC_SW | 25 | NC | NC |
| | VDDS_DCDC | 26 | VDDS | VDDS |

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

| | | MIN | MAX | UNIT |
|-------------------------------------|---|---|----------------------------------|------------------------|
| V _{DDS} ^{(3) (6)} | Supply voltage | - 0.3 | 4.1 | V |
| | Voltage on any digital pin ^{(4) (5)} | - 0.3 | V _{DDS} + 0.3, max 4.1 | V |
| | Voltage on crystal oscillator pins, X32K_Q1, X32K_Q2, X48M_N and X48M_P | - 0.3 | V _{DDR} + 0.3, max 2.25 | V |
| V _{in} | Voltage on ADC input | Voltage scaling enabled | - 0.3 | V _{DDS} |
| | | Voltage scaling disabled, internal reference | - 0.3 | 1.49 |
| | | Voltage scaling disabled, V _{DDS} as reference | - 0.3 | V _{DDS} / 2.9 |
| | Input level, RF pins (RF_P and RF_N) | | 5 | dBm |
| T _{stg} | Storage temperature | - 40 | 150 | °C |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
- (2) All voltage values are with respect to ground, unless otherwise noted.
- (3) V_{DDS_DCDC}, V_{DDS2} and V_{DDS3} must be at the same potential as V_{DDS}.
- (4) Including analog capable DIOs.
- (5) Injection current is not supported on any GPIO pin
- (6) Connect V_{DDR} to the external PA bias voltage for +10dBm and V_{DDS} to the external PA bias voltage for +14dBm to +20dBm

8.2 ESD Ratings

| | | | VALUE | UNIT | |
|------------------|-------------------------|--|----------|-------|---|
| V _{ESD} | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS001 ⁽¹⁾ | All pins | ±2000 | V |
| | | Charged device model (CDM), per JESD22-C101 ⁽²⁾ | All pins | ±500 | V |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|------|-----|-------|
| Operating ambient temperature ^{(1) (2)} | - 40 | 105 | °C |
| Operating junction temperature ^{(1) (2)} | - 40 | 115 | °C |
| Operating supply voltage (V _{DDS}) | 1.8 | 3.8 | V |
| Rising supply voltage slew rate | 0 | 100 | mV/μs |
| Falling supply voltage slew rate ⁽³⁾ | 0 | 20 | mV/μs |

- (1) Operation at or near maximum operating temperature for extended durations will result in lifetime reduction.
- (2) For thermal resistance characteristics refer to [§ 8.8](#).
- (3) For small coin-cell batteries, with high worst-case end-of-life equivalent source resistance, a 22-μF V_{DDS} input capacitor must be used to ensure compliance with this slew rate.

8.4 Power Supply and Modules

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|-------------------|------------|------|-----|------|
| V _{DDS} Power-on-Reset (POR) threshold | | 1.1 - 1.55 | | | V |
| V _{DDS} Brown-out Detector (BOD) | Rising threshold | | 1.77 | | V |
| V _{DDS} Brown-out Detector (BOD), before initial boot ⁽¹⁾ | Rising threshold | | 1.70 | | V |
| V _{DDS} Brown-out Detector (BOD) | Falling threshold | | 1.75 | | V |

- (1) Brown-out Detector is trimmed at initial boot, value is kept until device is reset by a POR reset or the RESET_N pin

8.5 Power Consumption - Power Modes

When measured on the CC26x1-P3EM-XD24-PA24 reference design with $T_c = 25\text{ }^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$ with DC/DC enabled unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------|--|---|------|------|-----|---------------|
| Core Current Consumption | | | | | | |
| I_{core} | Reset and Shutdown | Reset. RESET_N pin asserted or VDD5 below power-on-reset threshold | | 150 | | nA |
| | | Shutdown. No clocks running, no retention | | 100 | | |
| | Standby without cache retention | RTC running, CPU, 32KB RAM and (partial) register retention. RCOSC_LF | | 0.8 | | μA |
| | | RTC running, CPU, 32KB RAM and (partial) register retention. XOSC_LF | | 0.9 | | μA |
| | Standby with cache retention | RTC running, CPU, 32KB RAM and (partial) register retention. RCOSC_LF | | 2.4 | | μA |
| | | RTC running, CPU, 32KB RAM and (partial) register retention. XOSC_LF | | 2.6 | | μA |
| | Idle | Supply Systems and RAM powered. RCOSC_HF | | 650 | | μA |
| Active | MCU running CoreMark at 48 MHz. RCOSC_HF | | 2.91 | | mA | |
| Peripheral Current Consumption | | | | | | |
| I_{peri} | Peripheral power domain | Delta current with domain enabled | | 56.0 | | μA |
| | Serial power domain | Delta current with domain enabled | | 5.0 | | |
| | RF Core | Delta current with power domain enabled, clock enabled, RF core idle | | 144 | | |
| | μDMA | Delta current with clock enabled, module is idle | | 68.6 | | |
| | Timers | Delta current with clock enabled, module is idle ⁽¹⁾ | | 102 | | |
| | I2C | Delta current with clock enabled, module is idle | | 12.1 | | |
| | I2S | Delta current with clock enabled, module is idle | | 30.8 | | |
| | SSI | Delta current with clock enabled, module is idle | | 71.7 | | |
| | UART | Delta current with clock enabled, module is idle | | 147 | | |
| | CRYPTO (AES) | Delta current with clock enabled, module is idle | | 28.1 | | |
| | TRNG | Delta current with clock enabled, module is idle | | 27.1 | | |

(1) Only one GPTimer running

8.6 Power Consumption - Radio Modes

When measured on the CC26x1-P3EM-XD24-PA24 reference design with $T_c = 25\text{ }^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$ with DC/DC enabled unless otherwise noted.

High-power PA connected to V_{DDS} unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|-----|-----|-----|------|
| Radio receive current | 2440 MHz | | 6.4 | | mA |
| Radio transmit current 2.4 GHz PA (Bluetooth Low Energy) | 0 dBm output power setting 2440 MHz | | 7.1 | | mA |
| | +5 dBm output power setting 2440 MHz | | 9.5 | | mA |
| Radio transmit current High-power PA | +20 dBm output power setting ⁽¹⁾ 2440 MHz. $V_{\text{DDS}} = 3.3\text{ V}$ | | 101 | | mA |
| Radio transmit current High-power PA, 10 dBm configuration ⁽²⁾ | +10 dBm output power setting 2440 MHz $V_{\text{DDR}} = 1.67\text{ V}$ | | 22 | | mA |

(1) +20 dBm is only available on the RGZ (7x7) package

(2) Measured on evaluation board as described in <https://www.ti.com/lit/pdf/swra636>.

8.7 Nonvolatile (Flash) Memory Characteristics

Over operating free-air temperature range and $V_{\text{DDS}} = 3.0\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|------|------|------|------------------|
| Flash sector size | | | 8 | | KB |
| Supported flash erase cycles before failure, full bank ^{(1) (5)} | | 30 | | | k Cycles |
| Supported flash erase cycles before failure, single sector ⁽²⁾ | | 60 | | | k Cycles |
| Maximum number of write operations per row before sector erase ⁽³⁾ | | | | 83 | Write Operations |
| Flash retention | 105 °C | 11.4 | | | Years |
| Flash sector erase current | Average delta current | | 9.7 | | mA |
| Flash sector erase time ⁽⁴⁾ | Zero cycles | | 10 | | ms |
| | 30k cycles | | | 4000 | ms |
| Flash write current | Average delta current, 4 bytes at a time | | 5.3 | | mA |
| Flash write time ⁽⁴⁾ | 4 bytes at a time | | 21.6 | | µs |

(1) A full bank erase is counted as a single erase cycle on each sector.

(2) Up to 4 customer-designated sectors can be individually erased an additional 30k times beyond the baseline bank limitation of 30k cycles

(3) Each wordline is 2048 bits (or 256 bytes) wide. This limitation corresponds to sequential memory writes of 4 (3.1) bytes minimum per write over a whole wordline. If additional writes to the same wordline are required, a sector erase is required once the maximum number of write operations per row is reached.

(4) This number is dependent on Flash aging and increases over time and erase cycles

(5) Aborting flash during erase or program modes is not a safe operation.

8.8 Thermal Resistance Characteristics

| THERMAL METRIC ⁽¹⁾ | | PACKAGE | | UNIT |
|-------------------------------|--|---------------|---------------|---------------------|
| | | RGZ (VQFN) | RKP (VQFN) | |
| | | 48 PINS | 40 PINS | |
| $R_{\theta\text{JA}}$ | Junction-to-ambient thermal resistance | 25.0 | 30.9 | °C/W ⁽²⁾ |
| $R_{\theta\text{JC(top)}}$ | Junction-to-case (top) thermal resistance | 14.5 | 20.2 | °C/W ⁽²⁾ |
| $R_{\theta\text{JB}}$ | Junction-to-board thermal resistance | 8.7 | 10.3 | °C/W ⁽²⁾ |
| ψ_{JT} | Junction-to-top characterization parameter | 0.2 | 0.2 | °C/W ⁽²⁾ |
| ψ_{JB} | Junction-to-board characterization parameter | 8.6 | 10.3 | °C/W ⁽²⁾ |
| $R_{\theta\text{JC(bot)}}$ | Junction-to-case (bottom) thermal resistance | 2.1 | 2.1 | °C/W ⁽²⁾ |

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

(2) °C/W = degrees Celsius per watt.

8.9 RF Frequency Bands

Over operating free-air temperature range (unless otherwise noted).

| PARAMETER | MIN | TYP | MAX | UNIT |
|-----------------|------|-----|------|------|
| Frequency bands | 2360 | | 2500 | MHz |

8.10 Bluetooth Low Energy - Receive (RX)

Measured on the CC26x1-P3EM-7XD24-PA24 reference design with $T_c = 25\text{ }^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, $f_{RF} = 2440\text{ MHz}$ with DC/DC enabled and high power PA connected to V_{DD5} unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|-----|-------------------------|-----|------|
| 125 kbps (LE Coded) | | | | | |
| Receiver sensitivity | Differential mode. BER = 10^{-3} | | - 104 | | dBm |
| Receiver sensitivity | Single ended mode. Measured on CC26x1-P3EM-5XS24, at the SMA connector, BER = 10^{-3} | | - 104 | | dBm |
| Receiver saturation | Differential mode. BER = 10^{-3} | | >5 | | dBm |
| Frequency error tolerance | Difference between the incoming carrier frequency and the internally generated carrier frequency | | > (- 300 / 300) | | kHz |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate (37-byte packets) | | > (- 320 / 240) | | ppm |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate (255-byte packets) | | > (- 125 / 125) | | ppm |
| Co-channel rejection ⁽¹⁾ | Wanted signal at - 79 dBm, modulated interferer in channel, BER = 10^{-3} | | - 1.5 | | dB |
| Selectivity, $\pm 1\text{ MHz}$ ⁽¹⁾ | Wanted signal at - 79 dBm, modulated interferer at $\pm 1\text{ MHz}$, BER = 10^{-3} | | 8 / 4.5 ⁽²⁾ | | dB |
| Selectivity, $\pm 2\text{ MHz}$ ⁽¹⁾ | Wanted signal at - 79 dBm, modulated interferer at $\pm 2\text{ MHz}$, BER = 10^{-3} | | 44 / 39 ⁽²⁾ | | dB |
| Selectivity, $\pm 3\text{ MHz}$ ⁽¹⁾ | Wanted signal at - 79 dBm, modulated interferer at $\pm 3\text{ MHz}$, BER = 10^{-3} | | 46 / 44 ⁽²⁾ | | dB |
| Selectivity, $\pm 4\text{ MHz}$ ⁽¹⁾ | Wanted signal at - 79 dBm, modulated interferer at $\pm 4\text{ MHz}$, BER = 10^{-3} | | 44 / 46 ⁽²⁾ | | dB |
| Selectivity, $\pm 6\text{ MHz}$ ⁽¹⁾ | Wanted signal at - 79 dBm, modulated interferer at $\geq \pm 6\text{ MHz}$, BER = 10^{-3} | | 48 / 44 ⁽²⁾ | | dB |
| Selectivity, $\pm 7\text{ MHz}$ | Wanted signal at - 79 dBm, modulated interferer at $\geq \pm 7\text{ MHz}$, BER = 10^{-3} | | 51 / 45 ⁽²⁾ | | dB |
| Selectivity, Image frequency ⁽¹⁾ | Wanted signal at - 79 dBm, modulated interferer at image frequency, BER = 10^{-3} | | 39 | | dB |
| Selectivity, Image frequency $\pm 1\text{ MHz}$ ⁽¹⁾ | Note that Image frequency + 1 MHz is the Co- channel - 1 MHz. Wanted signal at - 79 dBm, modulated interferer at $\pm 1\text{ MHz}$ from image frequency, BER = 10^{-3} | | 4.5 / 44 ⁽²⁾ | | dB |
| 500 kbps (LE Coded) | | | | | |
| Receiver sensitivity | Differential mode. BER = 10^{-3} | | - 100 | | dBm |
| Receiver sensitivity | Single ended mode. Measured on CC26x1-P3EM-5XS24, at the SMA connector, BER = 10^{-3} | | - 100 | | dBm |
| Receiver saturation | Differential mode. BER = 10^{-3} | | > 5 | | dBm |
| Frequency error tolerance | Difference between the incoming carrier frequency and the internally generated carrier frequency | | > (- 300 / 300) | | kHz |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate (37-byte packets) | | > (- 450 / 450) | | ppm |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate (255-byte packets) | | > (- 175 / 175) | | ppm |
| Co-channel rejection ⁽¹⁾ | Wanted signal at - 72 dBm, modulated interferer in channel, BER = 10^{-3} | | - 3.5 | | dB |
| Selectivity, $\pm 1\text{ MHz}$ ⁽¹⁾ | Wanted signal at - 72 dBm, modulated interferer at $\pm 1\text{ MHz}$, BER = 10^{-3} | | 8 / 4 ⁽²⁾ | | dB |
| Selectivity, $\pm 2\text{ MHz}$ ⁽¹⁾ | Wanted signal at - 72 dBm, modulated interferer at $\pm 2\text{ MHz}$, BER = 10^{-3} | | 44 / 37 ⁽²⁾ | | dB |
| Selectivity, $\pm 3\text{ MHz}$ ⁽¹⁾ | Wanted signal at - 72 dBm, modulated interferer at $\pm 3\text{ MHz}$, BER = 10^{-3} | | 46 / 46 ⁽²⁾ | | dB |
| Selectivity, $\pm 4\text{ MHz}$ ⁽¹⁾ | Wanted signal at - 72 dBm, modulated interferer at $\pm 4\text{ MHz}$, BER = 10^{-3} | | 45 / 47 ⁽²⁾ | | dB |
| Selectivity, $\pm 6\text{ MHz}$ ⁽¹⁾ | Wanted signal at - 72 dBm, modulated interferer at $\geq \pm 6\text{ MHz}$, BER = 10^{-3} | | 46 / 45 ⁽²⁾ | | dB |

8.10 Bluetooth Low Energy - Receive (RX) (continued)

Measured on the CC26x1-P3EM-7XD24-PA24 reference design with $T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, $f_{RF} = 2440\text{ MHz}$ with DC/DC enabled and high power PA connected to V_{DD5} unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----|------------------------|-----|------|
| Selectivity, $\pm 7\text{ MHz}$ | Wanted signal at -72 dBm , modulated interferer at $\geq \pm 7\text{ MHz}$, BER = 10^{-3} | | 49 / 45 ⁽²⁾ | | dB |
| Selectivity, Image frequency ⁽¹⁾ | Wanted signal at -72 dBm , modulated interferer at image frequency, BER = 10^{-3} | | 37 | | dB |
| Selectivity, Image frequency $\pm 1\text{ MHz}$ ⁽¹⁾ | Note that Image frequency + 1 MHz is the Co- channel - 1 MHz. Wanted signal at -72 dBm , modulated interferer at $\pm 1\text{ MHz}$ from image frequency, BER = 10^{-3} | | 4 / 46 ⁽²⁾ | | dB |
| 1 Mbps (LE 1M) | | | | | |
| Receiver sensitivity | Differential mode. BER = 10^{-3} | | - 97 | | dBm |
| Receiver sensitivity | Single ended mode. Measured on CC26x1-P3EM-5XS24, at the SMA connector, BER = 10^{-3} | | - 97 | | dBm |
| Receiver saturation | Differential mode. BER = 10^{-3} | | > 5 | | dBm |
| Frequency error tolerance | Difference between the incoming carrier frequency and the internally generated carrier frequency | | > (- 350 / 350) | | kHz |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate (37-byte packets) | | > (- 750 / 750) | | ppm |
| Co-channel rejection ⁽¹⁾ | Wanted signal at -67 dBm , modulated interferer in channel, BER = 10^{-3} | | - 6 | | dB |
| Selectivity, $\pm 1\text{ MHz}$ ⁽¹⁾ | Wanted signal at -67 dBm , modulated interferer at $\pm 1\text{ MHz}$, BER = 10^{-3} | | 7 / 4 ⁽²⁾ | | dB |
| Selectivity, $\pm 2\text{ MHz}$ ⁽¹⁾ | Wanted signal at -67 dBm , modulated interferer at $\pm 2\text{ MHz}$, BER = 10^{-3} | | 40 / 33 ⁽²⁾ | | dB |
| Selectivity, $\pm 3\text{ MHz}$ ⁽¹⁾ | Wanted signal at -67 dBm , modulated interferer at $\pm 3\text{ MHz}$, BER = 10^{-3} | | 36 / 41 ⁽²⁾ | | dB |
| Selectivity, $\pm 4\text{ MHz}$ ⁽¹⁾ | Wanted signal at -67 dBm , modulated interferer at $\pm 4\text{ MHz}$, BER = 10^{-3} | | 37 / 45 ⁽²⁾ | | dB |
| Selectivity, $\pm 5\text{ MHz}$ or more ⁽¹⁾ | Wanted signal at -67 dBm , modulated interferer at $\geq \pm 5\text{ MHz}$, BER = 10^{-3} | | 40 | | dB |
| Selectivity, image frequency ⁽¹⁾ | Wanted signal at -67 dBm , modulated interferer at image frequency, BER = 10^{-3} | | 33 | | dB |
| Selectivity, image frequency $\pm 1\text{ MHz}$ ⁽¹⁾ | Note that Image frequency + 1 MHz is the Co- channel - 1 MHz. Wanted signal at -67 dBm , modulated interferer at $\pm 1\text{ MHz}$ from image frequency, BER = 10^{-3} | | 4 / 41 ⁽²⁾ | | dB |
| Out-of-band blocking ⁽³⁾ | 30 MHz to 2000 MHz | | - 10 | | dBm |
| Out-of-band blocking | 2003 MHz to 2399 MHz | | - 18 | | dBm |
| Out-of-band blocking | 2484 MHz to 2997 MHz | | - 12 | | dBm |
| Out-of-band blocking | 3000 MHz to 12.75 GHz | | - 2 | | dBm |
| Intermodulation | Wanted signal at 2402 MHz, -64 dBm . Two interferers at 2405 and 2408 MHz respectively, at the given power level | | - 42 | | dBm |
| Spurious emissions, 30 to 1000 MHz | Measurement in a $50\text{-}\Omega$ single-ended load. | | < - 59 | | dBm |
| Spurious emissions, 1 to 12.75 GHz | Measurement in a $50\text{-}\Omega$ single-ended load. | | < - 47 | | dBm |
| RSSI dynamic range | | | 70 | | dB |
| RSSI accuracy | | | ± 4 | | dB |
| 2 Mbps (LE 2M) | | | | | |
| Receiver sensitivity | Differential mode. Measured at SMA connector, BER = 10^{-3} | | - 92 | | dBm |
| Receiver sensitivity | Single ended mode. Measured on CC26x1-P3EM-5XS24, at the SMA connector, BER = 10^{-3} | | - 92 | | dBm |
| Receiver saturation | Differential mode. Measured at SMA connector, BER = 10^{-3} | | > 5 | | dBm |

8.10 Bluetooth Low Energy - Receive (RX) (continued)

Measured on the CC26x1-P3EM-7XD24-PA24 reference design with $T_c = 25\text{ }^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, $f_{RF} = 2440\text{ MHz}$ with DC/DC enabled and high power PA connected to V_{DD5} unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----|-------------------------|-----|------|
| Frequency error tolerance | Difference between the incoming carrier frequency and the internally generated carrier frequency | | > (- 500 / 500) | | kHz |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate (37-byte packets) | | > (- 700 / 750) | | ppm |
| Co-channel rejection ⁽¹⁾ | Wanted signal at - 67 dBm, modulated interferer in channel, BER = 10^{-3} | | - 7 | | dB |
| Selectivity, $\pm 2\text{ MHz}$ ⁽¹⁾ | Wanted signal at - 67 dBm, modulated interferer at $\pm 2\text{ MHz}$, Image frequency is at - 2 MHz, BER = 10^{-3} | | 8 / 4 ⁽²⁾ | | dB |
| Selectivity, $\pm 4\text{ MHz}$ ⁽¹⁾ | Wanted signal at - 67 dBm, modulated interferer at $\pm 4\text{ MHz}$, BER = 10^{-3} | | 36 / 31 ⁽²⁾ | | dB |
| Selectivity, $\pm 6\text{ MHz}$ ⁽¹⁾ | Wanted signal at - 67 dBm, modulated interferer at $\pm 6\text{ MHz}$, BER = 10^{-3} | | 37 / 36 ⁽²⁾ | | dB |
| Selectivity, image frequency ⁽¹⁾ | Wanted signal at - 67 dBm, modulated interferer at image frequency, BER = 10^{-3} | | 4 | | dB |
| Selectivity, image frequency $\pm 2\text{ MHz}$ ⁽¹⁾ | Note that Image frequency + 2 MHz is the Co-channel. Wanted signal at - 67 dBm, modulated interferer at $\pm 2\text{ MHz}$ from image frequency, BER = 10^{-3} | | - 7 / 36 ⁽²⁾ | | dB |
| Out-of-band blocking ⁽³⁾ | 30 MHz to 2000 MHz | | - 16 | | dBm |
| Out-of-band blocking | 2003 MHz to 2399 MHz | | - 21 | | dBm |
| Out-of-band blocking | 2484 MHz to 2997 MHz | | - 15 | | dBm |
| Out-of-band blocking | 3000 MHz to 12.75 GHz | | - 12 | | dBm |
| Intermodulation | Wanted signal at 2402 MHz, - 64 dBm. Two interferers at 2408 and 2414 MHz respectively, at the given power level | | - 38 | | dBm |

(1) Numbers given as I/C dB

(2) X / Y, where X is +N MHz and Y is - N MHz

(3) Excluding one exception at $F_{\text{wanted}} / 2$, per Bluetooth Specification

8.11 Bluetooth Low Energy - Transmit (TX)

Measured on the CC26x1-P3EM-7XD24-PA24 reference design with $T_c = 25\text{ }^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, $f_{RF} = 2440\text{ MHz}$ with DC/DC enabled and high power PA connected to V_{DD5} unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|--------------------------------|-------|-----|------|
| General Parameters | | | | | |
| Max output power, high power PA | Differential mode, delivered to a single-ended $50\ \Omega$ load through a balun | | 20 | | dBm |
| Output power programmable range high power PA | Differential mode, delivered to a single-ended $50\ \Omega$ load through a balun | | 6 | | dB |
| Max output power, high power PA, 10 dBm configuration ⁽³⁾ | Differential mode, delivered to a single-ended $50\ \Omega$ load through a balun | | 10.5 | | dBm |
| Max output power, high power PA, 10 dBm configuration ⁽³⁾ | Single-ended mode. Measured on CC26x1-P3EM-5XS24, delivered to a single-ended $50\ \Omega$ load through a balun | | 9 | | dBm |
| Output power programmable range high power PA, 10 dBm configuration ⁽³⁾ | Differential mode, delivered to a single-ended $50\ \Omega$ load through a balun | | 5 | | dB |
| Max output power, regular PA | Differential mode, delivered to a single-ended $50\ \Omega$ load through a balun | | 5 | | dBm |
| Max output power, regular PA | Single-ended mode. Measured on CC26x1-P3EM-5XS24, delivered to a single-ended $50\ \Omega$ load through a balun | | 3 | | dBm |
| Output power programmable range, regular PA | Differential mode, delivered to a single-ended $50\ \Omega$ load through a balun | | 26 | | dB |
| Spurious emissions and harmonics | | | | | |
| Spurious emissions, high-power PA ⁽¹⁾ | f < 1 GHz, outside restricted bands | +20 dBm setting | < -36 | | dBm |
| | f < 1 GHz, restricted bands FCC | | < -55 | | dBm |
| | f > 1 GHz, including harmonics | | -37 | | dBm |
| Harmonics, high-power PA ⁽²⁾ | Second harmonic | | -35 | | dBm |
| | Third harmonic | | -42 | | dBm |
| Spurious emissions, high-power PA, 10 dBm configuration ⁽¹⁾ ⁽³⁾ | f < 1 GHz, outside restricted bands | +10 dBm setting ⁽³⁾ | < -36 | | dBm |
| | f < 1 GHz, restricted bands ETSI | | < -54 | | dBm |
| | f < 1 GHz, restricted bands FCC | | < -55 | | dBm |
| | f > 1 GHz, including harmonics | | -41 | | dBm |
| Harmonics, high-power PA, 10 dBm configuration ⁽³⁾ | Second harmonic | | < -42 | | dBm |
| | Third harmonic | | < -42 | | dBm |
| Spurious emissions, regular PA | f < 1 GHz, outside restricted bands | +5 dBm setting | < -36 | | dBm |
| | f < 1 GHz, restricted bands ETSI | | < -54 | | dBm |
| | f < 1 GHz, restricted bands FCC | | < -55 | | dBm |
| | f > 1 GHz, including harmonics | | < -42 | | dBm |
| Harmonics, regular PA | Second harmonic | | < -42 | | dBm |
| | Third harmonic | | < -42 | | dBm |

- (1) To ensure margins for passing FCC band edge requirements at 2483.5 MHz, a lower than maximum output-power setting or less than 100% duty cycle may be used when operating at the upper Bluetooth Low Energy channel(s).
- (2) To ensure margins for passing FCC requirements for harmonic emission, duty cycling may be required. The CC2651P3 LaunchPad reference design should also be reviewed as the filter provides higher attenuation of harmonics compared to the CC26x1-P3EM-XD24-PA24 reference design.
- (3) Measured on evaluation board as described in www.ti.com/lit/pdf/swra636.

8.12 Zigbee - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - RX

Measured on the CC26x1-P3EM-7XD24-PA24 reference design with $T_c = 25\text{ }^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, $f_{RF} = 2440\text{ MHz}$ with DC/DC enabled and high power PA connected to V_{DD5} unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-----|---------|-----|------|
| General Parameters | | | | | |
| Receiver sensitivity | Differential mode PER = 1% | | - 100 | | dBm |
| Receiver sensitivity | Single-Ended mode. Measured on CC26x1-P3EM-5XS24 at the SMA connector. PER = 1% | | -99 | | dBm |
| Receiver saturation | PER = 1% | | > 5 | | dBm |
| Adjacent channel rejection | Wanted signal at - 82 dBm, modulated interferer at $\pm 5\text{ MHz}$, PER = 1% | | 36 | | dB |
| Alternate channel rejection | Wanted signal at - 82 dBm, modulated interferer at $\pm 10\text{ MHz}$, PER = 1% | | 57 | | dB |
| Channel rejection, $\pm 15\text{ MHz}$ or more | Wanted signal at - 82 dBm, undesired signal is IEEE 802.15.4 modulated channel, stepped through all channels 2405 to 2480 MHz, PER = 1% | | 59 | | dB |
| Blocking and desensitization, 5 MHz from upper band edge | Wanted signal at - 97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 57 | | dB |
| Blocking and desensitization, 10 MHz from upper band edge | Wanted signal at - 97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 63 | | dB |
| Blocking and desensitization, 20 MHz from upper band edge | Wanted signal at - 97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 63 | | dB |
| Blocking and desensitization, 50 MHz from upper band edge | Wanted signal at - 97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 66 | | dB |
| Blocking and desensitization, - 5 MHz from lower band edge | Wanted signal at - 97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 60 | | dB |
| Blocking and desensitization, - 10 MHz from lower band edge | Wanted signal at - 97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 60 | | dB |
| Blocking and desensitization, - 20 MHz from lower band edge | Wanted signal at - 97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 63 | | dB |
| Blocking and desensitization, - 50 MHz from lower band edge | Wanted signal at - 97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 65 | | dB |
| Spurious emissions, 30 MHz to 1000 MHz | Measurement in a 50- Ω single-ended load ⁽¹⁾ | | - 66 | | dBm |
| Spurious emissions, 1 GHz to 12.75 GHz | Measurement in a 50- Ω single-ended load ⁽¹⁾ | | - 53 | | dBm |
| Frequency error tolerance | Difference between the incoming carrier frequency and the internally generated carrier frequency | | > 350 | | ppm |
| Symbol rate error tolerance | Difference between incoming symbol rate and the internally generated symbol rate | | > 1000 | | ppm |
| RSSI dynamic range | | | 95 | | dB |
| RSSI accuracy | | | ± 4 | | dB |

(1) Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66

8.13 Zigbee - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - TX

Measured on the CC26x1-P3EM-7XD24-PA24 reference design with $T_c = 25\text{ }^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, $f_{RF} = 2440\text{ MHz}$ with DC/DC enabled and high power PA connected to V_{DD5} unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|--------------------------------|-------|-----|------|
| General Parameters | | | | | |
| Max output power, high power PA | Differential mode, delivered to a single-ended 50- Ω load through a balun | | 20 | | dBm |
| Output power programmable range, high power PA | Differential mode, delivered to a single-ended 50- Ω load through a balun | | 6 | | dB |
| Max output power, high power PA, 10 dBm configuration ⁽⁴⁾ | Differential mode, delivered to a single-ended 50- Ω load through a balun | | 10.5 | | dBm |
| Max output power, high power PA, 10 dBm configuration ⁽⁴⁾ | Single-ended mode. Measured on CC26x1-P3EM-5XS24, delivered to a single-ended 50- Ω load through a balun | | 9 | | dBm |
| Output power programmable range, high power PA, 10 dBm configuration ⁽⁴⁾ | Differential mode, delivered to a single-ended 50- Ω load through a balun | | 5 | | dB |
| Max output power, regular PA | Differential mode, delivered to a single-ended 50- Ω load through a balun | | 5 | | dBm |
| Output power programmable range, regular PA | Differential mode, delivered to a single-ended 50- Ω load through a balun | | 26 | | dB |
| Spurious emissions and harmonics | | | | | |
| Spurious emissions, high-power PA ⁽²⁾ | f < 1 GHz, outside restricted bands | +20 dBm setting | < -39 | | dBm |
| | f < 1 GHz, restricted bands FCC | | < -49 | | dBm |
| | f > 1 GHz, including harmonics | | -40 | | dBm |
| Harmonics, high-power PA ⁽³⁾ | Second harmonic | | -35 | | dBm |
| | Third harmonic | | -42 | | dBm |
| Spurious emissions, high-power PA, 10 dBm configuration ^{(2) (4)} | f < 1 GHz, outside restricted bands | +10 dBm setting ⁽⁴⁾ | < -36 | | dBm |
| | f < 1 GHz, restricted bands ETSI | | < -47 | | dBm |
| | f < 1 GHz, restricted bands FCC | | < -55 | | dBm |
| | f > 1 GHz, including harmonics | | -42 | | dBm |
| Harmonics, high-power PA, 10 dBm configuration ⁽⁴⁾ | Second harmonic | | < -42 | | dBm |
| | Third harmonic | | < -42 | | dBm |
| Spurious emissions, regular PA ⁽¹⁾ | f < 1 GHz, outside restricted bands | +5 dBm setting | < -36 | | dBm |
| | f < 1 GHz, restricted bands ETSI | | < -47 | | dBm |
| | f < 1 GHz, restricted bands FCC | | < -55 | | dBm |
| | f > 1 GHz, including harmonics | | < -42 | | dBm |
| Harmonics, regular PA | Second harmonic | | < -42 | | dBm |
| | Third harmonic | | < -42 | | dBm |
| IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) | | | | | |
| Error vector magnitude, high power PA | +20 dBm setting | | 2 | | % |
| Error vector magnitude, high power PA, 10 dBm configuration ⁽⁴⁾ | +10 dBm setting | | 2 | | % |
| Error vector magnitude Regular PA | +5 dBm setting | | 2 | | % |

(1) To ensure margins for passing FCC band edge requirements at 2483.5 MHz, a lower than maximum output-power setting or less than 100% duty cycle may be used when operating at 2480 MHz.

- (2) To ensure margins for passing FCC band edge requirements at 2483.5 MHz, a lower than maximum output-power setting or less than 100% duty cycle may be used when operating at the upper 802.15.4 channel(s).
- (3) To ensure margins for passing FCC requirements for harmonic emission, duty cycling may be required. The CC2651P3 LaunchPad reference design should also be reviewed as the filter provides higher attenuation of harmonics compared to the CC26x1-P3EM-7XD24-PA24 reference design.
- (4) Measured on evaluation board as described in <https://www.ti.com/lit/pdf/swra636>.

8.14 Timing and Switching Characteristics

8.14.1 Reset Timing

| PARAMETER | MIN | TYP | MAX | UNIT |
|----------------------|-----|-----|-----|------|
| RESET_N low duration | 1 | | | μs |

8.14.2 Wakeup Timing

Measured over operating free-air temperature with $V_{DD5} = 3.0\text{ V}$ (unless otherwise noted). The times listed here do not include software overhead.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------|-----|------|-----|------|
| MCU, Reset to Active ⁽¹⁾ | | 850 | 4000 | | μs |
| MCU, Shutdown to Active ⁽¹⁾ | | 850 | 4000 | | μs |
| MCU, Standby to Active | | | 160 | | μs |
| MCU, Active to Standby | | | 36 | | μs |
| MCU, Idle to Active | | | 14 | | μs |

- (1) The wakeup time is dependent on remaining charge on VDDR capacitor when starting the device, and thus how long the device has been in Reset or Shutdown before starting up again. The wake up time increases with a higher capacitor value.

8.14.3 Clock Specifications

8.14.3.1 48 MHz Crystal Oscillator (XOSC_HF)

Measured on a Texas Instruments reference design with $T_c = 25\text{ }^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.⁽¹⁾

| | PARAMETER | MIN | TYP | MAX | UNIT |
|-------|---|-----|-------------------------------|-----|------|
| | Crystal frequency | | 48 | | MHz |
| ESR | Equivalent series resistance $6\text{ pF} < C_L \leq 9\text{ pF}$ | | 20 | 60 | Ω |
| ESR | Equivalent series resistance $5\text{ pF} < C_L \leq 6\text{ pF}$ | | | 80 | Ω |
| L_M | Motional inductance, relates to the load capacitance that is used for the crystal (C_L in Farads) ⁽⁵⁾ | | $< 3 \times 10^{-25} / C_L^2$ | | H |
| C_L | Crystal load capacitance ⁽⁴⁾ | 5 | 7 ⁽³⁾ | 9 | pF |
| | Start-up time ⁽²⁾ | | 200 | | μs |

- (1) Probing or otherwise stopping the crystal while the DC/DC converter is enabled may cause permanent damage to the device.
- (2) Start-up time using the TI-provided power driver. Start-up time may increase if driver is not used.
- (3) On-chip default connected capacitance including reference design parasitic capacitance. Connected internal capacitance is changed through software in the Customer Configuration section (CCFG).
- (4) Adjustable load capacitance is integrated into the device. External load capacitors are required for systems targeting compliance with certain regulations. See the device errata for further details.
- (5) The crystal manufacturer's specification must satisfy this requirement for proper operation.

8.14.3.2 48 MHz RC Oscillator (RCOSC_HF)

Measured on a Texas Instruments reference design with $T_c = 25\text{ }^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.

| | MIN | TYP | MAX | UNIT |
|--|-----|-------|-----|------|
| Frequency | | 48 | | MHz |
| Uncalibrated frequency accuracy | | ±1 | | % |
| Calibrated frequency accuracy ⁽¹⁾ | | ±0.25 | | % |
| Start-up time | | 5 | | μs |

- (1) Accuracy relative to the calibration source (XOSC_HF)

8.14.3.3 32.768 kHz Crystal Oscillator (XOSC_LF)

Measured on a Texas Instruments reference design with $T_c = 25\text{ }^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.

| | | MIN | TYP | MAX | UNIT |
|-------|------------------------------|-----|------------------|-----|------------|
| | Crystal frequency | | 32.768 | | kHz |
| ESR | Equivalent series resistance | | 30 | 100 | k Ω |
| C_L | Crystal load capacitance | 6 | 7 ⁽¹⁾ | 12 | pF |

- (1) Default load capacitance using TI reference designs including parasitic capacitance. Crystals with different load capacitance may be used.

8.14.3.4 32 kHz RC Oscillator (RCOSC_LF)

Measured on a Texas Instruments reference design with $T_c = 25\text{ }^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.

| | | MIN | TYP | MAX | UNIT |
|---|--|-----|--------------------------|-----|-----------------------|
| | Calibrated frequency | | 32.8 | | kHz |
| Calibrated RTC variation ⁽¹⁾ | Calibrated periodically against XOSC_HF ⁽²⁾ | | ± 600 ⁽³⁾ | | ppm |
| | Temperature coefficient. | | 50 | | ppm/ $^\circ\text{C}$ |

- (1) When using RCOSC_LF as source for the low frequency system clock (SCLK_LF), the accuracy of the SCLK_LF-derived Real Time Clock (RTC) can be improved by measuring RCOSC_LF relative to XOSC_HF and compensating for the RTC tick speed. This functionality is available through the TI-provided Power driver.
- (2) TI driver software calibrates the RTC every time XOSC_HF is enabled.
- (3) Some device's variation can exceed 1000 ppm. Further calibration will not improve variation.

8.14.4 Synchronous Serial Interface (SSI) Characteristics

8.14.4.1 Synchronous Serial Interface (SSI) Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|-------------------|------------------------|-------------------|-----|-----|-------|------------------------------|
| S1 | $t_{\text{clk_per}}$ | SSIClk cycle time | 12 | | 65024 | System Clocks ⁽²⁾ |
| S2 ⁽¹⁾ | $t_{\text{clk_high}}$ | SSIClk high time | | 0.5 | | $t_{\text{clk_per}}$ |
| S3 ⁽¹⁾ | $t_{\text{clk_low}}$ | SSIClk low time | | 0.5 | | $t_{\text{clk_per}}$ |

- (1) Refer to SSI timing diagrams 图 8-1, 图 8-2, and 图 8-3.
- (2) When using the TI-provided Power driver, the SSI system clock is always 48 MHz.

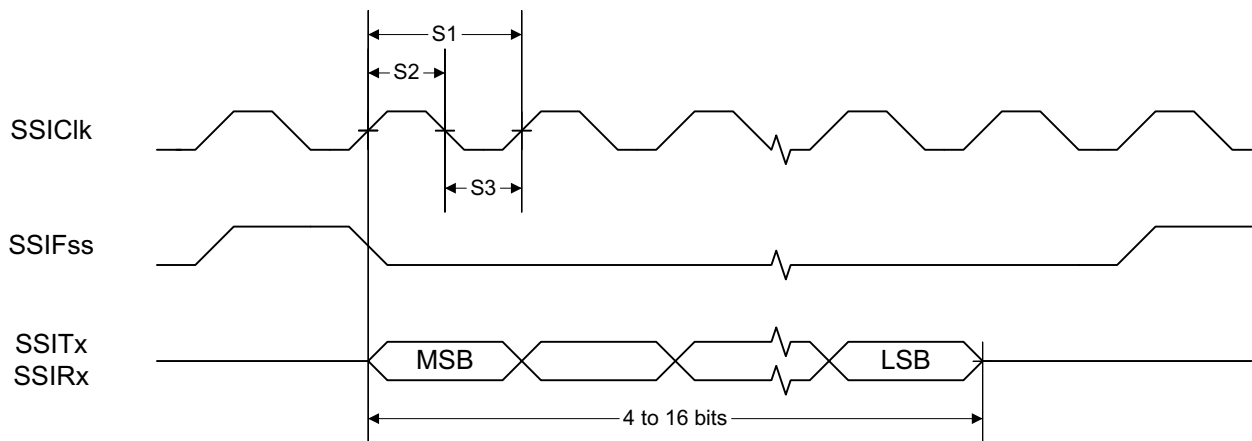


图 8-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

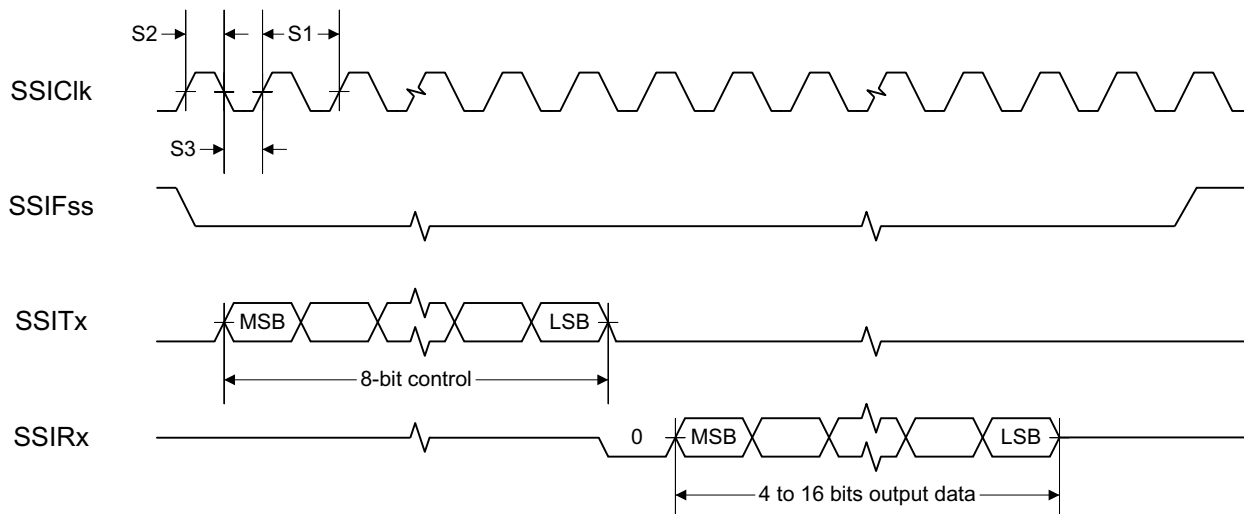


图 8-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer

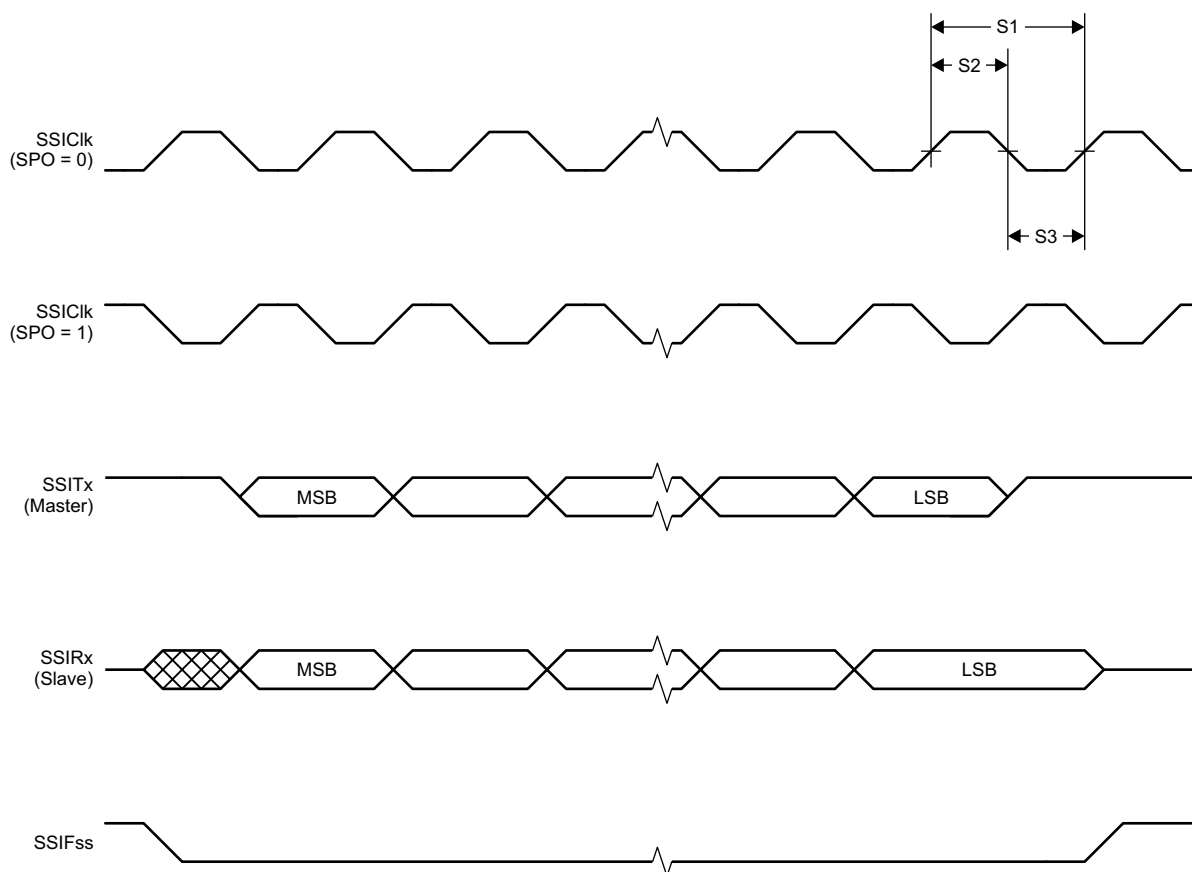


图 8-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

8.14.5 UART

8.14.5.1 UART Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | MIN | TYP | MAX | UNIT |
|-----------|-----|-----|-----|-------|
| UART rate | | | 3 | MBaud |

8.15 Peripheral Characteristics

8.15.1 ADC

8.15.1.1 Analog-to-Digital Converter (ADC) Characteristics

$T_c = 25\text{ }^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$ and voltage scaling enabled, unless otherwise noted.⁽¹⁾

Performance numbers require use of offset and gain adjustments in software by TI-provided ADC drivers.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|--------------------------------------|---|-----|--|------------------|--------------|
| | Input voltage range | | 0 | | V _{DD5} | V |
| | Resolution | | | 12 | | Bits |
| | Sample Rate | | | | 200 | ksps |
| | Offset | Internal 4.3 V equivalent reference ⁽²⁾ | | - 0.24 | | LSB |
| | Gain error | Internal 4.3 V equivalent reference ⁽²⁾ | | 7.14 | | LSB |
| DNL ⁽⁴⁾ | Differential nonlinearity | | | > - 1 | | LSB |
| INL | Integral nonlinearity | | | ±4 | | LSB |
| ENOB | Effective number of bits | Internal 4.3 V equivalent reference ⁽²⁾ , 200 kSamples/s, 9.6 kHz input tone | | 9.8 | | Bits |
| | | Internal 4.3 V equivalent reference ⁽²⁾ , 200 kSamples/s, 9.6 kHz input tone, DC/DC enabled | | 9.8 | | |
| | | V _{DD5} as reference, 200 kSamples/s, 9.6 kHz input tone | | 10.1 | | |
| | | Internal reference, voltage scaling disabled, 32 samples average (software), 200 kSamples/s, 300 Hz input tone | | 11.1 | | |
| | | Internal reference, voltage scaling disabled, 14-bit mode, 200 kSamples/s, 300 Hz input tone ⁽⁵⁾ | | 11.3 | | |
| | | Internal reference, voltage scaling disabled, 15-bit mode, 200 kSamples/s, 300 Hz input tone ⁽⁵⁾ | | 11.6 | | |
| THD | Total harmonic distortion | Internal 4.3 V equivalent reference ⁽²⁾ , 200 kSamples/s, 9.6 kHz input tone | | - 65 | | dB |
| | | V _{DD5} as reference, 200 kSamples/s, 9.6 kHz input tone | | - 70 | | |
| | | Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone | | - 72 | | |
| SINAD, SNDR | Signal-to-noise and distortion ratio | Internal 4.3 V equivalent reference ⁽²⁾ , 200 kSamples/s, 9.6 kHz input tone | | 60 | | dB |
| | | V _{DD5} as reference, 200 kSamples/s, 9.6 kHz input tone | | 63 | | |
| | | Internal reference, voltage scaling disabled, 32 samples average (software), 200 kSamples/s, 300 Hz input tone | | 68 | | |
| SFDR | Spurious-free dynamic range | Internal 4.3 V equivalent reference ⁽²⁾ , 200 kSamples/s, 9.6 kHz input tone | | 70 | | dB |
| | | V _{DD5} as reference, 200 kSamples/s, 9.6 kHz input tone | | 73 | | |
| | | Internal reference, voltage scaling disabled, 32 samples average (software), 200 kSamples/s, 300 Hz input tone | | 75 | | |
| | Conversion time | Serial conversion, time-to-output, 24 MHz clock | | 50 | | Clock Cycles |
| | Current consumption | Internal 4.3 V equivalent reference ⁽²⁾ | | 0.39 | | mA |
| | Current consumption | V _{DD5} as reference | | 0.56 | | mA |
| | Reference voltage | Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1 | | 4.3 ⁽²⁾ ⁽³⁾ | | V |
| | Reference voltage | Fixed internal reference (input voltage scaling disabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows: $V_{ref} = 4.3\text{ V} \times 1408 / 4095$ | | 1.48 | | V |
| | Reference voltage | V _{DD5} as reference, input voltage scaling enabled | | V _{DD5} | | V |
| | Reference voltage | V _{DD5} as reference, input voltage scaling disabled | | V _{DD5} / 2.82 ⁽³⁾ | | V |

8.15.1.1 Analog-to-Digital Converter (ADC) Characteristics (continued)

$T_c = 25\text{ }^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$ and voltage scaling enabled, unless otherwise noted.⁽¹⁾

Performance numbers require use of offset and gain adjustments in software by TI-provided ADC drivers.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|-----------------|--|-----|-----|-----|------------|
| | Input impedance | 200 kSamples/s, voltage scaling enabled. Capacitive input, Input impedance depends on sampling frequency and sampling time | | >1 | | M Ω |

- (1) Using IEEE Std 1241-2010 for terminology and test methods
- (2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V
- (3) Applied voltage must be within Absolute Maximum Ratings at all times
- (4) No missing codes
- (5) $\text{ADC_output} = \Sigma(4^n \text{ samples}) \gg n$, $n = \text{desired extra bits}$

8.15.2 DAC

8.15.2.1 Digital-to-Analog Converter (DAC) Characteristics

$T_c = 25\text{ }^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|---|-----|------------|------|--------------------|
| General Parameters | | | | | | |
| | Resolution | | | 8 | | Bits |
| V_{DD5} | Supply voltage | Any load, any V_{REF} , pre-charge OFF, DAC charge-pump ON | 1.8 | | 3.8 | V |
| | | External Load ⁽⁴⁾ , any V_{REF} , pre-charge OFF, DAC charge-pump OFF | 2.0 | | 3.8 | |
| | | Any load, $V_{REF} = \text{DCOUP}$, pre-charge ON | 2.6 | | 3.8 | |
| F_{DAC} | Clock frequency | Buffer ON (recommended for external load) | 16 | | 250 | kHz |
| | | Buffer OFF (internal load) | 16 | | 1000 | |
| | Voltage output settling time | $V_{REF} = V_{DD5}$, buffer OFF, internal load | | 13 | | 1 / F_{DAC} |
| | | $V_{REF} = V_{DD5}$, buffer ON, external capacitive load = 20 pF ⁽³⁾ | | 13.8 | | |
| | External capacitive load | | | 20 | 200 | pF |
| | External resistive load | | 10 | | | M Ω |
| | Short circuit current | | | | 400 | μA |
| Z_{MAX} | Max output impedance $V_{ref} = V_{DD5}$, buffer ON, CLK 250 kHz | $V_{DD5} = 3.8\text{ V}$, DAC charge-pump OFF | | 50.8 | | k Ω |
| | | $V_{DD5} = 3.0\text{ V}$, DAC charge-pump ON | | 51.7 | | |
| | | $V_{DD5} = 3.0\text{ V}$, DAC charge-pump OFF | | 53.2 | | |
| | | $V_{DD5} = 2.0\text{ V}$, DAC charge-pump ON | | 48.7 | | |
| | | $V_{DD5} = 2.0\text{ V}$, DAC charge-pump OFF | | 70.2 | | |
| | | $V_{DD5} = 1.8\text{ V}$, DAC charge-pump ON | | 46.3 | | |
| | | $V_{DD5} = 1.8\text{ V}$, DAC charge-pump OFF | | 88.9 | | |
| Internal Load - Continuous Time Comparator / Low Power Clocked Comparator | | | | | | |
| DNL | Differential nonlinearity | $V_{REF} = V_{DD5}$, load = Continuous Time Comparator or Low Power Clocked Comparator $F_{DAC} = 250\text{ kHz}$ | | ± 1 | | LSB ⁽¹⁾ |
| | Differential nonlinearity | $V_{REF} = V_{DD5}$, load = Continuous Time Comparator or Low Power Clocked Comparator $F_{DAC} = 16\text{ kHz}$ | | ± 1.2 | | |
| | Offset error ⁽²⁾ Load = Continuous Time Comparator | $V_{REF} = V_{DD5} = 3.8\text{ V}$ | | ± 0.64 | | LSB ⁽¹⁾ |
| | | $V_{REF} = V_{DD5} = 3.0\text{ V}$ | | ± 0.81 | | |
| | | $V_{REF} = V_{DD5} = 1.8\text{ V}$ | | ± 1.27 | | |
| | | $V_{REF} = \text{DCOUP}$, pre-charge ON | | ± 3.43 | | |
| | | $V_{REF} = \text{DCOUP}$, pre-charge OFF | | ± 2.88 | | |
| | | $V_{REF} = \text{ADCRE}$ | | ± 2.37 | | |

8.15.2.1 Digital-to-Analog Converter (DAC) Characteristics (continued)

T_c = 25 °C, V_{DD5} = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | | |
|---|---|---|---|------|--------------------|--------------------|---|
| Offset error ⁽²⁾ Load = Low Power Clocked Comparator | V _{REF} = VDD5 = 3.8 V | | ±0.78 | | LSB ⁽¹⁾ | | |
| | V _{REF} = VDD5 = 3.0 V | | ±0.77 | | | | |
| | V _{REF} = VDD5 = 1.8 V | | ±3.46 | | | | |
| | V _{REF} = DCOUPL, pre-charge ON | | ±3.44 | | | | |
| | V _{REF} = DCOUPL, pre-charge OFF | | ±4.70 | | | | |
| | V _{REF} = ADCREF | | ±4.11 | | | | |
| Max code output voltage variation ⁽²⁾ Load = Continuous Time Comparator | V _{REF} = VDD5 = 3.8 V | | ±1.53 | | LSB ⁽¹⁾ | | |
| | V _{REF} = VDD5 = 3.0 V | | ±1.71 | | | | |
| | V _{REF} = VDD5 = 1.8 V | | ±2.10 | | | | |
| | V _{REF} = DCOUPL, pre-charge ON | | ±6.00 | | | | |
| | V _{REF} = DCOUPL, pre-charge OFF | | ±3.85 | | | | |
| | V _{REF} = ADCREF | | ±5.84 | | | | |
| Max code output voltage variation ⁽²⁾ Load = Low Power Clocked Comparator | V _{REF} = VDD5 = 3.8 V | | ±2.92 | | LSB ⁽¹⁾ | | |
| | V _{REF} = VDD5 = 3.0 V | | ±3.06 | | | | |
| | V _{REF} = VDD5 = 1.8 V | | ±3.91 | | | | |
| | V _{REF} = DCOUPL, pre-charge ON | | ±7.84 | | | | |
| | V _{REF} = DCOUPL, pre-charge OFF | | ±4.06 | | | | |
| | V _{REF} = ADCREF | | ±6.94 | | | | |
| Output voltage range ⁽²⁾ Load = Continuous Time Comparator | V _{REF} = VDD5 = 3.8 V, code 1 | | 0.03 | | V | | |
| | V _{REF} = VDD5 = 3.8 V, code 255 | | 3.62 | | | | |
| | V _{REF} = VDD5 = 3.0 V, code 1 | | 0.02 | | | | |
| | V _{REF} = VDD5 = 3.0 V, code 255 | | 2.86 | | | | |
| | V _{REF} = VDD5 = 1.8 V, code 1 | | 0.01 | | | | |
| | V _{REF} = VDD5 = 1.8 V, code 255 | | 1.71 | | | | |
| | V _{REF} = DCOUPL, pre-charge OFF, code 1 | | 0.01 | | | | |
| | V _{REF} = DCOUPL, pre-charge OFF, code 255 | | 1.21 | | | | |
| | V _{REF} = DCOUPL, pre-charge ON, code 1 | | 1.27 | | | | |
| | V _{REF} = DCOUPL, pre-charge ON, code 255 | | 2.46 | | | | |
| | V _{REF} = ADCREF, code 1 | | 0.01 | | | | |
| | V _{REF} = ADCREF, code 255 | | 1.41 | | | | |
| | Output voltage range ⁽²⁾ Load = Low Power Clocked Comparator | V _{REF} = VDD5 = 3.8 V, code 1 | | 0.03 | | | V |
| | | V _{REF} = VDD5 = 3.8 V, code 255 | | 3.61 | | | |
| V _{REF} = VDD5 = 3.0 V, code 1 | | | 0.02 | | | | |
| V _{REF} = VDD5 = 3.0 V, code 255 | | | 2.85 | | | | |
| V _{REF} = VDD5 = 1.8 V, code 1 | | | 0.01 | | | | |
| V _{REF} = VDD5 = 1.8 V, code 255 | | | 1.71 | | | | |
| V _{REF} = DCOUPL, pre-charge OFF, code 1 | | | 0.01 | | | | |
| V _{REF} = DCOUPL, pre-charge OFF, code 255 | | | 1.21 | | | | |
| V _{REF} = DCOUPL, pre-charge ON, code 1 | | | 1.27 | | | | |
| V _{REF} = DCOUPL, pre-charge ON, code 255 | | | 2.46 | | | | |
| V _{REF} = ADCREF, code 1 | | | 0.01 | | | | |
| V _{REF} = ADCREF, code 255 | | | 1.41 | | | | |
| External Load (Keysight 34401A Multimeter) | | | | | | | |
| INL | | Integral nonlinearity | V _{REF} = VDD5, F _{DAC} = 250 kHz | | ±1 | LSB ⁽¹⁾ | |
| | V _{REF} = DCOUPL, F _{DAC} = 250 kHz | | | ±1 | | | |
| | V _{REF} = ADCREF, F _{DAC} = 250 kHz | | | ±1 | | | |
| DNL | Differential nonlinearity | V _{REF} = VDD5, F _{DAC} = 250 kHz | | ±1 | LSB ⁽¹⁾ | | |

8.15.2.1 Digital-to-Analog Converter (DAC) Characteristics (continued)

$T_c = 25\text{ }^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|-----|------------|-----|--------------------|
| Offset error | $V_{REF} = V_{DD5} = 3.8\text{ V}$ | | ± 0.20 | | LSB ⁽¹⁾ |
| | $V_{REF} = V_{DD5} = 3.0\text{ V}$ | | ± 0.25 | | |
| | $V_{REF} = V_{DD5} = 1.8\text{ V}$ | | ± 0.45 | | |
| | $V_{REF} = \text{DCOUPPL}$, pre-charge ON | | ± 1.55 | | |
| | $V_{REF} = \text{DCOUPPL}$, pre-charge OFF | | ± 1.30 | | |
| | $V_{REF} = \text{ADCREFL}$ | | ± 1.10 | | |
| Max code output voltage variation | $V_{REF} = V_{DD5} = 3.8\text{ V}$ | | ± 0.60 | | LSB ⁽¹⁾ |
| | $V_{REF} = V_{DD5} = 3.0\text{ V}$ | | ± 0.55 | | |
| | $V_{REF} = V_{DD5} = 1.8\text{ V}$ | | ± 0.60 | | |
| | $V_{REF} = \text{DCOUPPL}$, pre-charge ON | | ± 3.45 | | |
| | $V_{REF} = \text{DCOUPPL}$, pre-charge OFF | | ± 2.10 | | |
| | $V_{REF} = \text{ADCREFL}$ | | ± 1.90 | | |
| Output voltage range Load = Low Power Clocked Comparator | $V_{REF} = V_{DD5} = 3.8\text{ V}$, code 1 | | 0.03 | | V |
| | $V_{REF} = V_{DD5} = 3.8\text{ V}$, code 255 | | 3.61 | | |
| | $V_{REF} = V_{DD5} = 3.0\text{ V}$, code 1 | | 0.02 | | |
| | $V_{REF} = V_{DD5} = 3.0\text{ V}$, code 255 | | 2.85 | | |
| | $V_{REF} = V_{DD5} = 1.8\text{ V}$, code 1 | | 0.02 | | |
| | $V_{REF} = V_{DD5} = 1.8\text{ V}$, code 255 | | 1.71 | | |
| | $V_{REF} = \text{DCOUPPL}$, pre-charge OFF, code 1 | | 0.02 | | |
| | $V_{REF} = \text{DCOUPPL}$, pre-charge OFF, code 255 | | 1.20 | | |
| | $V_{REF} = \text{DCOUPPL}$, pre-charge ON, code 1 | | 1.27 | | |
| | $V_{REF} = \text{DCOUPPL}$, pre-charge ON, code 255 | | 2.46 | | |
| | $V_{REF} = \text{ADCREFL}$, code 1 | | 0.02 | | |
| | $V_{REF} = \text{ADCREFL}$, code 255 | | 1.42 | | |

(1) 1 LSB ($V_{REF} = 3.8\text{ V}/3.0\text{ V}/1.8\text{ V}/\text{DCOUPPL}/\text{ADCREFL}$) = 14.10 mV/11.13 mV/6.68 mV/4.67 mV/5.48 mV

(2) Includes comparator offset

(3) A load > 20 pF will increase the settling time

(4) Keysight 34401A Multimeter

8.15.3 Temperature and Battery Monitor

8.15.3.1 Temperature Sensor

Measured on a Texas Instruments reference design with $T_c = 25\text{ }^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|-----|-----------|-----|---------------------------|
| Resolution | | | 2 | | $^\circ\text{C}$ |
| Accuracy | -40 $^\circ\text{C}$ to 0 $^\circ\text{C}$ | | ± 4.0 | | $^\circ\text{C}$ |
| Accuracy | 0 $^\circ\text{C}$ to 105 $^\circ\text{C}$ | | ± 2.5 | | $^\circ\text{C}$ |
| Supply voltage coefficient ⁽¹⁾ | | | 3.9 | | $^\circ\text{C}/\text{V}$ |

(1) The temperature sensor is automatically compensated for V_{DD5} variation when using the TI-provided driver.

8.15.3.2 Battery Monitor

Measured on a Texas Instruments reference design with $T_c = 25\text{ }^\circ\text{C}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|--------------------------|-----|------|-----|------|
| Resolution | | | 25 | | mV |
| Range | | 1.8 | | 3.8 | V |
| Integral nonlinearity (max) | | | 23 | | mV |
| Accuracy | $V_{DD5} = 3.0\text{ V}$ | | 22.5 | | mV |
| Offset error | | | -32 | | mV |
| Gain error | | | -1 | | % |

8.15.4 Comparator

8.15.4.1 Continuous Time Comparator

$T_c = 25\text{ }^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------|---------------------------|-----|---------|-----------|---------------|
| Input voltage range ⁽¹⁾ | | 0 | | V_{DD5} | V |
| Offset | Measured at $V_{DD5} / 2$ | | ± 5 | | mV |
| Decision time | Step from -10 mV to 10 mV | | 0.78 | | μs |
| Current consumption | Internal reference | | 9.2 | | μA |

(1) The input voltages can be generated externally and connected throughout I/Os or an internal reference voltage can be generated using the DAC

8.15.5 GPIO

8.15.5.1 GPIO DC Characteristics

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-----|------|-----|---------------|
| $T_A = 25\text{ }^\circ\text{C}$, $V_{DD5} = 1.8\text{ V}$ | | | | | |
| GPIO VOH at 8 mA load | IOCURR = 2, high-drive GPIOs only | | 1.56 | | V |
| GPIO VOL at 8 mA load | IOCURR = 2, high-drive GPIOs only | | 0.24 | | V |
| GPIO VOH at 4 mA load | IOCURR = 1 | | 1.59 | | V |
| GPIO VOL at 4 mA load | IOCURR = 1 | | 0.21 | | V |
| GPIO pullup current | Input mode, pullup enabled, $V_{pad} = 0\text{ V}$ | | 73 | | μA |
| GPIO pulldown current | Input mode, pulldown enabled, $V_{pad} = V_{DD5}$ | | 19 | | μA |
| GPIO low-to-high input transition, with hysteresis | IH = 1, transition voltage for input read as 0 \rightarrow 1 | | 1.08 | | V |
| GPIO high-to-low input transition, with hysteresis | IH = 1, transition voltage for input read as 1 \rightarrow 0 | | 0.73 | | V |
| GPIO input hysteresis | IH = 1, difference between 0 \rightarrow 1 and 1 \rightarrow 0 points | | 0.35 | | V |
| $T_A = 25\text{ }^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$ | | | | | |
| GPIO VOH at 8 mA load | IOCURR = 2, high-drive GPIOs only | | 2.59 | | V |
| GPIO VOL at 8 mA load | IOCURR = 2, high-drive GPIOs only | | 0.42 | | V |
| GPIO VOH at 4 mA load | IOCURR = 1 | | 2.63 | | V |
| GPIO VOL at 4 mA load | IOCURR = 1 | | 0.40 | | V |

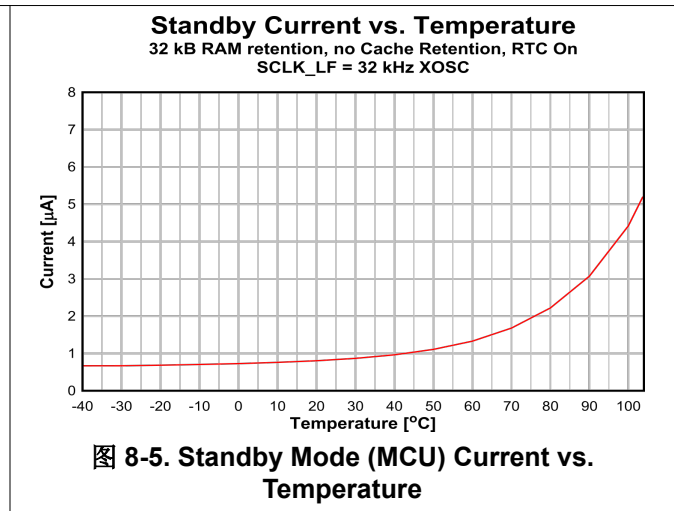
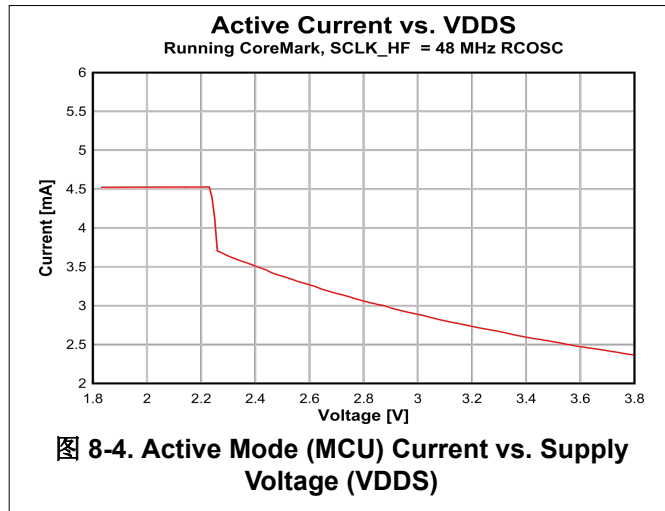
8.15.5.1 GPIO DC Characteristics (continued)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|----------------------|------|----------------------|------|
| T_A = 25 °C, V_{DDs} = 3.8 V | | | | | |
| GPIO pullup current | Input mode, pullup enabled, V _{pad} = 0 V | | 282 | | μA |
| GPIO pulldown current | Input mode, pulldown enabled, V _{pad} = V _{DDs} | | 110 | | μA |
| GPIO low-to-high input transition, with hysteresis | IH = 1, transition voltage for input read as 0 → 1 | | 1.97 | | V |
| GPIO high-to-low input transition, with hysteresis | IH = 1, transition voltage for input read as 1 → 0 | | 1.55 | | V |
| GPIO input hysteresis | IH = 1, difference between 0 → 1 and 1 → 0 points | | 0.42 | | V |
| T_A = 25 °C | | | | | |
| VIH | Lowest GPIO input voltage reliably interpreted as a <i>High</i> | 0.8*V _{DDs} | | | V |
| VIL | Highest GPIO input voltage reliably interpreted as a <i>Low</i> | | | 0.2*V _{DDs} | V |

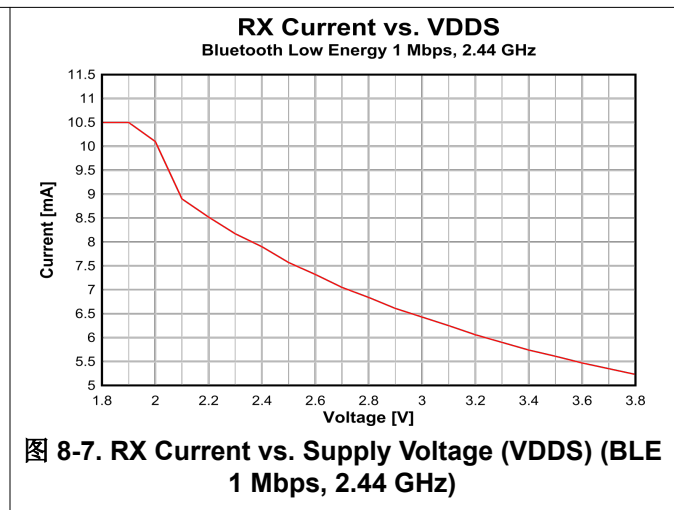
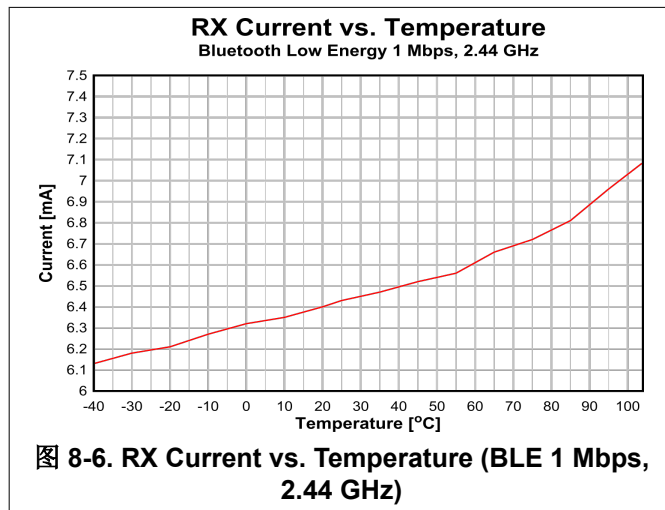
8.16 Typical Characteristics

All measurements in this section are done with $T_c = 25\text{ }^\circ\text{C}$ and $V_{DD5} = 3.0\text{ V}$, unless otherwise noted. See *Recommended Operating Conditions*, 节 8.3, for device limits. Values exceeding these limits are for reference only.

8.16.1 MCU Current



8.16.2 RX Current



8.16.3 TX Current

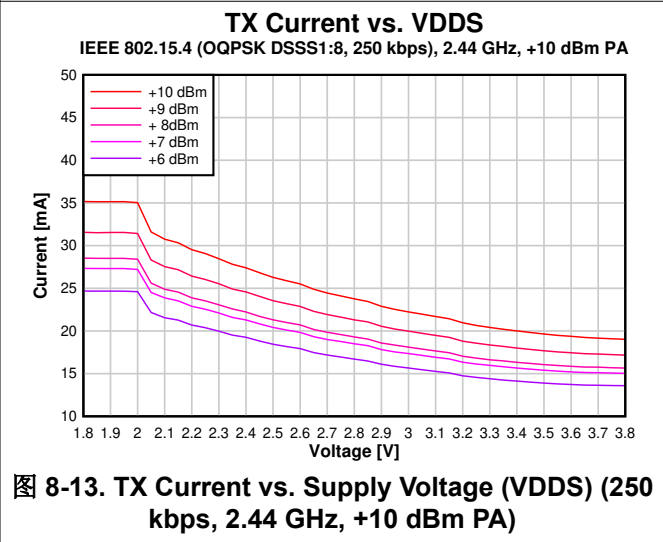
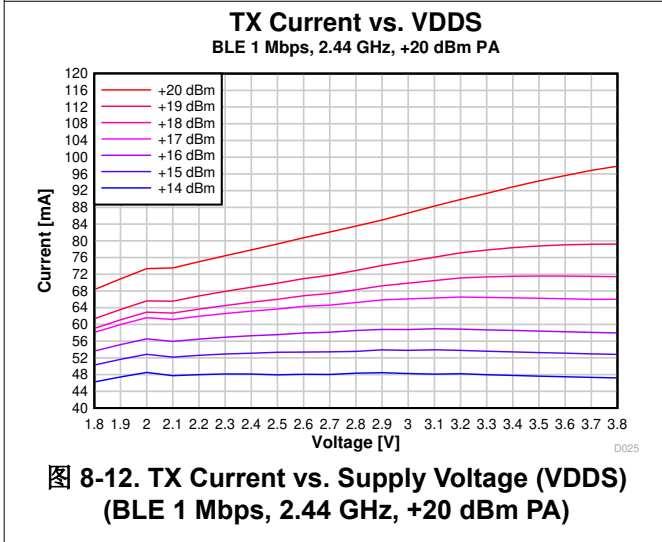
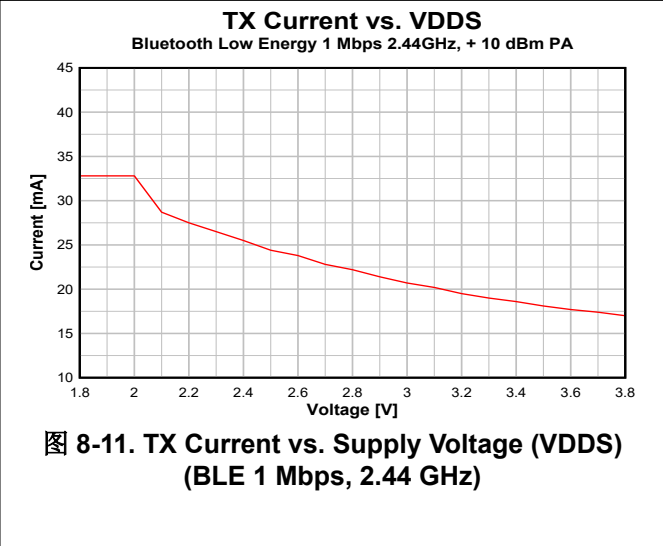
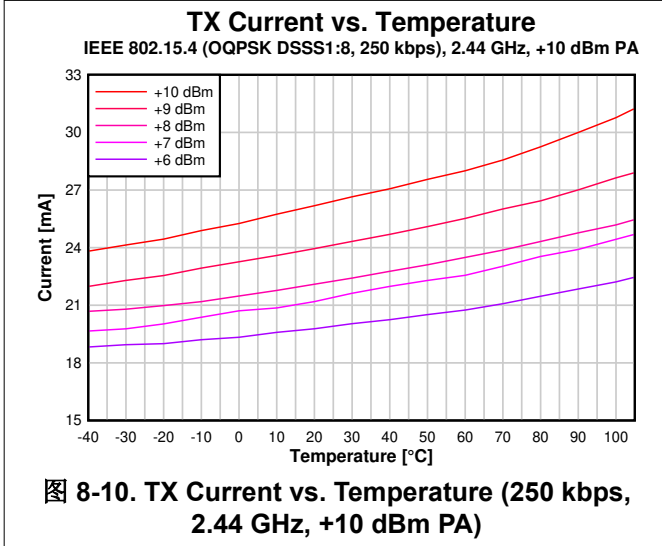
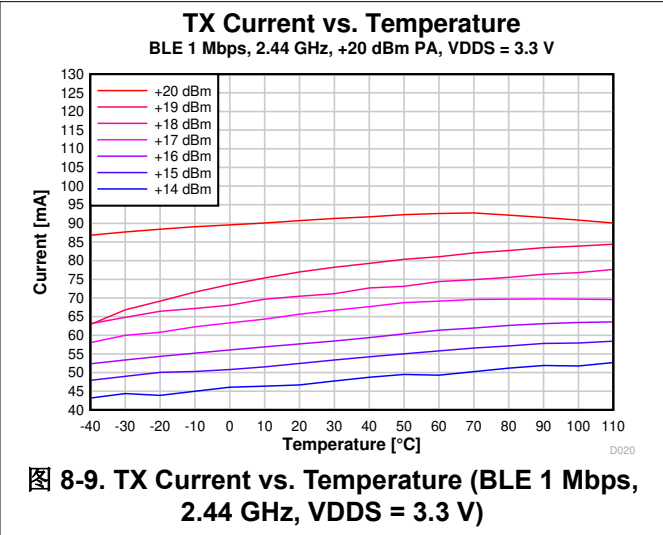
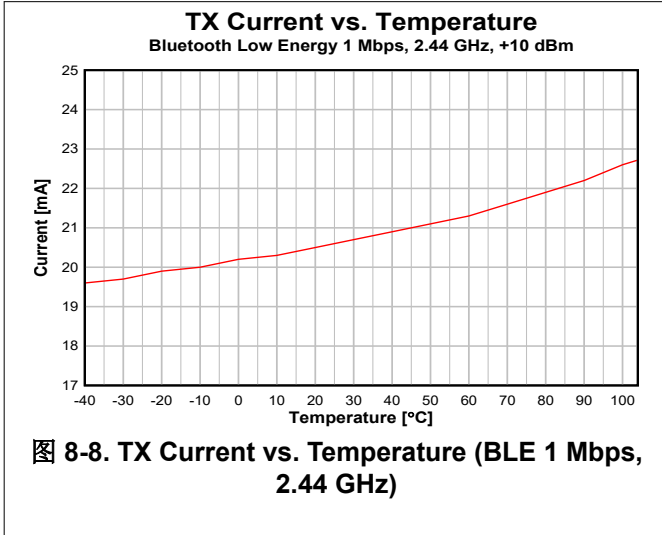


表 8-1. Typical TX Current and Output Power, regular PA

| CC2651P3 at 2.4 GHz, VDD5 = 3.0 V (Measured on CC2651-P3EM-7XD24-PA24) | | | |
|--|-----------------------------------|----------------------------|----------------------------------|
| txPower | TX Power Setting (SmartRF Studio) | Typical Output Power [dBm] | Typical Current Consumption [mA] |
| 0x701F | 5 | 5.5 | 12.5 |
| 0x3A17 | 4 | 4.5 | 11.9 |
| 0x3A64 | 3 | 3.1 | 11.2 |
| 0x325F | 2 | 2.0 | 10.8 |
| 0x2C5C | 1 | 1.3 | 10.5 |
| 0x2659 | 0 | 0.4 | 10.2 |
| 0x1697 | -3 | -2.8 | 9.4 |
| 0x1693 | -5 | -4.8 | 8.9 |
| 0x1292 | -6 | -5.4 | 8.8 |
| 0xCD3 | -9 | -9.0 | 8.4 |
| 0xAD1 | -10 | -10.4 | 8.2 |
| 0xACF | -12 | -12.0 | 8.1 |
| 0x6CD | -15 | -13.7 | 7.9 |
| 0x6CA | -18 | -16.8 | 7.7 |
| 0x4C8 | -20 | -19.3 | 7.6 |

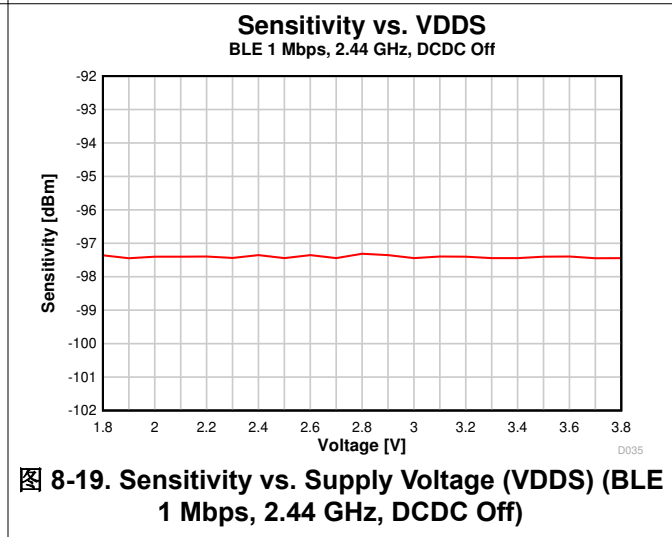
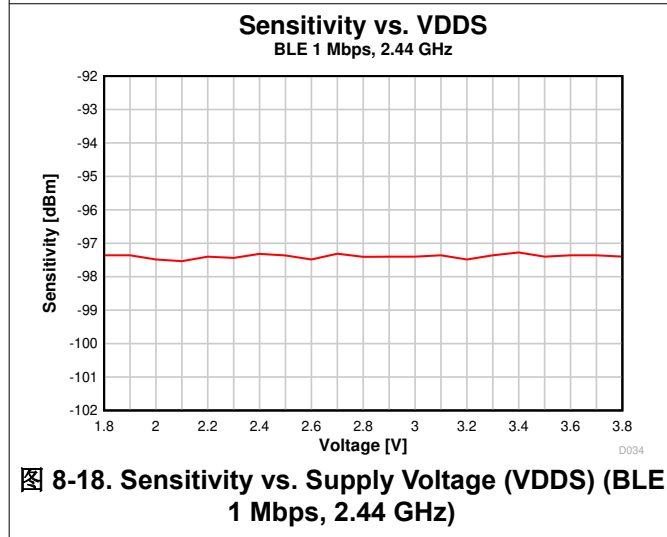
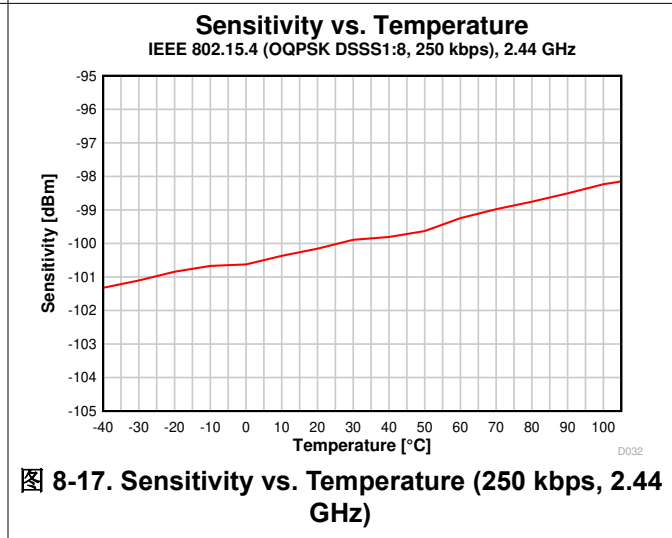
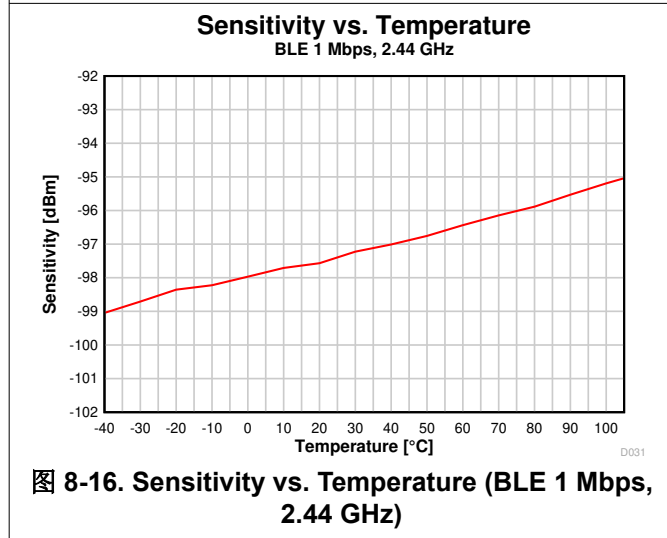
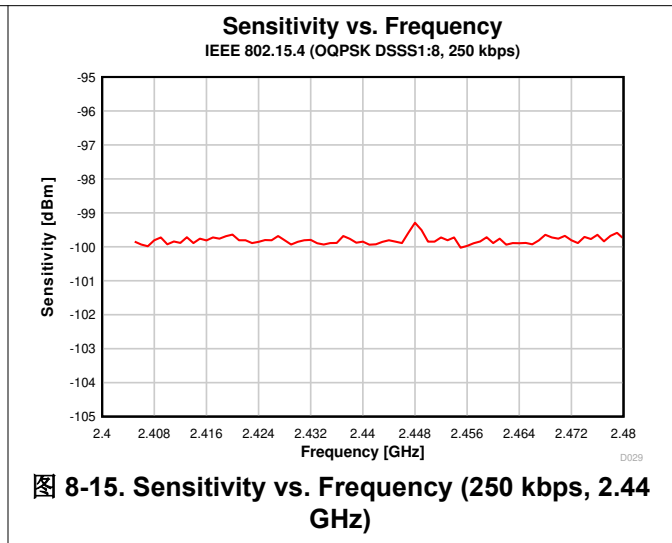
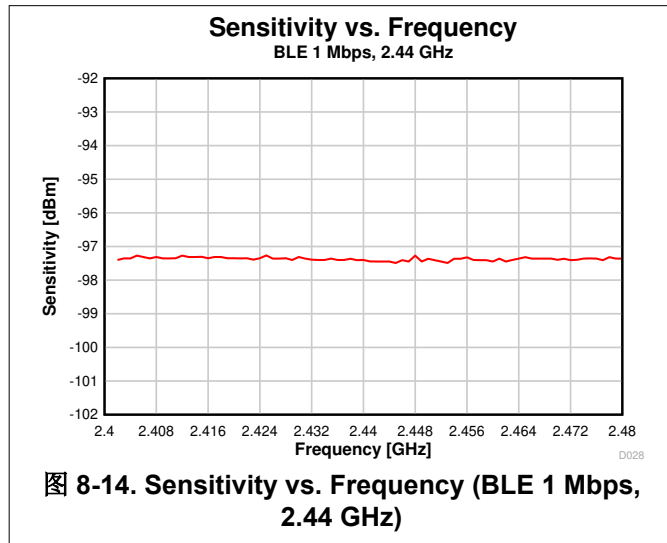
表 8-2. Typical TX Current and Output Power, high power PA, 10 dBm mode

| CC2651P3 at 2.4 GHz, VDD5 = 3.0 V (Measured on CC261-P3EM-5XS24-PA24_10dBm) | | | |
|---|-----------------------------------|----------------------------|----------------------------------|
| txPower | TX Power Setting (SmartRF Studio) | Typical Output Power [dBm] | Typical Current Consumption [mA] |
| 0x14395A | 10 | 10.1 | 23.6 |
| 0x142F55 | 9 | 9.0 | 22.1 |
| 0x62F35 | 8 | 7.8 | 21.1 |
| 0x63930 | 7 | 6.9 | 20.1 |
| 0x6292B | 6 | 5.9 | 19.1 |

表 8-3. Typical TX Current and Output Power, high power PA, 20 dBm mode

| CC2651P3 at 2.4 GHz, VDD5 = 3.3 V (Measured on CC2651-P3EM-7XD24-PA24) | | | |
|--|-----------------------------------|----------------------------|----------------------------------|
| txPower | TX Power Setting (SmartRF Studio) | Typical Output Power [dBm] | Typical Current Consumption [mA] |
| 0x3F75F5 | 20 | 20.0 | 100.1 |
| 0x3F61E2 | 19 | 19.4 | 91.1 |
| 0x3047E0 | 18 | 19.0 | 86.4 |
| 0x1B4FE5 | 17 | 18.1 | 78.3 |
| 0x1B39DE | 16 | 17.3 | 71.8 |
| 0x1B2FDA | 15 | 16.7 | 67.1 |
| 0x1B27D6 | 14 | 15.9 | 61.8 |

8.16.4 RX Performance



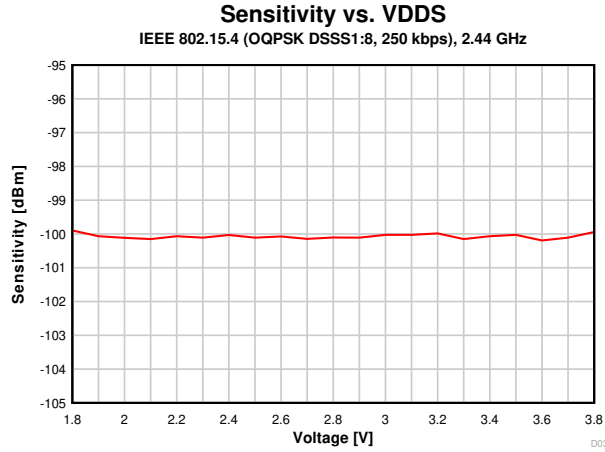
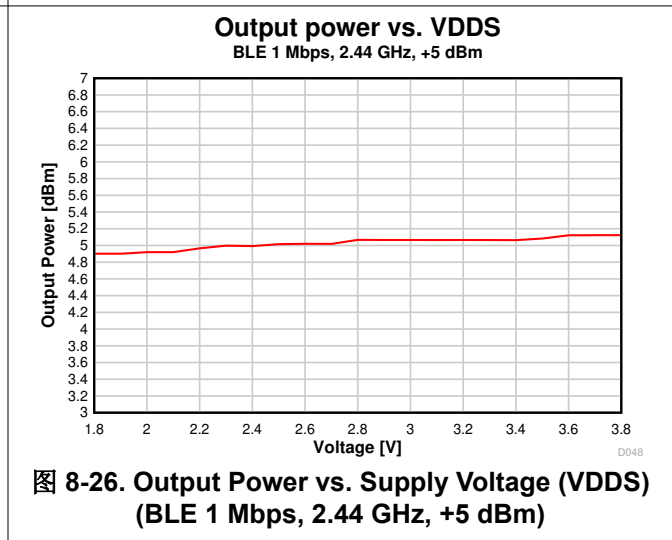
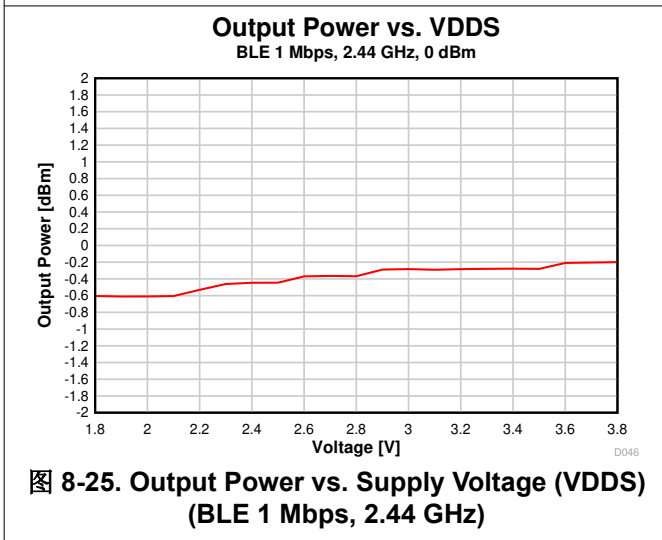
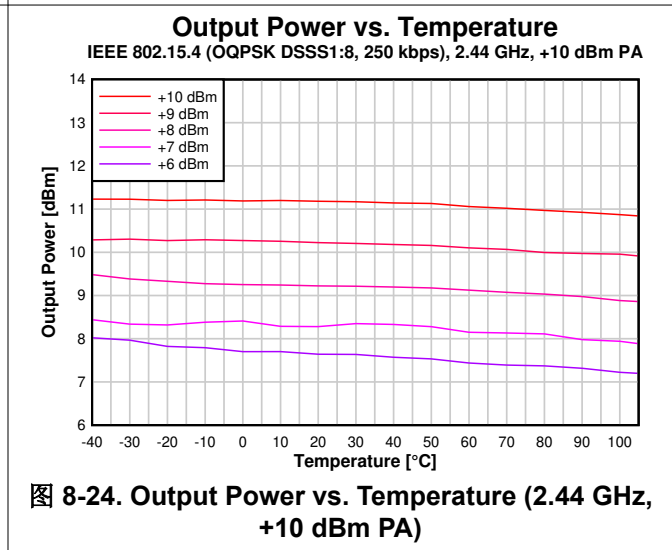
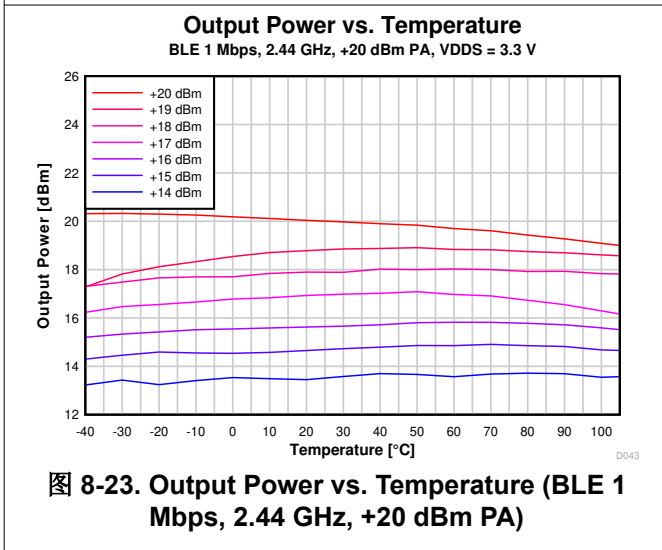
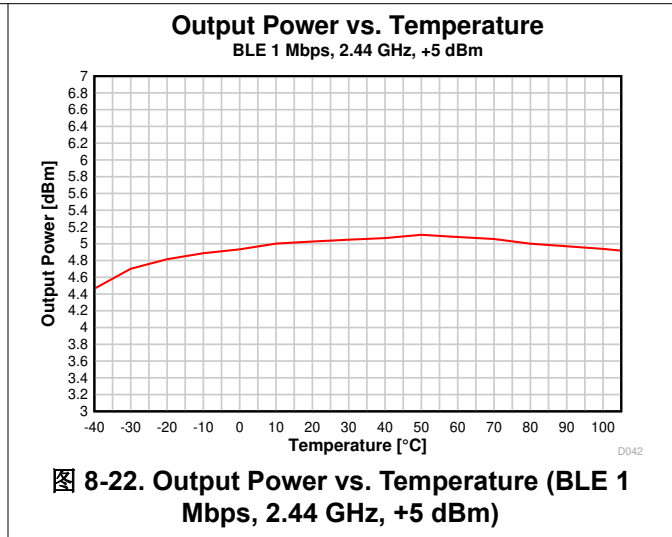
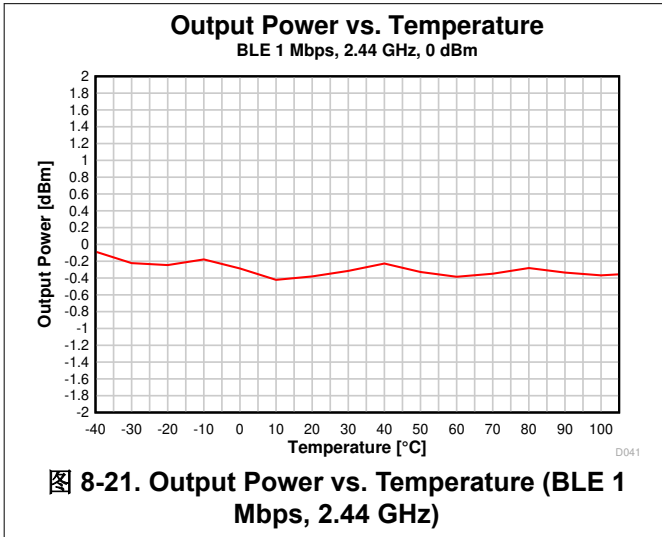
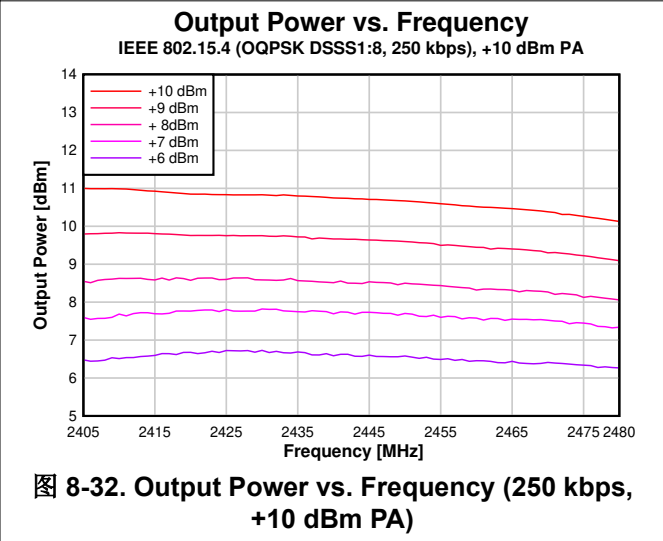
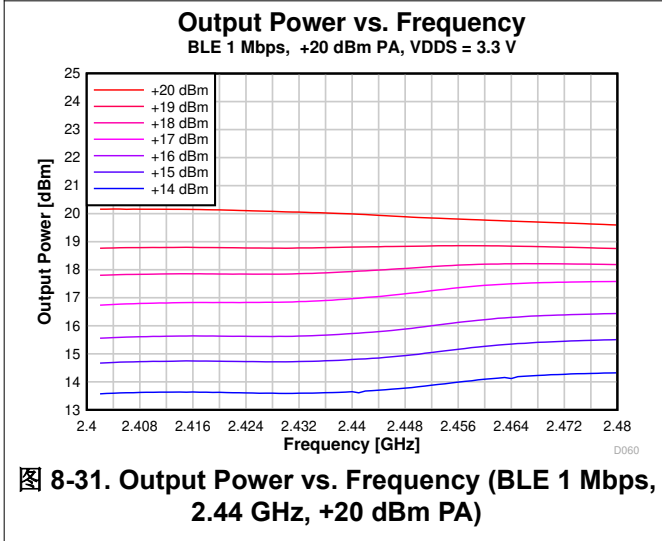
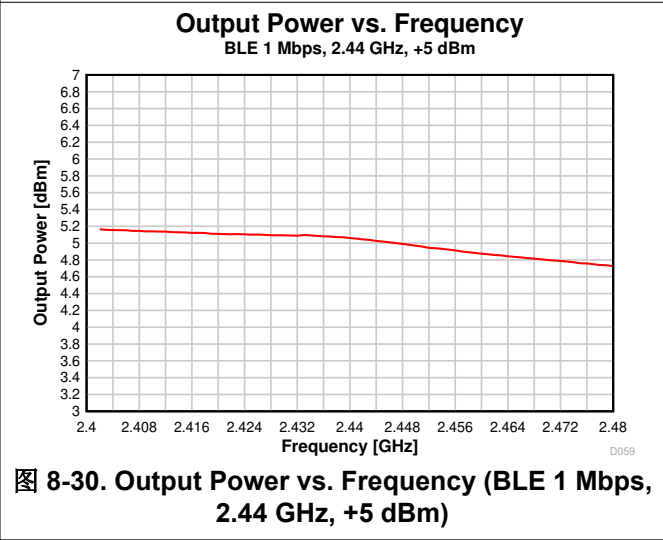
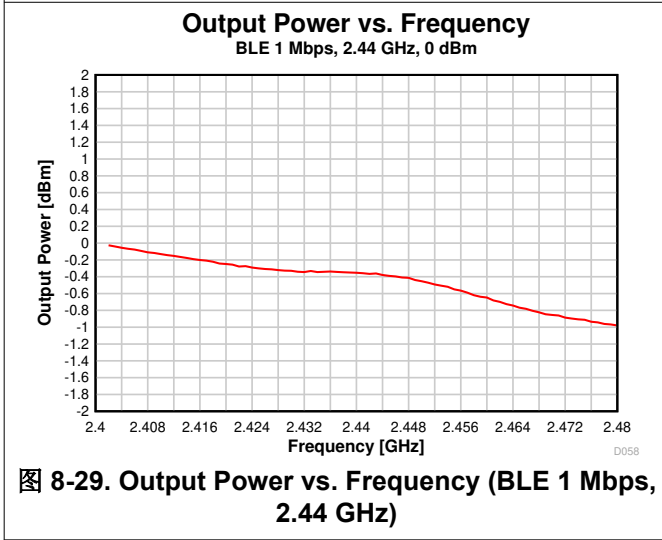
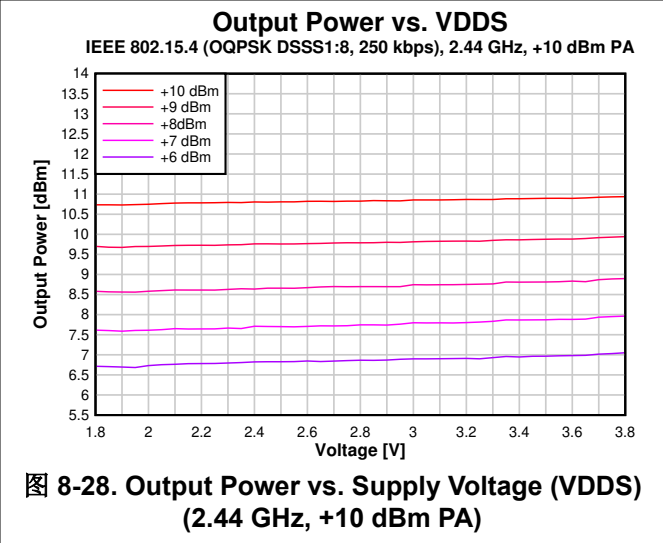
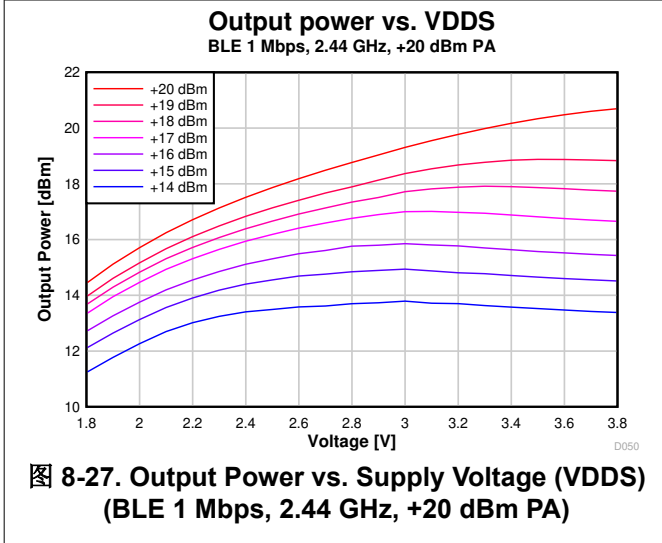


图 8-20. Sensitivity vs. Supply Voltage (VDD5) (250 kbps, 2.44 GHz)

8.16.5 TX Performance





8.16.6 ADC Performance

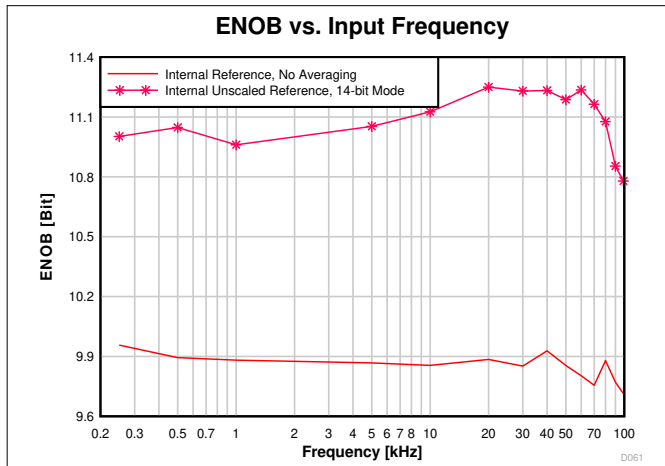


图 8-33. ENOB vs. Input Frequency

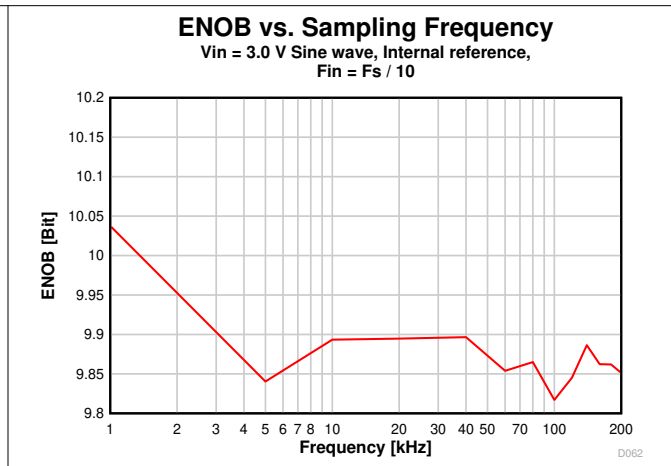


图 8-34. ENOB vs. Sampling Frequency

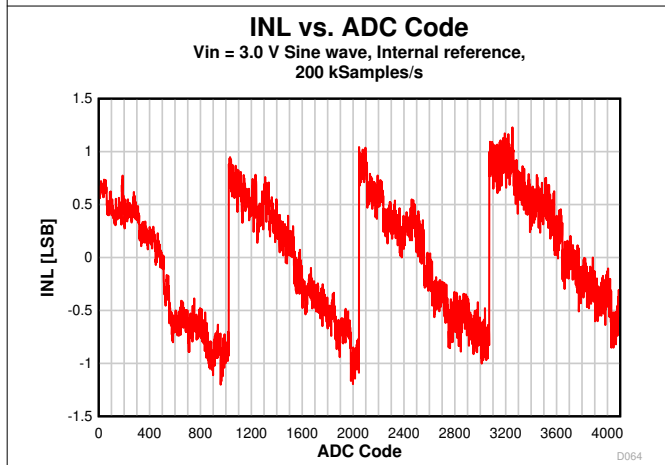


图 8-35. INL vs. ADC Code

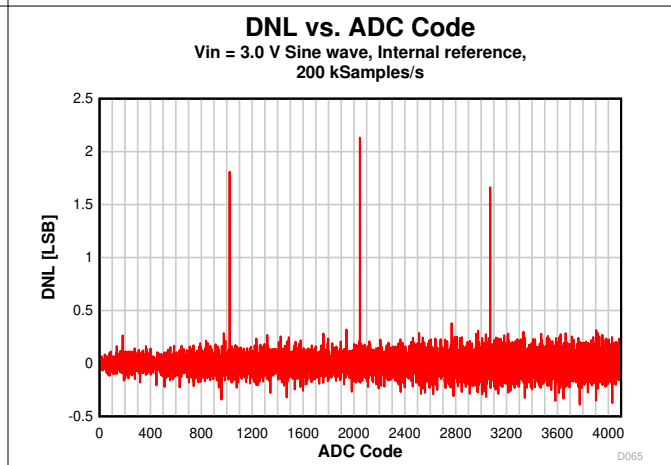


图 8-36. DNL vs. ADC Code

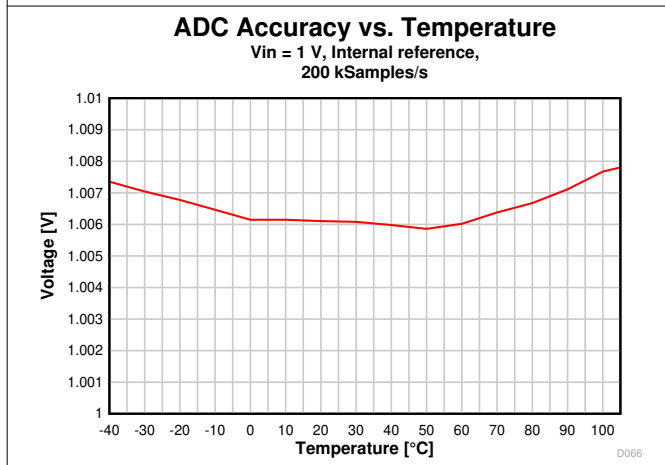


图 8-37. ADC Accuracy vs. Temperature

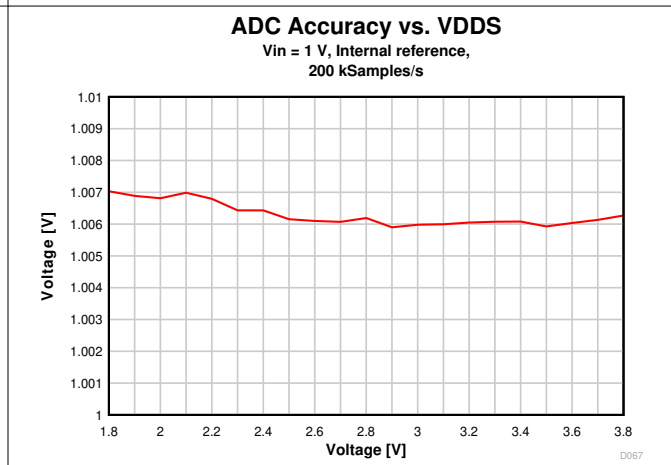


图 8-38. ADC Accuracy vs. Supply Voltage (VDD5)

9 Detailed Description

9.1 Overview

节 4 shows the core modules of the CC2651P3 device.

9.2 System CPU

The CC2651P3 SimpleLink™ Wireless MCU contains an Arm® Cortex®-M4 system CPU, which runs the application and the higher layers of radio protocol stacks.

The system CPU is the foundation of a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

Its features include the following:

- ARMv7-M architecture optimized for small-footprint embedded applications
- Arm Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit Arm core in a compact memory size
- Fast code execution permits increased sleep mode time
- Deterministic, high-performance interrupt handling for time-critical applications
- Single-cycle multiply instruction and hardware divide
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- Full debug with data matching for watchpoint generation
 - Data Watchpoint and Trace Unit (DWT)
 - JTAG Debug Access Port (DAP)
 - Flash Patch and Breakpoint Unit (FPB)
- Trace support reduces the number of pins required for debugging and tracing
 - Instrumentation Trace Macrocell Unit (ITM)
 - Trace Port Interface Unit (TPIU) with asynchronous serial wire output (SWO)
- Optimized for single-cycle flash memory access
- Tightly connected to 8-KB 4-way random replacement cache for minimal active power consumption and wait states
- Ultra-low-power consumption with integrated sleep modes
- 48 MHz operation
- 1.25 DMIPS per MHz

9.3 Radio (RF Core)

The RF Core is a highly flexible and future proof radio module which contains an Arm Cortex-M0 processor that interfaces the analog RF and base-band circuitry, handles data to and from the system CPU side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU that configurations and data are passed through. The Arm Cortex-M0 processor is not programmable by customers and is interfaced through the TI-provided RF driver that is included with the SimpleLink Software Development Kit (SDK).

The RF core can autonomously handle the time-critical aspects of the radio protocols, thus offloading the main CPU, which reduces power and leaves more resources for the user application. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

The various physical layer radio formats are partly built as a software defined radio where the radio behavior is either defined by radio ROM contents or by non-ROM radio formats delivered in form of firmware patches with the SimpleLink SDKs. This allows the radio platform to be updated for support of future versions of standards even with over-the-air (OTA) updates while still using the same silicon.

9.3.1 Bluetooth 5.2 Low Energy

The RF Core offers full support for Bluetooth 5.2 Low Energy, including the high-speed 2-Mbps physical layer and the 500-kbps and 125-kbps long range PHYs (Coded PHY) through the TI provided Bluetooth 5.2 stack or through a high-level Bluetooth API.

The new high-speed mode allows data transfers up to 2 Mbps, twice the speed of Bluetooth 4.2 and five times the speed of Bluetooth 4.0, without increasing power consumption. In addition to faster speeds, this mode offers significant improvements for energy efficiency and wireless coexistence with reduced radio communication time.

Bluetooth 5.2 also enables unparalleled flexibility for adjustment of speed and range based on application needs, which capitalizes on the high-speed or long-range modes respectively. Data transfers are now possible at 2 Mbps, enabling development of applications using voice, audio, imaging, and data logging that were not previously an option using Bluetooth low energy. With high-speed mode, existing applications deliver faster responses, richer engagement, and longer battery life. Bluetooth 5.2 enables fast, reliable firmware updates.

9.3.2 802.15.4 (Zigbee and 6LoWPAN)

Through a dedicated IEEE radio API, the RF Core supports the 2.4-GHz IEEE 802.15.4-2011 physical layer (2 Mcps per second Offset-QPSK with DSSS 1:8), used in Zigbee and 6LoWPAN protocols. TI provides royalty-free protocol stacks for Zigbee as part of the SimpleLink SDK, enabling a robust end-to-end solution.

9.4 Memory

The up to 352-KB nonvolatile (Flash) memory provides storage for code and data. The flash memory is in-system programmable and erasable. The last flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the `ccfg.c` source file that is included in all TI provided examples.

The ultra-low leakage system static RAM (SRAM) is a single 32-KB block and can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers.

To improve code execution speed and lower power when executing code from nonvolatile memory, a 4-way nonassociative 8-KB cache is enabled by default to cache and prefetch instructions read by the system CPU. The cache can be used as a general-purpose RAM by enabling this feature in the Customer Configuration Area (CCFG).

The ROM contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

9.5 Cryptography

The CC2651P3 device comes with a wide set of cryptography-related hardware accelerators, reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations run in a background hardware thread.

The hardware accelerator modules are:

- **True Random Number Generator (TRNG)** module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear-combinatorial circuit.
- **Advanced Encryption Standard (AES)** with 128 bit key lengths

Together with the hardware accelerator module, a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), this allows for secure and future proof IoT applications to be easily built on top of the platform. The TI provided cryptography drivers are:

- **Key Agreement Schemes**
 - Elliptic curve Diffie-Hellman with static or ephemeral keys (ECDH and ECDHE)
- **Signature Generation**
 - Elliptic curve Diffie-Hellman Digital Signature Algorithm (ECDSA)
- **Curve Support**
 - Short Weierstrass form (full hardware support), such as:
 - NIST-P256
 - Montgomery form (hardware support for multiplication), such as:
 - Curve25519
- **Hash**
 - SHA256
- **MACs**
 - HMAC with SHA256
 - AES CBC-MAC
- **Block ciphers**
 - AESECB
 - AESCBC
 - AESCTR
- **Authenticated Encryption**
 - AESCCM
- **Random number generation**
 - True Random Number Generator
 - AES CTR DRBG

9.6 Timers

A large selection of timers are available as part of the CC2651P3 device. These timers are:

- **Real-Time Clock (RTC)**

A 70-bit 3-channel timer running on the 32 kHz low frequency system clock (SCLK_LF)

This timer is available in all power modes except Shutdown. The timer can be calibrated to compensate for frequency drift when using the LF RCOSC as the low frequency system clock. If an external LF clock with frequency different from 32.768 kHz is used, the RTC tick speed can be adjusted to compensate for this. When using TI-RTOS, the RTC is used as the base timer in the operating system and should thus only be accessed through the kernel APIs such as the Clock module. By default, the RTC halts when a debugger halts the device.

- **General Purpose Timers (GPTIMER)**

The four flexible GPTIMERS can be used as either 4× 32 bit timers or 8× 16 bit timers, all running on up to 48 MHz. Each of the 16- or 32-bit timers support a wide range of features such as one-shot or periodic counting, pulse width modulation (PWM), time counting between edges and edge counting. The inputs and outputs of the timer are connected to the device event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA and ADC. The GPTIMERS are available in Active and Idle power modes.

- **Radio Timer**

A multichannel 32-bit timer running at 4 MHz is available as part of the device radio. The radio timer is typically used as the timing base in wireless network communication using the 32-bit timing word as the network time. The radio timer is synchronized with the RTC by using a dedicated radio API when the device radio is turned on or off. This ensures that for a network stack, the radio timer seems to always be running when the radio is enabled. The radio timer is in most cases used indirectly through the trigger time fields in the radio APIs and should only be used when running the accurate 48 MHz high frequency crystal is the source of SCLK_HF.

- **Watchdog timer**

The watchdog timer is used to regain control if the system operates incorrectly due to software errors. It is typically used to generate an interrupt to and reset of the device for the case where periodic monitoring of the system components and tasks fails to verify proper functionality. The watchdog timer runs on a 1.5 MHz clock rate and cannot be stopped once enabled. The watchdog timer pauses to run in Standby power mode and when a debugger halts the device.

9.7 Serial Peripherals and I/O

The SSI is a synchronous serial interface that is compatible with SPI, MICROWIRE, and TI's synchronous serial interfaces. The SSI support both SPI master and slave up to 4 MHz. The SSI module support configurable phase and polarity.

The UART implement universal asynchronous receiver and transmitter functions. It support flexible baud-rate generation up to a maximum of 3 Mbps.

The I²S interface is used to handle digital audio and can also be used to interface pulse-density modulation microphones (PDM).

The I²C interface is also used to communicate with devices compatible with the I²C standard. The I²C interface can handle 100 kHz and 400 kHz operation, and can serve as both master and slave.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high-drive capabilities, which are marked in **bold** in 节 7. All digital peripherals can be connected to any digital pin on the device.

For more information, see the [CC13x1x3, CC26x1x3 SimpleLink™ Wireless MCU Technical Reference Manual](#).

9.8 Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the CC2651P3 device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

9.9 μ DMA

The device includes a direct memory access (μ DMA) controller. The μ DMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The μ DMA controller can perform a transfer between memory and peripherals. The μ DMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

Some features of the μ DMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits
- Ping-pong mode for continuous streaming of data

9.10 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface. The device boots by default into cJTAG mode and must be reconfigured to use 4-pin JTAG.

9.11 Power Management

To minimize power consumption, the CC2651P3 supports a number of power modes and power management features (see [表 9-1](#)).

表 9-1. Power Modes

| MODE | SOFTWARE CONFIGURABLE POWER MODES | | | | RESET PIN HELD |
|-----------------------------------|-----------------------------------|---------------------|---------------------|-----------|----------------|
| | ACTIVE | IDLE | STANDBY | SHUTDOWN | |
| CPU | Active | Off | Off | Off | Off |
| Flash | On | Available | Off | Off | Off |
| SRAM | On | On | Retention | Off | Off |
| Supply System | On | On | Duty Cycled | Off | Off |
| Register and CPU retention | Full | Full | Partial | No | No |
| SRAM retention | Full | Full | Full | No | No |
| 48 MHz high-speed clock (SCLK_HF) | XOSC_HF or RCOSC_HF | XOSC_HF or RCOSC_HF | Off | Off | Off |
| 32 kHz low-speed clock (SCLK_LF) | XOSC_LF or RCOSC_LF | XOSC_LF or RCOSC_LF | XOSC_LF or RCOSC_LF | Off | Off |
| Peripherals | Available | Available | Off | Off | Off |
| Wake-up on RTC | Available | Available | Available | Off | Off |
| Wake-up on pin edge | Available | Available | Available | Available | Off |
| Wake-up on reset pin | On | On | On | On | On |
| Brownout detector (BOD) | On | On | Duty Cycled | Off | Off |
| Power-on reset (POR) | On | On | On | Off | Off |
| Watchdog timer (WDT) | Available | Available | Paused | Off | Off |

In **Active** mode, the application system CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see [表 9-1](#)).

In **Idle** mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event brings the processor back into active mode.

In **Standby** mode, only the always-on (AON) domain is active. An external wake-up event or RTC event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In **Shutdown** mode, the device is entirely turned off (including the AON domain), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the flash memory contents.

备注

The power, RF and clock management for the CC2651P3 device require specific configuration and handling by software for optimized performance. This configuration and handling is implemented in the TI-provided drivers that are part of the CC2651P3 software development kit (SDK). Therefore, TI highly recommends using this software framework for all application development on the device. The complete [SDK](#) with TI-RTOS (optional), device drivers, and examples are offered free of charge in source code.

9.12 Clock Systems

The CC2651P3 device has several internal system clocks.

The 48 MHz SCLK_HF is used as the main system (MCU and peripherals) clock. This can be driven by the internal 48 MHz RC Oscillator (RCOSC_HF) or an external 48 MHz crystal (XOSC_HF). Radio operation requires an external 48 MHz crystal.

SCLK_LF is the 32.768 kHz internal low-frequency system clock. It can be used for the RTC and to synchronize the radio timer before or after Standby power mode. SCLK_LF can be driven by the internal 32.8 kHz RC Oscillator (RCOSC_LF), a 32.768 kHz watch-type crystal, or a clock input on any digital IO.

When using a crystal or the internal RC oscillator, the device can output the 32 kHz SCLK_LF signal to other devices, thereby reducing the overall system cost.

9.13 Network Processor

Depending on the product configuration, the CC2651P3 device can function as a wireless network processor (WNP - a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC) with the application and protocol stack running on the system CPU inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

10 Application, Implementation, and Layout

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

For general design guidelines and hardware configuration guidelines, refer to [CC13xx/CC26xx Hardware Configuration and PCB Design Considerations Application Report](#).

For optimum RF performance, especially when using the high-power PA, it is important to accurately follow the reference design with respect to component values and layout. Failure to do so may lead to reduced RF performance due to balun mismatch. The amplitude- and phase balance through the balun must be <1 dB and <6 degrees, respectively.

PCB stack-up is also critical for proper operation. The CC2651P3 EVMs and characterization boards use a finished thickness between the top layer (RF signals) and layer 2 (ground plane) of 175 μm . It is very important to use the same substrate thickness, or slightly thicker, in an end product implementing the CC2651P3 device.

10.1 Reference Designs

The following reference designs should be followed closely when implementing designs using the CC2651P3 device.

Special attention must be paid to RF component placement, decoupling capacitors and DCDC regulator components, as well as ground connections for all of these.

[CC26x1-P3EM-5XS24-PA24_10dBm Design Files](#)

The CC26x1PEM-5XS24-PA24_10dBm reference design provides schematic, layout and production files for the characterization board used for deriving the performance number found in this document. This design is optimized for operating the high power PA at 10 dBm output power and is using a single-ended front-end configuration with external LNA bias for RX.

[CC26x1-P3EM-7XD24-PA24 Design Files](#)

The CC26x1-P3EM-7XD24-PA24 reference design provides schematic, layout and production files for the characterization board used for deriving the performance number found in this document. This design is configured for 20 dBm operation on the high output power PA.

[LP-CC2651P3 Design Files](#)

The CC2651P3 LaunchPad Design Files contain detailed schematics and layouts to build application specific boards using the CC2651P3 device.

[Sub-1 GHz and 2.4 GHz Antenna Kit for LaunchPad™ Development Kit and SensorTag](#)

The antenna kit allows real-life testing to identify the optimal antenna for your application. The antenna kit includes 16 antennas for frequencies from 169 MHz to 2.4 GHz, including:

- PCB antennas
- Helical antennas
- Chip antennas
- Dual-band antennas for 868 MHz and 915 MHz combined with 2.4 GHz

The antenna kit includes a JSC cable to connect to the Wireless MCU LaunchPad Development Kits and SensorTags.

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed as follows.

11.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and/or date-code. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, XCC2651P3 is in preview; therefore, an X prefix/identification is assigned).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

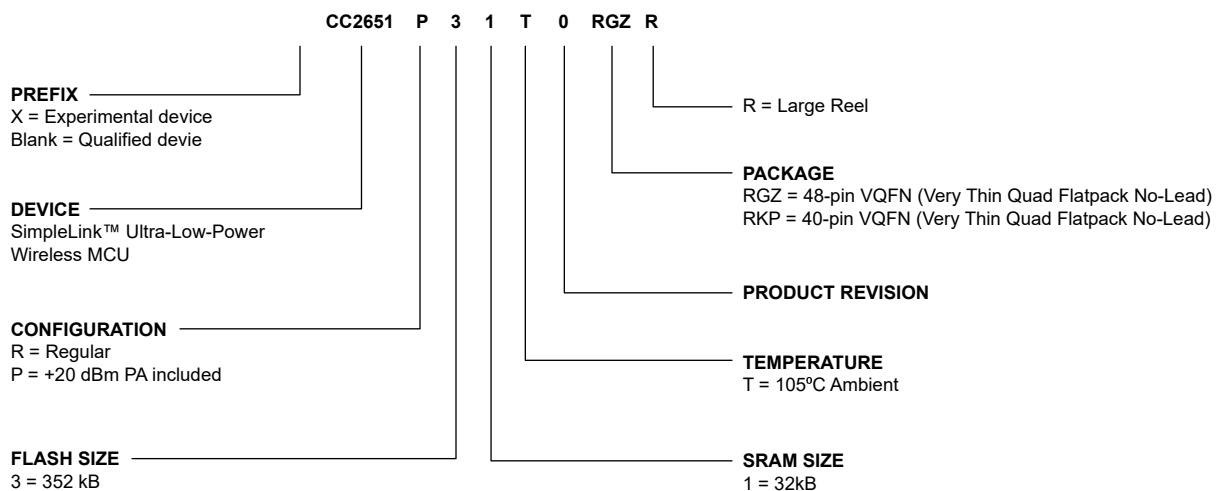
"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, RGZ).

For orderable part numbers of CC2651P3 devices in the RGZ (7-mm x 7-mm) package type, see the *Package Option Addendum* of this document, the Device Information in [§ 3](#), the TI website (www.ti.com), or contact your TI sales representative.



11-1. Device Nomenclature

11.2 Tools and Software

The CC2651P3 device is supported by a variety of software and hardware development tools.

Development Kit

[CC2651P3 LaunchPad™ Development Kit](#)

The CC2651P3 LaunchPad™ Development Kit enables development of high-performance wireless applications that benefit from low-power operation. The kit features the CC2651P3 SimpleLink Wireless MCU, which allows you to quickly evaluate and prototype 2.4-GHz wireless applications such as Bluetooth 5 Low Energy, Zigbee and Thread, plus combinations of these. The kit works with the LaunchPad ecosystem, easily enabling additional functionality like sensors, display and more.

Software

[SimpleLink™ CC13XX- CC26XX SDK](#)

The SimpleLink CC13xx and CC26xx Software Development Kit (SDK) provides a complete package for the development of wireless applications on the CC13XX / CC26XX family of devices. The SDK includes a comprehensive software package for the CC2651P3 device, including the following protocol stacks:

- Bluetooth Low Energy 4 and 5.2
- Thread (based on OpenThread)
- Zigbee 3.0
- Wi-SUN®
- TI 15.4-Stack - an IEEE 802.15.4-based star networking solution for Sub-1 GHz and 2.4 GHz
- Proprietary RF - a large set of building blocks for building proprietary RF software
- Multiprotocol support - concurrent operation between stacks using the Dynamic Multiprotocol Manager (DMM)

The SimpleLink CC13XX-CC26XX SDK is part of TI' s SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit <http://www.ti.com/simplelink>.

Development Tools

Code Composer Studio™ Integrated Development Environment (IDE)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse® software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

CCS has support for all SimpleLink Wireless MCUs and includes support for EnergyTrace™ software (application energy usage profiling). A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK.

Code Composer Studio is provided free of charge when used in conjunction with the XDS debuggers included on a LaunchPad Development Kit.

Code Composer Studio™ Cloud IDE

Code Composer Studio (CCS) Cloud is a web-based IDE that allows you to create, edit and build CCS and Energia™ projects. After you have successfully built your project, you can download and run on your connected LaunchPad. Basic debugging, including features like setting breakpoints and viewing variable values is now supported with CCS Cloud.

IAR Embedded Workbench® for Arm®

IAR Embedded Workbench® is a set of development tools for building and debugging embedded system applications using assembler, C and C++. It provides a completely integrated development environment that includes a project manager, editor, and build tools. IAR has support for all SimpleLink Wireless MCUs. It offers broad debugger support, including XDS110, IAR I-jet™ and Segger J-Link™. A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK. IAR is also supported out-of-the-box on most software examples provided as part of the SimpleLink SDK.

A 30-day evaluation or a 32 KB size-limited version is available through iar.com.

SmartRF™ Studio

SmartRF™ Studio is a Windows® application that can be used to evaluate and configure SimpleLink Wireless MCUs from Texas Instruments. The application will help designers of RF systems to easily evaluate the radio at an early stage in the design process. It is especially useful for generation of configuration register values and for practical testing and debugging of the RF system. SmartRF Studio can be used either as a standalone application or together with applicable evaluation boards or debug probes for the RF device. Features of the SmartRF Studio include:

- Link tests - send and receive packets between nodes
- Antenna and radiation tests - set the radio in continuous wave TX and RX states
- Export radio configuration code for use with the TI SimpleLink SDK RF driver
- Custom GPIO configuration for signaling and control of external switches

CCS UniFlash

CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

11.2.1 SimpleLink™ Microcontroller Platform

The SimpleLink microcontroller platform sets a new standard for developers with the broadest portfolio of wired and wireless Arm® MCUs (System-on-Chip) in a single software development environment. Delivering flexible hardware, software and tool options for your IoT applications. Invest once in the SimpleLink software development kit and use throughout your entire portfolio. Learn more on ti.com/simplelink.

11.3 Documentation Support

To receive notification of documentation updates on data sheets, errata, application notes and similar, navigate to the device product folder on ti.com/product/CC2651P3. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the MCU, related peripherals, and other technical collateral is listed as follows.

TI Resource Explorer

[TI Resource Explorer](#) Software examples, libraries, executables, and documentation are available for your device and development board.

Errata

[CC2651P3 Silicon Errata](#) The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device and description on how to recognize a device revision.

Application Reports

All application reports for the CC2651P3 device are found on the device product folder at: ti.com/product/CC2651P3/#tech-docs.

Technical Reference Manual (TRM)

[CC13x1x, CC26x1x SimpleLink™ Wireless MCU TRM](#) The TRM provides a detailed description of all modules and peripherals available in the device family.

11.4 支持资源

[TI E2E™ 支持论坛](#)是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

11.5 Trademarks

SimpleLink™, LaunchPad™, Code Composer Studio™, EnergyTrace™, and TI E2E™ are trademarks of Texas Instruments.

I-jet™ is a trademark of IAR Systems AB.

J-Link™ is a trademark of SEGGER Microcontroller Systeme GmbH.

Arm® and Cortex® are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

CoreMark® is a registered trademark of Embedded Microprocessor Benchmark Consortium Corporation.

Zigbee® is a registered trademark of Zigbee Alliance Inc.

Bluetooth® is a registered trademark of Bluetooth SIG Inc.

Arm Thumb® is a registered trademark of Arm Limited (or its subsidiaries).

Wi-SUN® is a registered trademark of Wi-SUN Alliance Inc.

Eclipse® is a registered trademark of Eclipse Foundation.

IAR Embedded Workbench® is a registered trademark of IAR Systems AB.

Windows® is a registered trademark of Microsoft Corporation.

所有商标均为其各自所有者的财产。

11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| CC2651P31T0RGZR | Active | Production | VQFN (RGZ) 48 | 2500 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | CC2651 P31 |
| CC2651P31T0RGZR.A | Active | Production | VQFN (RGZ) 48 | 2500 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | CC2651 P31 |
| CC2651P31T0RGZR.B | Active | Production | VQFN (RGZ) 48 | 2500 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | CC2651 P31 |
| CC2651P31T0RKPR | Active | Production | VQFN (RKP) 40 | 3000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | CC2651 P31 |
| CC2651P31T0RKPR.A | Active | Production | VQFN (RKP) 40 | 3000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | CC2651 P31 |
| CC2651P31T0RKPR.B | Active | Production | VQFN (RKP) 40 | 3000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | CC2651 P31 |
| CC2651P31T0RKPRG4 | Active | Production | VQFN (RKP) 40 | 3000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | CC2651 P31 |
| CC2651P31T0RKPRG4.A | Active | Production | VQFN (RKP) 40 | 3000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | CC2651 P31 |
| CC2651P31T0RKPRG4.B | Active | Production | VQFN (RKP) 40 | 3000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | CC2651 P31 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

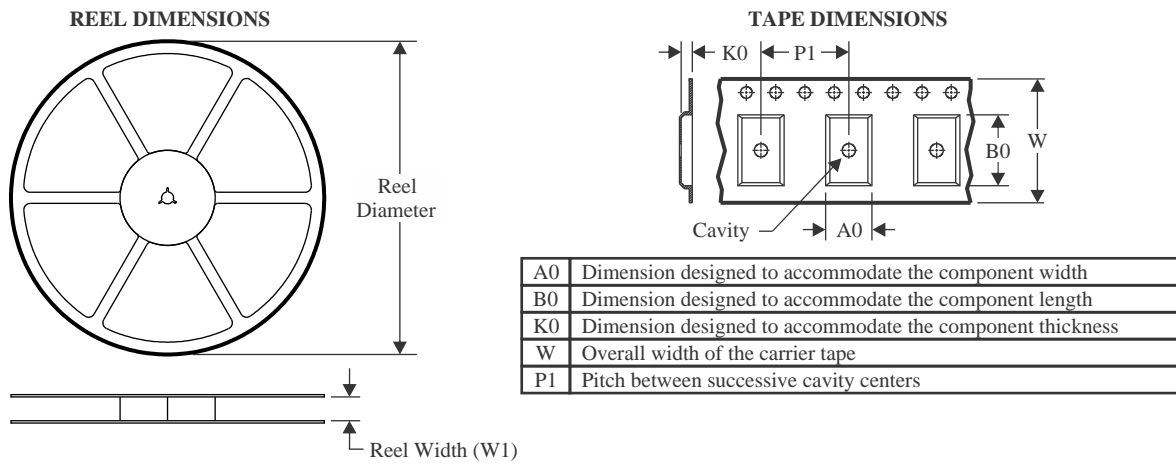
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CC2651P31T0RGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| CC2651P31T0RGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| CC2651P31T0RKPR | VQFN | RKP | 40 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| CC2651P31T0RKPR | VQFN | RKP | 40 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| CC2651P31T0RKPRG4 | VQFN | RKP | 40 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CC2651P31T0RGZR | VQFN | RGZ | 48 | 2500 | 360.0 | 360.0 | 36.0 |
| CC2651P31T0RGZR | VQFN | RGZ | 48 | 2500 | 367.0 | 367.0 | 35.0 |
| CC2651P31T0RKPR | VQFN | RKP | 40 | 3000 | 360.0 | 360.0 | 36.0 |
| CC2651P31T0RKPR | VQFN | RKP | 40 | 3000 | 367.0 | 367.0 | 35.0 |
| CC2651P31T0RKPRG4 | VQFN | RKP | 40 | 3000 | 367.0 | 367.0 | 35.0 |

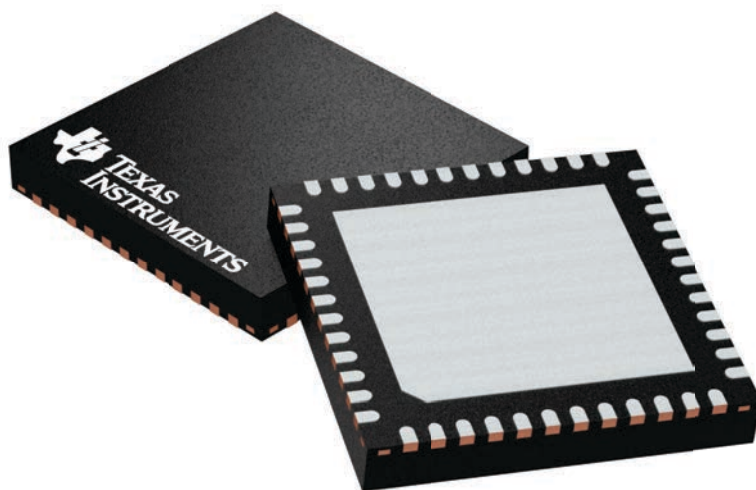
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

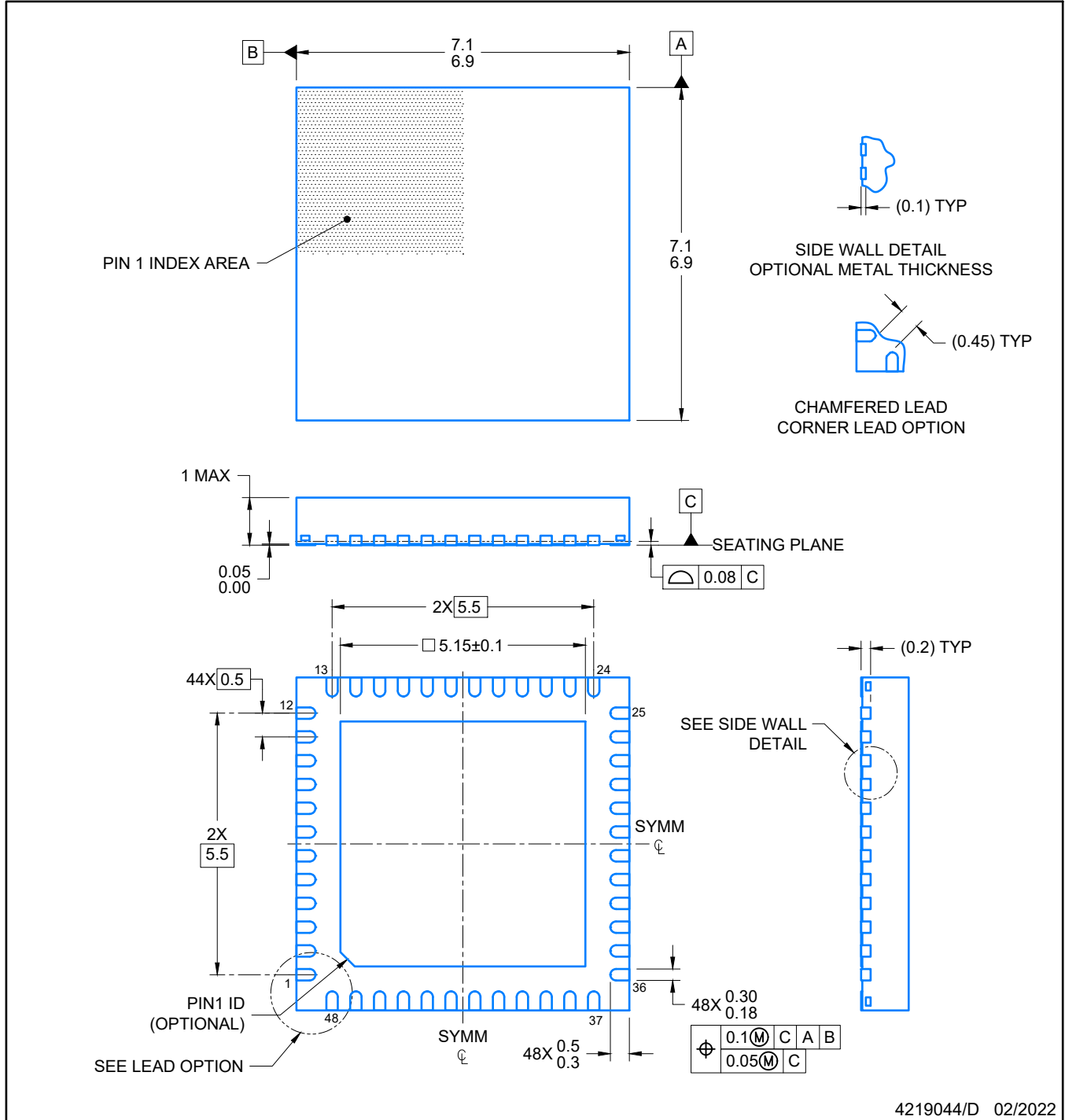
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A



NOTES:

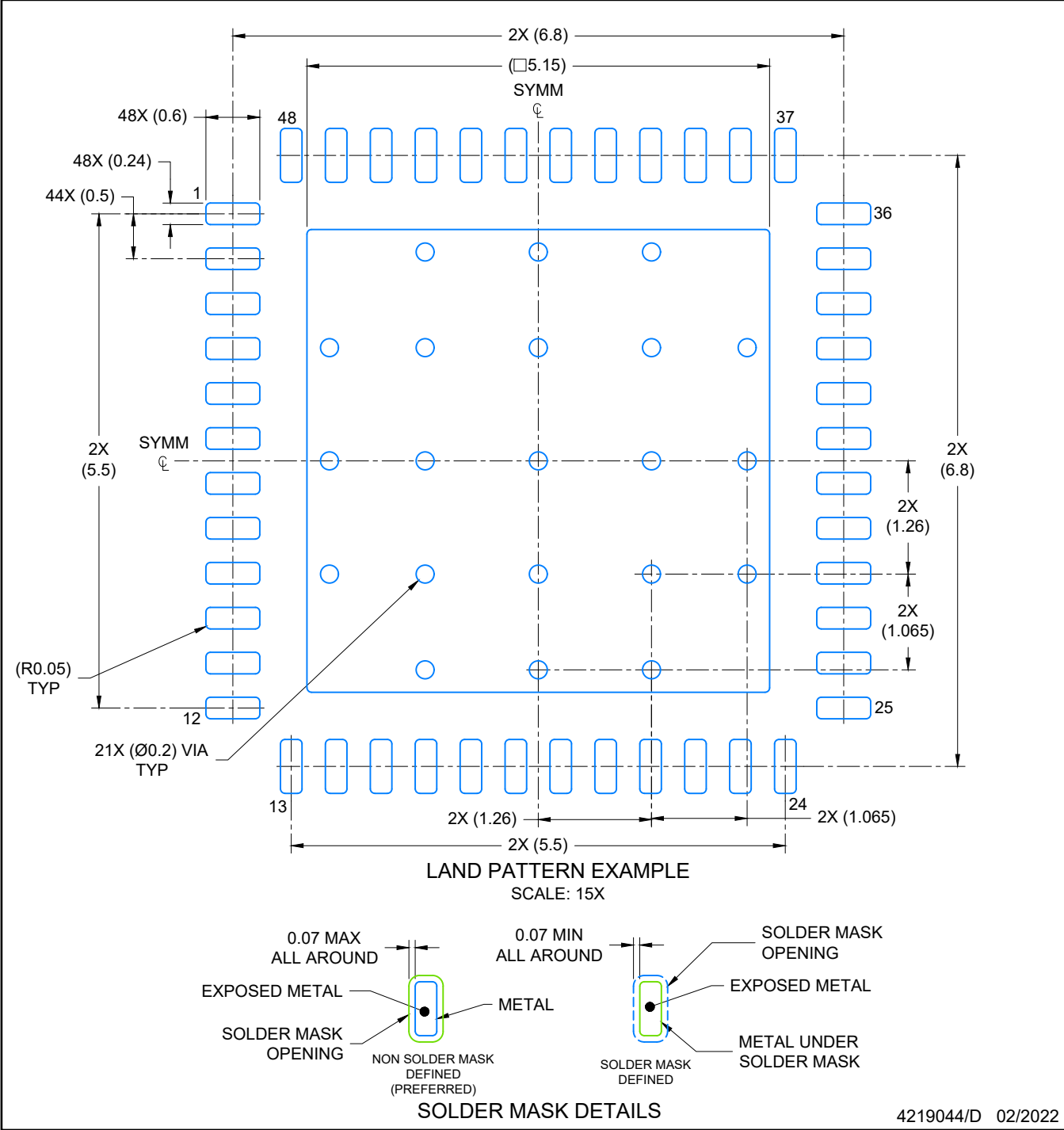
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RGZ0048A

VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD



NOTES: (continued)

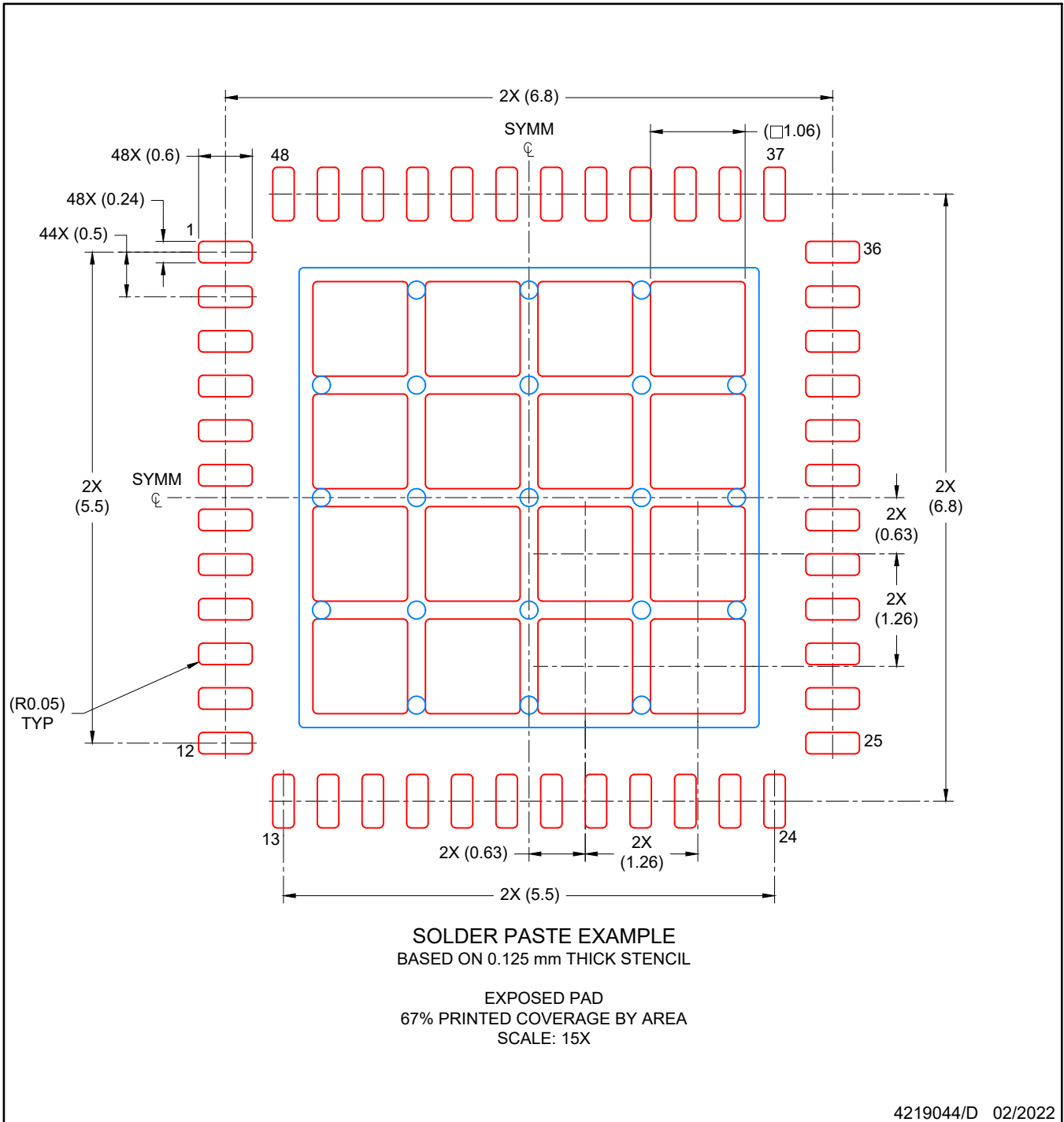
- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGZ0048A

VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

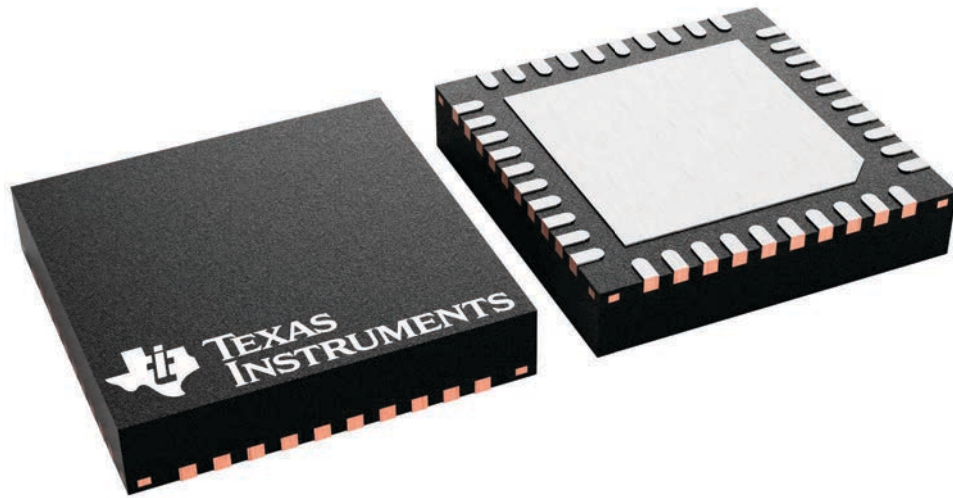
RKP 40

VQFN - 1 mm max height

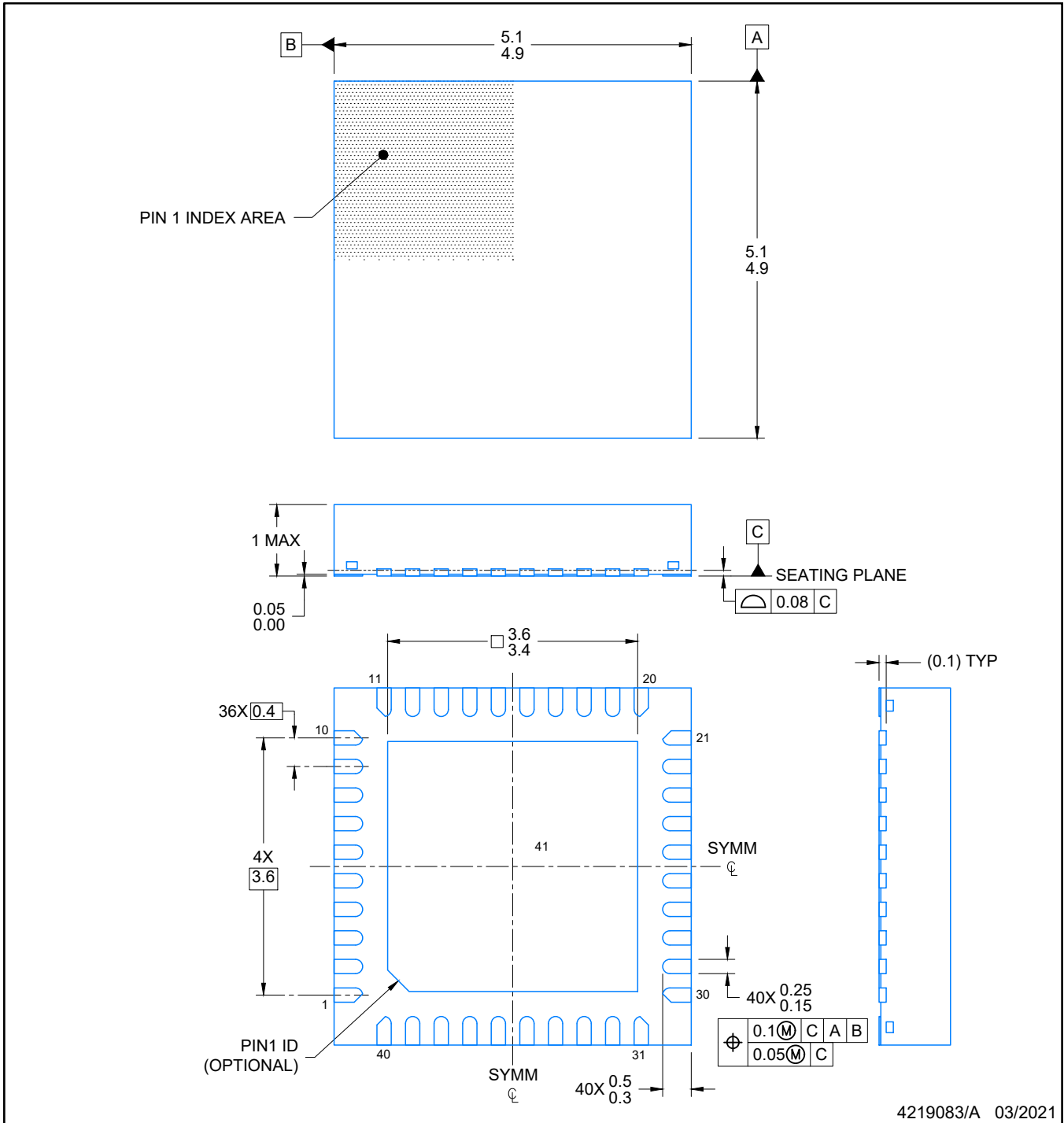
5 x 5, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229305/A



NOTES:

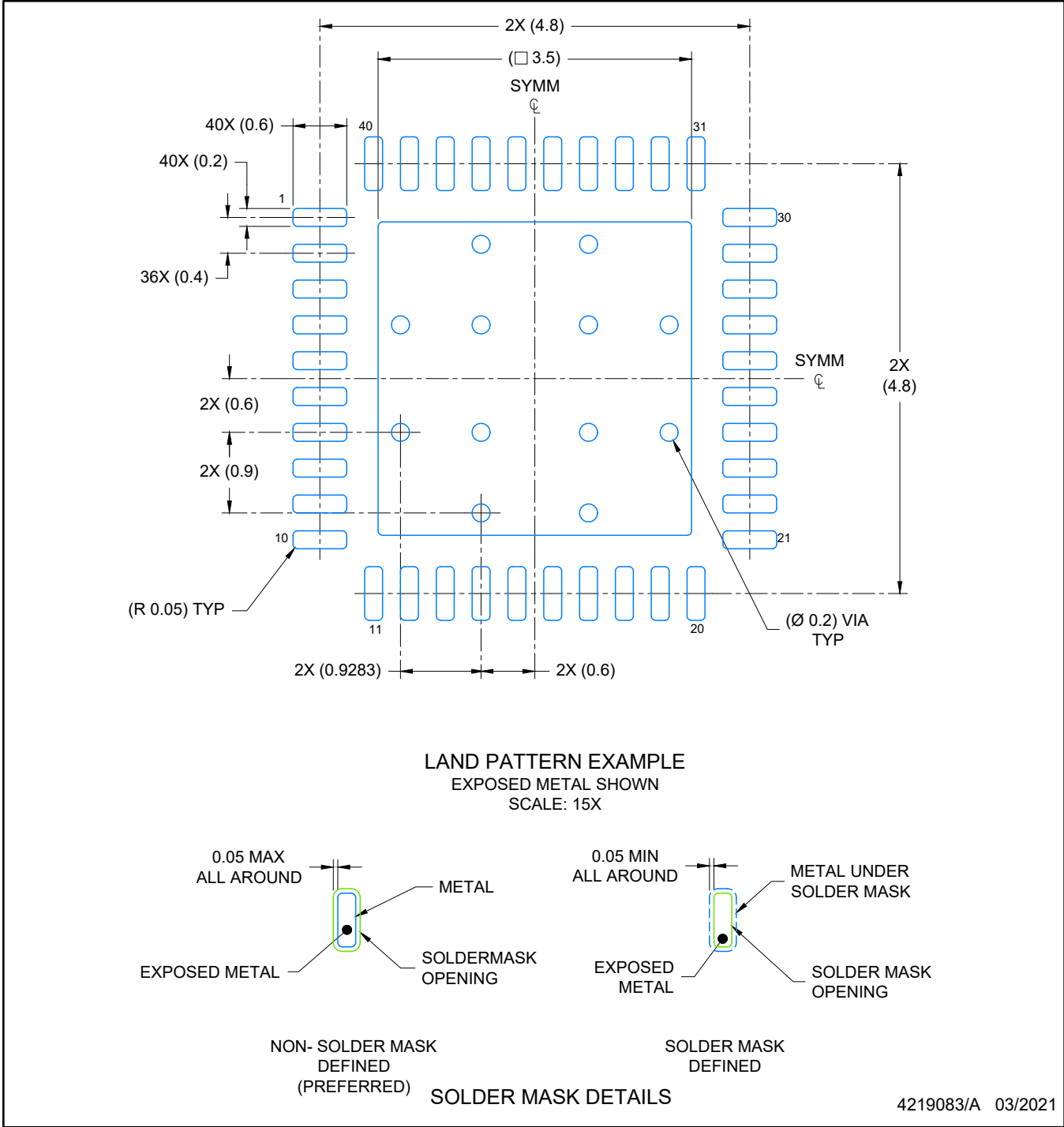
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

VQFN - 1 mm max height

RKP0040B

PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月