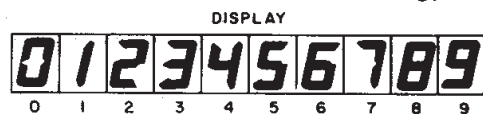


CD40110B Types

CMOS Decade Up-Down Counter/Latch/Display Driver

High-Voltage Type (20-V Rating)



Features:

- Separate clock-up and clock-down lines-
- Capable of driving common cathode LEDs and other displays directly
- Allows cascading without any external circuitry
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25° C

■ CD40110B is a dual-clocked up/down counter with a special preconditioning circuit that allows the counter to be clocked, via positive going inputs, up or down regardless of the state or timing (within 100 ns typ.) of the other clock line.

The clock signal is fed into the control logic and Johnson counter after it is preconditioned. The outputs of the Johnson counter (which include anti-lock gating to avoid being locked at an illegal state) are fed into a latch. This data can be fed directly to the decoder through the latch or can be strobed to hold a particular count while the Johnson counter continues to be clocked. The decoder feeds a seven-segment bipolar output driver which can source up to 25 mA to drive LEDs and other displays such as low-voltage fluorescent and incandescent lamps.

A short duration negative-going pulse appears on the BORROW output when the count changes from 0 to 9 or the CARRY output when the count changes from 9 to 0. At the other times the BORROW and CARRY outputs are a logic 1.

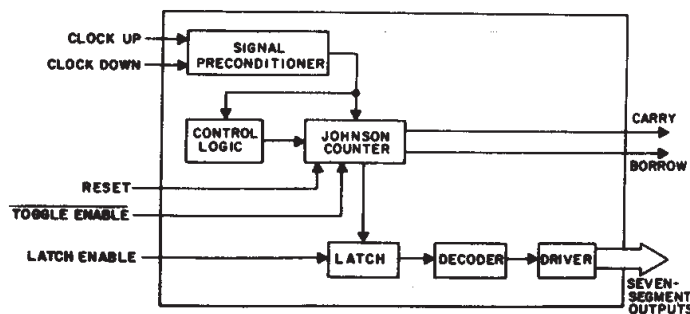
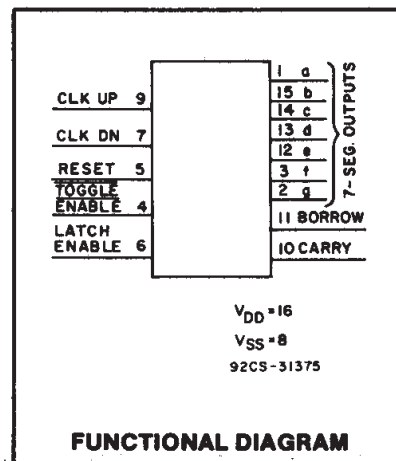
The CARRY and BORROW outputs can be tied directly to the clock-up and clock-down lines respectively of another CD40110B for easy cascading of several counters.

- Noise margin (full package-temperature range) =
1 V at $V_{DD} = 5$ V
2 V at $V_{DD} = 10$ V
2.5 V at $V_{DD} = 15$ V
- 5 V, 10 V and 15 V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices".

Applications:

- Rate comparators
- General counting applications where display is desired
- Up-down counting applications where input pulses are random in nature

The CD40110B types are supplied in 16-lead dual-in-line ceramic packages (D and F suffixes), and 16-lead dual-in-line plastic package (E suffix), and also available in chip form, (H suffix).



92CS-29200RI

Fig. 1 - Functional diagram.

CD40110B Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS

..... -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT

..... ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW

OPERATING-TEMPERATURE RANGE (T_A)

..... -55°C to $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg})

..... -65°C to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10s max $+265^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} V	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For $T_A = \text{Full Package Temperature Range}$)	—	3	18	V
Clock Input Frequency (Sum of CL_{UP} & CL_{DN} Freqs.) f_{CL}	5	—	1	MHz
	10	—	3	
	15	—	5	
Clock Pulse Width t_w	5	110	—	ns
	10	40	—	
	15	30	—	
Latch Enable Pulse Width	5	110	—	
	10	30	—	
	15	24	—	
Reset Removal-Time	5	550	—	
	10	200	—	
	15	130	—	
Reset Pulse Width	5	350	—	
	10	170	—	
	15	120	—	

CD40110B Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions				LIMITS AT INDICATED TEMPERATURES (°C)							Units
	I _{OH} (mA)	V _{OH} (V)	V _{IN} (V)	V _{DD} (V)					+25			
					-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current Max. I _{DD}	—	—	—	5	5	5	150	150	—	0.04	5	μA
	—	—	—	10	10	10	300	300	—	0.04	10	
	—	—	—	15	20	20	600	600	—	0.04	20	
	—	—	—	20	100	100	3000	3000	—	0.08	100	
Output Voltage Low-Level Max. V _{OL}	—	—	0.5	5	0.05				—	0	0.05	V
	—	—	0.10	10	0.05				—	0	0.05	
	—	—	0.15	15	0.05				—	0	0.05	
High-Level Min. V _{OH}	—	—	0.5	5	—	—	—	—	—	4.55	—	V
	—	—	0.10	10	—	—	—	—	—	9.55	—	
	—	—	0.15	15	—	—	—	—	—	14.55	—	
Input Low Voltage Max. V _{IL}	—	0.5, 3.8	—	5	1.5				—	—	1.5	V
	—	1, 8.8	—	10	3				—	—	3	
	—	1.5, 13.8	—	15	4				—	—	4	
Input High Voltage Min. V _{IH}	—	0.5, 3.8	—	5	3.8				3.5	—	—	V
	—	1, 8.8	—	10	7				7	—	—	
	—	1.5, 13.8	—	15	11				11	—	—	
7-Segment Outputs Output Drive Voltage, High Min. V _{OH}	■	—	—	5	3.9		4		3.9	4.5	—	V
	-5	—	—		3.65		3.7		3.7	4.3	—	
	-10	—	—		3.55		3.65		3.65	4.25	—	
	-15	—	—		3.5		3.5		3.6	4.15	—	
	-20	—	—		3.45		3.35		3.45	4	—	
	-25	—	—		3.4		3.3		3.4	3.9	—	
	■	—	—	10	8.75		8.85		8.75	9.5	—	
	-5	—	—		8.45		8.55		8.55	9.3	—	
	-10	—	—		8.42		8.5		8.5	9.25	—	
	-15	—	—		8.4		8.47		8.47	9.2	—	
	-20	—	—		8.4		8.40		8.45	9.1	—	
	-25	—	—		8.3		8.25		8.3	9	—	
	■	—	—	15	13.8		13.9		13.8	14.5	—	
	-5	—	—		13.65		13.75		13.75	14.35	—	
	-10	—	—		13.6		13.72		13.72	14.3	—	
	-15	—	—		13.6		13.7		13.7	14.2	—	
	-20	—	—		13.6		13.6		13.65	14.1	—	
	-25	—	—		13.3		13.25		13.3	14.0	—	
7-Segment Outputs Output Low (Sink) Current Min. I _{OL}	—	0.4	0.5	5	1.28	1.22	0.84	0.72	1	2	—	mA
	—	0.5	0.10	10	3.2	3	2.2	1.8	2.6	5.2	—	
	—	1.5	0.15	15	8.4	8	5.6	4.8	6.8	13.6	—	
Carry Outputs Output Low (Sink) Current Min. I _{OL}	—	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	—	
	—	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	—	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current Min. I _{OH}	—	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	
	—	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	—	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	—	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Input Current Max. I _{IN}	—	0.18	0.18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA

■ 0(10 μA)

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD40110B Types

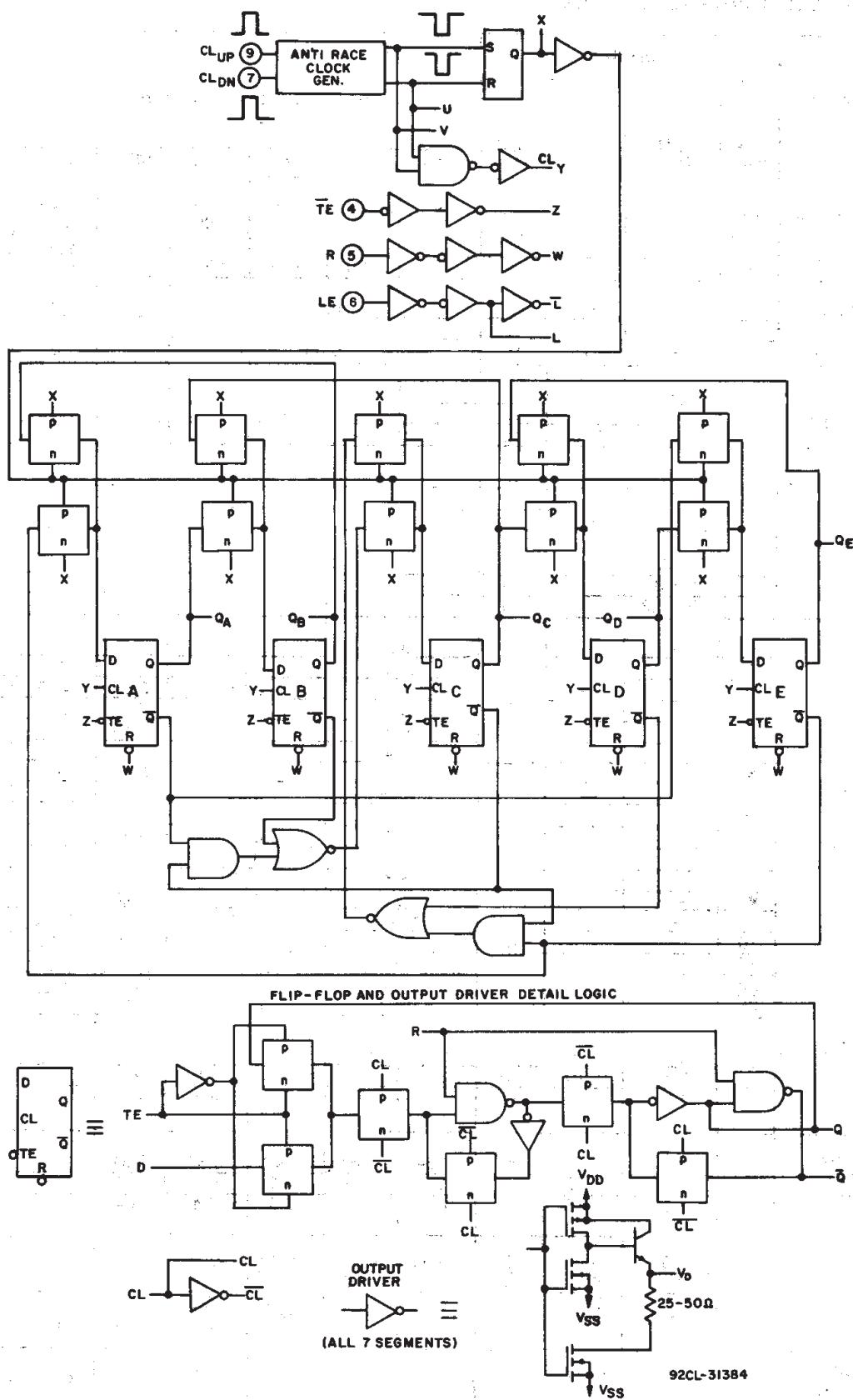
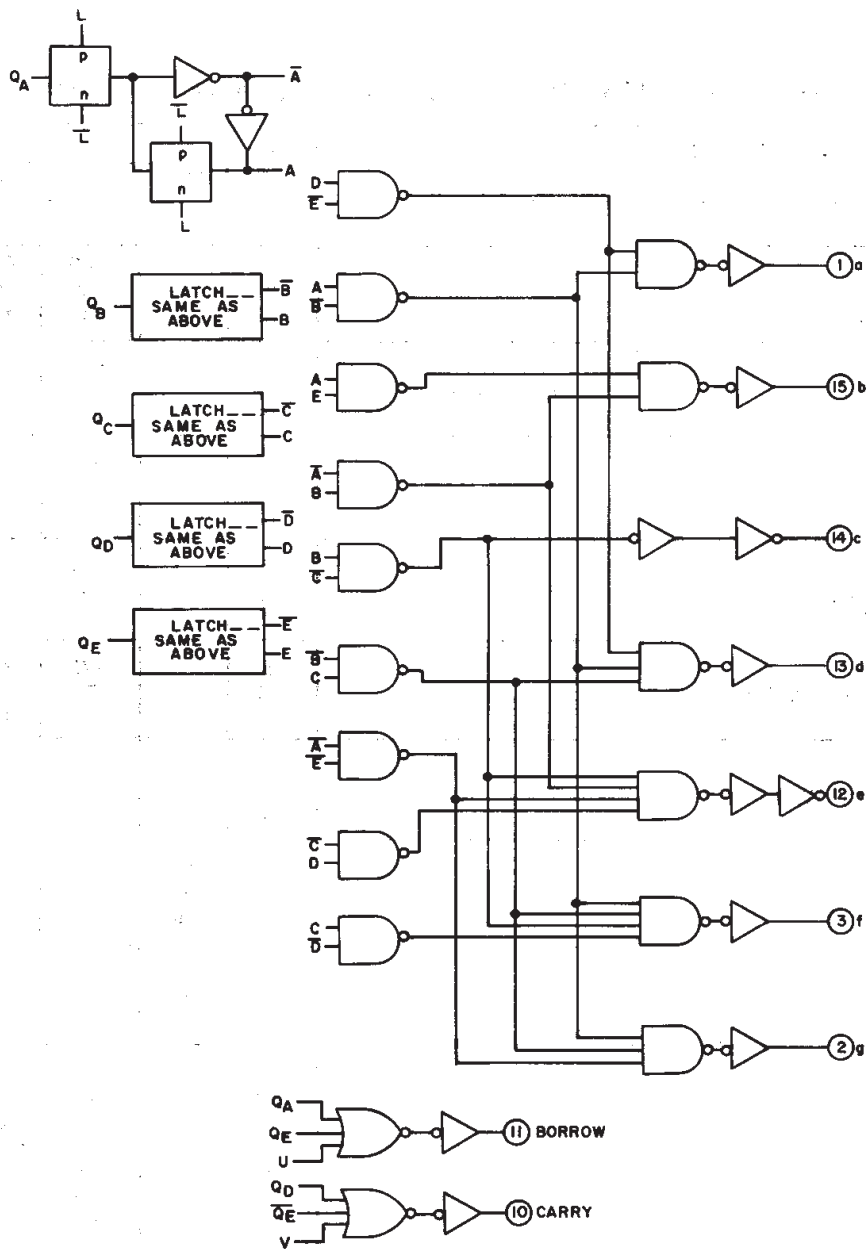


Fig. 2 - Logic diagram with flip-flop and output-driver details.
(cont'd on page 5)

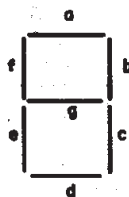
CD40110B Types



92CL-31384

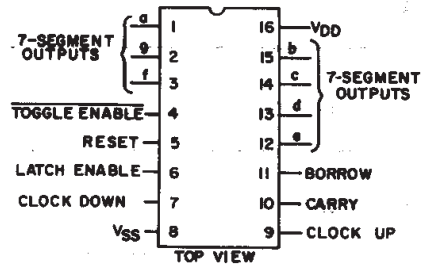
Fig. 2 - Logic diagram with flip-flop and output-driver details.

DISPLAY SEGMENTS



92CS-31376

TERMINAL ASSIGNMENT



92CS-31377

CD40110B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	V _{DD} (V)	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Clock Up/Clock Down					
Propagation Delay Time: Clock to Carry or Borrow t_{PLH}, t_{PHL}	5	—	300	600	ns
	10	—	100	200	
	15	—	70	140	
Clock to Segment t_{PLH}, t_{PHL}	5	—	925	1850	
	10	—	360	720	
	15	—	250	500	
Minimum Clock Pulse Width	5	—	55	110	
	10	—	20	40	
	15	—	15	30	
Maximum Clock Input Frequency (Sum of CL _{UP} & CL _{DN} F) f_{CL}	5	1	2.5	—	MHz
	10	3	6	—	
	15	5	8.5	—	
Minimum Toggle Enable Pulse Width	5	—	175	350	ns
	10	—	75	150	
	15	—	55	110	
Minimum Latch Enable Pulse Width	5	—	55	110	
	10	—	15	30	
	15	—	12	24	
Output Pulse Width: Carry	5	115	230	—	
	10	60	120	—	
	15	40	75	—	
Borrow	5	140	275	—	
	10	65	130	—	
	15	45	85	—	
Transition Time: Carry or Borrow t_{TLH}, t_{THL}	5	—	85	170	
	10	—	45	90	
	15	—	30	60	
Minimum Delay Time Between CL _{UP} & CL _{DN}	5	—	100	—	
	10	—	80	—	
	15	—	60	—	
Maximum Clock Rise or Fall Time t_{rCL}, t_{fCL}	5	—	—	15	μs
	10	—	—	15	
	15	—	—	15	
Reset					
Propagation Delay Time Reset to Output t_{PLH}, t_{PHL}	5	—	650	1300	ns
	10	—	350	700	
	15	—	160	320	
Minimum Reset Removal Time	5	—	-275	0	
	10	—	-100	0	
	15	—	-65	0	
Minimum Reset Pulse Width	5	—	175	350	
	10	—	85	170	
	15	—	60	120	

CD40110B Types

TRUTH TABLE

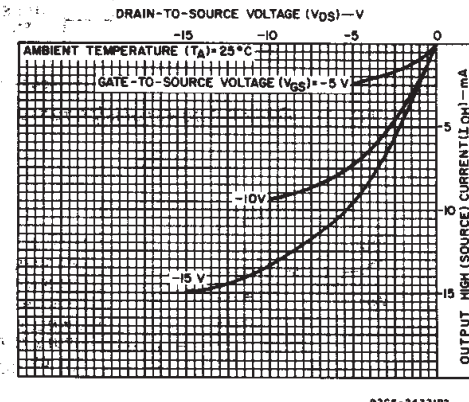
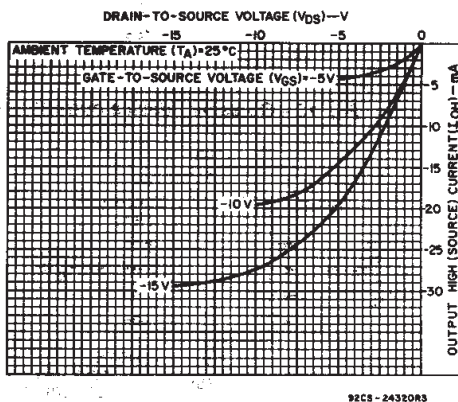
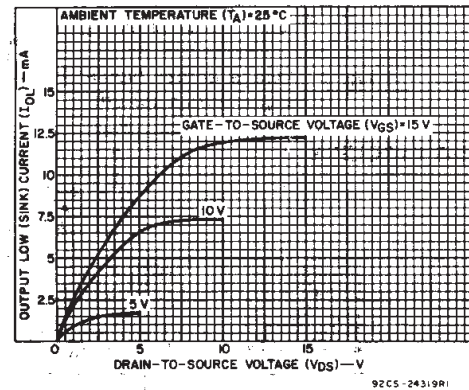
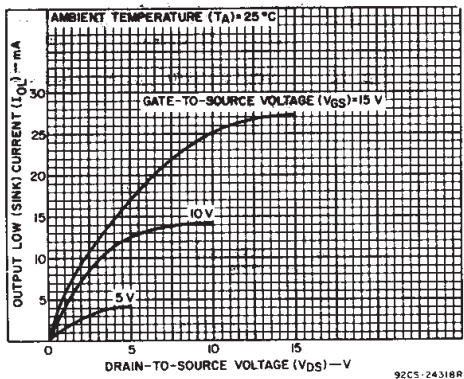
CLOCK UP *	CLOCK DOWN *	LATCH ENABLE	TOGGLE ENABLE	RESET	COUNTER	DISPLAY
	X	0	0	0	Increments by 1	Follows Counter
X		0	0	0	Decrements by 1	Follows Counter
		X	X	0	No Change	No Change
X	X	1	X	1	Goes to 00000	Remains Fixed
X	X	0	X	1	Goes to 00000	Follows Counter (Display = )
X	X	X	1	0	Inhibited	Remains Fixed
	X	1	0	0	Increments by 1	Remains Fixed
X		1	0	0	Decrements by 1	Remains Fixed

X = Don't Care

1 = High State

0 = Low State

* Typically 100 ns between clock-up and clock-down positive transitions are required to ensure proper counting.



CD40110B Types

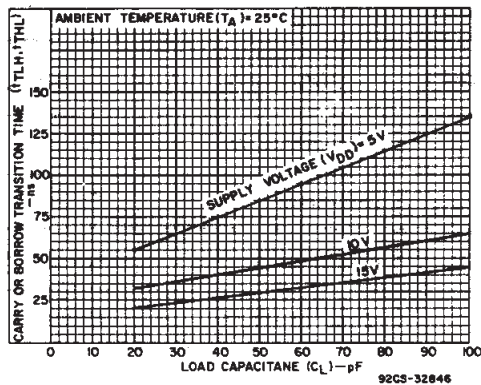


Fig. 7 - Typical carry or borrow transition time vs. load capacitance.

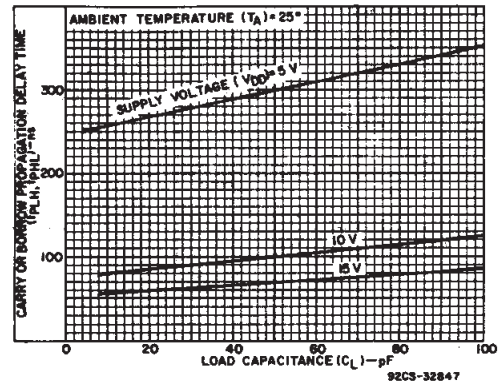


Fig. 8 - Typical carry or borrow propagation delay time vs. load capacitance.

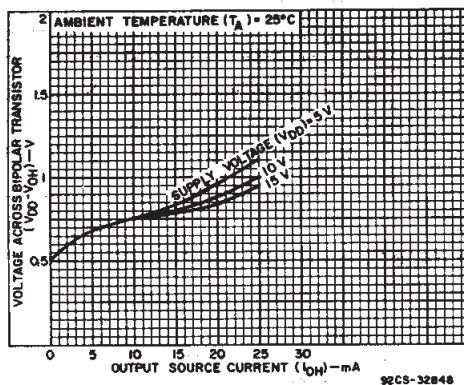


Fig. 9 - Voltage across bipolar transistor vs. output source current.

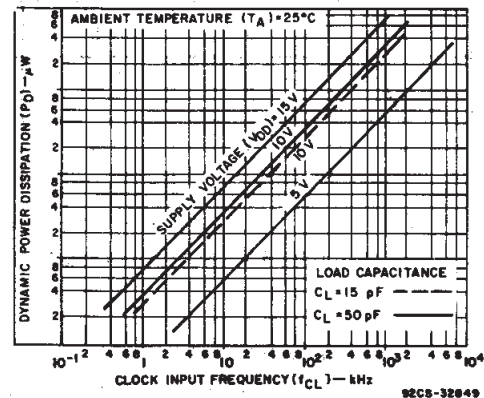


Fig. 10 - Typical dynamic power dissipation vs. frequency.

TEST CIRCUITS

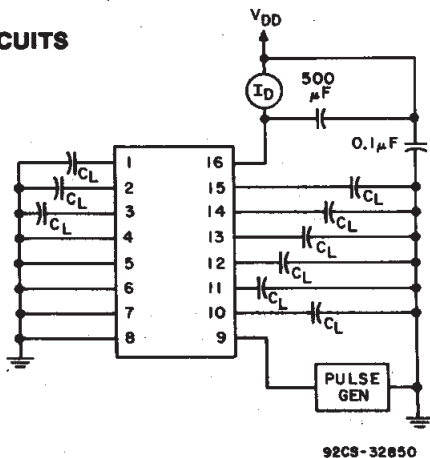


Fig. 11 - Dynamic power dissipation test circuit.

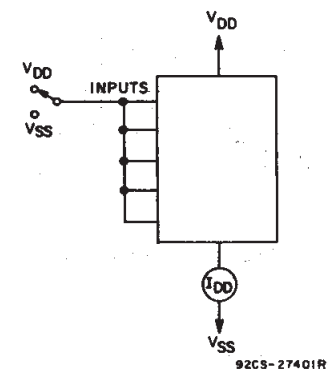


Fig. 12 - Quiescent device current.

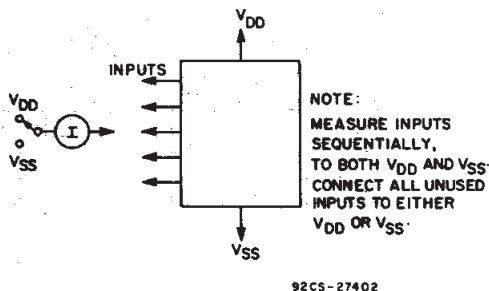


Fig. 13 - Input current.

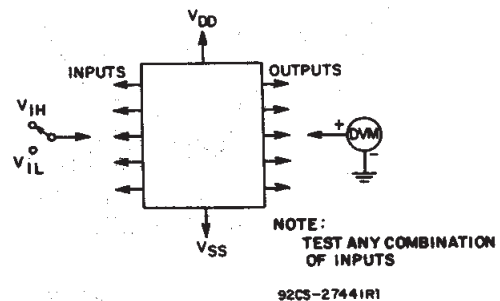


Fig. 14 - Input voltage.

CD40110B Types

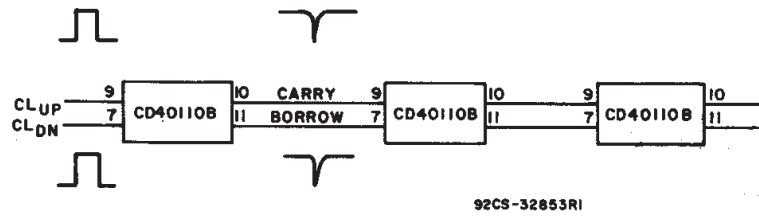
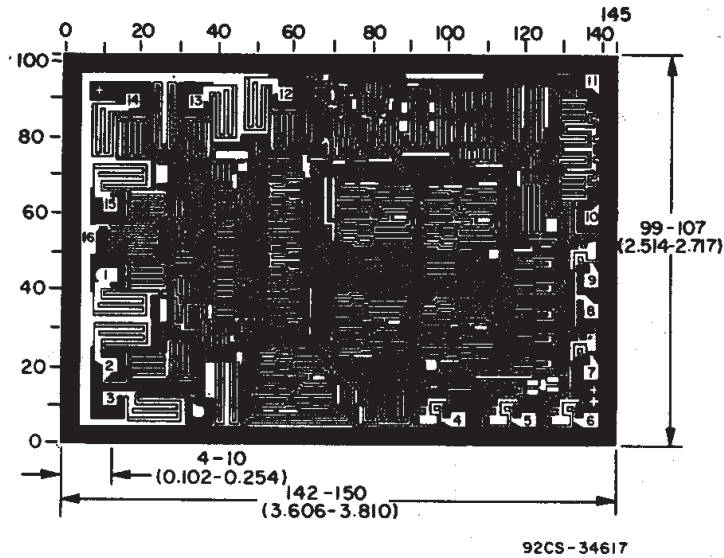


Fig. 15 - Cascading diagram.



Dimensions and pad layout for CD40110B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD40110BE	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD40110BE
CD40110BE.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD40110BE

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE



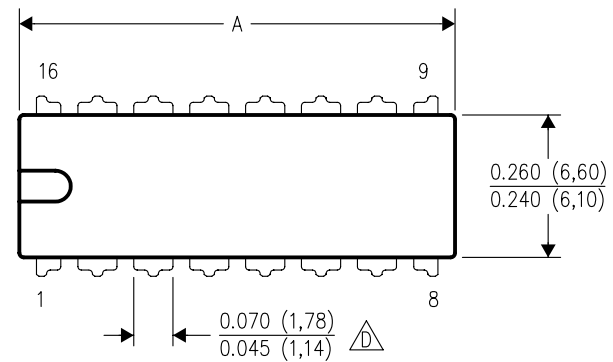
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD40110BE	N	PDIP	16	25	506	13.97	11230	4.32
CD40110BE	N	PDIP	16	25	506	13.97	11230	4.32
CD40110BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD40110BE.A	N	PDIP	16	25	506	13.97	11230	4.32

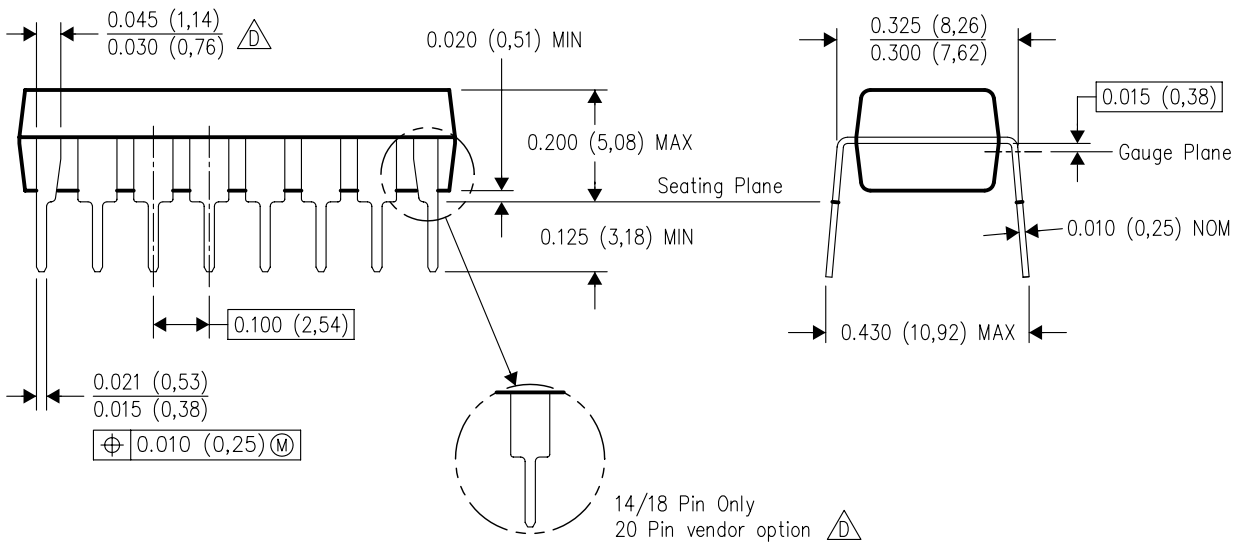
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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