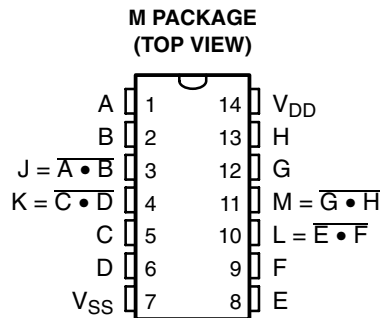


CD4093B-Q1

CMOS QUAD 2-INPUT NAND SCHMITT TRIGGER

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- Qualified for Automotive Applications
- Schmitt-Trigger Action on Each Input With No External Components
- Hysteresis Voltage Typically 0.9 V at $V_{DD} = 5\text{ V}$ and 2.3 V at $V_{DD} = 10\text{ V}$
- Noise Immunity Greater Than 50%
- No Limit on Input Rise and Fall Times
- Standardized, Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20 V
- Maximum Input Current of $1\mu\text{A}$ at 18 V Over Full Package Temperature Range, 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V Parametric Ratings
- ESD Protection Level Per AEC-Q100 Classification
 - 2000-V (H2) Human-Body Model
 - 200-V (M3) Machine-Model
 - 1000-V (C5) Charge-Device Model
- Applications
 - Wave and Pulse Shapers
 - High-Noise-Environment Systems
 - Monostable Multivibrators
 - Astable Multivibrators
 - NAND Logic



description/ordering information

The CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate, with Schmitt-trigger action on both inputs. The gate switches at different points for positive- and negative-going signals. The difference between the positive voltage (V_P) and the negative voltage (V_N) is defined as hysteresis voltage (V_H) (see Figure 2).

The CD4093B is available in 14-lead small-outline plastic package (M96) and 14-lead thin shrink small-outline packages (PWR suffixes).

ORDERING INFORMATION[†]

T_A	PACKAGE [‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC (M)	Reel of 2000	CD4093BQM96Q1	CD4093BQ

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

[‡] Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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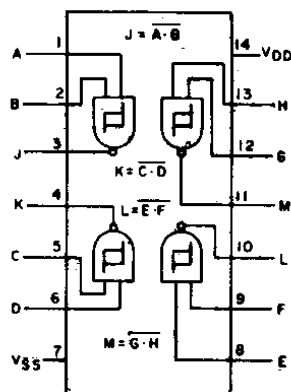
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CD4093B-Q1

CMOS QUAD 2-INPUT NAND SCHMITT TRIGGER

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functional block diagram



logic diagram

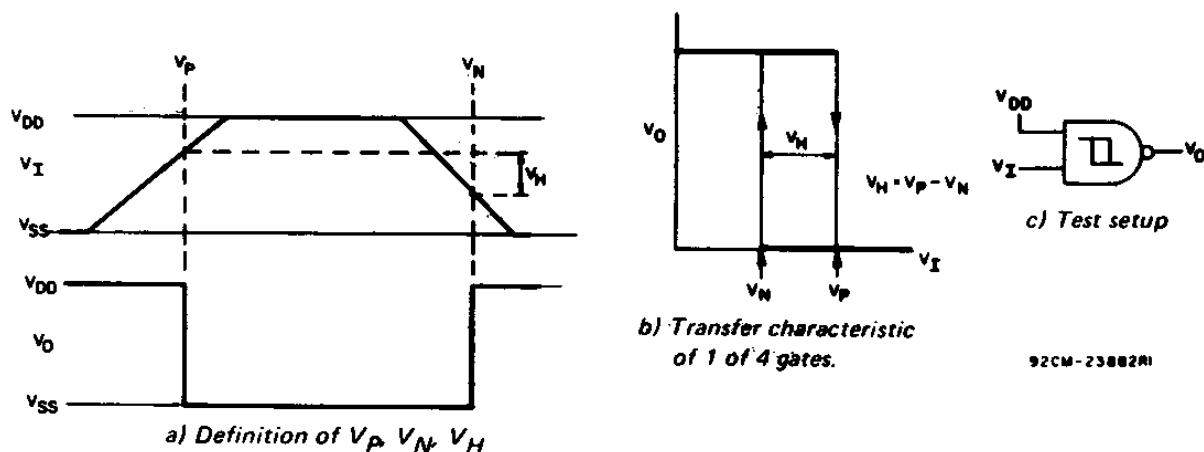
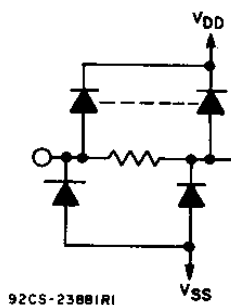
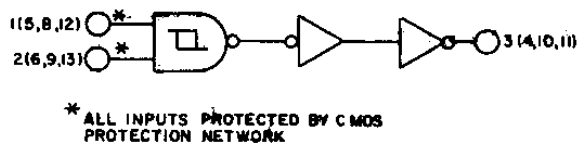


Figure 1. Hysteresis Definition, Characteristic, and Test Setup

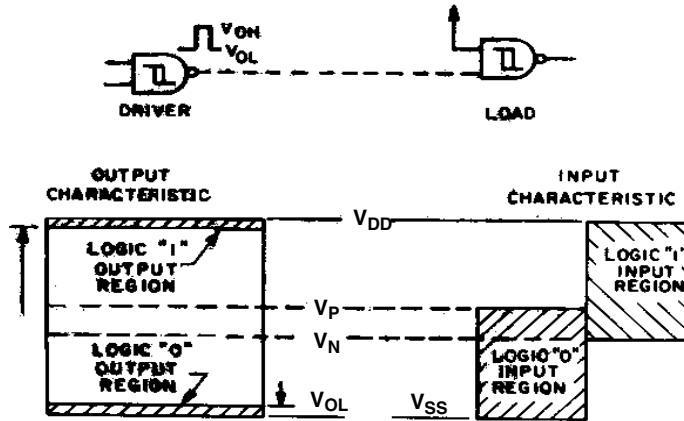


Figure 2. Input and Output Characteristics

TYPICAL CHARACTERISTICS

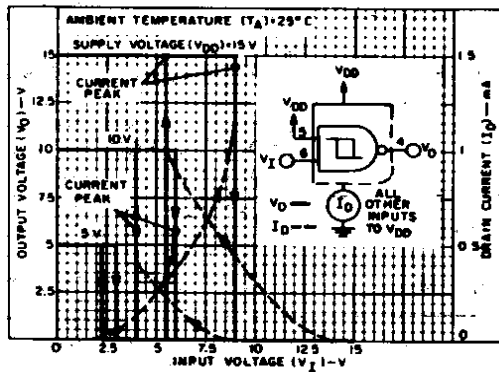


Figure 3. Typical Current and Voltage Transfer Characteristics

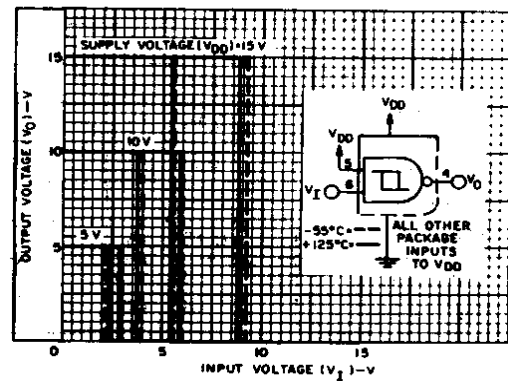


Figure 4. Typical Voltage Transfer Characteristics as a Function of Temperature

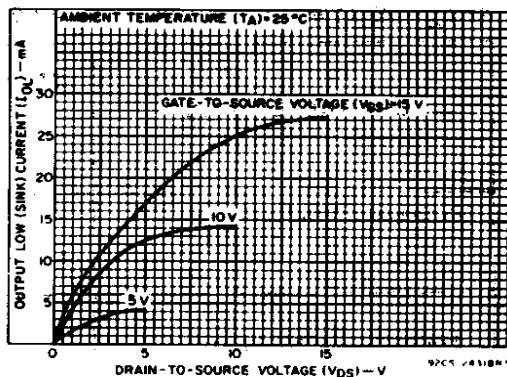


Figure 5. Typical Output Low (Sink) Current Characteristics

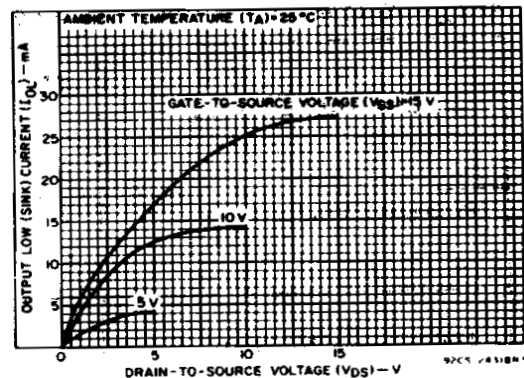


Figure 6. Minimum Output Low (Sink) Current Characteristics

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CMOS QUAD 2-INPUT NAND SCHMITT TRIGGER

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TYPICAL CHARACTERISTICS

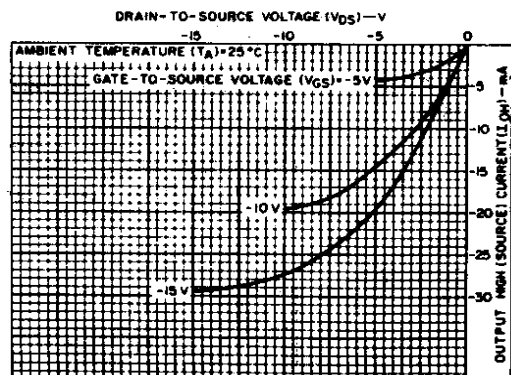


Figure 7. Typical Output High (Source) Current Characteristics

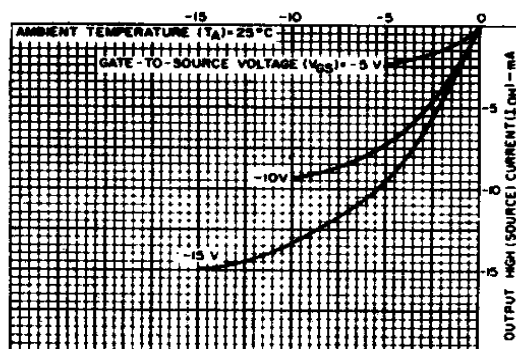


Figure 8. Minimum Output High (Source) Current Characteristics

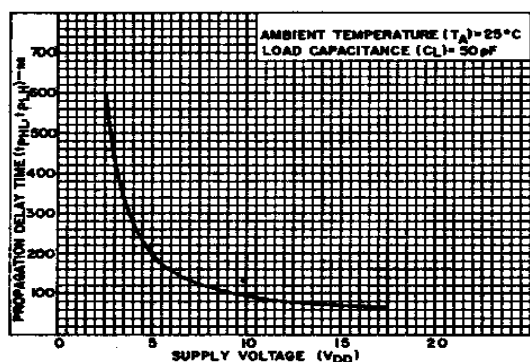


Figure 9. Typical Propagation Delay Time vs Supply Voltage

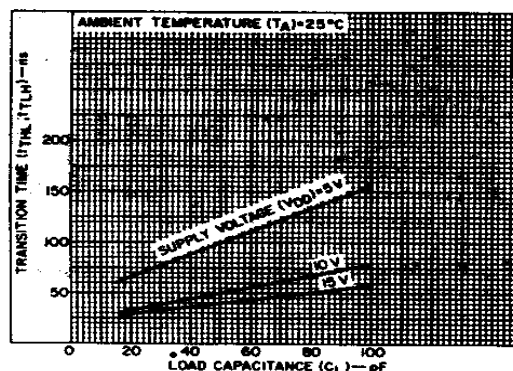


Figure 10. Typical Transition Time vs Load Capacitance

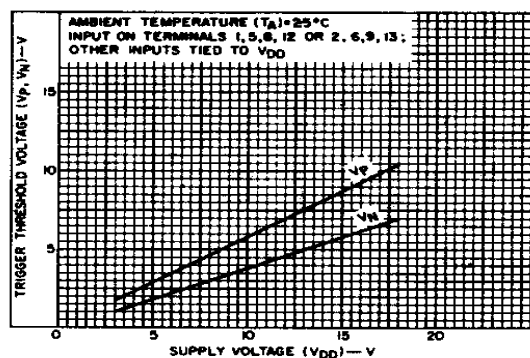


Figure 11. Typical Trigger Threshold Voltage vs V_{DD}

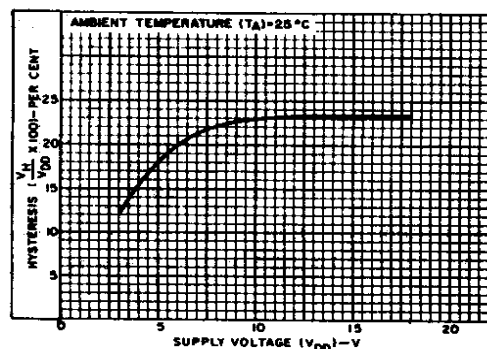


Figure 12. Typical Percent Hysteresis vs Supply Voltage

TYPICAL CHARACTERISTICS

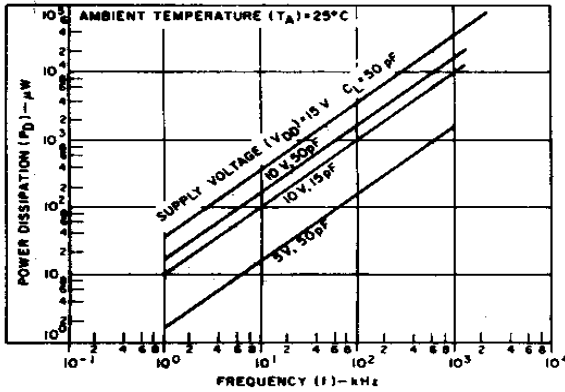


Figure 13. Typical Power Dissipation vs Frequency Characteristics

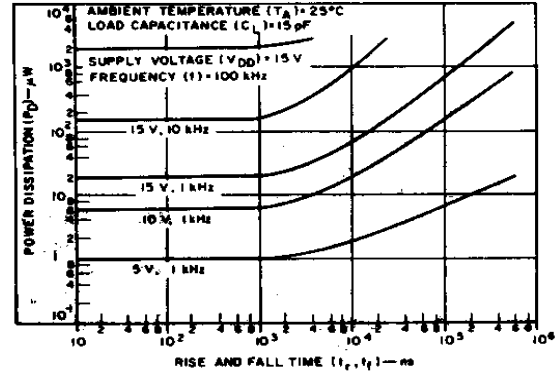


Figure 14. Typical Power Dissipation vs Rise and Fall Times

APPLICATION INFORMATION

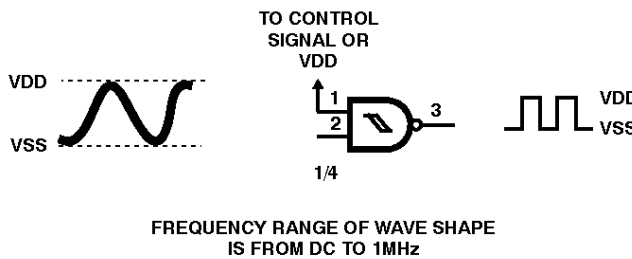


Figure 15. Wave Shaper

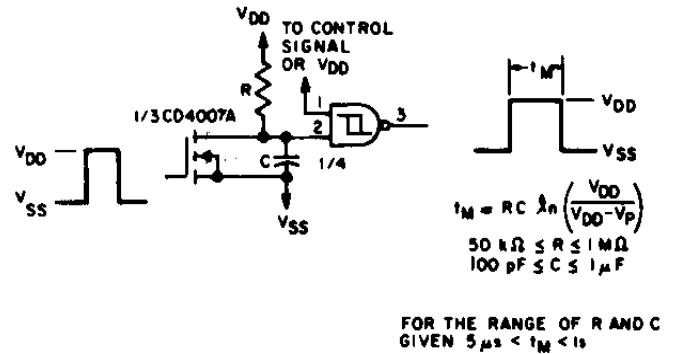
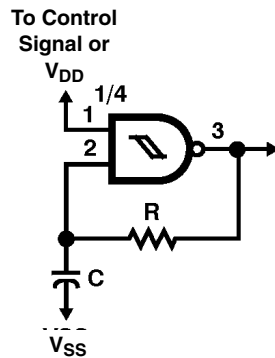


Figure 16. Monostable Multivibrator



$$t_A = RC \ln \left[\left(\frac{V_P}{V_N} \right) \left(\frac{V_{DD} - V_N}{V_{DD} - V_P} \right) \right]$$

50 kΩ ≤ R ≤ 1 MΩ
100 pF ≤ C ≤ 1 μF
For the Range of R and C
Given 2 ms < t_A < 0.4 s

Figure 17. Astable Multivibrator

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CMOS QUAD 2-INPUT NAND SCHMITT TRIGGER

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

DC supply voltage range, V_{DD}	–0.5 V to 20 V
Input voltage range, V_I , all inputs	–0.5 V to $V_{DD} + 0.5$ V
DC input current, any one input	± 10 mA
Package thermal impedance, θ_{JA} (see Note 1)	86°C/W
Device dissipation per output transistor for T_A , all package types	100 mW
Operating temperature range, T_A	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions‡

	MIN	MAX	UNIT
V_{CC} Supply voltage range (T_A = full package temperature range)	3	18	V

‡ For maximum reliability, nominal operating conditions should be selected so that operation is always within the given range.

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CMOS QUAD 2-INPUT NAND SCHMITT TRIGGER

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static electrical characteristics

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)					UNIT
	V _O (V)	V _I (V)	V _{DD} (V)	-40	85	125	25		
							MIN	TYP†	MAX
Quiescent device current, I _{DD} max		0,5	5	1	30	30	0.02	1	μA
		0,10	10	2	60	60	0.02	2	
		0,15	15	4	120	120	0.02	4	
		0,20	20	20	600	600	0.04	20	
Positive trigger threshold voltage, V _P min		A	5	2.2	2.2	2.2	2.2	2.9	V
		A	10	4.6	4.6	4.6	4.6	5.9	
		A	15	6.8	6.8	6.8	6.8	8.8	
		B	5	2.6	2.6	2.6	2.6	3.3	
		B	10	5.6	5.6	5.6	5.6	7	
		B	15	6.3	6.3	6.3	6.3	9.4	
V _P max		A	5	3.6	3.6	3.6	2.9	3.6	V
		A	10	7.1	7.1	7.1	5.9	7.1	
		A	15	10.8	10.8	10.8	8.8	10.8	
		B	5	4	4	4	3.3	4	
		B	10	8.2	8.2	8.2	7	8.2	
		B	15	12.7	12.7	12.7	9.4	12.7	
Negative trigger threshold voltage, V _N min		A	5	0.9	0.9	0.9	0.9	1.9	V
		A	10	2.5	2.5	2.5	2.5	3.9	
		A	15	4	4	4	4	5.8	
		B	5	1.4	1.4	1.4	1.4	2.3	
		B	10	3.4	3.4	3.4	3.4	5.1	
		B	15	4.8	4.8	4.8	4.8	7.3	
V _N max		A	5	2.8	2.8	2.8	1.9	2.8	V
		A	10	5.2	5.2	5.2	3.9	5.2	
		A	15	7.4	7.4	7.4	5.8	7.4	
		B	5	3.2	3.2	3.2	2.3	3.2	
		B	10	6.6	6.6	6.6	5.1	6.6	
		B	15	9.6	9.6	9.6	7.3	9.6	
Hysteresis voltage, V _H min		A	5	0.3	0.3	0.3	0.3	0.9	V
		A	10	1.2	1.2	1.2	1.2	2.3	
		A	15	1.6	1.6	1.6	1.6	3.5	
		B	5	0.3	0.3	0.3	0.3	0.9	
		B	10	1.2	1.2	1.2	1.2	2.3	
		B	15	1.6	1.6	1.6	1.6	3.5	
V _H max		A	5	1.6	1.6	1.6	0.9	1.6	V
		A	10	3.4	3.4	3.4	2.3	3.4	
		A	15	5	5	5	3.5	5	
		B	5	1.6	1.6	1.6	0.9	1.6	
		B	10	3.4	3.4	3.4	2.3	3.4	
		B	15	5	5	5	3.5	5	

NOTES: A. Inputs on terminals 1, 5, 8, 12 or 2, 6, 9, 13; other inputs to V_{DD}.
 B. Inputs on terminals 1 and 2, 5 and 6, 8 and 9, or 12 and 13; other inputs to V_{DD}.



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CMOS QUAD 2-INPUT NAND SCHMITT TRIGGER

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static electrical characteristics (continued)

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNIT
	V _O (V)	V _I (V)	V _{DD} (V)	-40	85	125	25			
							MIN	TYP†	MAX	
Output low (sink) current, I _{OL} min	0.4	0,5	5	0.61	0.42	0.36	0.51	1	mA	
	0.5	0,10	10	1.5	1.1	0.9	1.3	2.6		
	1.5	0,15	15	4	2.8	2.4	3.4	6.8		
Output high (source) current, I _{OH} min	4.6	0,5	5	-0.61	-0.42	-0.36	-0.51	-1	mA	
	2.5	0,5	5	-1.8	-1.3	-1.15	-1.6	-3.2		
	9.5	0,10	10	-1.5	-1.1	-0.9	-1.3	-2.6		
	13.5	0,15	15	-4	-2.8	-2.4	-3.4	-6.8		
Output voltage low level, V _{OL} max		0,5	5	0.05	0.05	0.05	0	0.05	V	
		0,10	10	0.05	0.05	0.05	0	0.05		
		0,15	15	0.05	0.05	0.05	0	0.05		
Output voltage high level, V _{OH} min		0,5	5	4.95	4.95	4.95	4.95	5	V	
		0,10	10	9.95	9.95	9.95	9.95	10		
		0,15	15	14.95	14.95	14.95	14.95			
Input current, I _{IN} max		0,18	18	±0.1	±1	±1	±10 ⁻⁵	±0.1	μA	

dynamic electrical characteristics

T_A = 25°C, input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V _{DD} (V)	LIMITS			UNIT
			MIN	TYP	MAX	
Propagation delay time, t _{PHL} , t _{PLH}		5		190	380	ns
		10		90	180	
		15		65	130	
Transition time, t _{THL} , t _{TLH}		5		100	200	ns
		10		50	100	
		15		40	80	
Input capacitance, C _{IN}	Any Input			5	7.5	pF

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4093BQM96G4Q1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD4093BQ
CD4093BQM96G4Q1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD4093BQ
CD4093BQM96Q1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD4093BQ
CD4093BQM96Q1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD4093BQ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD4093B-Q1 :

- Catalog : [CD4093B](#)
- Military : [CD4093B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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