

CD4511B Types

CMOS BCD-to-7-Segment Latch Decoder Drivers

High-Voltage Types (20-Volt Rating)

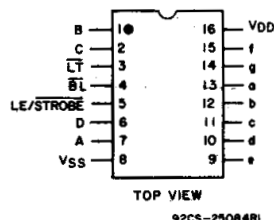


■ CD4511B types are BCD-to-7-segment latch decoder drivers constructed with CMOS logic and n-p-n bipolar transistor output devices on a single monolithic structure. These devices combine the low quiescent power dissipation and high noise immunity features of RCA CMOS with n-p-n bipolar output transistors capable of sourcing up to 25 mA. This capability allows the CD4511B types to drive LED's and other displays directly.

Lamp Test (LT), Blanking (BL), and Latch Enable or Strobe inputs are provided to test the display, shut off or intensity-modulate it, and store or strobe a BCD code, respectively. Several different signals may be multiplexed and displayed when external multiplexing circuitry is used.

The CD4511B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

These devices are similar to the type MC14511.



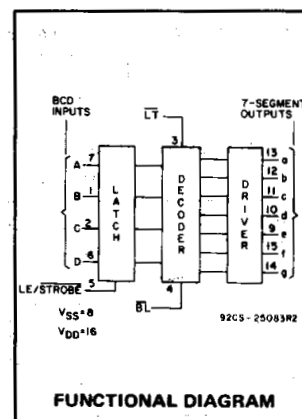
**CD4511B
TERMINAL ASSIGNMENT**

Features:

- High-output-sourcing capability up to 25 mA
- Input latches for BCD Code storage
- Lamp Test and Blanking capability
- 7-segment outputs blanked for BCD input codes > 1001
- 100% tested for quiescent current at 20 V
- Max. input current of 1 μ A at 18 V, over full package-temperature range, 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings

Applications:

- Driving common-cathode LED displays
- Multiplexing with common-cathode LED displays
- Driving incandescent displays
- Driving low-voltage fluorescent displays



FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V _{DD})	
Voltages referenced to V _{SS} Terminal)	–0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5V to V _{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION, PER PACKAGE (P _D):	
For T _A = –55°C to +100°C	500mW
For T _A = +100°C to +125°C	Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T _A)	–55°C to +125°C
STORAGE TEMPERATURE RANGE (T _{stg})	–65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265°C

OPERATING CONDITIONS AT T_A = 25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

Characteristic	V _{DD}	Min.	Max.	Units
Supply-Voltage Range (T _A): (Full Package-Temperature Range)	–	3	18	V
Set-Up Time (t _S)	5	150	–	ns
	10	70	–	ns
	15	40	–	ns
Hold Time (t _H)	5	0	–	ns
	10	0	–	ns
	15	0	–	ns
Strobe Pulse Width (t _W)	5	400	–	ns
	10	160	–	ns
	15	100	–	ns

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS				LIMITS AT INDICATED TEMPERATURES (°C)							Units
	I _{OH} (mA)	V _O (V)	V _{IN} (V)	V _{DD} (V)								
					−55	−40	+85	+125	+25			
					Min.	Typ.	Max.					
Quiescent Device Current: I _{DD} Max.	—	—	—	5	5	5	150	150	—	0.04	5	μA
	—	—	—	10	10	10	300	300	—	0.04	10	
	—	—	—	15	20	20	600	600	—	0.04	20	
	—	—	—	20	100	100	3000	3000	—	0.08	100	
Output Voltage:												
Low-Level V _{OL} Max.	—	—	0.5	5	0.05				—	0	0.05	V
	—	—	0.10	10	0.05				—	0	0.05	
	—	—	0.15	15	0.05				—	0	0.05	
High-Level V _{OH} Min.	—	—	0.5	5	4	4	4.2	4.2	4.1	4.55	—	V
	—	—	0.10	10	9	9	9.2	9.2	9.1	9.55	—	
	—	—	0.15	15	14	14	14.2	14.2	14.1	14.55	—	
Input Low Voltage, V _{IL} Max.	—	0.5,3.8		5	1.5				—	—	1.5	V
	—	1.8,8	—	10	3				—	—	3	
	—	1.5,13.8		15	4				—	—	4	
Input High Voltage, V _{IH} Min.	—	0.5,3.8		5	3.5				3.5	—	—	V
	—	1.8,8		10	7				7	—	—	
	—	1.5,13.8		15	11				11	—	—	
Output Drive Voltage: High Level V _{OH} Min.	0			5	4.0	4.0	4.20	4.20	4.10	4.55	—	V
	5	—			—	—	—	—	—	4.25	—	
	10	—			3.80	3.80	3.90	3.90	3.90	4.10	—	
	15	—			—	—	3.50	3.50	—	3.95	—	
	20	—			3.55	3.55	3.30	—	3.40	3.75	—	
	25	—		10	3.40	3.40	—	—	3.10	3.55	—	V
	0	—			9.0	9.0	9.20	9.20	9.10	9.55	—	
	5	—			—	—	—	—	—	9.25	—	
	10	—			8.85	8.85	9.00	9.00	9.00	9.15	—	
	15	—			—	—	—	—	—	9.05	—	
	20	—		15	8.70	8.70	8.40	8.40	8.60	8.90	—	V
	25	—			8.60	8.60	—	—	8.30	8.75	—	
	0	—			14.0	14.0	14.20	14.20	14.10	14.55	—	
	5	—			—	—	—	—	—	14.30	—	
	10	—			13.90	13.90	14.0	14.0	14.0	14.20	—	
	15	—		20	—	—	—	—	—	14.10	—	V
	20	—			13.75	13.75	13.50	13.50	13.70	13.95	—	
	25	—			13.65	13.65	—	—	13.50	13.80	—	
	0	—			—	—	—	—	—	—	—	
	5	—			—	—	—	—	—	—	—	
Output Low (Sink) Current, I _{OL} Min.	—	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	—	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	—	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Input Current, I _{IN} Max.	—	0.18	0.18	18	±0.1	±0.1	±1	±1	—	±10 ^{−5}	±0.1	μA

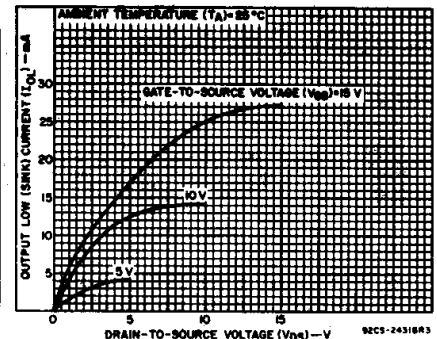


Fig. 1 - Typical output low (sink) current characteristics.

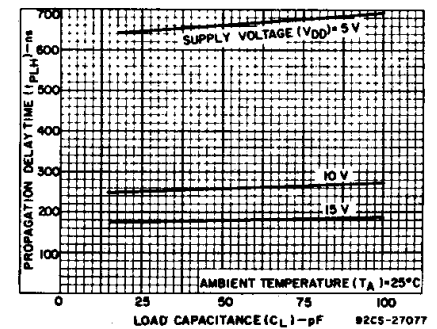


Fig. 2 - Typical data-to-output, low-to-high-level propagation delay time as a function of load capacitance.

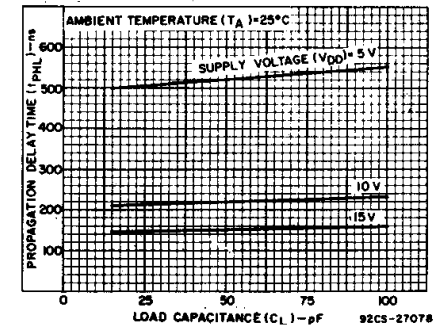


Fig. 3 - Typical data-to-output, high-to-low-level propagation delay time as a function of load capacitance.

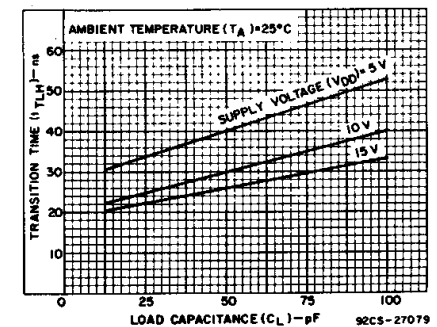


Fig. 4 - Typical low-to-high-level transition time as a function of load capacitance.

CD4511B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$,
 $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	Test Conditions	LIMITS All Packages			UNITS
	V_{DD} Volts	Min.	Typ.	Max.	
Propagation Delay Time: (Data) High-to-Low Level, t_{PHL}	5	—	520	1040	ns
	10	—	210	420	
	15	—	150	300	
Low-to-High Level, t_{PLH}	5	—	660	1320	ns
	10	—	260	520	
	15	—	180	360	
Propagation Delay Time: (BL) High-to-Low Level, t_{PHL}	5	—	350	700	ns
	10	—	175	350	
	15	—	125	250	
Low-to-High Level, t_{PLH}	5	—	400	800	ns
	10	—	175	350	
	15	—	150	300	
Propagation Delay Time: (LT) High-to-Low Level, t_{PHL}	5	—	250	500	ns
	10	—	125	250	
	15	—	85	170	
Low-to-High Level, t_{PLH}	5	—	150	300	ns
	10	—	75	150	
	15	—	50	100	
Transition Time: Low-to-High Level, t_{TLH}	5	—	40	80	ns
	10	—	30	60	
	15	—	25	50	
High-to-Low Level, t_{THL}	5	—	125	310	ns
	10	—	75	185	
	15	—	65	160	
Minimum Set-Up Time, t_S	5	150	75	—	ns
	10	70	35	—	
	15	40	20	—	
Minimum Hold Time, t_H	5	0	-75	—	ns
	10	0	-35	—	
	15	0	-20	—	
Strobe Pulse Width, t_W	5	400	200	—	ns
	10	160	80	—	
	15	100	50	—	
Input Capacitance, C_{IN}		—	5	7.5	pF

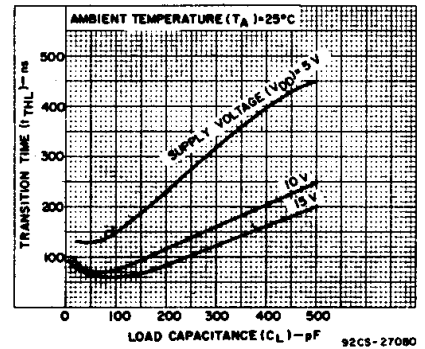


Fig. 5 — Typical high-to-low transition time as a function of load capacitance.

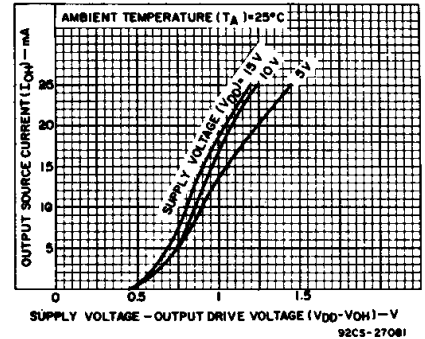


Fig. 6 — Typical voltage drop (V_{DD} to output) vs. output source current as a function of supply.

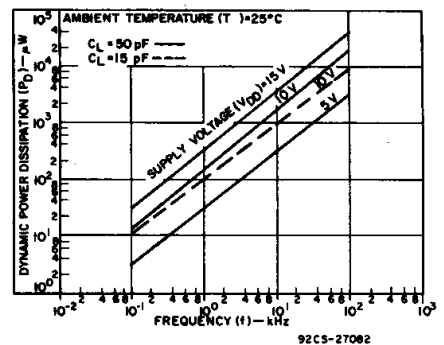


Fig. 7 — Typical dynamic power dissipation characteristics.

3

COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4511B Types

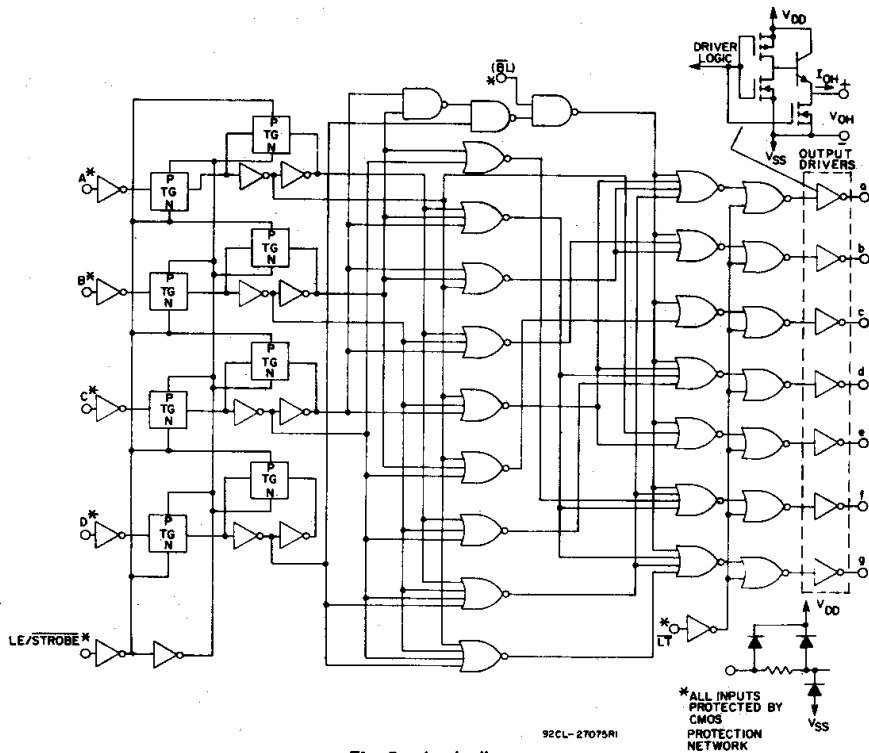


Fig. 8 - Logic diagram.

TRUTH TABLE												
LE	BI	LT	D	C	B	A	a	b	c	d	e	f
X	X	0	X	X	X	X	1	1	1	1	1	1
X	0	1	X	X	X	X	0	0	0	0	0	0
0	1	1	0	0	0	0	1	1	1	1	1	0
0	1	1	0	0	0	1	0	1	1	0	0	0
0	1	1	0	0	1	0	1	1	0	1	1	0
0	1	1	0	0	1	1	1	1	1	0	0	1
0	1	1	0	1	0	0	0	1	1	0	0	1
0	1	1	0	1	0	1	1	0	1	1	0	1
0	1	1	0	1	1	0	0	0	1	1	1	1
0	1	1	0	1	1	1	0	0	1	1	1	1
0	1	1	1	0	0	0	0	0	1	1	1	1
0	1	1	1	0	0	1	1	1	1	0	0	0
0	1	1	1	0	0	0	1	1	1	1	1	1
0	1	1	1	0	0	1	1	1	0	0	1	1
0	1	1	1	0	1	0	0	0	0	0	0	0
0	1	1	1	0	1	1	0	0	0	0	0	0
0	1	1	1	1	0	0	0	0	0	0	0	0
0	1	1	1	1	1	0	0	0	0	0	0	0
0	1	1	1	1	1	1	0	0	0	0	0	0
1	1	1	X	X	X	X	*	*	*	*	*	*

X = Don't Care

* Depends on BCD code previously applied when LE = 0

Note: Display is blank for all illegal input codes (BCD > 1001).

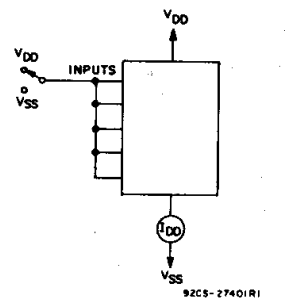


Fig. 9 - Quiescent device current.

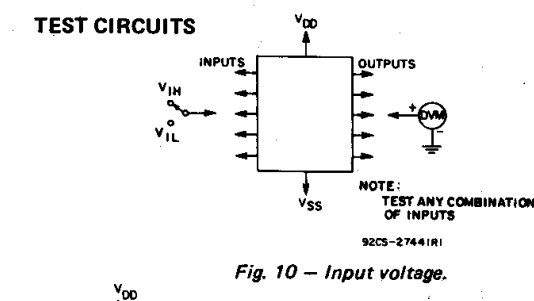


Fig. 10 - Input voltage.

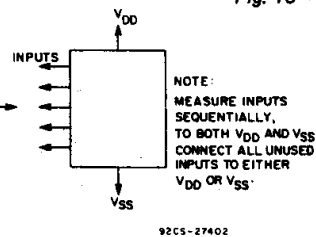


Fig. 11 - Input current.

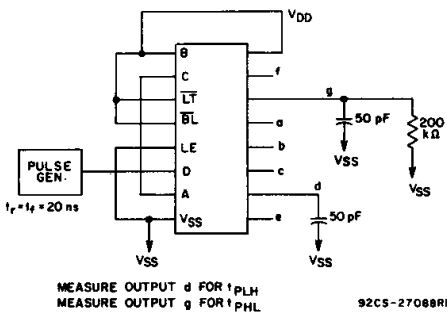


Fig. 12 - Data propagation delay.

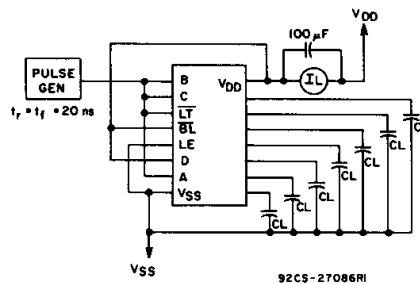


Fig. 13 - Dynamic power dissipation.

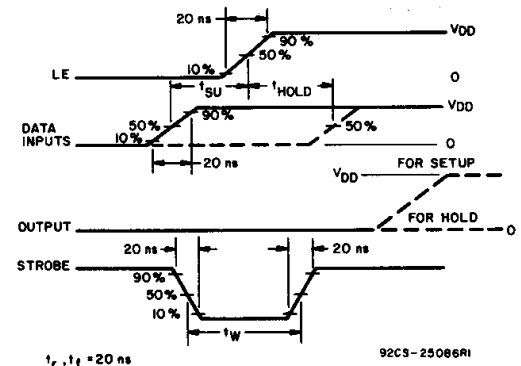
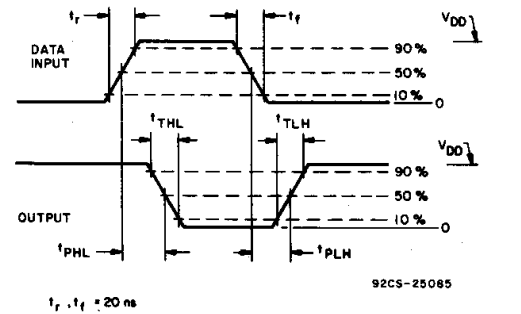
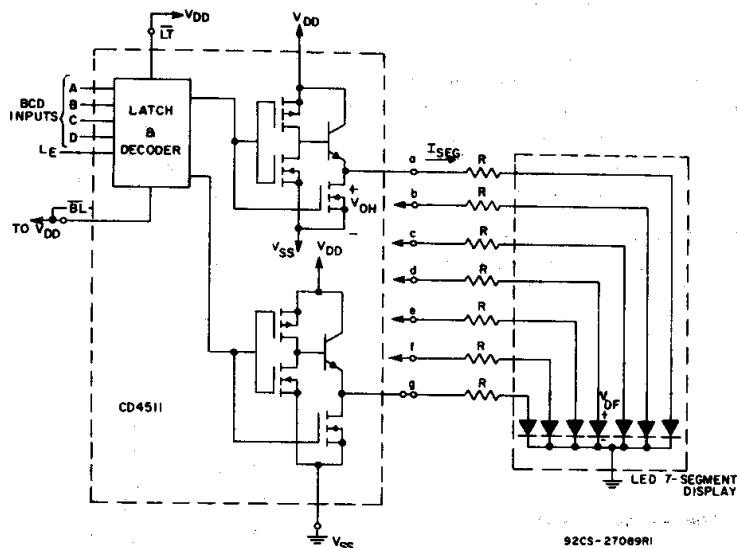


Fig. 14 - Dynamic waveforms.

CD4511B Types

APPLICATIONS Interfacing with Various Displays

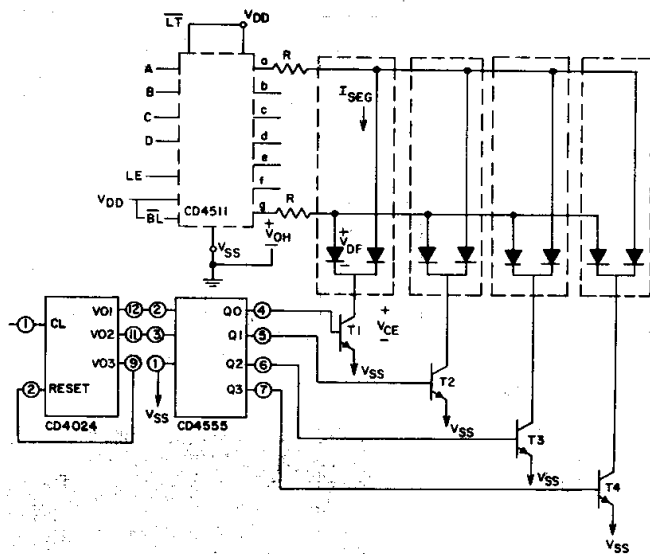


Duty Cycle = 100%

$I_{SEG} = I_{DIODE\ AVG.} = 20\text{ mA at Luminous Intensity/Segment} = 250\text{ microcandles}$

$$R = \frac{V_{OH} - V_{DF}}{I_{SEG}}$$

Fig. 15 - Driving common-cathode 7-segment LED displays (example Hewlett-Packard 5082-7740).



Multiplexing Scheme Showing 2 of 7 Segments Connected

Transistors T_1-T_4 (RCA-2N3053 or 2N2102) have I_C Max. rating $> 7 \times I_{SEG}$

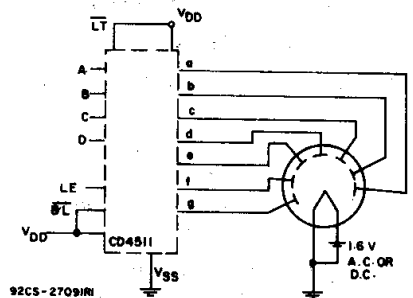
Duty Cycle = 25%

$$I_{SEG} = (I_{DIODE\ AVG.}) \times 4$$

$$R = \frac{(V_{OH} - V_{DF} - V_{CE})}{I_{SEG}}$$

All unused inputs on CD4555 are connected to V_{DD} or V_{SS} .

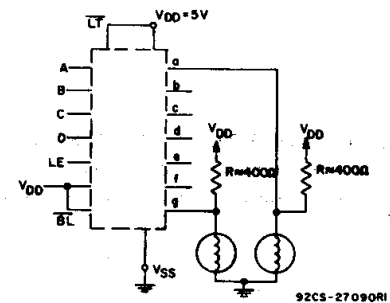
Fig. 18 - Multiplexing with common-cathode 7-segment LED displays (example Hewlett-Packard 5082-7404 4 character display or 4 discrete Monosanto Man 3 displays).



A medium-brightness intensity display can be obtained with low-voltage fluorescent displays such as the Tung-Sol Digivac S/G** Series.

**Trademark Tung-Sol Division Wagner Electric Co.

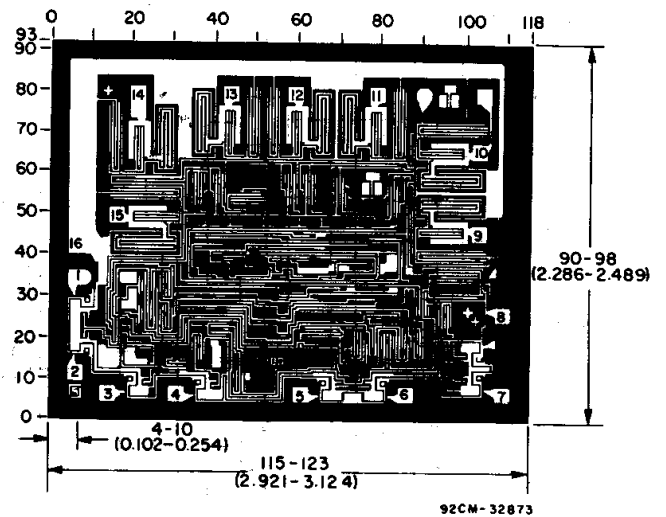
Fig. 16 - Driving low-voltage fluorescent displays.



2 of 7 Segments Shown Connected

Resistors R from V_{DD} to each 7-segment driver output are chosen to keep all Numitron segments slightly on and warm.

Fig. 17 - Driving incandescent displays (RCA Numitron DR2000 series displays).



Dimensions and pad layout for CD4511B chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4511BE	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4511BE
CD4511BE.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4511BE
CD4511BEE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4511BE
CD4511BF	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4511BF
CD4511BF.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4511BF
CD4511BF3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4511BF3A
CD4511BF3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4511BF3A
CD4511BNSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4511B
CD4511BNSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4511B
CD4511BNSRG4	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4511B
CD4511BPW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	CM511B
CD4511BPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	CM511B
CD4511BPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM511B
CD4511BPWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM511B

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD4511B, CD4511B-MIL :

- Catalog : [CD4511B](#)
- Military : [CD4511B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4511BNSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4511BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4511BPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4511BNSR	SOP	NS	16	2000	353.0	353.0	32.0
CD4511BPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
CD4511BPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4511BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4511BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4511BEE4	N	PDIP	16	25	506	13.97	11230	4.32

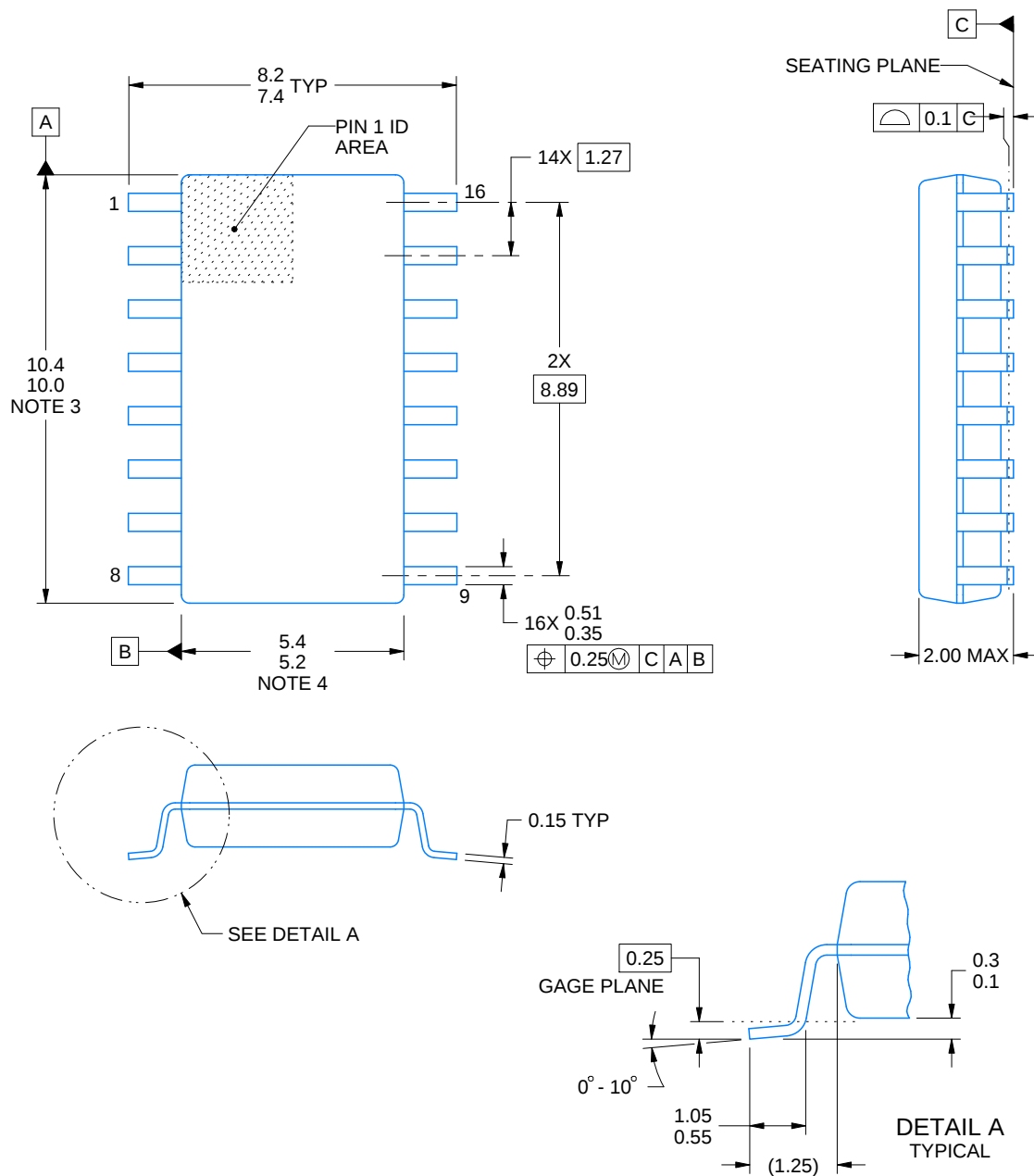


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE

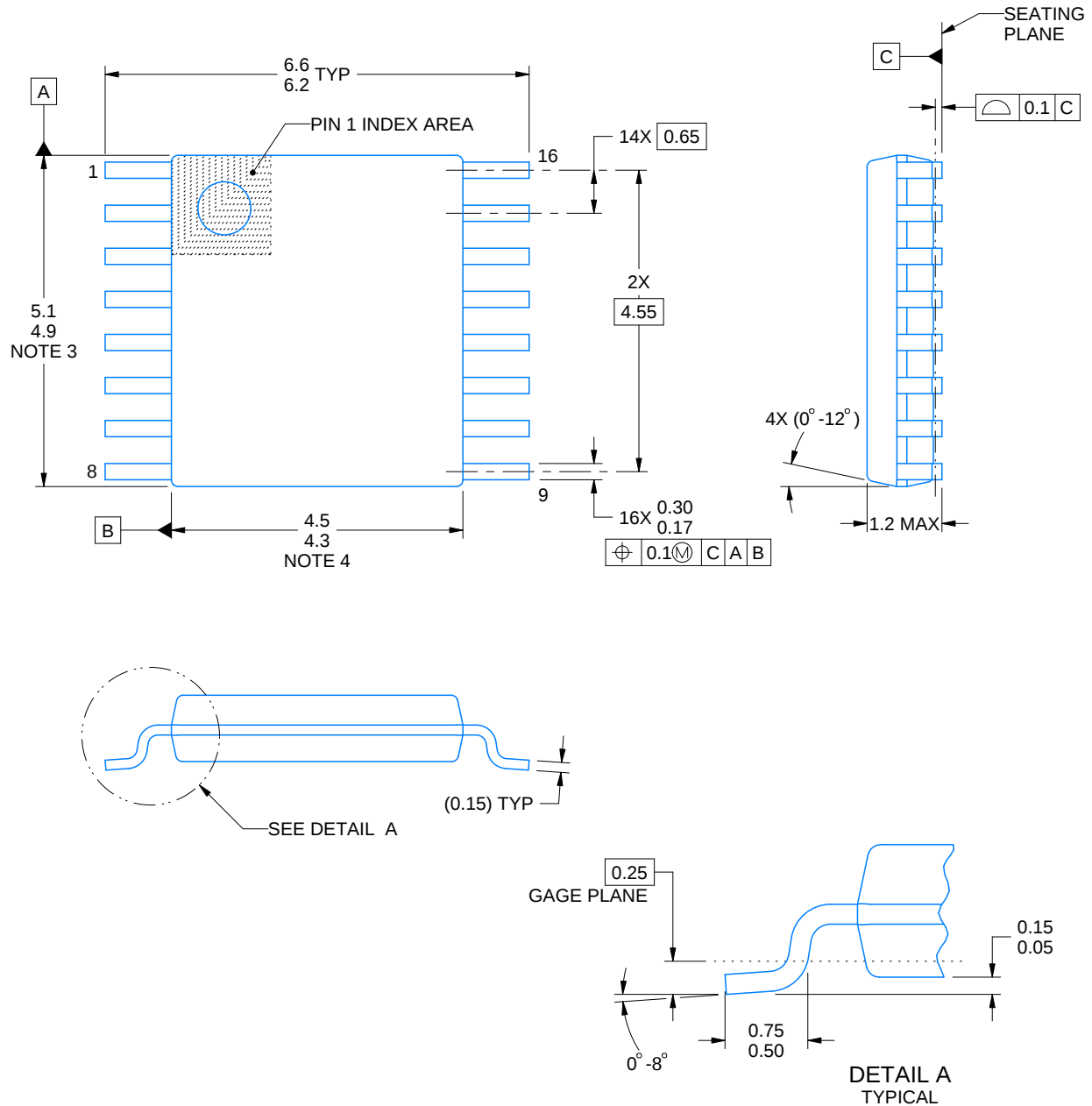
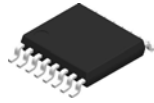


PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



4220204/B 12/2023

NOTES:

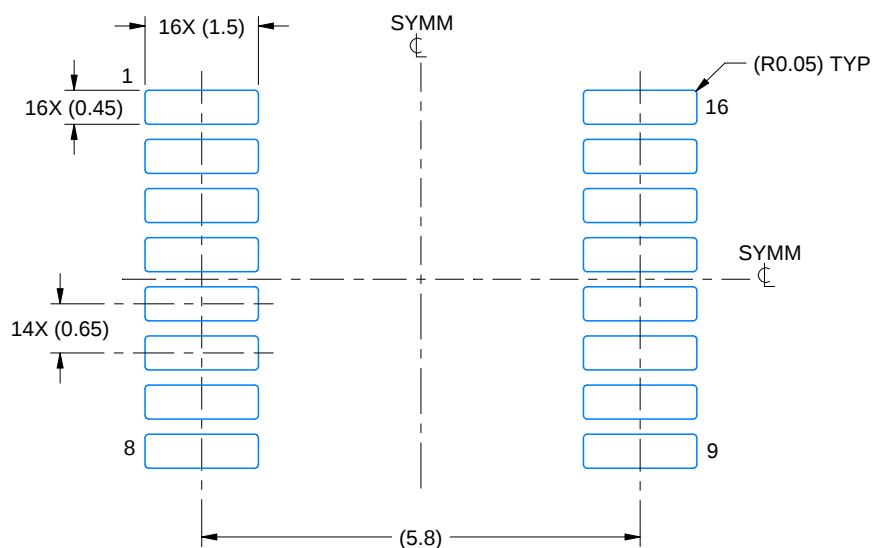
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

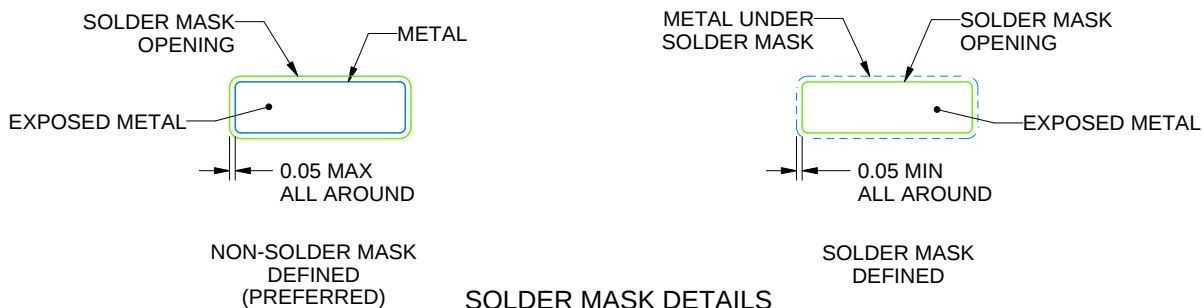
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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