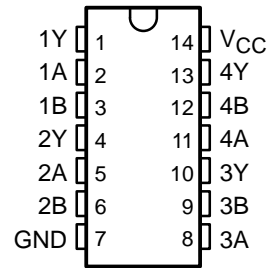


# CD54ACT02, CD74ACT02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCHS309B – JANUARY 2001 – REVISED MAY 2002

- Inputs Are TTL-Voltage Compatible
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- $\pm 24$ -mA Output Drive Current  
– Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

CD54ACT02 . . . F PACKAGE  
CD74ACT02 . . . E OR M PACKAGE  
(TOP VIEW)



## description

The 'ACT02 devices contain four independent 2-input NOR gates that perform the Boolean function  $Y = \overline{A} \cdot \overline{B}$  or  $Y = \overline{A + B}$  in positive logic.

## ORDERING INFORMATION

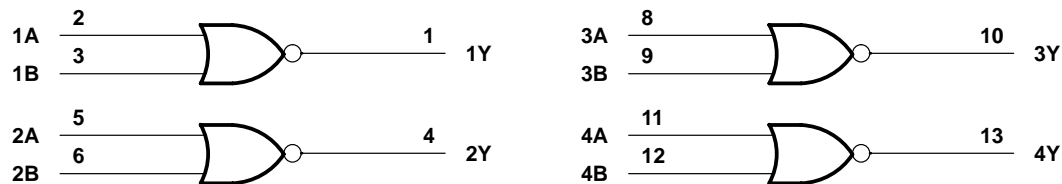
T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	PDIP – E	Tube	CD74ACT02E	CD74ACT02E
	SOIC – M	Tube	CD74ACT02M	ACT02M
		Tape and reel	CD74ACT02M96	
	CDIP – F	Tube	CD54ACT02F3A	CD54ACT02F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

## logic diagram (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# CD54ACT02, CD74ACT02

## QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCHS309B – JANUARY 2001 – REVISED MAY 2002

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 6 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): E package	80°C/W
M package	86°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

		$T_A = 25^\circ\text{C}$		–40°C TO 85°C		–55°C TO 125°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–24		–24	mA
$I_{OL}$	Low-level output current		24		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10		10	ns/V

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$V_{CC}$	$T_A = 25^\circ\text{C}$		–40°C TO 85°C		–55°C TO 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\ \mu\text{A}$	4.5 V	4.4		4.4		4.4		V
		$I_{OH} = -24\ \text{mA}$	4.5 V	3.94		3.8		3.7		
		$I_{OH} = -50\ \text{mA}^\ddagger$	5.5 V					3.85		
		$I_{OH} = -75\ \text{mA}^\ddagger$	5.5 V			3.85				
$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\ \mu\text{A}$	4.5 V		0.1		0.1		0.1	V
		$I_{OL} = 24\ \text{mA}$	4.5 V		0.36		0.44		0.5	
		$I_{OL} = 50\ \text{mA}^\ddagger$	5.5 V						1.65	
		$I_{OL} = 75\ \text{mA}^\ddagger$	5.5 V				1.65			
$I_I$	$V_I = V_{CC}$ or GND		5.5 V		±0.1		±1		±1	μA
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$		5.5 V		4		40		80	μA
$\Delta I_{CC}$	$V_I = V_{CC} - 2.1\ \text{V}$		4.5 V to 5.5 V		2.4		2.8		3	mA
$C_i$					10		10		10	pF

<sup>‡</sup> Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.



# CD54ACT02, CD74ACT02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCHS309B – JANUARY 2001 – REVISED MAY 2002

ACT INPUT LOAD TABLE

INPUT	UNIT LOAD
A or B	0.32

Unit load is  $\Delta I_{CC}$  limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ ,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C TO 85°C		–55°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	Y	3.1	11.1	3.1	12.2	ns
$t_{PHL}$			3.1	11.1	3.1	12.2	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	55	pF

## SCHS309B – JANUARY 2001 – REVISED MAY 2002

From Output Under Test

$C_L = 50 \text{ pF}$   
(see Note A)

$R1 = 500 \Omega$

$R2 = 500 \Omega$

S1

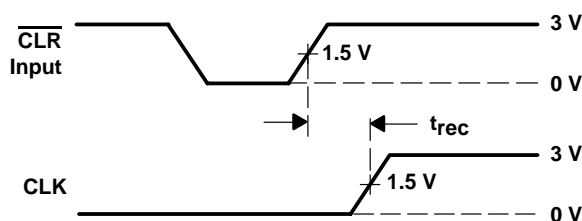
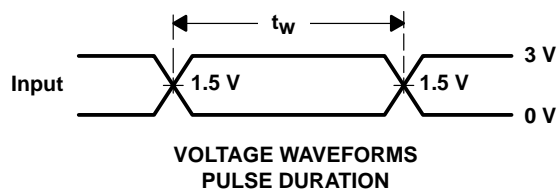
$2 \times V_{CC}$

Open

GND

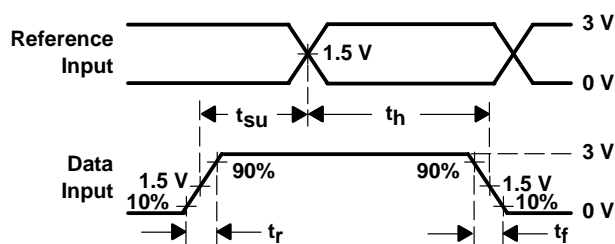
LOAD CIRCUIT

TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	2 × V <sub>CC</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND



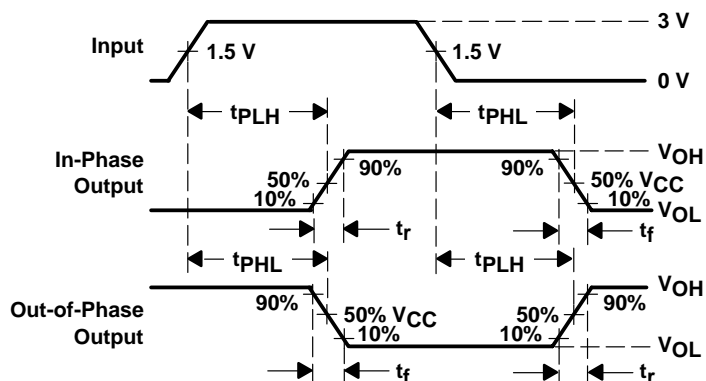
## VOLTAGE WAVEFORMS

### RECOVERY TIME



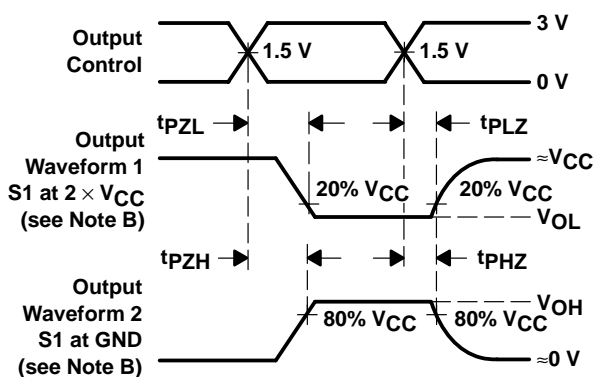
## VOLTAGE WAVEFORMS

### SETUP AND HOLD AND INPUT RISE AND FALL TIMES



## VOLTAGE WAVEFORMS

### PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



## VOLTAGE WAVEFORMS

### OUTPUT ENABLE AND DISABLE TIMES

- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns. Phase relationships between waveforms are arbitrary.
  - D. For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.
  - E. The outputs are measured one at a time with one input transition per measurement.
  - F.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - G.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - H.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

### Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CD54ACT02F3A</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT02F3A
CD54ACT02F3A.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT02F3A
<a href="#">CD74ACT02BQAR</a>	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AD02
<a href="#">CD74ACT02E</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT02E
CD74ACT02E.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT02E
CD74ACT02EE4	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT02E
<a href="#">CD74ACT02M</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-55 to 125	ACT02M
<a href="#">CD74ACT02M96</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT02M
CD74ACT02M96.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT02M
<a href="#">CD74ACT02PWR</a>	Active	Production	TSSOP (PW)   14	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 125	AD02

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF CD54ACT02, CD74ACT02 :**

- Catalog : [CD74ACT02](#)
- Military : [CD54ACT02](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74ACT02BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
CD74ACT02M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74ACT02PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74ACT02BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
CD74ACT02M96	SOIC	D	14	2500	353.0	353.0	32.0
CD74ACT02PWR	TSSOP	PW	14	3000	353.0	353.0	32.0



## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74ACT02E	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT02E	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT02E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT02E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT02EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT02EE4	N	PDIP	14	25	506	13.97	11230	4.32

**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**BQA 14**

**WQFN - 0.8 mm max height**

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

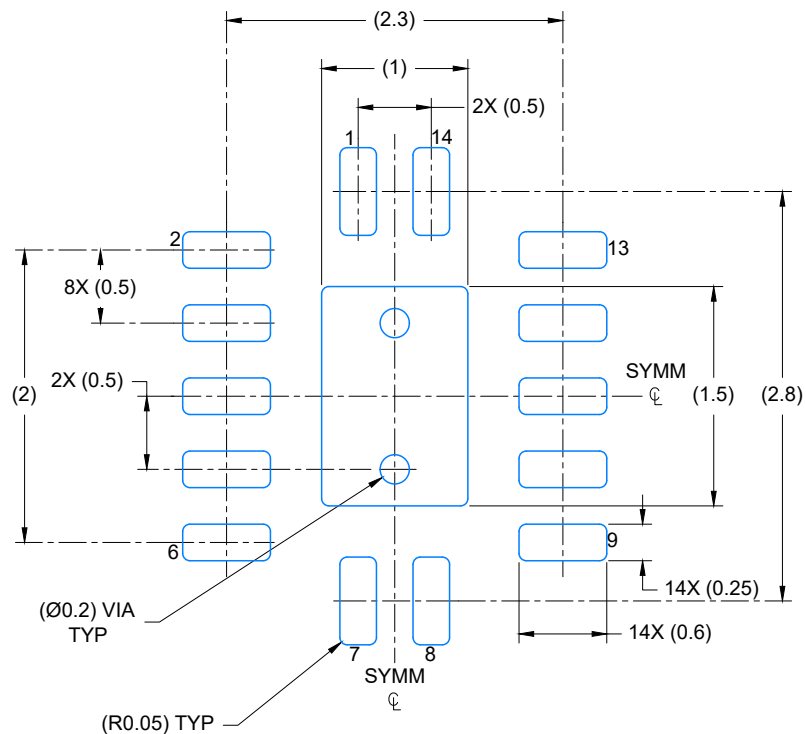


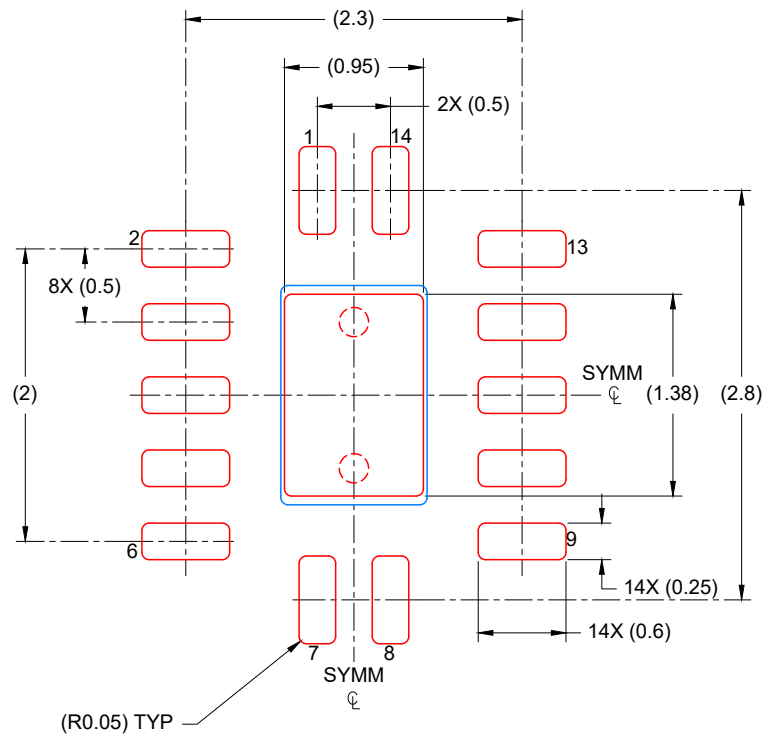
**WQFN - 0.8 mm max height**

The drawing shows a 15-pin connector with the following dimensions and features:

- Overall Dimensions:**
  - Width: 2.6 (max), 2.4 (min)
  - Height: 3.1 (max), 2.9 (min)
- Pin 1 Index Area:** Indicated by a shaded rectangular region on the left side.
- Seating Plane:** Indicated by a dashed line and a triangle symbol labeled 'C'.
- Pin Dimensions and Spacing:**
  - Pin 1 ID (Optional): 0.05 (max), 0.00 (min)
  - Pin 7 and 8: 1.1 (max), 0.9 (min) spacing, 2X 0.5 (max) width.
  - Pin 9: 1.6 (max), 1.4 (min) height.
  - Pin 13 and 14: 14X 0.3 (max), 0.2 (min) height, 14X 0.5 (max), 0.3 (min) width.
  - Pin 15: 2X 2 (max) width, 2 (min) height.
- Symmetry:** Indicated by 'SYMM' and a center line symbol.
- Material and Surface Finish:**
  - Material: 0.1 (max), 0.05 (max) (M) C A B
  - Surface Finish: 0.05 (max) (M) C
- Other Dimensions:**
  - Pin 6: 8X 0.5 (max) width, 0.8 (max), 0.7 (min) height.
  - Pin 12: 0.08 (max) width, 0.00 (min) height.
  - Pin 10 and 11: 0.2 (typical) width.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.





SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 88% PRINTED COVERAGE BY AREA  
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



**J 14**

## GENERIC PACKAGE VIEW

**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

**J0014A****PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



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# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

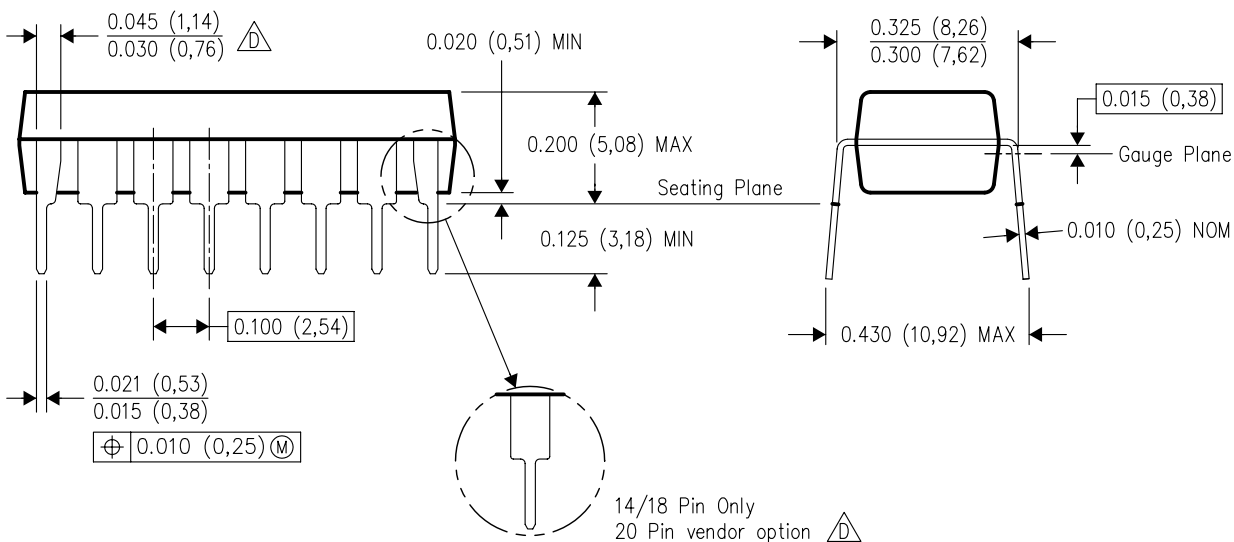
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

**PW0014A**

## PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

**PW0014A**

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



## SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025