

## CD74AC238 3 线至 8 线解码器/多路信号分离器

### 1 特性

- 交流类型的工作电压范围为 1.5V 至 5.5V，并在电源电压的 30% 时具有平衡的抗噪性能
- 双极 F、AS 和 S 的速度，同时功耗显著降低
- 专门为高速存储器解码器和数据传输系统设计
- 包含三个使能输入以简化级联和/或数据接收
- 平衡传播延迟
- $\pm 24\text{mA}$  输出驱动电流
  - 扇出至 15 个 F 器件
- 防 SCR 闩锁 CMOS 工艺和电路设计
- ESD 保护超过 2kV ( 根据 MIL-STD-883 方法 3015 )

### 2 说明

CD74AC238 解码器/多路信号分离器设计用于需要极短传播延迟时间的高性能存储器解码和数据路由应用。在高性能存储器系统中，可使用此解码器来尽可能地消除系统解码的影响。

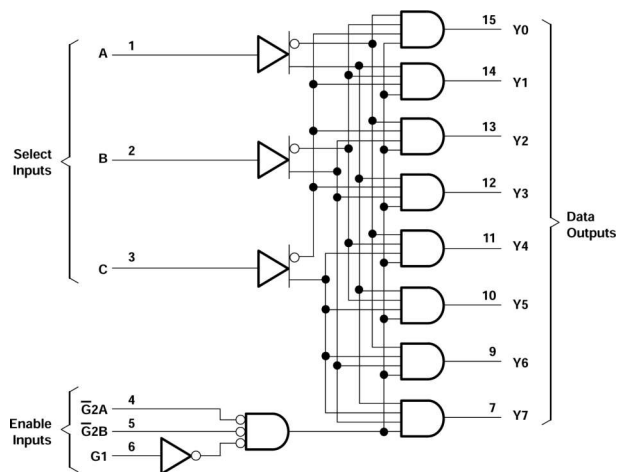
#### 封装信息

| 器件型号      | 封装 <sup>(1)</sup> | 封装尺寸 <sup>(2)</sup> | 本体尺寸 <sup>(3)</sup> |
|-----------|-------------------|---------------------|---------------------|
| CD74AC238 | BQB ( WQFN , 16 ) | 3.5mm × 2.5mm       | 3.5mm × 2.5mm       |
|           | D ( SOIC , 16 )   | 9.9mm × 6mm         | 9.9mm × 3.9mm       |
|           | PW ( TSSOP , 16 ) | 5.00mm × 6.4mm      | 5.00mm × 4.40mm     |

(1) 有关更多信息，请参阅节 10。

(2) 封装尺寸 ( 长 × 宽 ) 为标称值，并包括引脚 ( 如适用 )。

(3) 本体尺寸 ( 长 × 宽 ) 为标称值，不包括引脚。



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## 3 Pin Configuration and Functions

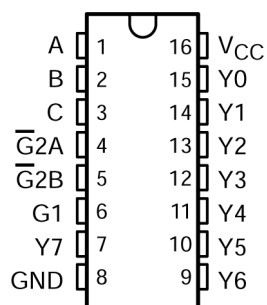


图 3-1. CD74AC238 D or PW Package; 16-Pin SOIC or TSSOP (Top View)

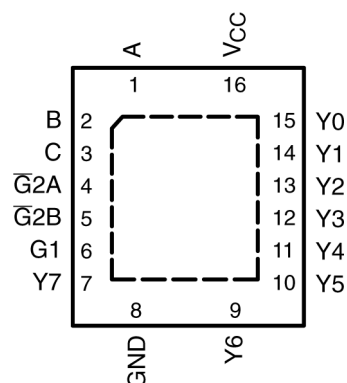


图 3-2. CD74AC238 BQB Package, 16-Pin WQFN (Top View)

表 3-1. Pin Functions

| PIN                        |     | TYPE <sup>(1)</sup> | DESCRIPTION                 |
|----------------------------|-----|---------------------|-----------------------------|
| NAME                       | NO. |                     |                             |
| A                          | 1   | I                   | Input A                     |
| B                          | 2   | I                   | Input B                     |
| C                          | 3   | I                   | Input C                     |
| G2A                        | 4   | I                   | Strobe Input 2A, active low |
| G2B                        | 5   | I                   | Strobe Input 2B, active low |
| G1                         | 6   | I                   | Strobe Input                |
| Y7                         | 7   | O                   | Output 7                    |
| GND                        | 8   | G                   | Ground                      |
| Y6                         | 9   | O                   | Output 6                    |
| Y5                         | 10  | O                   | Output 5                    |
| Y4                         | 11  | O                   | Output 4                    |
| Y3                         | 12  | O                   | Output 3                    |
| Y2                         | 13  | O                   | Output 2                    |
| Y1                         | 14  | O                   | Output 1                    |
| Y0                         | 15  | O                   | Output 0                    |
| V <sub>CC</sub>            | 16  | P                   | Positive Supply             |
| Thermal Pad <sup>(2)</sup> |     | —                   | Thermal Pad                 |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

(2) BQB package only

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                         |                                            | MIN                                    | MAX | UNIT    |
|-------------------------|--------------------------------------------|----------------------------------------|-----|---------|
| $V_{CC}$                | Supply voltage range                       | - 0.5                                  | 6   | V       |
| $I_{IK}$ <sup>(2)</sup> | Input clamp current                        | $(V_I < 0 \text{ V or } V_I > V_{CC})$ |     | ±20 mA  |
| $I_{OK}$ <sup>(2)</sup> | Output clamp current                       | $(V_O < 0 \text{ V or } V_O > V_{CC})$ |     | ±50 mA  |
| $I_O$                   | Continuous output current                  | $(V_O > 0 \text{ V or } V_O < V_{CC})$ |     | ±50 mA  |
|                         | Continuous current through $V_{CC}$ or GND |                                        |     | ±200 mA |
| $T_{stg}$               | Storage temperature range                  | - 65                                   | 150 | °C      |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 4.2 ESD Ratings

|                                                                                                       | VALUE | UNIT |
|-------------------------------------------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ Electrostatic discharge Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup> | ±2000 | V    |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 4.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                       |                                    |                                            | $T_A = 25^\circ\text{C}$ |          | $-55^\circ\text{C to } 125^\circ\text{C}$ |          | $-40^\circ\text{C to } 85^\circ\text{C}$ |          | UNIT |
|-----------------------|------------------------------------|--------------------------------------------|--------------------------|----------|-------------------------------------------|----------|------------------------------------------|----------|------|
|                       |                                    |                                            | MIN                      | MAX      | MIN                                       | MAX      | MIN                                      | MAX      |      |
| $V_{CC}$              | Supply voltage                     |                                            | 1.5                      | 5.5      | 1.5                                       | 5.5      | 1.5                                      | 5.5      | V    |
| $V_{IH}$              | High-level input voltage           | $V_{CC} = 1.5 \text{ V}$                   | 1.2                      |          | 1.2                                       |          | 1.2                                      |          | V    |
|                       |                                    | $V_{CC} = 3 \text{ V}$                     | 2.1                      |          | 2.1                                       |          | 2.1                                      |          |      |
|                       |                                    | $V_{CC} = 5.5 \text{ V}$                   | 3.85                     |          | 3.85                                      |          | 3.85                                     |          |      |
| $V_{IL}$              | Low-level input voltage            | $V_{CC} = 1.5 \text{ V}$                   |                          | 0.3      |                                           | 0.3      |                                          | 0.3      | V    |
|                       |                                    | $V_{CC} = 3 \text{ V}$                     |                          | 0.9      |                                           | 0.9      |                                          | 0.9      |      |
|                       |                                    | $V_{CC} = 5.5 \text{ V}$                   |                          | 1.65     |                                           | 1.65     |                                          | 1.65     |      |
| $V_I$                 | Input voltage                      |                                            | 0                        | $V_{CC}$ | 0                                         | $V_{CC}$ | 0                                        | $V_{CC}$ | V    |
| $V_O$                 | Output voltage                     |                                            | 0                        | $V_{CC}$ | 0                                         | $V_{CC}$ | 0                                        | $V_{CC}$ | V    |
| $I_{OH}$              | High-level output current          | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ |                          | -24      |                                           | -24      |                                          | -24      | mA   |
| $I_{OL}$              | Low-level output current           | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ |                          | 24       |                                           | 24       |                                          | 24       | mA   |
| $\Delta t / \Delta v$ | Input transition rise or fall rate | $V_{CC} = 1.5 \text{ V to } 3 \text{ V}$   |                          | 50       |                                           | 50       |                                          | 50       | ns/V |
|                       |                                    | $V_{CC} = 3.6 \text{ V to } 5.5 \text{ V}$ |                          | 20       |                                           | 20       |                                          | 20       |      |

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 4.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                        | CD74AC238  |          |            | UNIT |
|-------------------------------|----------------------------------------|------------|----------|------------|------|
|                               |                                        | BQB (WQFN) | D (SOIC) | PW (TSSOP) |      |
|                               |                                        | 16 PINS    | 16 PINS  | 16 PINS    |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance | 83.9       | 106.6    | 126.2      | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS                                |                                 | $V_{CC}$ | $T_A = 25^\circ\text{C}$ |           | $-55^\circ\text{C to } 125^\circ\text{C}$ |         | $-40^\circ\text{C to } 85^\circ\text{C}$ |         | UNIT          |
|-----------|------------------------------------------------|---------------------------------|----------|--------------------------|-----------|-------------------------------------------|---------|------------------------------------------|---------|---------------|
|           |                                                |                                 |          | MIN                      | MAX       | MIN                                       | MAX     | MIN                                      | MAX     |               |
| $V_{OH}$  | $V_I = V_{IH} \text{ or } V_{IL}$              | $I_{OH} = -50 \mu\text{A}$      | 1.5 V    | 1.4                      |           | 1.4                                       |         | 1.4                                      |         | V             |
|           |                                                |                                 | 3 V      | 2.9                      |           | 2.9                                       |         | 2.9                                      |         |               |
|           |                                                |                                 | 4.5 V    | 4.4                      |           | 4.4                                       |         | 4.4                                      |         |               |
|           |                                                | $I_{OH} = -4 \text{ mA}$        | 3 V      | 2.58                     |           | 2.4                                       |         | 2.48                                     |         |               |
|           |                                                | $I_{OH} = -24 \text{ mA}$       | 4.5 V    | 3.94                     |           | 3.7                                       |         | 3.8                                      |         |               |
|           |                                                | $I_{OH} = -50 \text{ mA}^{(1)}$ | 5.5 V    |                          |           | 3.85                                      |         |                                          |         |               |
| $V_{OL}$  | $V_I = V_{IH} \text{ or } V_{IL}$              | $I_{OL} = 50 \mu\text{A}$       | 1.5 V    |                          | 0.1       |                                           | 0.1     |                                          | 0.1     | V             |
|           |                                                |                                 | 3 V      |                          | 0.1       |                                           | 0.1     |                                          | 0.1     |               |
|           |                                                |                                 | 4.5 V    |                          | 0.1       |                                           | 0.1     |                                          | 0.1     |               |
|           |                                                | $I_{OL} = 12 \text{ mA}$        | 3 V      |                          | 0.36      |                                           | 0.5     |                                          | 0.44    |               |
|           |                                                | $I_{OL} = 24 \text{ mA}$        | 4.5 V    |                          | 0.36      |                                           | 0.5     |                                          | 0.44    |               |
|           |                                                | $I_{OL} = 50 \text{ mA}^{(1)}$  | 5.5 V    |                          |           |                                           | 1.65    |                                          |         |               |
| $I_I$     | $V_I = V_{CC} \text{ or } \text{GND}$          |                                 | 5.5 V    |                          | $\pm 0.1$ |                                           | $\pm 1$ |                                          | $\pm 1$ | $\mu\text{A}$ |
| $I_{CC}$  | $V_I = V_{CC} \text{ or } \text{GND}, I_O = 0$ |                                 | 5.5 V    |                          | 8         |                                           | 160     |                                          | 80      | $\mu\text{A}$ |
| $C_i$     |                                                |                                 |          |                          | 10        |                                           | 10      |                                          | 10      | pF            |

(1) Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50- $\Omega$  transmission-line drive capability at 85°C and 75- $\Omega$  transmission-line drive capability at 125°C.

## 4.6 Switching Characteristics, $V_{CC} = 1.5 \text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 1.5 \text{ V}$ ,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $-55^\circ\text{C to } 125^\circ\text{C}$ |     | $-40^\circ\text{C to } 85^\circ\text{C}$ |     | UNIT |
|-----------|--------------|-------------|-------------------------------------------|-----|------------------------------------------|-----|------|
|           |              |             | MIN                                       | MAX | MIN                                      | MAX |      |
| $t_{PLH}$ | A, B, C      | Any Y       |                                           | 187 |                                          | 170 | ns   |
| $t_{PHL}$ |              |             |                                           | 187 |                                          | 170 |      |
| $t_{PLH}$ | G1           | Any Y       |                                           | 208 |                                          | 189 | ns   |
| $t_{PHL}$ |              |             |                                           | 208 |                                          | 189 |      |
| $t_{PLH}$ | G2A, G2B     | Any Y       |                                           | 149 |                                          | 135 | ns   |
| $t_{PHL}$ |              |             |                                           | 149 |                                          | 135 |      |

#### 4.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER | FROM (INPUT)                     | TO (OUTPUT) | -55°C to 125°C |      | -40°C to 85°C |      | UNIT |
|-----------|----------------------------------|-------------|----------------|------|---------------|------|------|
|           |                                  |             | MIN            | MAX  | MIN           | MAX  |      |
| $t_{PLH}$ | A, B, C                          | Any Y       | 5.3            | 21   | 5.4           | 19.1 | ns   |
| $t_{PHL}$ |                                  |             | 5.3            | 21   | 5.4           | 19.1 |      |
| $t_{PLH}$ | G1                               | Any Y       | 5.8            | 23.2 | 6             | 21.1 | ns   |
| $t_{PHL}$ |                                  |             | 5.8            | 23.2 | 6             | 21.1 |      |
| $t_{PLH}$ | $\overline{G}2A, \overline{G}2B$ | Any Y       | 4.2            | 16.7 | 4.3           | 15.2 | ns   |
| $t_{PHL}$ |                                  |             | 4.2            | 16.7 | 4.3           | 15.2 |      |

#### 4.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ ,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

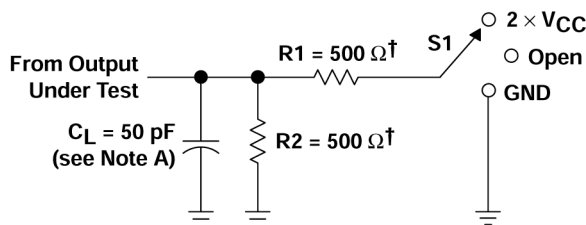
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -55°C to 125°C |      | -40°C to 85°C |      | UNIT |
|-----------|--------------|-------------|----------------|------|---------------|------|------|
|           |              |             | MIN            | MAX  | MIN           | MAX  |      |
| $t_{PLH}$ | A, B, C      | Any Y       | 3.8            | 15   | 3.9           | 13.6 | ns   |
| $t_{PHL}$ |              |             | 3.8            | 15   | 3.9           | 13.6 |      |
| $t_{PLH}$ | G1           | Any Y       | 4.2            | 16.6 | 4.3           | 15.1 | ns   |
| $t_{PHL}$ |              |             | 4.2            | 16.6 | 4.3           | 15.1 |      |
| $t_{PLH}$ | G2A, G2B     | Any Y       | 3              | 11.9 | 3.1           | 10.7 | ns   |
| $t_{PHL}$ |              |             | 3              | 11.9 | 3.1           | 10.7 |      |

#### 4.9 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

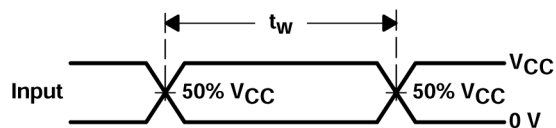
| PARAMETER |                               | TYP | UNIT |
|-----------|-------------------------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance | 110 | pF   |

## 5 Parameter Measurement Information

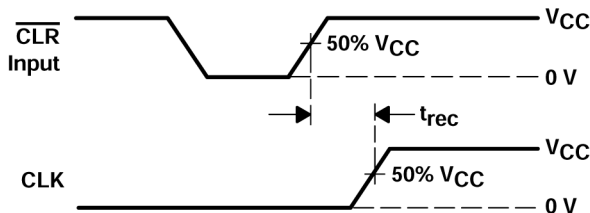


$^\dagger$  When  $V_{CC} = 1.5 \text{ V}$ ,  $R1 = R2 = 1 \text{ k}\Omega$

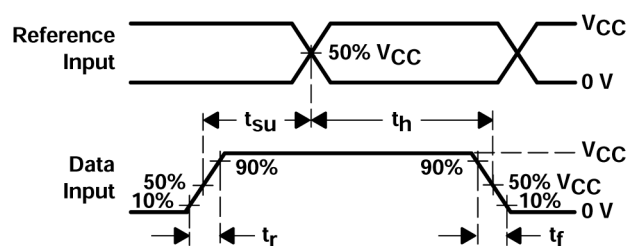
LOAD CIRCUIT



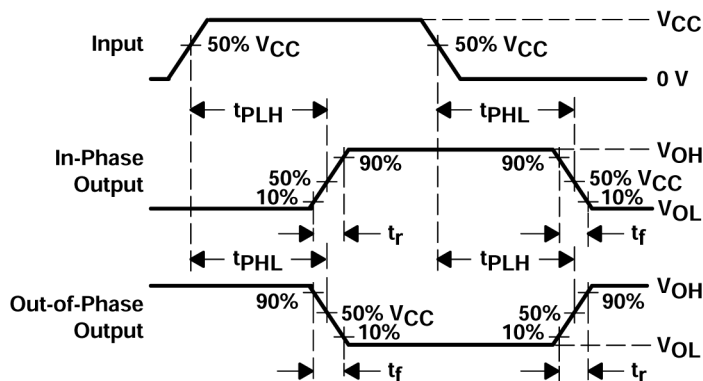
VOLTAGE WAVEFORMS  
PULSE DURATION



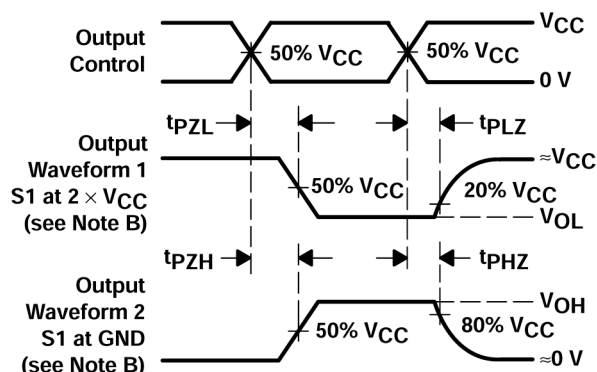
VOLTAGE WAVEFORMS  
RECOVERY TIME



VOLTAGE WAVEFORMS  
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS  
OUTPUT ENABLE AND DISABLE TIMES

- $C_L$  includes probe and test-fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ . Phase relationships between waveforms are arbitrary.
- For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.
- The outputs are measured one at a time with one input transition per measurement.
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- All parameters and waveforms are not applicable to all devices.

图 5-1. Load Circuit and Voltage Waveforms

| TEST              | S1                |
|-------------------|-------------------|
| $t_{PLH}/t_{PHL}$ | Open              |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND               |

## 6 Detailed Description

### 6.1 Overview

When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications (see Application Information).

### 6.2 Functional Block Diagram

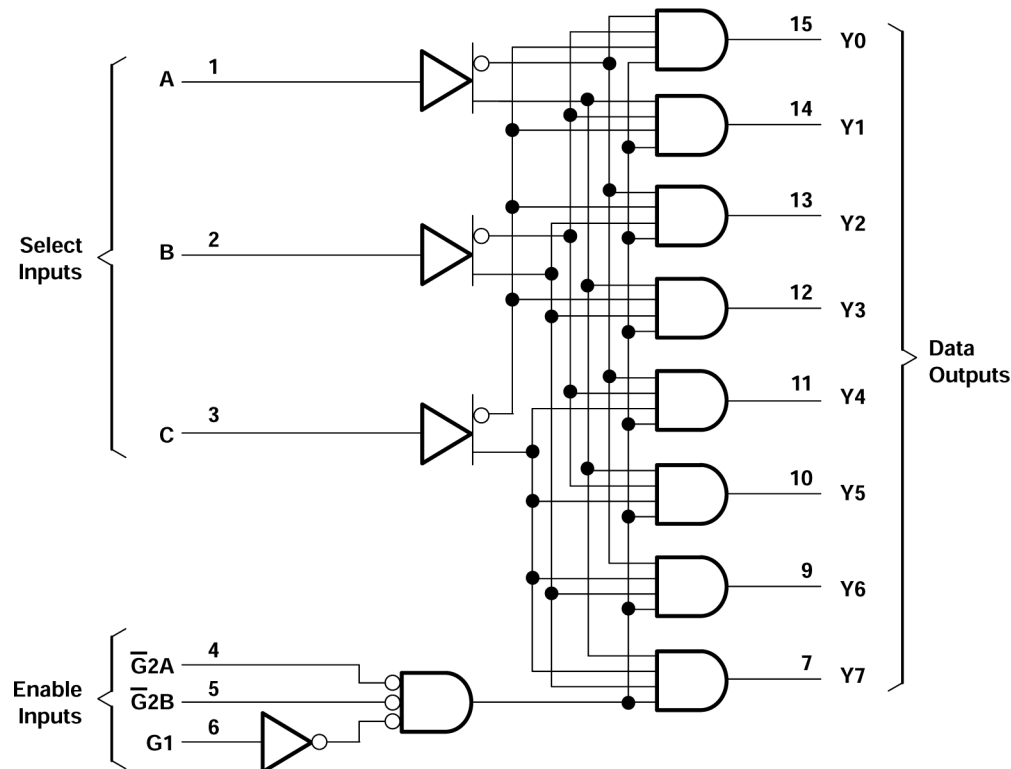


图 6-1. Logic Diagram (Positive Logic)

### 6.3 Device Functional Modes

表 6-1. Function Table

| ENABLE INPUTS |     |     | SELECT INPUTS |   |   | OUTPUTS |    |    |    |    |    |    |    |
|---------------|-----|-----|---------------|---|---|---------|----|----|----|----|----|----|----|
| G1            | G2A | G2B | C             | B | A | Y0      | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X             | H   | X   | X             | X | X | L       | L  | L  | L  | L  | L  | L  | L  |
| X             | X   | H   | X             | X | X | L       | L  | L  | L  | L  | L  | L  | L  |
| L             | X   | X   | X             | X | X | L       | L  | L  | L  | L  | L  | L  | L  |
| H             | L   | L   | L             | L | L | H       | L  | L  | L  | L  | L  | L  | L  |
| H             | L   | L   | L             | L | H | L       | H  | L  | L  | L  | L  | L  | L  |
| H             | L   | L   | L             | H | L | L       | L  | H  | L  | L  | L  | L  | L  |
| H             | L   | L   | L             | H | H | L       | L  | L  | H  | L  | L  | L  | L  |
| H             | L   | L   | H             | L | L | L       | L  | L  | L  | H  | L  | L  | L  |

表 6-1. Function Table ( 续 )

| ENABLE INPUTS |                         |                         | SELECT INPUTS |   |   | OUTPUTS |    |    |    |    |    |    |    |
|---------------|-------------------------|-------------------------|---------------|---|---|---------|----|----|----|----|----|----|----|
| G1            | $\overline{\text{G2A}}$ | $\overline{\text{G2B}}$ | C             | B | A | Y0      | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| H             | L                       | L                       | H             | L | H | L       | L  | L  | L  | L  | H  | L  | L  |
| H             | L                       | L                       | H             | H | L | L       | L  | L  | L  | L  | L  | H  | L  |
| H             | L                       | L                       | H             | H | H | L       | L  | L  | L  | L  | L  | L  | H  |

## 7 Application Information

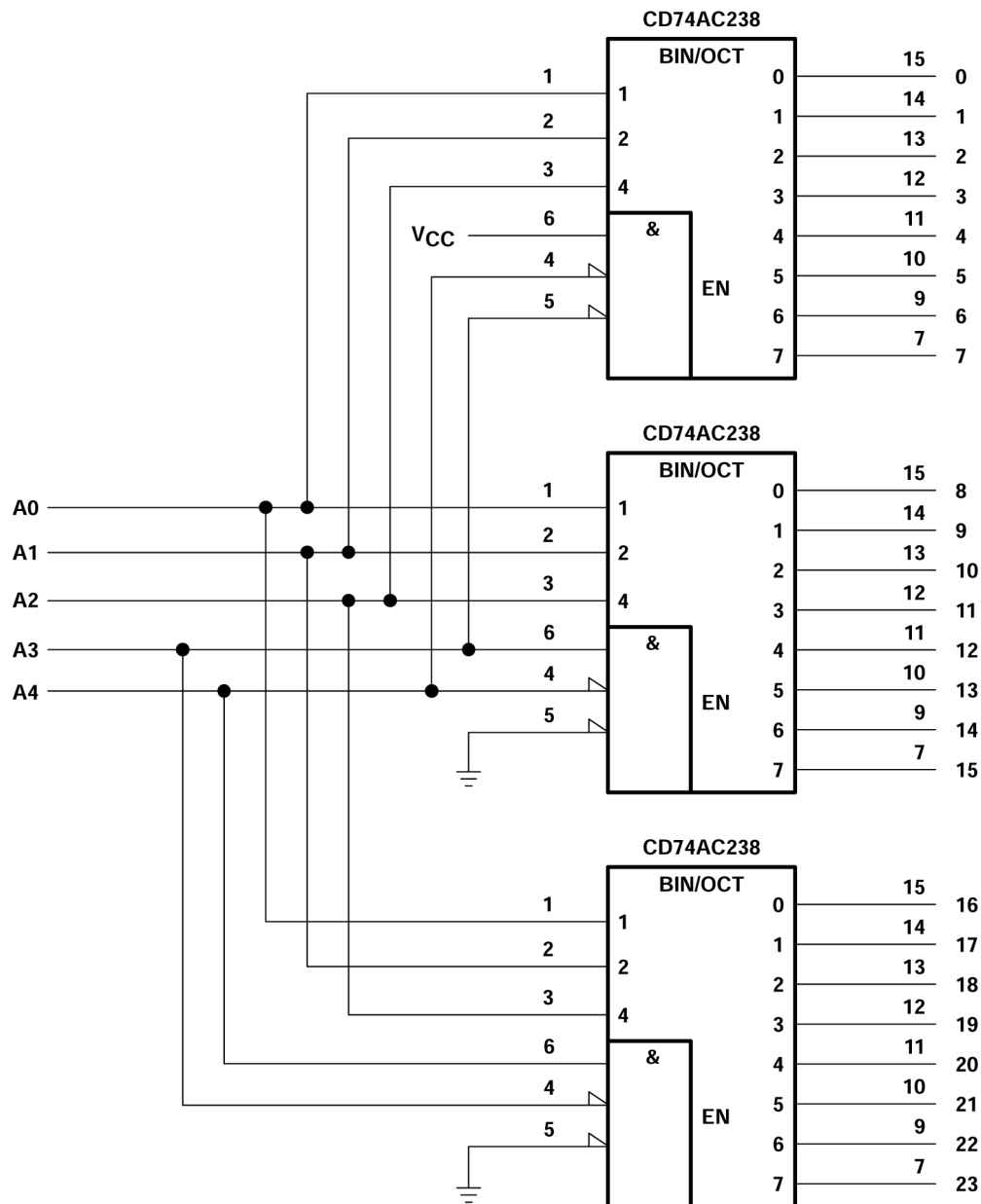


图 7-1. 24-Bit Decoding Scheme

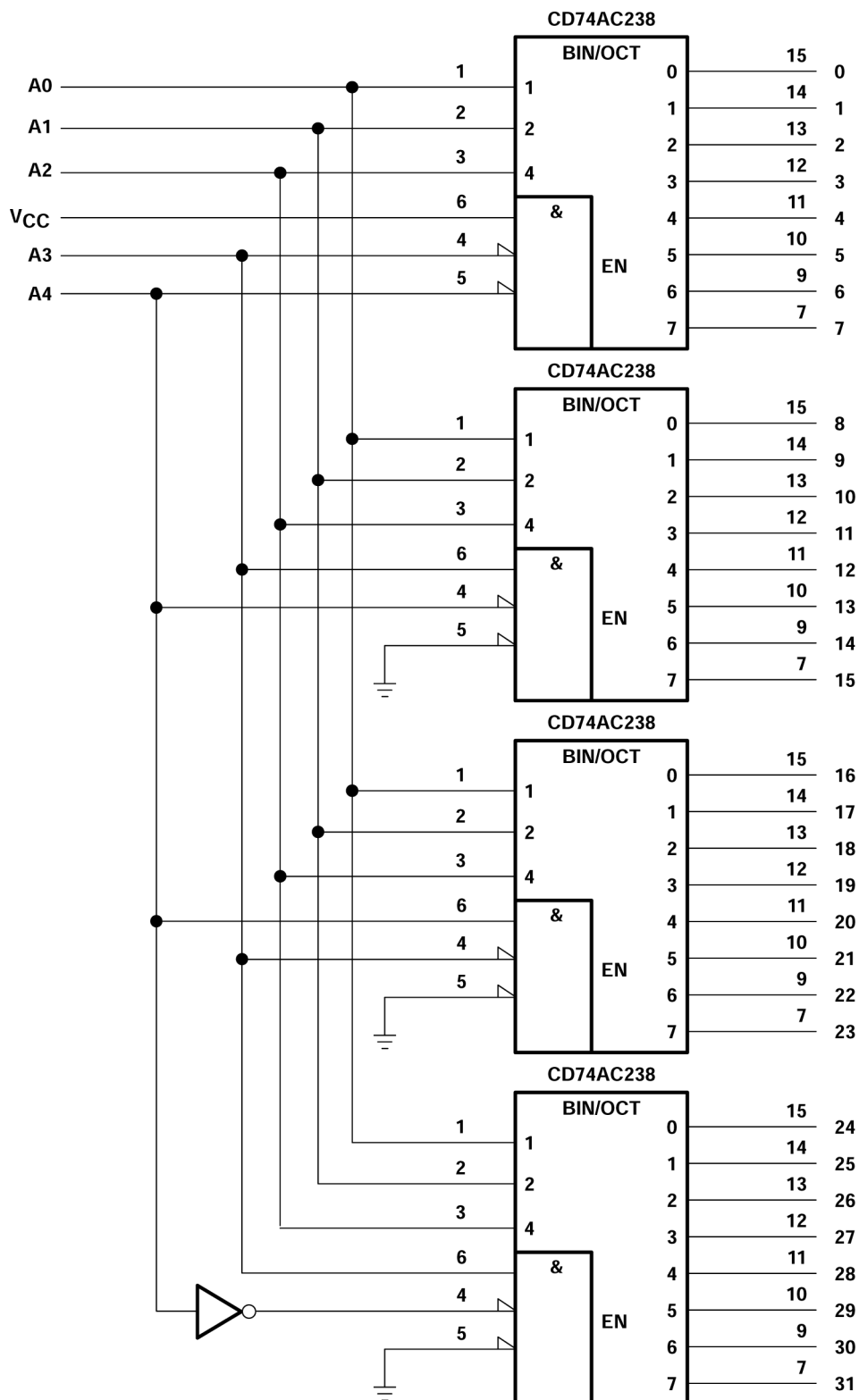


图 7-2. 32-Bit Decoding Scheme

## 7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A  $0.1\ \mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The  $0.1\ \mu\text{F}$  and  $1\ \mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 7.2 Layout

### 7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 7.2.2 Layout Example

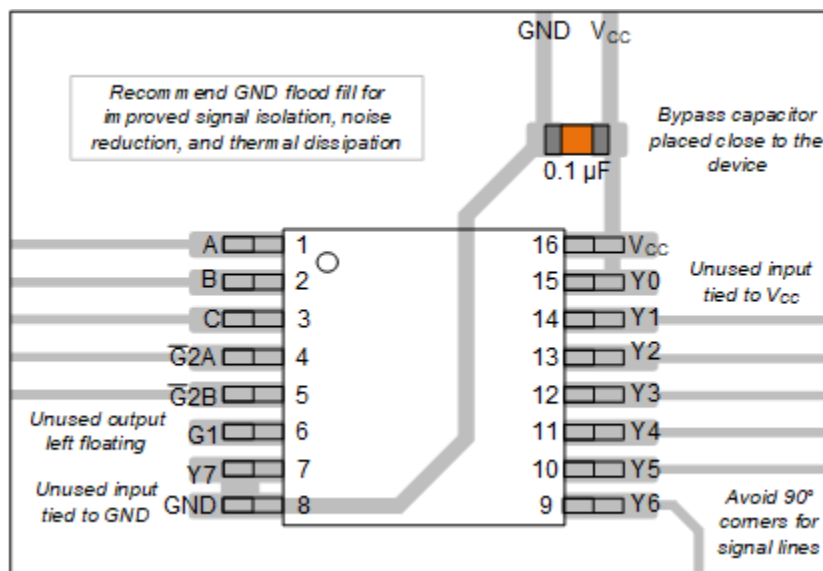


图 7-3. Example Layout for the CD74AC238

## 8 Device and Documentation Support

### 8.1 Documentation Support (Analog)

#### 8.1.1 Related Documentation

| PARTS     | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|-----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| CD74AC238 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 8.3 支持资源

**TI E2E™ 中文支持论坛** 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 8.4 Trademarks

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### 8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 8.6 术语表

**TI 术语表** 本术语表列出并解释了术语、首字母缩略词和定义。

## 9 Revision History

#### Changes from Revision A (April 2024) to Revision B (July 2024) Page

- 向 **封装信息表**、**引脚配置和功能** 部分以及 **热性能信息表** 中添加了 BQB 和 PW 封装..... [1](#)
- 将整个数据表中的所有 M 封装更改为 D 封装..... [1](#)

#### Changes from Revision \* (February 2003) to Revision A (April 2024) Page

- 添加了 **封装信息表**、**引脚功能表**、**ESD 等级表**、**热性能信息表**、**器件功能模式**、“应用和实施”部分、**器件和文档支持** 部分以及 **机械、封装和可订购信息** 部分..... [1](#)
- Updated R<sub>θJA</sub> values: M = 73 to 106.6, all values in °C/W ..... [5](#)

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CD74AC238BQBR</a> | Active        | Production           | WQFN (BQB)   16 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | AC238               |
| CD74AC238BQBR.A               | Active        | Production           | WQFN (BQB)   16 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | AC238               |
| <a href="#">CD74AC238M96</a>  | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | AC238M              |
| CD74AC238M96.A                | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | AC238M              |
| <a href="#">CD74AC238PWR</a>  | Active        | Production           | TSSOP (PW)   16 | 3000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 125   | AC238               |
| CD74AC238PWR.A                | Active        | Production           | TSSOP (PW)   16 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | AC238               |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74AC238BQBR | WQFN         | BQB             | 16   | 3000 | 180.0              | 12.4               | 2.8     | 3.8     | 1.2     | 4.0     | 12.0   | Q1            |
| CD74AC238M96  | SOIC         | D               | 16   | 2500 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |
| CD74AC238M96  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD74AC238PWR  | TSSOP        | PW              | 16   | 3000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

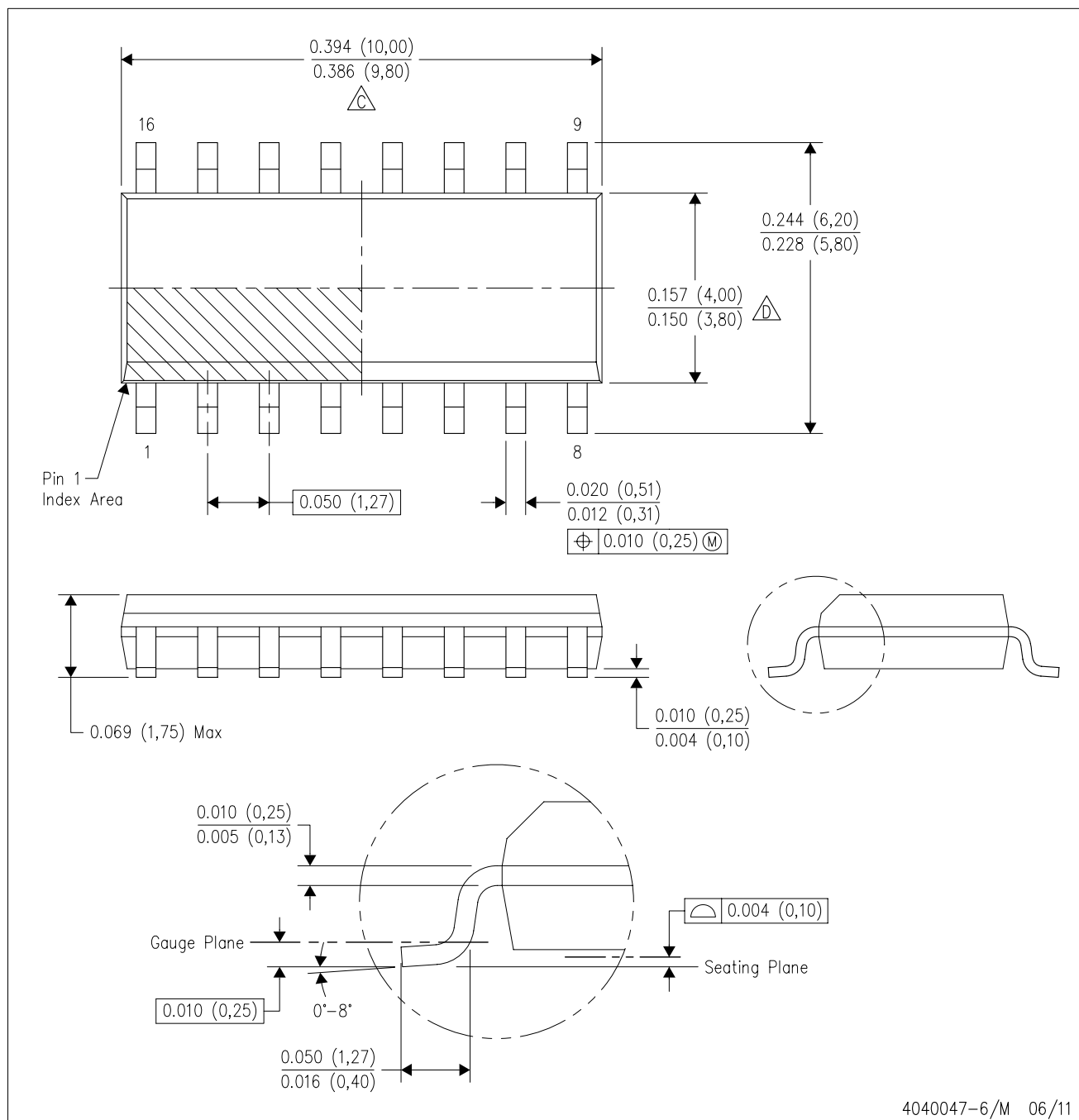


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74AC238BQBR | WQFN         | BQB             | 16   | 3000 | 210.0       | 185.0      | 35.0        |
| CD74AC238M96  | SOIC         | D               | 16   | 2500 | 340.5       | 336.1      | 32.0        |
| CD74AC238M96  | SOIC         | D               | 16   | 2500 | 353.0       | 353.0      | 32.0        |
| CD74AC238PWR  | TSSOP        | PW              | 16   | 3000 | 353.0       | 353.0      | 32.0        |

## D (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

## GENERIC PACKAGE VIEW

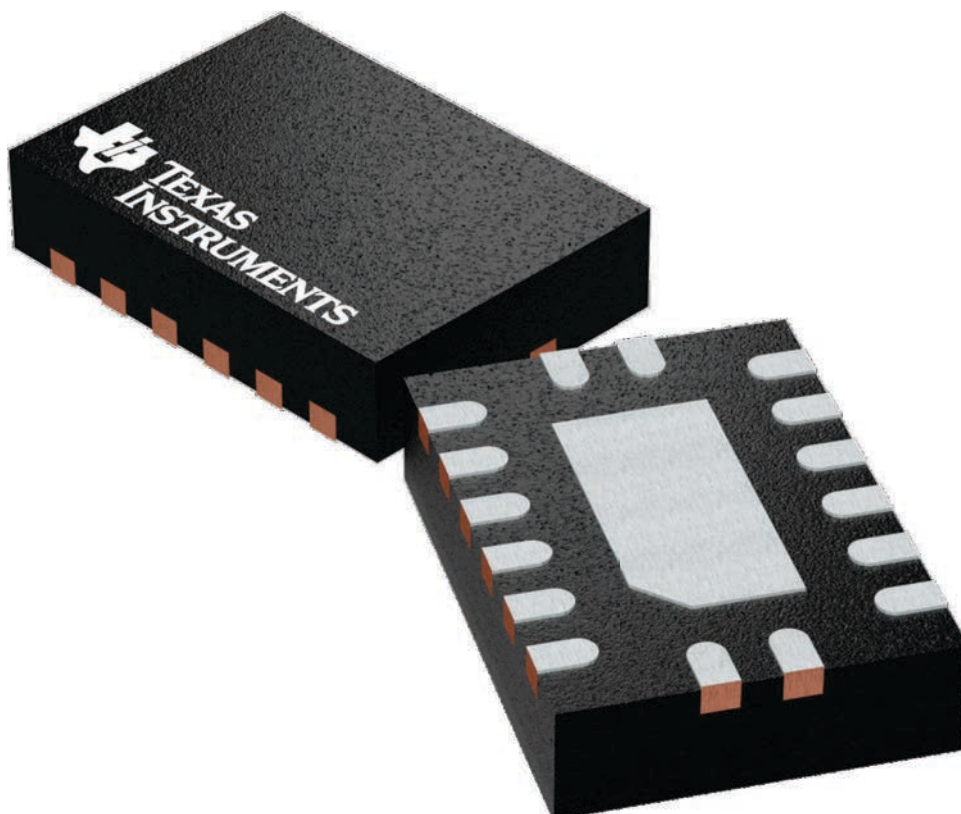
**BQB 16**

**WQFN - 0.8 mm max height**

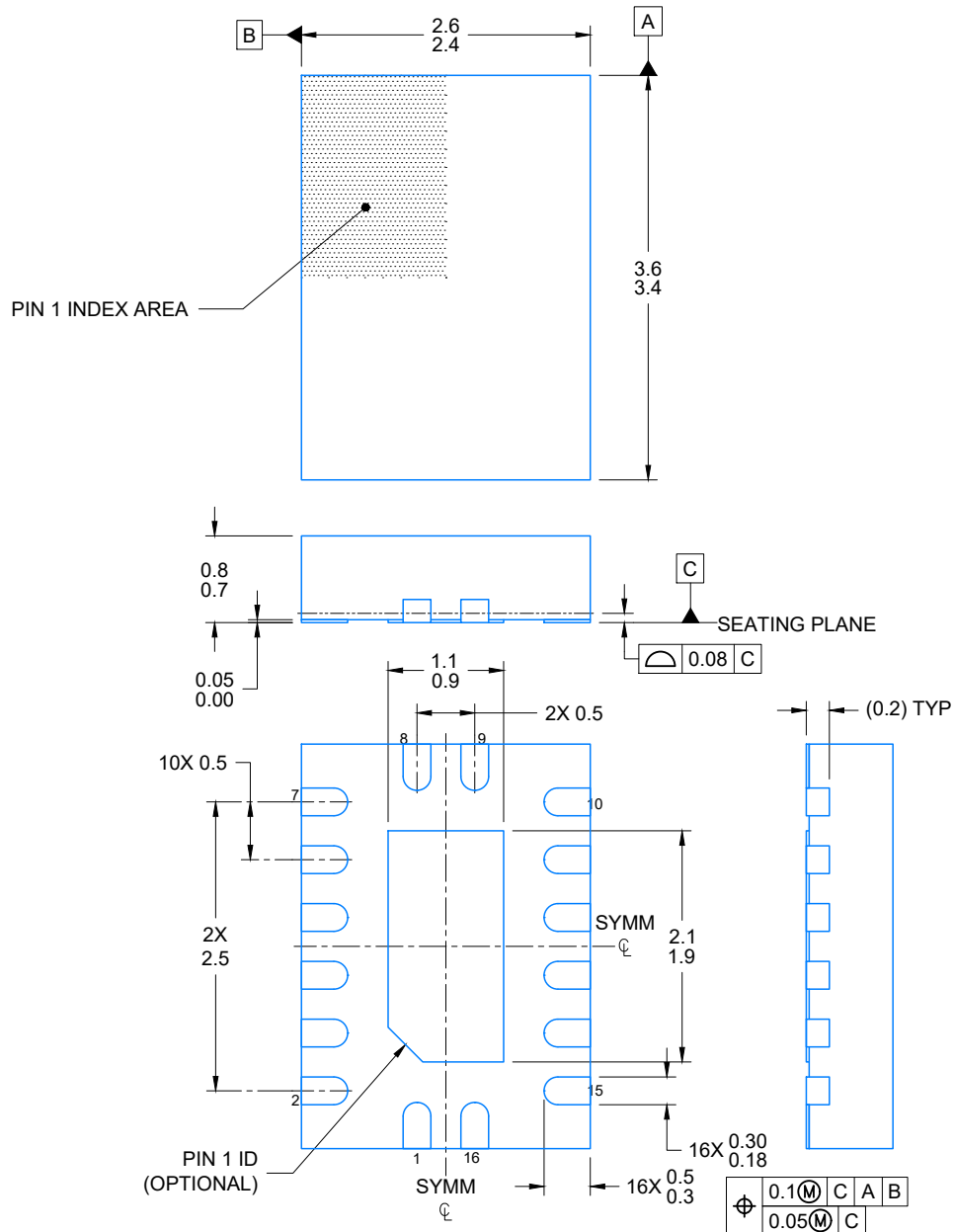
2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



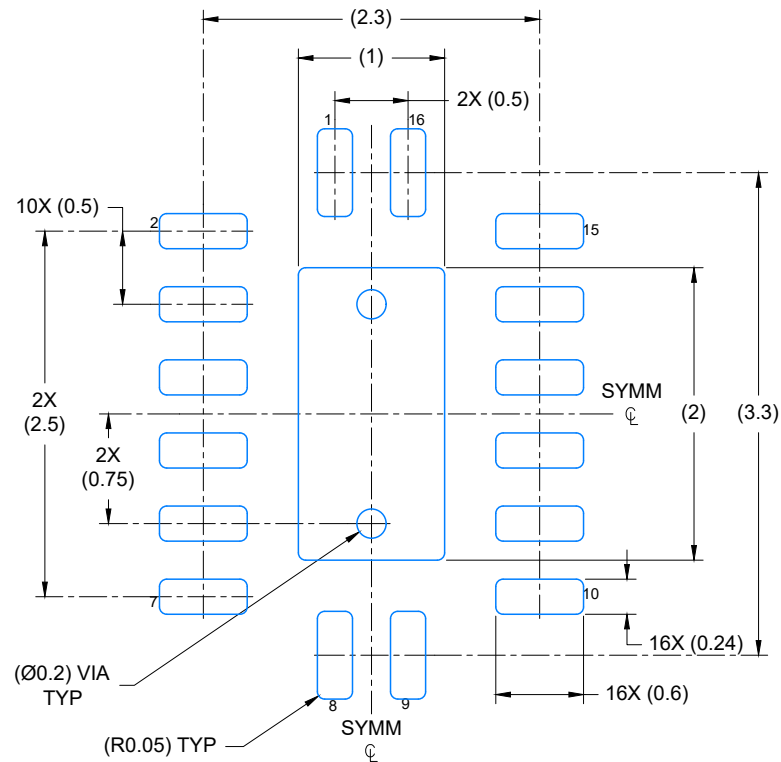
4226161/A



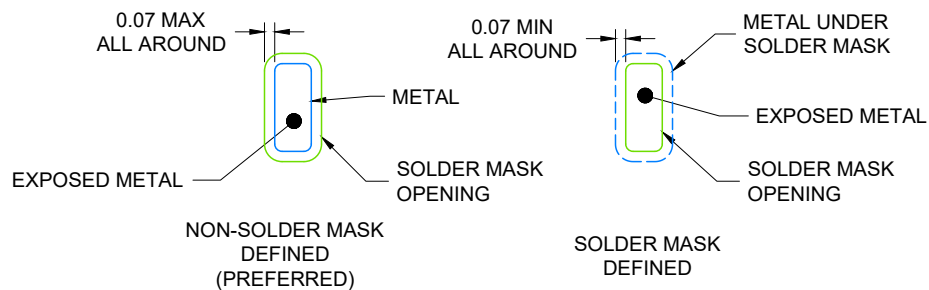
4224640/A 11/2018

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224640/A 11/2018

## NOTES: (continued)

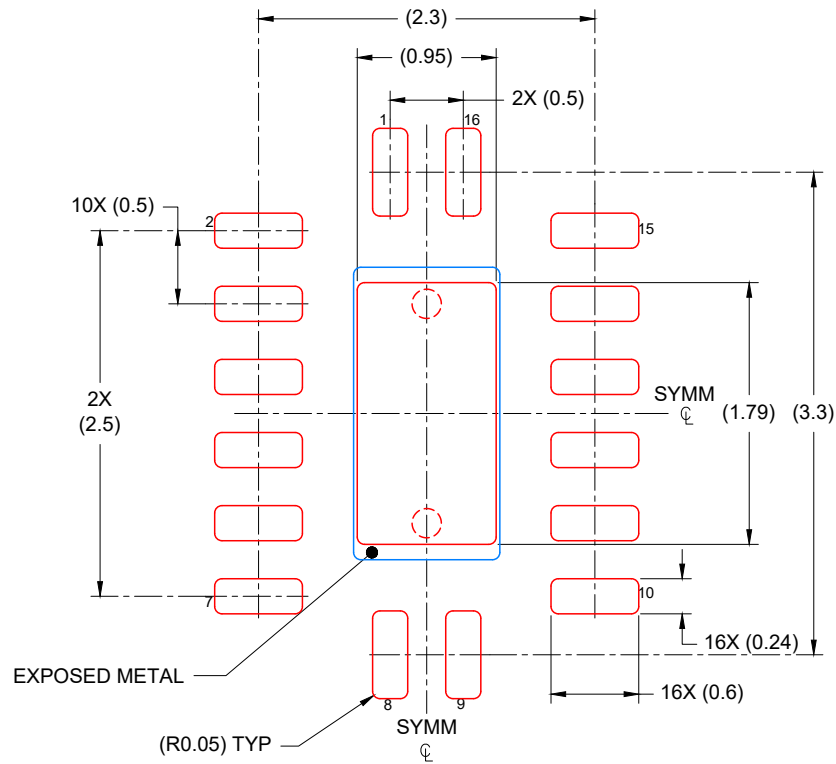
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

BQB0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



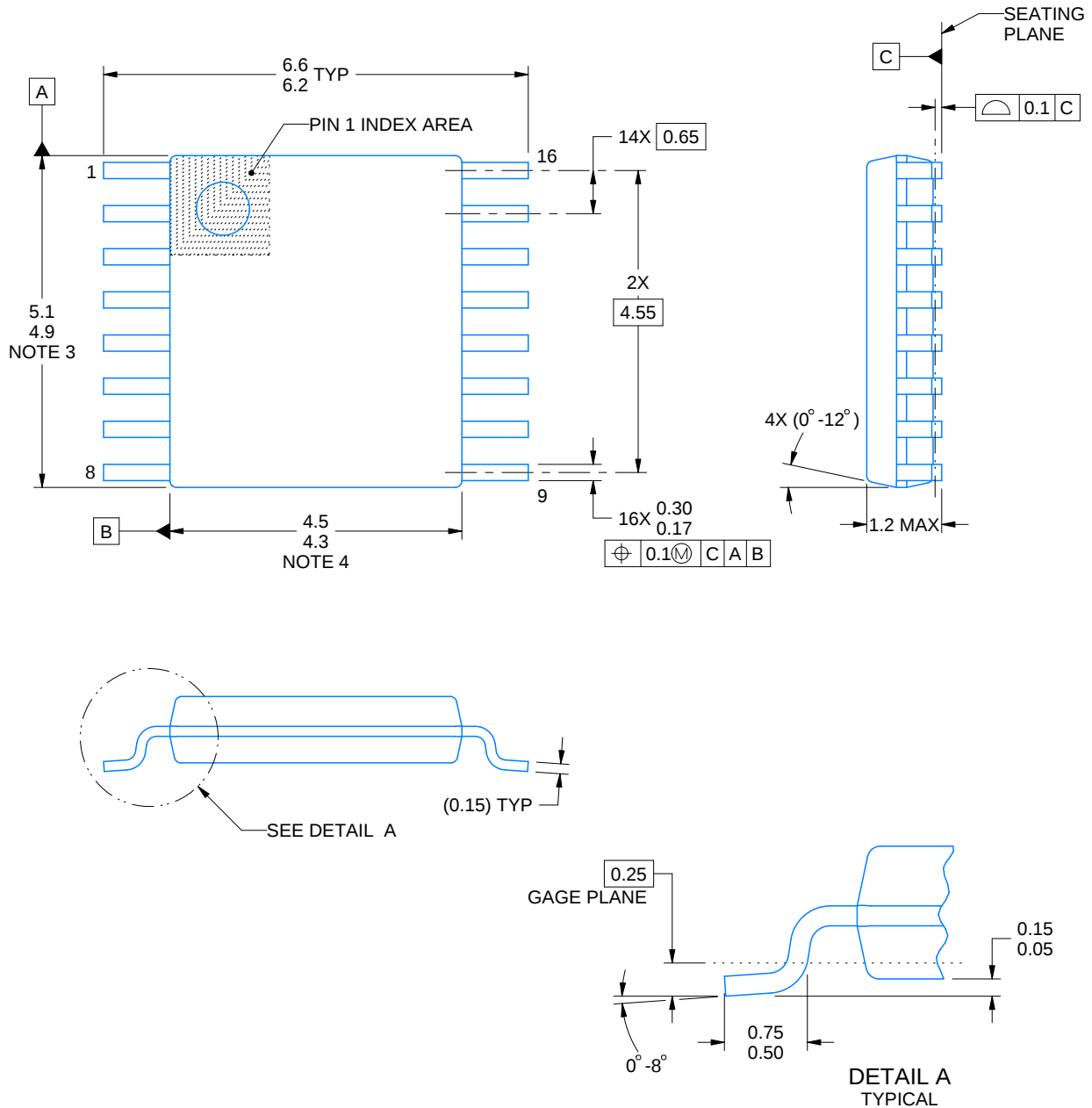
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
85% PRINTED COVERAGE BY AREA  
SCALE: 20X

4224640/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220204/B 12/2023

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

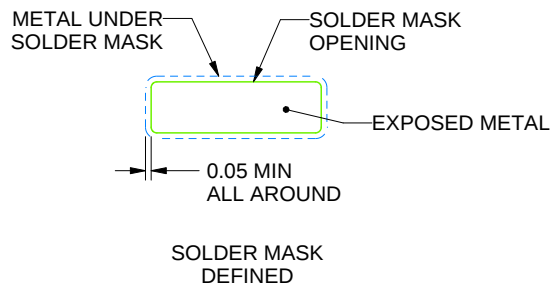
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月