

### Features

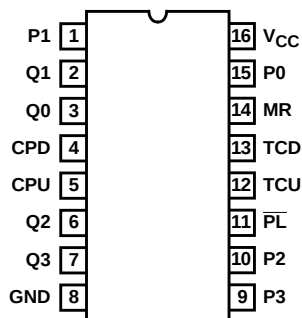
- Synchronous Counting and Asynchronous Loading
- Two Outputs for N-Bit Cascading
- Look-Ahead Carry for High-Speed Counting
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The 'HC192, 'HC193 and 'HCT193 are asynchronously presettable BCD Decade and Binary Up/Down synchronous counters, respectively.

### Pinout

CD54HC192, CD54HC193, CD54HCT193 (CERDIP)  
CD74HC192 (PDIP, SOP, TSSOP)  
CD74HC193 (PDIP, SOIC)  
CD74HCT193 (PDIP)  
TOP VIEW



Presetting the counter to the number on the preset data inputs (P0-P3) is accomplished by a LOW asynchronous parallel load input ( $\overline{PL}$ ). The counter is incremented on the low-to-high transition of the Clock-Up input (and a high level on the Clock-Down input) and decremented on the low to high transition of the Clock-Down input (and a high level on the Clock-up input). A high level on the MR input overrides any other input to clear the counter to its zero state. The Terminal Count up (carry) goes low half a clock period before the zero count is reached and returns to a high level at the zero count. The Terminal Count Down (borrow) in the count down mode likewise goes low half a clock period before the maximum count (9 in the 192 and 15 in the 193) and returns to high at the maximum count. Cascading is effected by connecting the carry and borrow outputs of a less significant counter to the Clock-Up and Clock-Down inputs, respectively, of the next most significant counter.

If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one count as shown in state diagram.

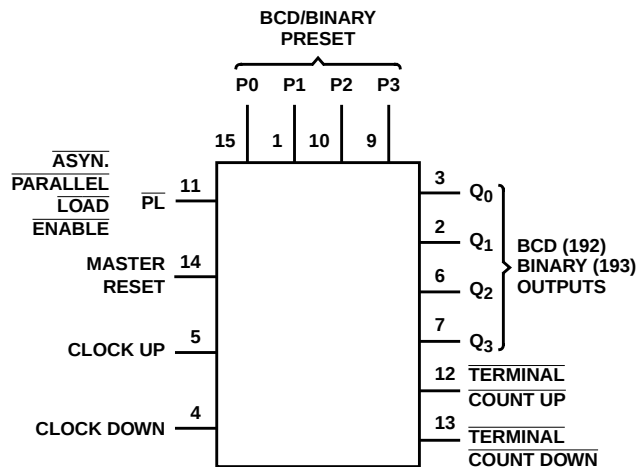
### Ordering Information

| PART NUMBER   | TEMP. RANGE (°C) | PACKAGE      |
|---------------|------------------|--------------|
| CD54HC192F3A  | -55 to 125       | 16 Ld CERDIP |
| CD54HC193F3A  | -55 to 125       | 16 Ld CERDIP |
| CD54HCT193F3A | -55 to 125       | 16 Ld CERDIP |
| CD74HC192E    | -55 to 125       | 16 Ld PDIP   |
| CD74HC192NSR  | -55 to 125       | 16 Ld SOP    |
| CD74HC192PW   | -55 to 125       | 16 Ld TSSOP  |
| CD74HC192PWR  | -55 to 125       | 16 Ld TSSOP  |
| CD74HC192PWT  | -55 to 125       | 16 Ld TSSOP  |
| CD74HC193E    | -55 to 125       | 16 Ld PDIP   |
| CD74HC193M    | -55 to 125       | 16 Ld SOIC   |
| CD74HC193MT   | -55 to 125       | 16 Ld SOIC   |
| CD74HC193M96  | -55 to 125       | 16 Ld SOIC   |
| CD74HCT193E   | -55 to 125       | 16 Ld PDIP   |

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

# CD54/74HC192, CD54/74HC193, CD54/74HCT193

## Functional Diagram



TRUTH TABLE

| CLOCK UP | CLOCK DOWN | RESET | PARALLEL LOAD | FUNCTION           |
|----------|------------|-------|---------------|--------------------|
| ↑        | H          | L     | H             | Count Up           |
| H        | ↑          | L     | H             | Count Down         |
| X        | X          | H     | X             | Reset              |
| X        | X          | L     | L             | Load Preset Inputs |

H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High Level

# CD54/74HC192, CD54/74HC193, CD54/74HCT193

## Absolute Maximum Ratings

DC Supply Voltage,  $V_{CC}$  ..... -0.5V to 7V  
 DC Input Diode Current,  $I_{IK}$   
 For  $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Diode Current,  $I_{OK}$   
 For  $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Source or Sink Current per Output Pin,  $I_O$   
 For  $V_O > -0.5V$  or  $V_O < V_{CC} + 0.5V$  .....  $\pm 25mA$   
 DC  $V_{CC}$  or Ground Current,  $I_{CC}$  or  $I_{GND}$  .....  $\pm 50mA$

## Thermal Information

Package Thermal Impedance,  $\theta_{JA}$  (see Note 1):  
 E (PDIP) Package .....  $67^{\circ}C/W$   
 M (SOIC) Package .....  $73^{\circ}C/W$   
 NS (SOP) Package .....  $64^{\circ}C/W$   
 PW (TSSOP) Package .....  $108^{\circ}C/W$   
 Maximum Junction Temperature .....  $150^{\circ}C$   
 Maximum Storage Temperature Range .....  $-65^{\circ}C$  to  $150^{\circ}C$   
 Maximum Lead Temperature (Soldering 10s) .....  $300^{\circ}C$   
 (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range ( $T_A$ ) .....  $-55^{\circ}C$  to  $125^{\circ}C$   
 Supply Voltage Range,  $V_{CC}$   
 HC Types ..... 2V to 6V  
 HCT Types ..... 4.5V to 5.5V  
 DC Input or Output Voltage,  $V_I$ ,  $V_O$  ..... 0V to  $V_{CC}$   
 Input Rise and Fall Time  
 2V ..... 1000ns (Max)  
 4.5V ..... 500ns (Max)  
 6V ..... 400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER                               | SYMBOL          | TEST CONDITIONS                       |                     |                     | 25°C |     |      | -40°C TO 85°C |      | -55°C TO 125°C |      | UNITS |
|-----------------------------------------|-----------------|---------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|------|-------|
|                                         |                 | V <sub>I</sub> (V)                    | I <sub>O</sub> (mA) | V <sub>CC</sub> (V) | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX  |       |
| HC TYPES                                |                 |                                       |                     |                     |      |     |      |               |      |                |      |       |
| High Level Input Voltage                | V <sub>IH</sub> | -                                     | -                   | 2                   | 1.5  | -   | -    | 1.5           | -    | 1.5            | -    | V     |
|                                         |                 |                                       |                     | 4.5                 | 3.15 | -   | -    | 3.15          | -    | 3.15           | -    | V     |
|                                         |                 |                                       |                     | 6                   | 4.2  | -   | -    | 4.2           | -    | 4.2            | -    | V     |
| Low Level Input Voltage                 | V <sub>IL</sub> | -                                     | -                   | 2                   | -    | -   | 0.5  | -             | 0.5  | -              | 0.5  | V     |
|                                         |                 |                                       |                     | 4.5                 | -    | -   | 1.35 | -             | 1.35 | -              | 1.35 | V     |
|                                         |                 |                                       |                     | 6                   | -    | -   | 1.8  | -             | 1.8  | -              | 1.8  | V     |
| High Level Output Voltage<br>CMOS Loads | V <sub>OH</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | -0.02               | 2                   | 1.9  | -   | -    | 1.9           | -    | 1.9            | -    | V     |
|                                         |                 |                                       | -0.02               | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -    | V     |
|                                         |                 |                                       | -0.02               | 6                   | 5.9  | -   | -    | 5.9           | -    | 5.9            | -    | V     |
| High Level Output Voltage<br>TTL Loads  | V <sub>OH</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | -4                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -    | V     |
|                                         |                 |                                       | -5.2                | 6                   | 5.48 | -   | -    | 5.34          | -    | 5.2            | -    | V     |
| Low Level Output Voltage<br>CMOS Loads  | V <sub>OL</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | 0.02                | 2                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                       | 0.02                | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                       | 0.02                | 6                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
| Low Level Output Voltage<br>TTL Loads   | V <sub>OL</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | 4                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |
|                                         |                 |                                       | 5.2                 | 6                   | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |
| Input Leakage Current                   | I <sub>I</sub>  | V <sub>CC</sub> or<br>GND             | -                   | 6                   | -    | -   | ±0.1 | -             | ±1   | -              | ±1   | μA    |
| Quiescent Device Current                | I <sub>CC</sub> | V <sub>CC</sub> or<br>GND             | 0                   | 6                   | -    | -   | 8    | -             | 80   | -              | 160  | μA    |

**CD54/74HC192, CD54/74HC193, CD54/74HCT193**

**DC Electrical Specifications (Continued)**

| PARAMETER                                                      | SYMBOL                    | TEST CONDITIONS                    |                     |                     | 25°C |     |      | -40°C TO 85°C |      | -55°C TO 125°C |     | UNITS |
|----------------------------------------------------------------|---------------------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
|                                                                |                           | V <sub>I</sub> (V)                 | I <sub>O</sub> (mA) | V <sub>CC</sub> (V) | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX |       |
| HCT TYPES                                                      |                           |                                    |                     |                     |      |     |      |               |      |                |     |       |
| High Level Input Voltage                                       | V <sub>IH</sub>           | -                                  | -                   | 4.5 to 5.5          | 2    | -   | -    | 2             | -    | 2              | -   | V     |
| Low Level Input Voltage                                        | V <sub>IL</sub>           | -                                  | -                   | 4.5 to 5.5          | -    | -   | 0.8  | -             | 0.8  | -              | 0.8 | V     |
| High Level Output Voltage<br>CMOS Loads                        | V <sub>OH</sub>           | V <sub>IH</sub> or V <sub>IL</sub> | -0.02               | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -   | V     |
| High Level Output Voltage<br>TTL Loads                         |                           |                                    | -4                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -   | V     |
| Low Level Output Voltage<br>CMOS Loads                         | V <sub>OL</sub>           | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1 | V     |
| Low Level Output Voltage<br>TTL Loads                          |                           |                                    | 4                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4 | V     |
| Input Leakage Current                                          | I <sub>I</sub>            | V <sub>CC</sub> to GND             | -                   | 5.5                 | -    | -   | ±0.1 | -             | ±1   | -              | ±1  | μA    |
| Quiescent Device Current                                       | I <sub>CC</sub>           | V <sub>CC</sub> or GND             | -                   | 5.5                 | -    | -   | 8    | -             | 80   | -              | 160 | μA    |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI <sub>CC</sub> (Note 2) | V <sub>CC</sub> - 2.1              | -                   | 4.5 to 5.5          | -    | 100 | 360  | -             | 450  | -              | 490 | μA    |

NOTE:

- For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

**HCT Input Loading Table**

| INPUT    | UNIT LOADS |
|----------|------------|
| P0-P3    | 0.4        |
| MR       | 1.45       |
| PL       | 0.85       |
| CPU, CPD | 1.45       |

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications table, e.g. 360µA max at 25°C.

# CD54/74HC192, CD54/74HC193, CD54/74HCT193

## Prerequisite For Switching Specifications

| PARAMETER                                           | SYMBOL           | V <sub>CC</sub><br>(V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|-----------------------------------------------------|------------------|------------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                                                     |                  |                        | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| HC TYPES                                            |                  |                        |      |     |     |               |     |                |     |       |
| Pulse Width<br>CPU, CPD<br>192                      | t <sub>W</sub>   | 2                      | 115  | -   | -   | 145           | -   | 175            | -   | ns    |
|                                                     |                  | 4.5                    | 23   | -   | -   | 29            | -   | 35             | -   | ns    |
|                                                     |                  | 6                      | 20   | -   | -   | 25            | -   | 30             | -   | ns    |
| CPU, CPD<br>193                                     | t <sub>W</sub>   | 2                      | 100  | -   | -   | 125           | -   | 150            | -   | ns    |
|                                                     |                  | 4.5                    | 20   | -   | -   | 25            | -   | 30             | -   | ns    |
|                                                     |                  | 6                      | 17   | -   | -   | 21            | -   | 26             | -   | ns    |
| $\overline{\text{PL}}$                              | t <sub>W</sub>   | 2                      | 80   | -   | -   | 100           | -   | 120            | -   | ns    |
|                                                     |                  | 4.5                    | 16   | -   | -   | 20            | -   | 24             | -   | ns    |
|                                                     |                  | 6                      | 14   | -   | -   | 17            | -   | 20             | -   | ns    |
| MR                                                  | t <sub>W</sub>   | 2                      | 100  | -   | -   | 125           | -   | 150            | -   | ns    |
|                                                     |                  | 4.5                    | 20   | -   | -   | 25            | -   | 30             | -   | ns    |
|                                                     |                  | 6                      | 17   | -   | -   | 21            | -   | 26             | -   | ns    |
| Set-up Time<br>Pn to $\overline{\text{PL}}$         | t <sub>SU</sub>  | 2                      | 80   | -   | -   | 100           | -   | 120            | -   | ns    |
|                                                     |                  | 4.5                    | 16   | -   | -   | 20            | -   | 24             | -   | ns    |
|                                                     |                  | 6                      | 14   | -   | -   | 17            | -   | 20             | -   | ns    |
| Hold Time<br>Pn to $\overline{\text{PL}}$           | t <sub>H</sub>   | 2                      | 0    | -   | -   | 0             | -   | 0              | -   | ns    |
|                                                     |                  | 4.5                    | 0    | -   | -   | 0             | -   | 0              | -   | ns    |
|                                                     |                  | 6                      | 0    | -   | -   | 0             | -   | 0              | -   | ns    |
| Hold Time<br>CPD to CPU or<br>CPU to CPD            | t <sub>H</sub>   | 2                      | 80   | -   | -   | 100           | -   | 120            | -   | ns    |
|                                                     |                  | 4.5                    | 16   | -   | -   | 20            | -   | 24             | -   | ns    |
|                                                     |                  | 6                      | 14   | -   | -   | 17            | -   | 20             | -   | ns    |
| Recovery Time<br>$\overline{\text{PL}}$ to CPU, CPD | t <sub>REC</sub> | 2                      | 80   | -   | -   | 100           | -   | 120            | -   | ns    |
|                                                     |                  | 4.5                    | 16   | -   | -   | 20            | -   | 24             | -   | ns    |
|                                                     |                  | 6                      | 14   | -   | -   | 17            | -   | 20             | -   | ns    |
| MR to CPU, CPD                                      | t <sub>REC</sub> | 2                      | 5    | -   | -   | 5             | -   | 5              | -   | ns    |
|                                                     |                  | 4.5                    | 5    | -   | -   | 5             | -   | 5              | -   | ns    |
|                                                     |                  | 6                      | 5    | -   | -   | 5             | -   | 5              | -   | ns    |
| Maximum Frequency<br>CPU, CPD<br>192                | f <sub>MAX</sub> | 2                      | 5    | -   | -   | 4             | -   | 3              | -   | MHz   |
|                                                     |                  | 4.5                    | 22   | -   | -   | 18            | -   | 15             | -   | MHz   |
|                                                     |                  | 6                      | 24   | -   | -   | 21            | -   | 18             | -   | MHz   |
| CPU, CPD<br>193                                     | f <sub>MAX</sub> | 2                      | 5    | -   | -   | 4             | -   | 3              | -   | MHz   |
|                                                     |                  | 4.5                    | 25   | -   | -   | 20            | -   | 17             | -   | MHz   |
|                                                     |                  | 6                      | 29   | -   | -   | 24            | -   | 20             | -   | MHz   |
| HCT TYPES                                           |                  |                        |      |     |     |               |     |                |     |       |
| Pulse Width<br>CPU, CPD<br>192                      | t <sub>W</sub>   | 2                      | -    | -   | -   | -             | -   | -              | -   | ns    |
|                                                     |                  | 4.5                    | 23   | -   | -   | 29            | -   | 35             | -   | ns    |
|                                                     |                  | 6                      | -    | -   | -   | -             | -   | -              | -   | ns    |
| CPU, CPD<br>193                                     | t <sub>W</sub>   | 2                      | -    | -   | -   | -             | -   | -              | -   | ns    |
|                                                     |                  | 4.5                    | 23   | -   | -   | 29            | -   | 35             | -   | ns    |
|                                                     |                  | 6                      | -    | -   | -   | -             | -   | -              | -   | ns    |

**CD54/74HC192, CD54/74HC193, CD54/74HCT193**

**Prerequisite For Switching Specifications (Continued)**

| PARAMETER                                               | SYMBOL    | V <sub>CC</sub><br>(V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|---------------------------------------------------------|-----------|------------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                                                         |           |                        | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| $\overline{\text{PL}}$                                  | $t_W$     | 2                      | -    | -   | -   | -             | -   | -              | -   | ns    |
|                                                         |           | 4.5                    | 16   | -   | -   | 20            | -   | 24             | -   | ns    |
|                                                         |           | 6                      | -    | -   | -   | -             | -   | -              | -   | ns    |
| MR                                                      | $t_W$     | 2                      | -    | -   | -   | -             | -   | -              | -   | ns    |
|                                                         |           | 4.5                    | 20   | -   | -   | 25            | -   | 30             | -   | ns    |
|                                                         |           | 6                      | -    | -   | -   | -             | -   | -              | -   | ns    |
| Set-up Time<br>P <sub>n</sub> to $\overline{\text{PL}}$ | $t_{SU}$  | 2                      | -    | -   | -   | -             | -   | -              | -   | ns    |
|                                                         |           | 4.5                    | 15   | -   | -   | 19            | -   | 22             | -   | ns    |
|                                                         |           | 6                      | -    | -   | -   | -             | -   | -              | -   | ns    |
| Hold Time<br>P <sub>n</sub> to $\overline{\text{PL}}$   | $t_H$     | 2                      | -    | -   | -   | -             | -   | -              | -   | ns    |
|                                                         |           | 4.5                    | 0    | -   | -   | 0             | -   | 0              | -   | ns    |
|                                                         |           | 6                      | -    | -   | -   | -             | -   | -              | -   | ns    |
| Hold Time<br>CPD to CPU or<br>CPU to CPD                | $t_H$     | 2                      | -    | -   | -   | -             | -   | -              | -   | ns    |
|                                                         |           | 4.5                    | 16   | -   | -   | 20            | -   | 24             | -   | ns    |
|                                                         |           | 6                      | -    | -   | -   | -             | -   | -              | -   | ns    |
| Recovery Time<br>$\overline{\text{PL}}$ to CPU, CPD     | $t_{REC}$ | 2                      | -    | -   | -   | -             | -   | -              | -   | ns    |
|                                                         |           | 4.5                    | 15   | -   | -   | 19            | -   | 22             | -   | ns    |
|                                                         |           | 6                      | -    | -   | -   | -             | -   | -              | -   | ns    |
| MR to CPU, CPD                                          | $t_{REC}$ | 2                      | -    | -   | -   | -             | -   | -              | -   | ns    |
|                                                         |           | 4.5                    | 5    | -   | -   | 5             | -   | 5              | -   | ns    |
|                                                         |           | 6                      | -    | -   | -   | -             | -   | -              | -   | ns    |
| Maximum Frequency<br>CPU, CPD<br>192                    | $f_{MAX}$ | 2                      | -    | -   | -   | -             | -   | -              | -   | MHz   |
|                                                         |           | 4.5                    | 22   | -   | -   | 18            | -   | 15             | -   | MHz   |
|                                                         |           | 6                      | -    | -   | -   | -             | -   | -              | -   | MHz   |
| CPU, CPD<br>193                                         | $f_{MAX}$ | 2                      | -    | -   | -   | -             | -   | -              | -   | MHz   |
|                                                         |           | 4.5                    | 22   | -   | -   | 18            | -   | 15             | -   | MHz   |
|                                                         |           | 6                      | -    | -   | -   | -             | -   | -              | -   | MHz   |

**Switching Specifications** Input  $t_r, t_f = 6\text{ns}$

| PARAMETER                                           | SYMBOL                           | TEST<br>CONDITIONS    | V <sub>CC</sub><br>(V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|-----------------------------------------------------|----------------------------------|-----------------------|------------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                                                     |                                  |                       |                        | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| HC TYPES                                            |                                  |                       |                        |      |     |     |               |     |                |     |       |
| Propagation Delay<br>CPU to $\overline{\text{TCU}}$ | $t_{\text{PLH}}, t_{\text{PHL}}$ | C <sub>L</sub> = 50pF | 2                      | -    | -   | 125 | -             | 155 | -              | 190 | ns    |
|                                                     |                                  | C <sub>L</sub> = 50pF | 4.5                    | -    | -   | 25  | -             | 31  | -              | 38  | ns    |
|                                                     |                                  | C <sub>L</sub> = 15pF | 5                      | -    | 10  | -   | -             | -   | -              | -   | ns    |
|                                                     |                                  | C <sub>L</sub> = 50pF | 6                      | -    |     | 21  | -             | 26  | -              | 32  | ns    |
| CPD to $\overline{\text{TCD}}$                      | $t_{\text{PLH}}, t_{\text{PHL}}$ | C <sub>L</sub> = 50pF | 2                      | -    | -   | 125 | -             | 155 | -              | 190 | ns    |
|                                                     |                                  | C <sub>L</sub> = 50pF | 4.5                    | -    | -   | 25  | -             | 31  | -              | 38  | ns    |
|                                                     |                                  | C <sub>L</sub> = 15pF | 5                      | -    | 10  | -   | -             | -   | -              | -   | ns    |
|                                                     |                                  | C <sub>L</sub> = 50pF | 6                      | -    | -   | 21  | -             | 26  | -              | 32  | ns    |
| CPU to Q <sub>n</sub>                               | $t_{\text{PLH}}, t_{\text{PHL}}$ | C <sub>L</sub> = 50pF | 2                      | -    | -   | 220 | -             | 270 | -              | 325 | ns    |
|                                                     |                                  | C <sub>L</sub> = 50pF | 4.5                    | -    | -   | 43  | -             | 54  | -              | 65  | ns    |
|                                                     |                                  | C <sub>L</sub> = 15pF | 5                      | -    | 18  | -   | -             | -   | -              | -   | ns    |
|                                                     |                                  | C <sub>L</sub> = 50pF | 6                      | -    | -   | 37  | -             | 46  | -              | 55  | ns    |

# CD54/74HC192, CD54/74HC193, CD54/74HCT193

## Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

| PARAMETER                                     | SYMBOL             | TEST CONDITIONS     | $V_{CC}$<br>(V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|-----------------------------------------------|--------------------|---------------------|-----------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                                               |                    |                     |                 | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| CPD to $Q_n$                                  | $t_{PLH}, t_{PHL}$ | $C_L = 50\text{pF}$ | 2               | -    | -   | 220 | -             | 270 | -              | 325 | ns    |
|                                               |                    | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 43  | -             | 54  | -              | 65  | ns    |
|                                               |                    | $C_L = 15\text{pF}$ | 5               | -    | 18  | -   | -             | -   | -              | -   | ns    |
|                                               |                    | $C_L = 50\text{pF}$ | 6               | -    | -   | 37  | -             | 46  | -              | 55  | ns    |
| $\overline{PL}$ to $Q_n$                      | $t_{PLH}, t_{PHL}$ | $C_L = 50\text{pF}$ | 2               | -    | -   | 220 | -             | 275 | -              | 330 | ns    |
|                                               |                    | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 44  | -             | 55  | -              | 66  | ns    |
|                                               |                    | $C_L = 15\text{pF}$ | 5               | -    | 18  | -   | -             | -   | -              | -   | ns    |
|                                               |                    | $C_L = 50\text{pF}$ | 6               | -    | -   | 37  | -             | 47  | -              | 56  | ns    |
| MR to $Q_n$                                   | $t_{PHL}$          | $C_L = 50\text{pF}$ | 2               | -    | -   | 200 | -             | 250 | -              | 300 | ns    |
|                                               |                    | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 40  | -             | 50  | -              | 60  | ns    |
|                                               |                    | $C_L = 15\text{pF}$ | 5               | -    | 17  | -   | -             | -   | -              | -   | ns    |
|                                               |                    | $C_L = 50\text{pF}$ | 6               | -    | -   | 34  | -             | 43  | -              | 51  | ns    |
| Transition Time<br>$Q, TCU, TCD$              | $t_{TLH}, t_{THL}$ | $C_L = 50\text{pF}$ | 2               | -    | -   | 75  | -             | 95  | -              | 110 | ns    |
|                                               |                    |                     | 4.5             | -    | -   | 15  | -             | 19  | -              | 22  | ns    |
|                                               |                    |                     | 6               | -    | -   | 13  | -             | 16  | -              | 19  | ns    |
| Input Capacitance                             | $C_{IN}$           | $C_L = 50\text{pF}$ | -               | -    | -   | 10  | -             | 10  | -              | 10  | pF    |
| Power Dissipation Capacitance<br>(Notes 3, 4) | $C_{PD}$           | $C_L = 15\text{pF}$ | 5               | -    | 40  | -   | -             | -   | -              | -   | pF    |
| <b>HCT TYPES</b>                              |                    |                     |                 |      |     |     |               |     |                |     |       |
| Propagation Delay<br>CPU to $\overline{TCU}$  | $t_{PLH}, t_{PHL}$ | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 27  | -             | 34  | -              | 41  | ns    |
|                                               |                    | $C_L = 15\text{pF}$ | 5               | -    | 11  | -   | -             | -   | -              | -   | ns    |
| CPU to $\overline{TCD}$                       | $t_{PLH}, t_{PHL}$ | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 27  | -             | 34  | -              | 41  | ns    |
|                                               |                    | $C_L = 15\text{pF}$ | 5               | -    | 11  | -   | -             | -   | -              | -   | ns    |
| CPU to $Q_n$                                  | $t_{PLH}, t_{PHL}$ | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 40  | -             | 50  | -              | 60  | ns    |
|                                               |                    | $C_L = 15\text{pF}$ | 5               | -    | 17  | -   | -             | -   | -              | -   | ns    |
| CPD to $Q_n$                                  | $t_{PLH}, t_{PHL}$ | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 40  | -             | 50  | -              | 60  | ns    |
|                                               |                    | $C_L = 15\text{pF}$ | 5               | -    | 17  | -   | -             | -   | -              | -   | ns    |
| $\overline{PL}$ to $Q_n$                      | $t_{PLH}, t_{PHL}$ | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 46  | -             | 58  | -              | 69  | ns    |
|                                               |                    | $C_L = 15\text{pF}$ | 5               | -    | 21  | -   | -             | -   | -              | -   | ns    |
| MR to $Q_n$                                   | $t_{PHL}$          | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 43  | -             | 54  | -              | 65  | ns    |
|                                               |                    | $C_L = 15\text{pF}$ | 5               | -    | 18  | -   | -             | -   | -              | -   | ns    |
| Transition Time<br>$Q, TCU, TCD$              | $t_{TLH}, t_{THL}$ | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 15  | -             | 19  | -              | 22  | ns    |
|                                               |                    |                     | 4.5             | -    | -   | 15  | -             | 19  | -              | 22  | ns    |
| Input Capacitance                             | $C_{IN}$           | $C_L = 50\text{pF}$ | -               | -    | -   | 10  | -             | 10  | -              | 10  | pF    |
| Power Dissipation Capacitance<br>(Notes 3, 4) | $C_{PD}$           | $C_L = 15\text{pF}$ | 5               | -    | 50  | -   | -             | -   | -              | -   | pF    |

### NOTES:

3.  $C_{PD}$  is used to determine the dynamic power consumption, per gate.
4.  $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2)$  where  $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

## Test Circuits and Waveforms

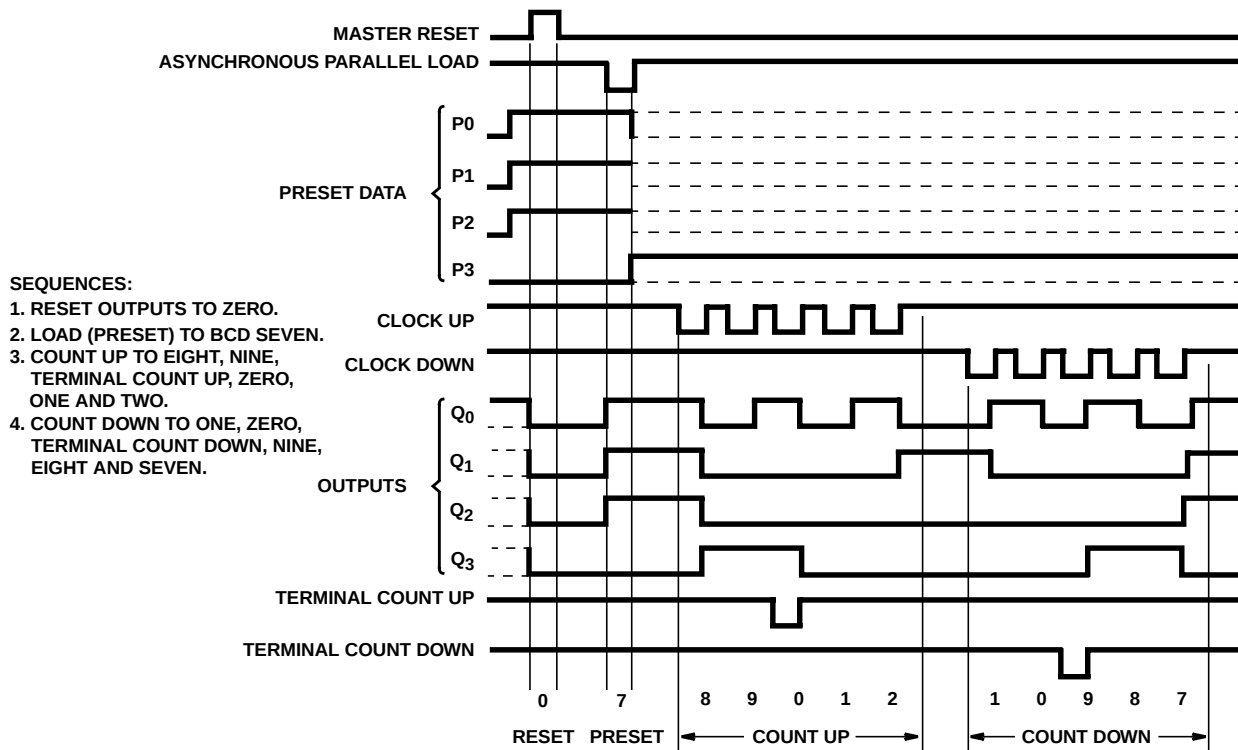


FIGURE 1. 'HC192 SYNCHRONOUS DECADE COUNTERS, TYPICAL RESET, PRESET AND COUNT SEQUENCES

# Test Circuits and Waveforms (Continued)

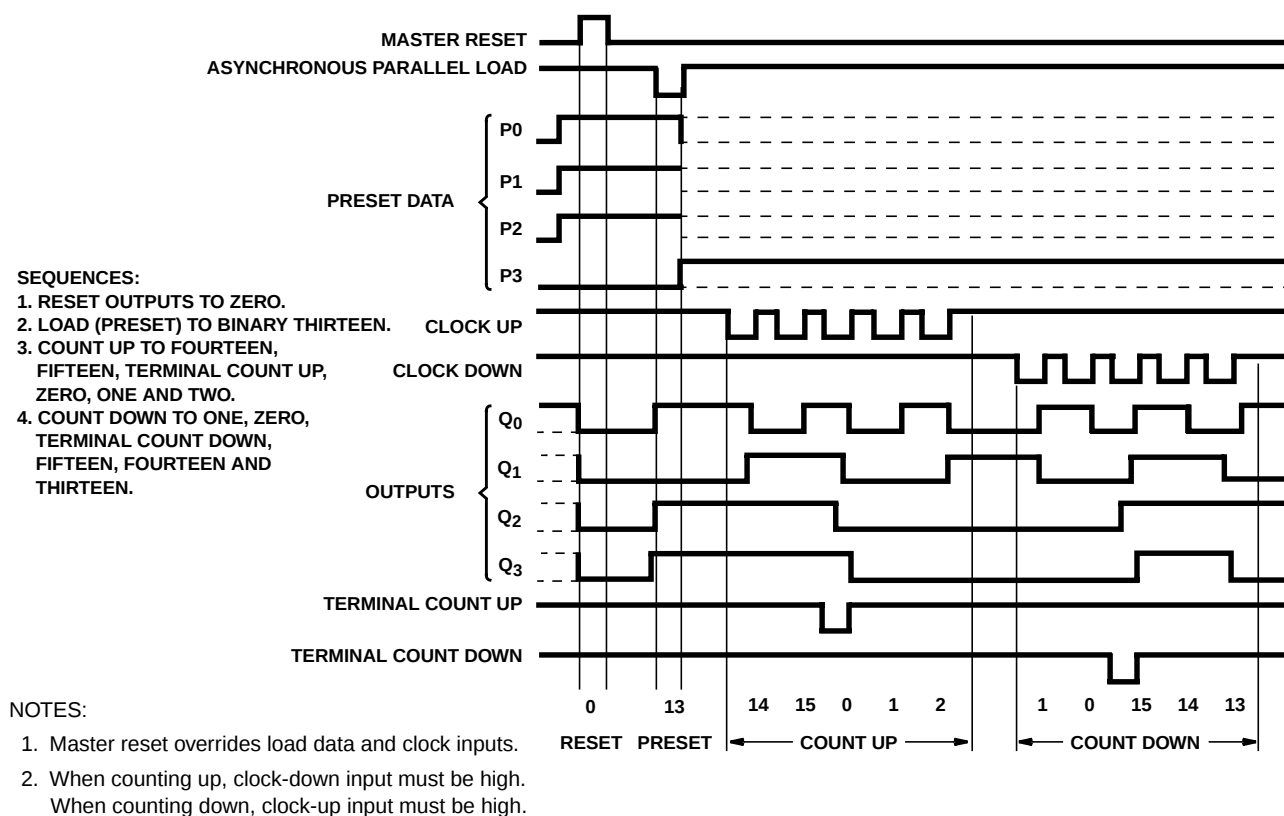


FIGURE 2. 'HC193 SYNCHRONOUS BINARY COUNTERS, TYPICAL RESET, PRESET AND COUNT SEQUENCES

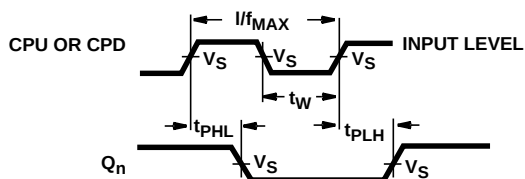


FIGURE 3. CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH

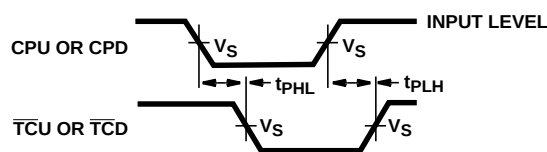


FIGURE 4. CLOCK TO TERMINAL COUNT DELAYS

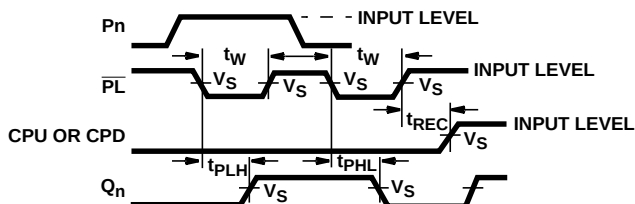


FIGURE 5. PARALLEL LOAD PULSE WIDTH, PARALLEL LOAD TO OUTPUT DELAYS, AND PARALLEL LOAD TO CLOCK RECOVERY TIME

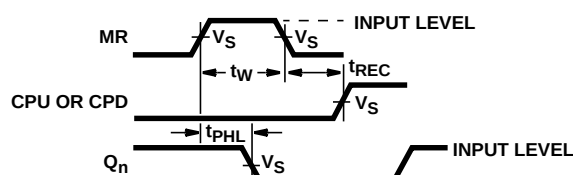
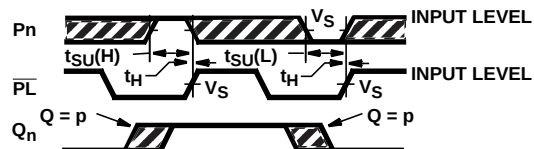
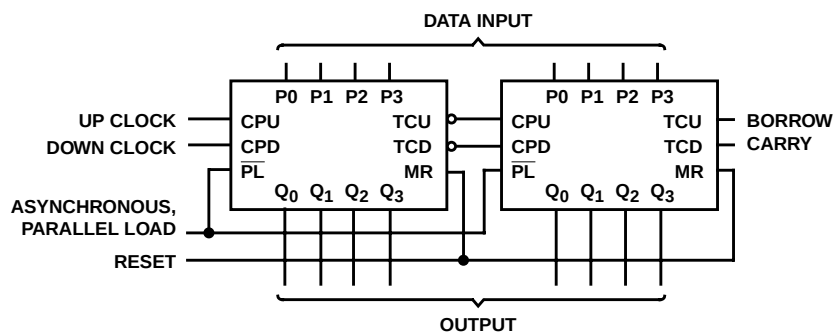


FIGURE 6. MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME

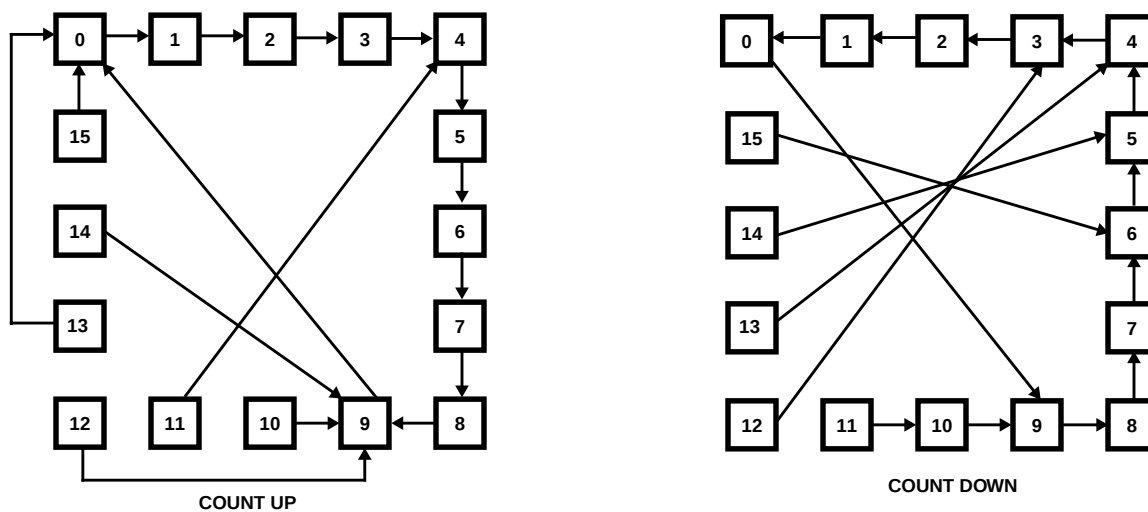
### Test Circuits and Waveforms (Continued)



**FIGURE 7. SET-UP AND HOLD TIMES DATA TO PARALLEL LOAD (PL)**



**FIGURE 8. CASCADED UP/DOWN COUNTER WITH PARALLEL LOAD**



NOTE: Illegal states in BCD counters corrected in one count.

NOTE: Illegal states in BCD counters corrected in one or two counts.

**FIGURE 9. 'HC192, 'HCT193 STATE DIAGRAMS**

**PACKAGING INFORMATION**

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                  |
|---------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|--------------------------------------|
| <a href="#">5962-8780801EA</a>  | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8780801EA<br>CD54HC192F3A       |
| <a href="#">5962-9084801MEA</a> | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9084801ME<br>A<br>CD54HCT193F3A |
| <a href="#">CD54HC192F3A</a>    | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8780801EA<br>CD54HC192F3A       |
| CD54HC192F3A.A                  | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8780801EA<br>CD54HC192F3A       |
| <a href="#">CD54HC193F3A</a>    | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8772401EA<br>CD54HC193F3A       |
| CD54HC193F3A.A                  | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8772401EA<br>CD54HC193F3A       |
| <a href="#">CD54HCT193F3A</a>   | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9084801ME<br>A<br>CD54HCT193F3A |
| CD54HCT193F3A.A                 | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9084801ME<br>A<br>CD54HCT193F3A |
| <a href="#">CD74HC192E</a>      | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC192E                           |
| CD74HC192E.A                    | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC192E                           |
| <a href="#">CD74HC192NSR</a>    | Active        | Production           | SOP (NS)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC192M                               |
| CD74HC192NSR.A                  | Active        | Production           | SOP (NS)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC192M                               |
| CD74HC192NSRG4                  | Active        | Production           | SOP (NS)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC192M                               |
| <a href="#">CD74HC192PWR</a>    | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HJ192                                |
| CD74HC192PWR.A                  | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HJ192                                |
| <a href="#">CD74HC192PWT</a>    | Obsolete      | Production           | TSSOP (PW)   16 | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HJ192                                |
| <a href="#">CD74HC193E</a>      | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC193E                           |
| CD74HC193E.A                    | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC193E                           |
| <a href="#">CD74HC193M</a>      | Obsolete      | Production           | SOIC (D)   16   | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HC193M                               |
| <a href="#">CD74HC193M96</a>    | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC193M                               |
| CD74HC193M96.A                  | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC193M                               |

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| CD74HC193MT           | Obsolete      | Production           | SOIC (D)   16  | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HC193M              |
| CD74HCT193E           | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HCT193E         |
| CD74HCT193E.A         | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HCT193E         |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC192, CD54HC193, CD54HCT193, CD74HC192, CD74HC193, CD74HCT193 :**

● Catalog : [CD74HC192](#), [CD74HC193](#), [CD74HCT193](#)

● Military : [CD54HC192](#), [CD54HC193](#), [CD54HCT193](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC192NSR | SOP          | NS              | 16   | 2000 | 330.0              | 16.4               | 8.1     | 10.4    | 2.5     | 12.0    | 16.0   | Q1            |
| CD74HC192PWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| CD74HC193M96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC192NSR | SOP          | NS              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| CD74HC192PWR | TSSOP        | PW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| CD74HC193M96 | SOIC         | D               | 16   | 2500 | 353.0       | 353.0      | 32.0        |

## TUBE



\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74HC192E    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC192E    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC192E.A  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC192E.A  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC193E    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC193E    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC193E.A  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC193E.A  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT193E   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT193E   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT193E.A | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT193E.A | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



**PW0016A**

## TSSOP - 1.2 mm max height

## SMALL OUTLINE PACKAGE



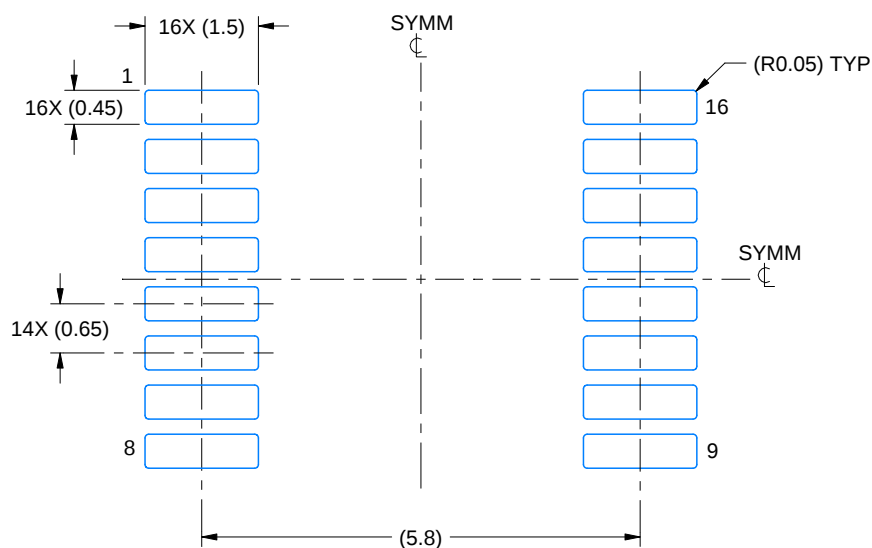
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

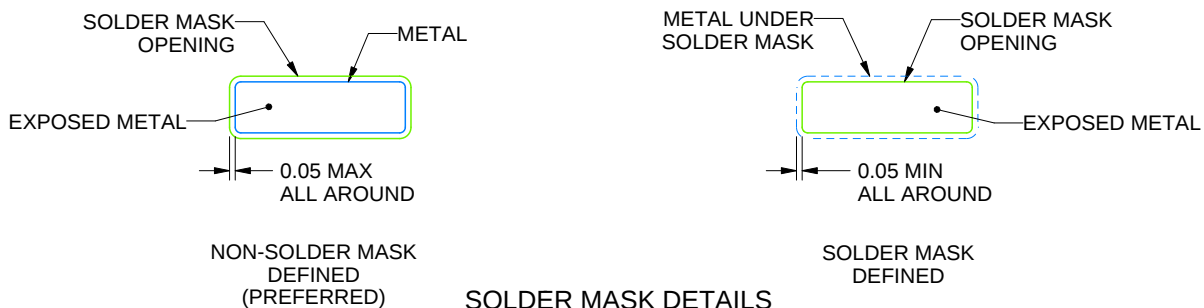
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

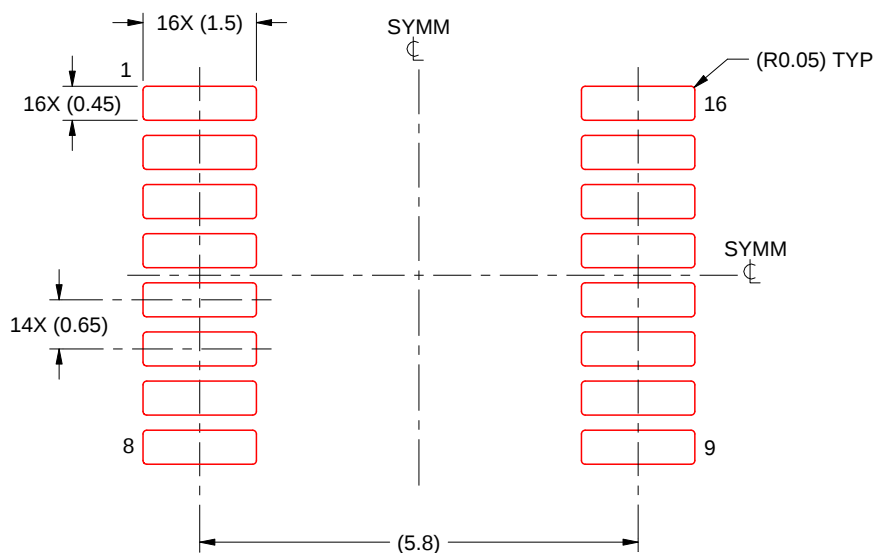
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



# PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.





SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:7X

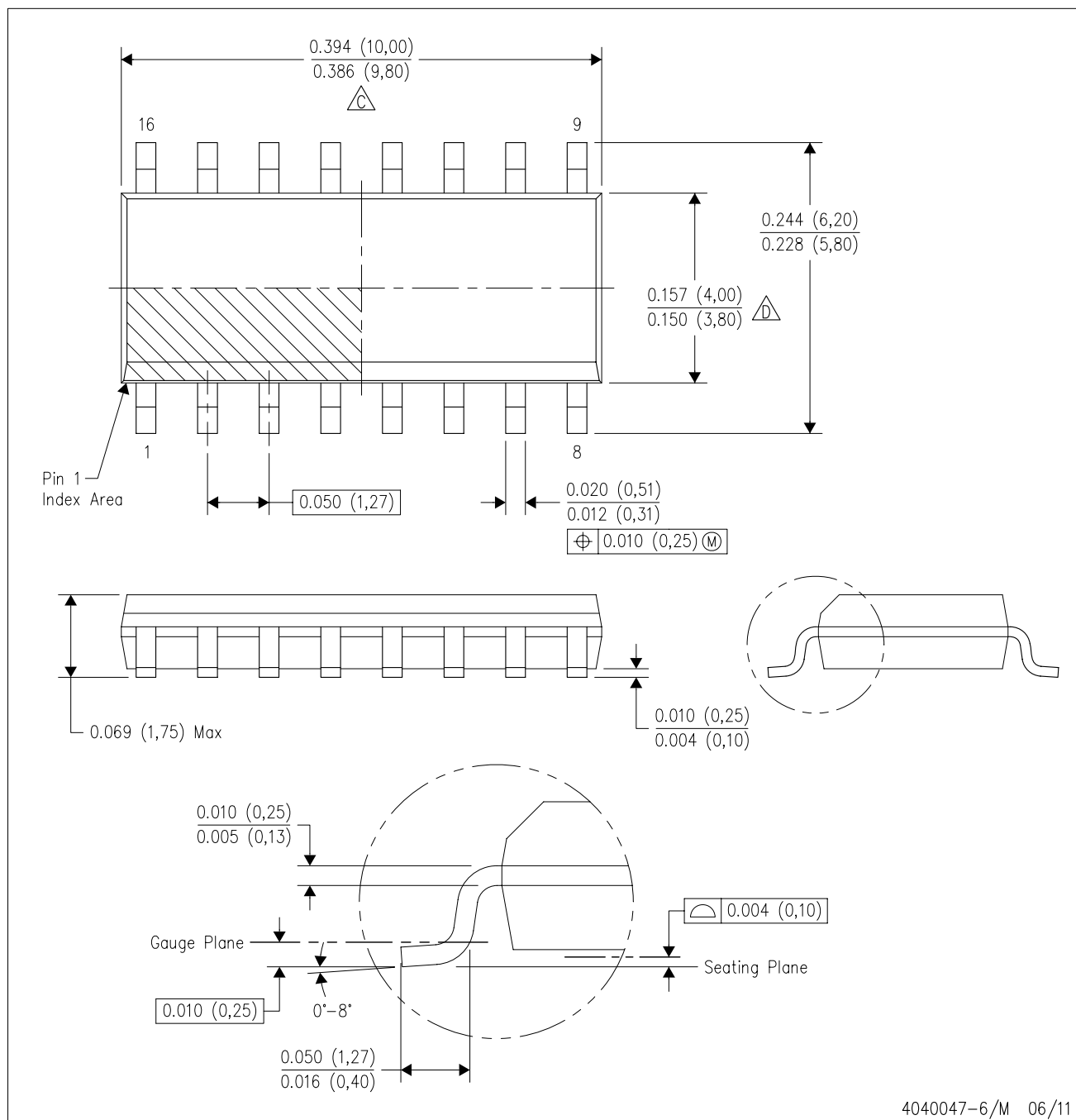
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025