TEXAS INSTRUMENTS

CD54HC4066, CD74HC4066, CD74HCT4066
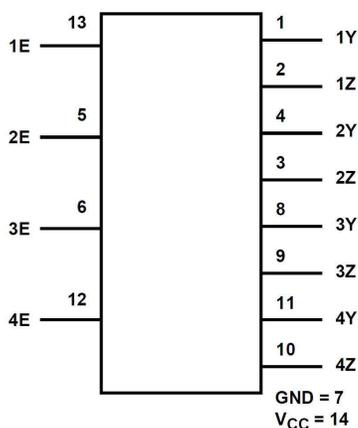ZHCSWP0E – FEBRUARY 1998 – REVISED JULY 2024

高速 CMOS 逻辑四路双向开关

1 特性

- 宽模拟输入电压范围：
  0V 至 10V
- 低导通电阻：
  - V_{CC} = 4.5V：25Ω
  - V_{CC} = 9V：15Ω
- 快速开关和传播延迟时间
- 低关断漏电流
- 宽工作温度范围：
  -55°C 至 125°C
- HC 类型：
  - 工作电压为 2 V 至 10 V
  - 高抗噪性：当 V_{CC} = 5V 和 10V 时，N_{IL} = 30%，N_{IH} = V_{CC} 的 30%
- HCT 类型：
  - 直接 LSTTL 输入逻辑兼容性，V_{IL} = 0.8V（最大值），V_{IH} = 2V（最小值）
  - CMOS 输入兼容性，在 V_{OL}、V_{OH} 时，$I_I \leqslant 1\mu A$

2 应用

- 模拟信号开关和多路复用：信号门控、调制器、静噪控制、解调器、斩波器、换向开关
- 数字信号开关和多路复用：模数和数模转换
- 频率、阻抗、相位和模拟信号增益的数字控制
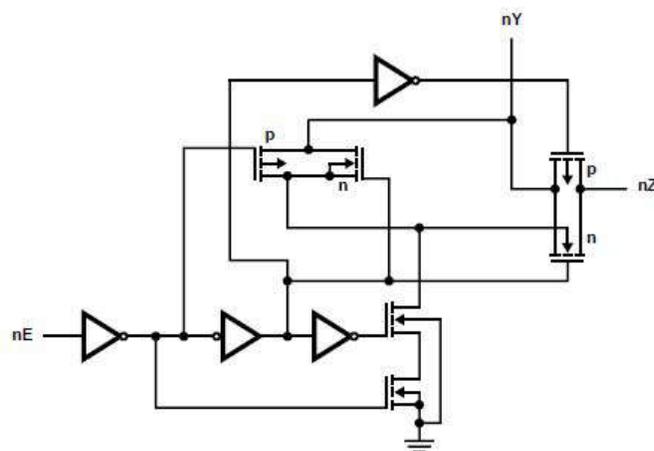- 楼宇自动化

3 说明

'HC4066 和 CD74HCT4066 器件包含四个独立的数控模拟开关，这些开关使用硅栅 CMOS 技术并借助标准 CMOS 集成电路的低功耗特性来实现与 LSTTL 接近的运行速度。

这些开关具有金属栅 CD4066B 器件的线性导通电阻特性。每个开关由其控制输入端的高电平电压进行开通。

器件信息

器件型号	温度范围 (°C)	封装[1]
CD74HC4066	-55 至 125	D（SOIC，14）
	-55 至 125	PW（TSSOP，14）
CD74HCT4066	-55 至 125	D（SOIC，14）

(1) 有关更多信息，请参阅节 19。

功能方框图

逻辑图

Table of Contents

4 Pin Configuration and Functions

图 4-1. CD74HC4066 D or PW Package, 14-Pin SOIC or TSSOP CD74HCT4066 r D Package, 14-Pin SOIC (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1Y	1	I/O	Input/Output for Switch 1
1Z	2	I/O	Input/Output for Switch 1
2Z	3	I/O	Input/Output for Switch 2
2Y	4	I/O	Input/Output for Switch 2
2E	5	I	Control pin for Switch 2
3E	6	I	Control pin for Switch 3
GND	7	-	Ground Pin
3Y	8	I/O	Input/Output for Switch 3
3Z	9	I/O	Input/Output for Switch 3
4Z	10	I/O	Input/Output for Switch 4
4Y	11	I/O	Input/Output for Switch 4
4E	12	I	Control pin for Switch 4
1E	13	I	Control pin for Switch 1
V_{CC}	14	-	Power Pin

(1)   Signal Types: I = Input, O = Output, I/O = Input or Output.

Product Folder Links: *CD54HC4066 CD74HC4066 CD74HCT4066*

English Data Sheet: SCHS208

5 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1] [2]

			MIN	MAX	UNIT
V_{CC} HCT	DC Supply voltage		– 0.5	7	V
V_{CC} HC[1]			-0.5	10.5	V
I_{IK}	DC input diode current	For V_I < -0.5V or V_I > V_{CC} + 0.5V	– 20	20	mA
I_O	DC switch current[2]	For V_I< -0.5V or V_I > VCC + 0.5V	-20	20	mA
I_{OK}	DC Output diode current	For V_O < -0.5V or V_O > V_{CC} + -0.5V	-25	25	mA
DC Output Source or Sink Current per Output Pin, I_O	For V_O > -0.5V or V_O < V_{CC} + -0.5V		– 25	25	mA
I_{CC}	DC V_{CC} or ground current		– 50	50	mA
T_{JMAX}	Maximum junction temperature (Plastic Package)			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) In certain applications, the external load-resistor current may include both VCC and signal-line components. To avoid drawing VCC current when switch current flows into the transmission gate inputs, (terminals 1, 4, 8 and 11) the voltage drop across the bidirectional switch must not exceed 0.6V (calculated from RON values shown in the DC Electrical Specifications Table). No VCC current will flow through RLif the switch current flows into terminals 2, 3, 9 and 10. 2.

6 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins[1]	±500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7 Thermal Information

THERMAL METRIC	CD74HCx4066		UNIT
	D (SOIC)	PW (TSSOP)	
	14 PINS	14 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	108.4	133.9	°C/W

Product Folder Links: *CD54HC4066 CD74HC4066 CD74HCT4066*

English Data Sheet: SCHS208

8 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range (T_A = full package temperature range)(2)	CD54 and 74HC types	2		10	V
		CD54 and 74HCT types	4.5		5.5	
V_{IS}	Analog switch I/O voltage		0		V_{CC}	V
T_A	Ambient temperature		−55		125	°C
t_r , t_f	Input rise and fall times	2 V	0		1000	ns
		4.5 V	0		500	
		6 V	0		400	

Product Folder Links: *CD54HC4066 CD74HC4066 CD74HCT4066*

English Data Sheet: SCHS208

9 Electrical Characteristics: HC Devices

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted)[1]

PARAMETER			TEST CONDITIONS				MIN	TYP	MAX	UNIT
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})										
		V_{IS} (V)	V_I (V)	V_{CC} (V)	T_A					
High Level Input Voltage	V_{IH}			2	25°C				1.5	V
					−40°C to +85°C				1.5	
					−55°C to +125°C				1.5	
				4.5	25°C				3.15	
					−40°C to +85°C				3.15	
					−55°C to +125°C				3.15	
				9	25°C				6.3	
					−40°C to +85°C				6.3	
					−55°C to +125°C				6.3	
Low Level Input Voltage	V_{IL}			2	25°C			0.5		V
					−40°C to +85°C			0.5		
					−55°C to +125°C			0.5		
				4.5	25°C			1.35		
					−40°C to +85°C			1.35		
					−55°C to +125°C			1.35		
				9	25°C			2.7		
					−40°C to +85°C			2.7		
					−55°C to +125°C			2.7		

Product Folder Links: *CD54HC4066 CD74HC4066 CD74HCT4066*

English Data Sheet: SCHS208

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
"ON" Resistance IO = 1mA	R_{ON}	V_{CC} or GND	VCC	4.5	25°C	25	80	Ω
					–40°C to +85°C			106	
					–55°C to +125°C			128	
				6	25°C	20	75	
					–40°C to +85°C			94	
					–55°C to +125°C			113	
				9	25°C	15	60	
					–40°C to +85°C			78	
					–55°C to +125°C			95	
		V_{CC} to GND		4.5	25°C	35	95	Ω
					–40°C to +85°C			118	
					–55°C to +125°C			142	
				6	25°C	24	84	
					–40°C to +85°C			105	
					–55°C to +125°C			126	
				9	25°C	31	70	
					–40°C to +85°C			88	
					–55°C to +125°C			105	
"ON" Resistance Between Any Two Switches	▲R_{ON}		VCC	4.5	25°C		1		Ω
			VCC	6	25°C		0.75		
			VCC	9	25°C		0.5		
Off-Switch Leakage Current	I_Z	V_{CC} or GND	V_{IL}	10	25°C			±0.1	µA
					–55°C to 85°C			±1	
					–55°C to 125°C			±1	
Input Leakage Current (Any Control)	I_{IL}		V_{CC} or GND	10	25°C			±0.1	µA
					–55°C to 85°C			±1	
					–55°C to 125°C			±1	
Quiescent Device Current	I_{CC}	V_{CC} or GND		6	25°C			18.5	µA
					–55°C to 85°C			20	
					–55°C to 125°C			40	
				10	25°C			35	
					–55°C to 85°C			160	
					–55°C to 125°C			320	
CONTROL (ADDRESS OR INHIBIT), V_C									

(1) Peak-to-Peak voltage symmetrical about (V_{DD} – V_{EE}) / 2.

Product Folder Links: *CD54HC4066 CD74HC4066 CD74HCT4066*

English Data Sheet: SCHS208

10 Electrical Characteristics: HCT Devices

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})									
		V_{IS} (V)	V_I (V)	V_{CC} (V)	T_A				
High Level Input Voltage	V_{IH}			4.5 to 5.5	25°C	2			V
					–40°C to +85°C	2			
					–55°C to +125°C	2			
Low Level Input Voltage	V_{IL}				25°C			0.8	V
					–40°C to +85°C			0.8	
					–55°C to +125°C			0.8	
"ON" Resistance IO = 1mA	R_{ON}	V_{CC} or GND	VCC	4.5	25°C		25	80	Ω
					–40°C to +85°C			106	
					–55°C to +125°C			128	
		V_{CC} to GND			25°C		35	95	Ω
					–40°C to +85°C			118	
					–55°C to +125°C			142	
"ON" Resistance Between Any Two Switches	▲R_{ON}		VCC	4.5	25°C			1	Ω
Off-Switch Leakage Current	I_Z	V_{CC} or GND	V_{IL}	5.5	25°C			±0.1	μA
					–55°C to 85°C			±1	
					–55°C to 125°C			±1	
Input Leakage Current (Any Control)	I_{IL}		V_{CC} or GND	5.5	25°C			±0.1	μA
					–55°C to 85°C			±1	
					–55°C to 125°C			±1	
Quiescent Device Current	I_{CC}		V_{CC} or GND	5.5	25°C			2	μA
					–55°C to 85°C			20	
					–55°C to 125°C			40	
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	▲I_{CC}		V_{CC} - 2.1	4.5 to 5.5	25°C		100	360	
					–55°C to 85°C			450	
					–55°C to 125°C			490	
CONTROL (ADDRESS OR INHIBIT), V_C									

(1)   Peak-to-Peak voltage symmetrical about (V_{DD} – V_{EE}) / 2.

Product Folder Links: *CD54HC4066 CD74HC4066 CD74HCT4066*

English Data Sheet: SCHS208

11 Switching Characteristics HC

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions		C_L (pF)	MIN NOM MAX	UNIT
Propagation Delay Time Switch In to Out	t_{PHL}, t_{PLH}	2	25°C	50	60	ns
			-40°C to 85°C		75	ns
			-55°C to 125°C		90	ns
		4.5	25°C		12	ns
			-40°C to 85°C		15	ns
			-55°C to 125°C		18	ns
		9	25°C		8	ns
			-40°C to 85°C		11	ns
			-55°C to 125°C		13	ns
		5	25°C	15	4	ns
Propagation Delay Time Switch Turn On Delay	t_{PZH}, t_{PZL}	2	25°C	50	100	ns
			-40°C to 85°C		125	ns
			-55°C to 125°C		150	ns
		4.5	25°C		20	ns
			-40°C to 85°C		25	ns
			-55°C to 125°C		30	ns
		9	25°C		12	ns
			-40°C to 85°C		15	ns
			-55°C to 125°C		18	ns
		5	25°C	15	4	ns
Propagation Delay Time Switch Turn Off Delay	t_{PHZ}, t_{PLZ}	2	25°C	50	150	ns
			-40°C to 85°C		190	ns
			-55°C to 125°C		225	ns
		4.5	25°C		30	ns
			-40°C to 85°C		38	ns
			-55°C to 125°C		45	ns
		9	25°C		24	ns
			-40°C to 85°C		30	ns
			-55°C to 125°C		36	ns
		5	25°C	15	9.5	ns
Input (Control) Capacitance	C_I		25°C		10	pF
			-40°C to 85°C		10	
			-55°C to 125°C		10	
C_{PD} Power dissipation capacitance(1)	C_{PD}	5	25°C		25	

Product Folder Links: *CD54HC4066 CD74HC4066 CD74HCT4066*

English Data Sheet: SCHS208

12 Switching Characteristics HCT

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions		C_L (pF)	MIN NOM MAX	UNIT
Propagation Delay Time Switch In to Out	t_{PHL}, t_{PLH}	4.5	25°C	50	12	ns
			-40°C to 85°C		15	ns
			-55°C to 125°C		18	ns
		5	25°C	15	1.3	ns
Propagation Delay Time Switch Turn On Delay	t_{PZH}, t_{PZL}	4.5	25°C	50	24	ns
			-40°C to 85°C		30	ns
			-55°C to 125°C		36	ns
		5	25°C	15	5	ns
Propagation Delay Time Switch Turn Off Delay	t_{PHZ}, t_{PLZ}	4.5	25°C	50	35	ns
			-40°C to 85°C		44	ns
			-55°C to 125°C		53	ns
		5	25°C	15	5.5	ns
Input (Control) Capacitance	C_I		25°C		10	pF
			-40°C to 85°C		10	
			-55°C to 125°C		10	
C_{PD} Power dissipation capacitance(1)	C_{PD}	5	25°C		38	

13 Analog Channel Specifications

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions		V_{CC} (V)	HC	HCT	UNIT
Switch Frequency Response Bandwidth at -3dB				4.5	200	200	MHz
Cross Talk Between Any Two Switches				4.5	-72	-72	dB
Total Harmonic Distortion		1kHz, V_{IS}= 4V_{PP}		4.5	0.022	0.023	%
		1kHz, V_{IS}= 8V_{PP}		9	0.019	N/A	%
Control to Switch Feedthrough Noise	Control to Switch Feedthrough Noise			4.5	200	130	mV
Control to Switch Feedthrough Noise				4.5	200	130	mV
				9	550	N/A	
Switch "OFF" signal feedthrough				4.5	-72	-72	dB
C_I Switch input capacitance					5	5	pF

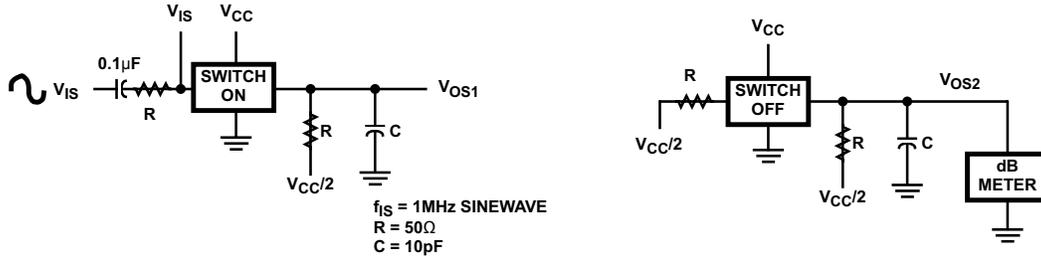English Data Sheet: SCHS208

14 Analog Test Circuits

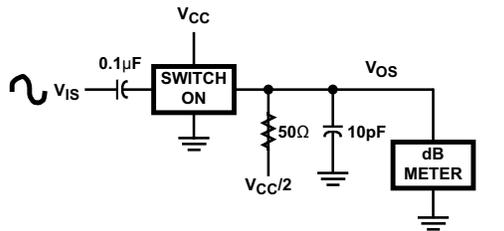图 14-1. Crosstalk Between Two Switches Test Circuit
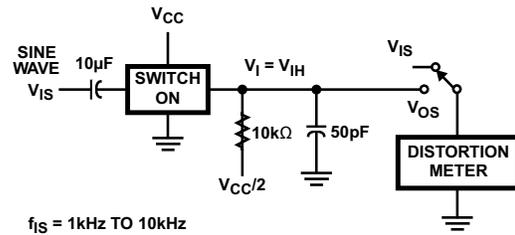
图 14-2. Frequency Response Test Circuit

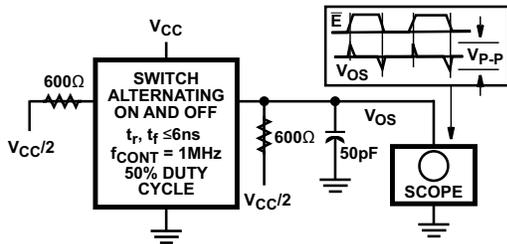图 14-3. Total Harmonic Distortion Test Circuit

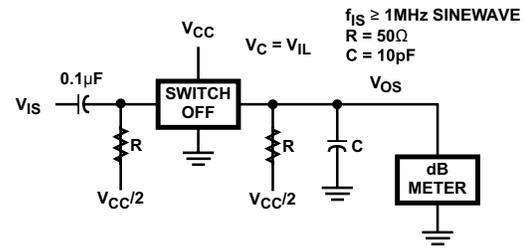图 14-4. Control-To-Switch Feedthrough Noise Test Circuit

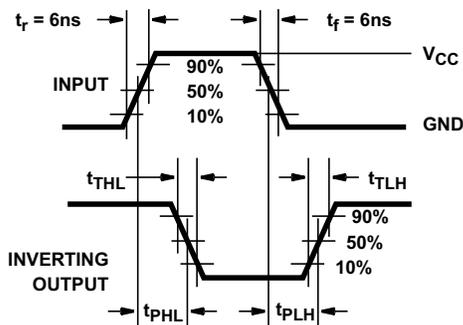图 14-5. Switch OFF Signal Feedthrough

15 Test Circuits and Waveforms

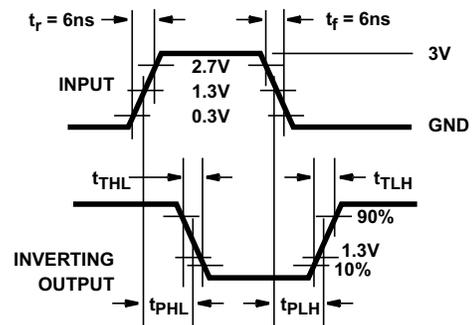图 15-1. HC Transition Times and Propagation Delay Times, Combination Logic

图 15-2. HCT Transition Times and Propagation Delay Times, Combination Logic

Product Folder Links: CD54HC4066 CD74HC4066 CD74HCT4066

English Data Sheet: SCHS208

16 Detailed Description

16.1 Functional Block Diagram
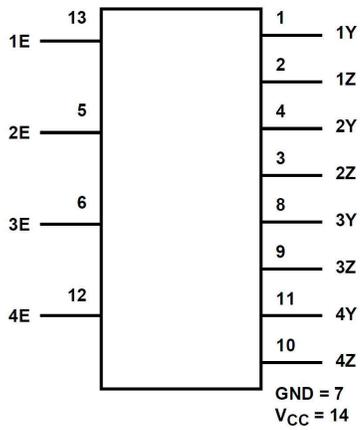
图 **16-1. Functional Block Diagram**
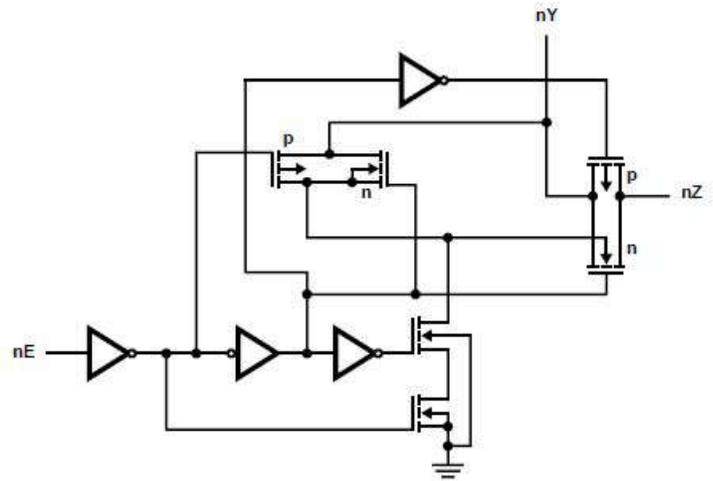
图 **16-2. Logic Diagram**

16.2 Device Functional Modes

表 **16-1. Truth Table**

INPUTnE	SWITCH
L[2]	Off
H[1]	On

(1)   H = High Level

(2)   L = Low Level

17 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

17.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

17.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者"按原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

17.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

17.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

17.5 术语表

TI 术语表　　　　　本术语表列出并解释了术语、首字母缩略词和定义。

18 Revision History

注：以前版本的页码可能与当前版本的页码不同

19 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: *CD54HC4066 CD74HC4066 CD74HCT4066*

English Data Sheet: SCHS208

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8950701CA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8950701CA CD54HC4066F3A
CD54HC4066F3A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8950701CA CD54HC4066F3A
CD54HC4066F3A.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8950701CA CD54HC4066F3A
CD74HC4066E	NRND	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4066E
CD74HC4066E.A	NRND	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4066E
CD74HC4066EE4	NRND	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4066E
CD74HC4066M	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HC4066M
CD74HC4066M96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4066M
CD74HC4066M96.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4066M
CD74HC4066M96E4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4066M
CD74HC4066MT	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HC4066M
CD74HC4066PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HP4066
CD74HC4066PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HP4066
CD74HC4066PWT	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-55 to 125	HP4066
CD74HCT4066E	NRND	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4066E
CD74HCT4066E.A	NRND	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4066E
CD74HCT4066M	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HCT4066M
CD74HCT4066M96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4066M
CD74HCT4066M96.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4066M
CD74HCT4066MT	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HCT4066M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC4066, CD74HC4066, CD74HCT4066 :

● Catalog : CD74HC4066

● Automotive : CD74HCT4066-Q1

● Military : CD54HC4066

NOTE: Qualified Version Definitions:

　　　● Catalog - TI's standard catalog product

　　　● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

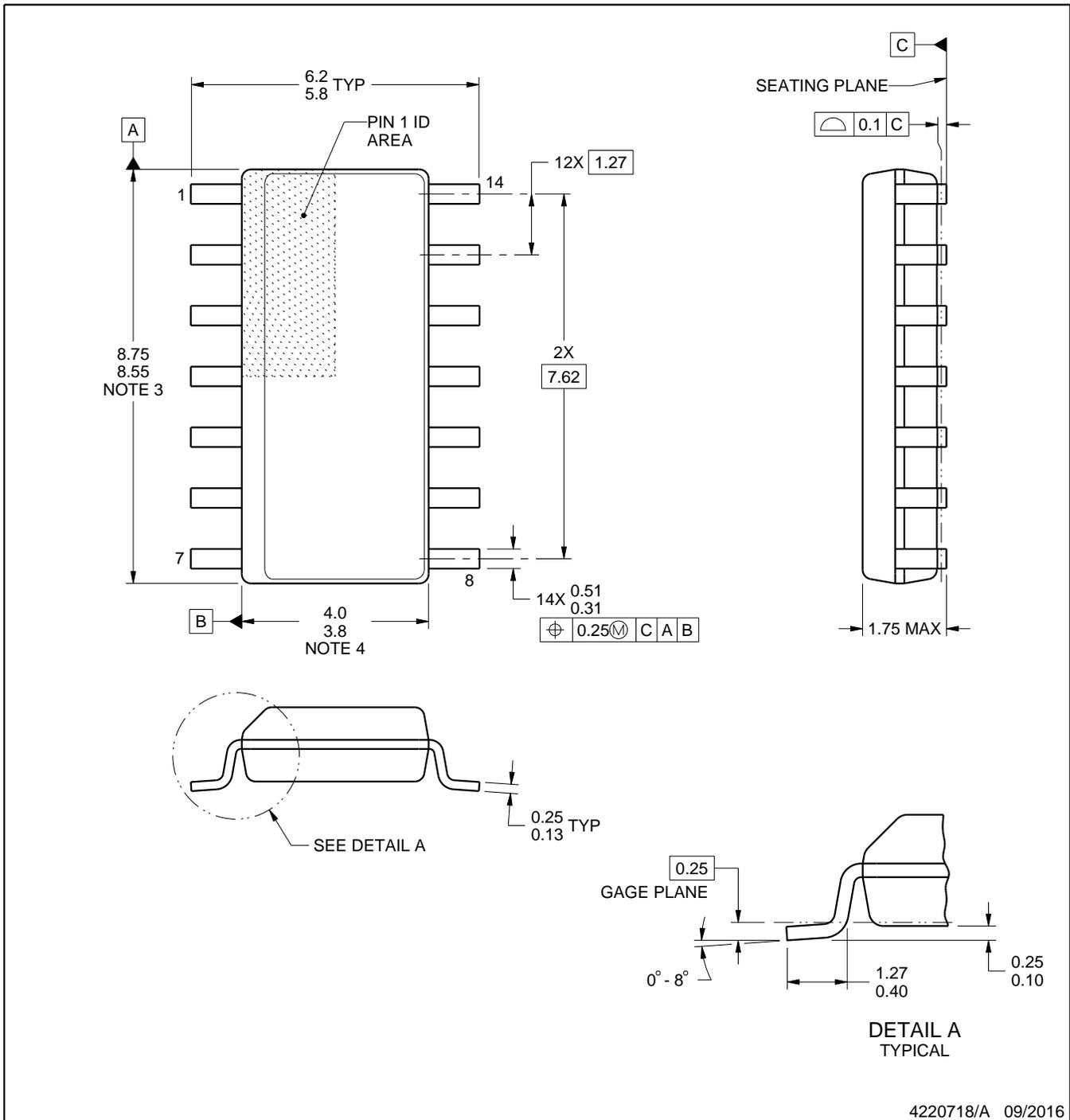　　　● Military - QML certified for Military and Defense Applications
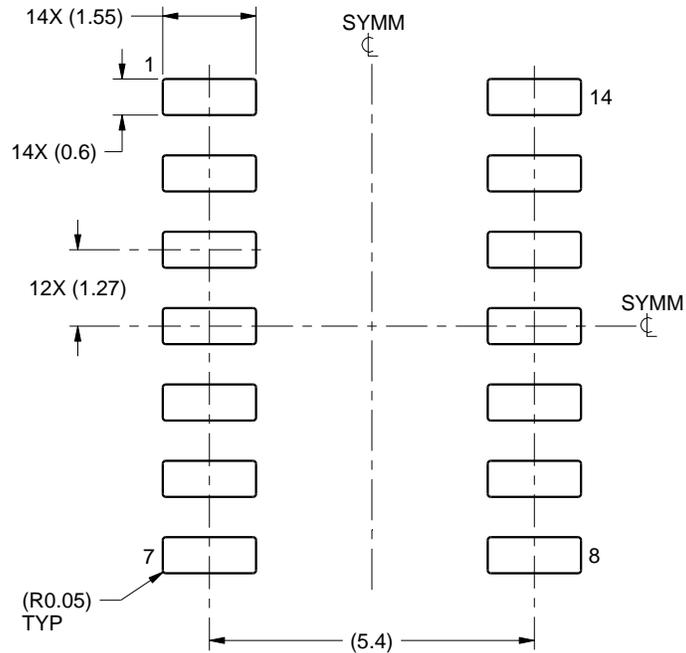
4220718/A   09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

D0014A

14X (1.55)
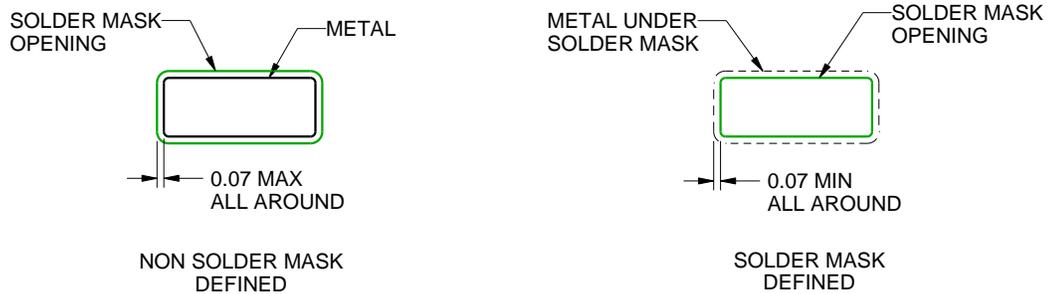
1

14X (0.6)

12X (1.27)

SYMM

14

SYMM

8

7

(R0.05)
TYP

(5.4)

LAND PATTERN EXAMPLE
SCALE:8X

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

**NON SOLDER MASK
DEFINED**

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MIN
ALL AROUND

**SOLDER MASK
DEFINED**

SOLDER MASK DETAILS

4220718/A   09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

TEXAS
INSTRUMENTS
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14X (1.55)

SYMM

1

14X (0.6)

12X (1.27)

SYMM

7

8

14

(5.4)
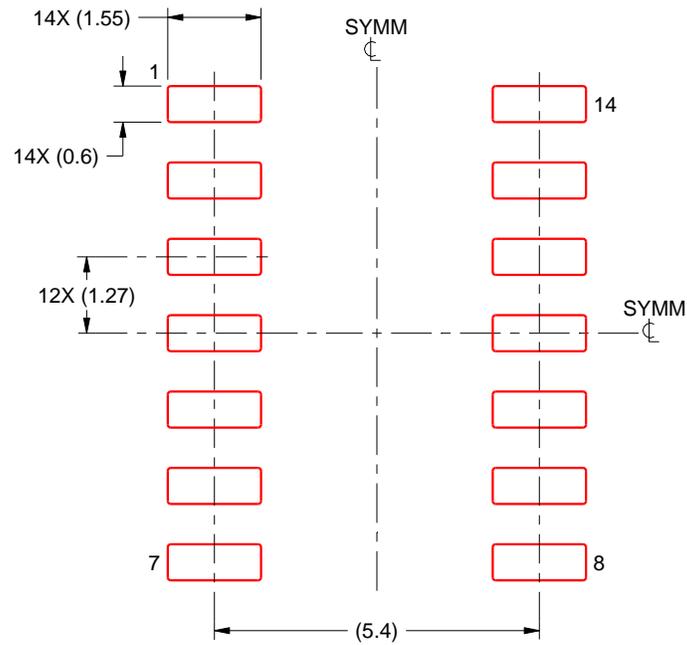
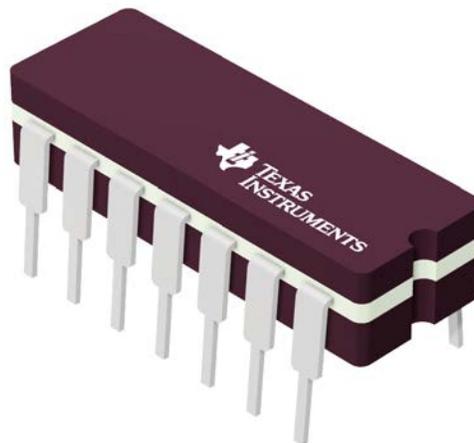SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A   09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

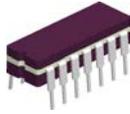Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.
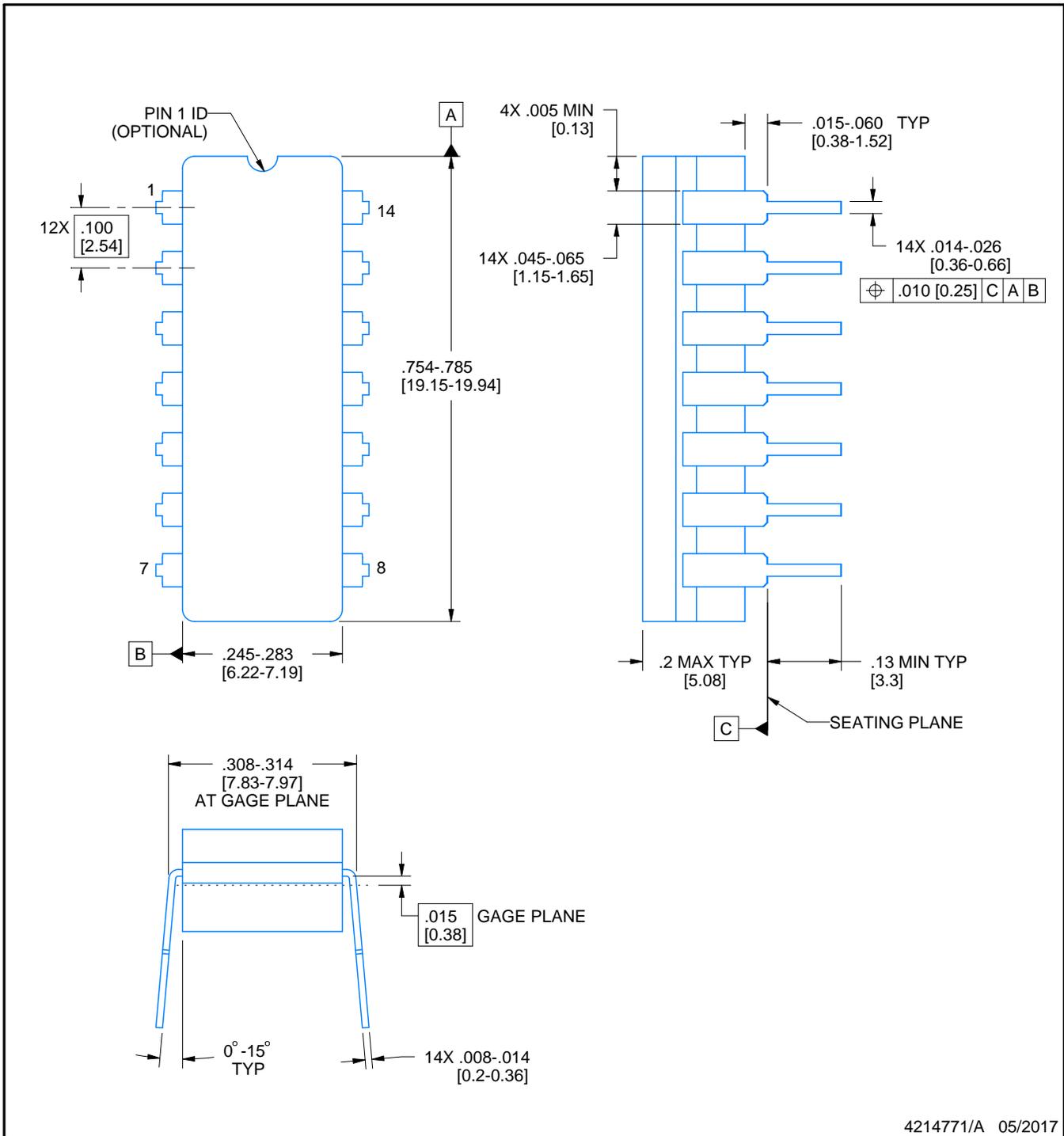
4040083-5/G

PIN 1 ID
(OPTIONAL)

A

4X .005 MIN
[0.13]

.015-.060 TYP
[0.38-1.52]

1

14

12X .100
[2.54]

14X .045-.065
[1.15-1.65]

14X .014-.026
[0.36-0.66]

⊕ .010 [0.25] C A B

.754-.785
[19.15-19.94]

7

8

B .245-.283
[6.22-7.19]

.2 MAX TYP
[5.08]

.13 MIN TYP
[3.3]

C

SEATING PLANE

.308-.314
[7.83-7.97]
AT GAGE PLANE

.015 GAGE PLANE
[0.38]

0°-15°
TYP

14X .008-.014
[0.2-0.36]
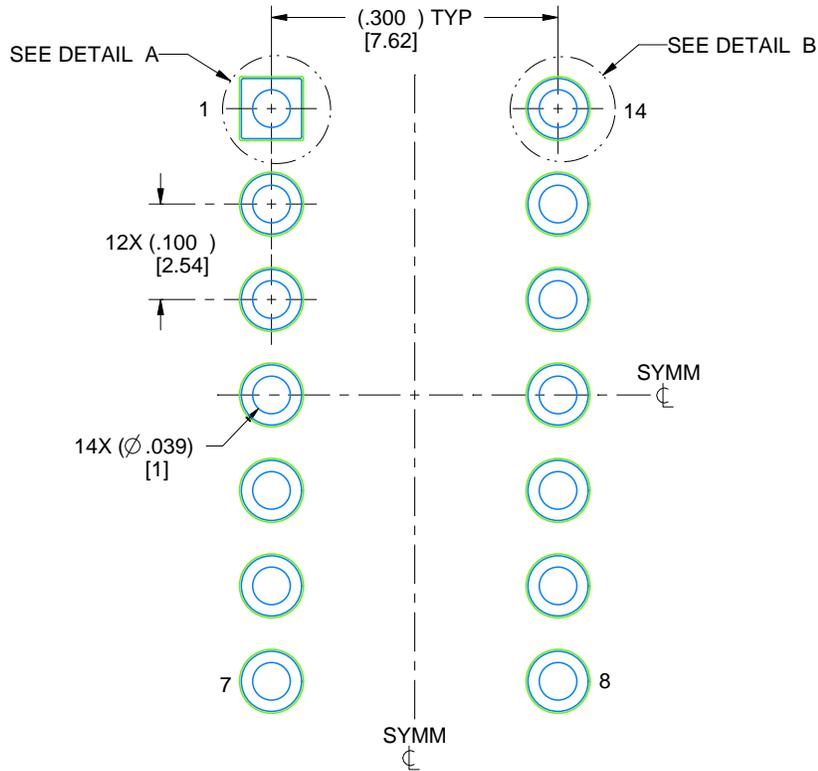
4214771/A   05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

(.300) TYP
[7.62]

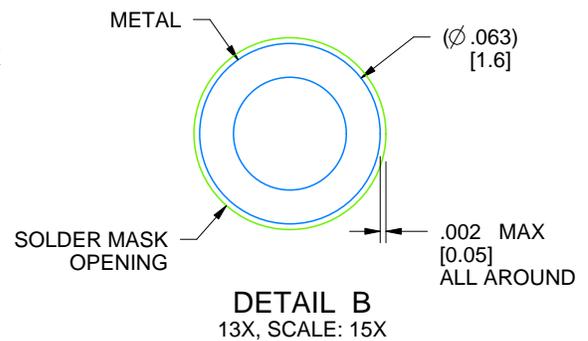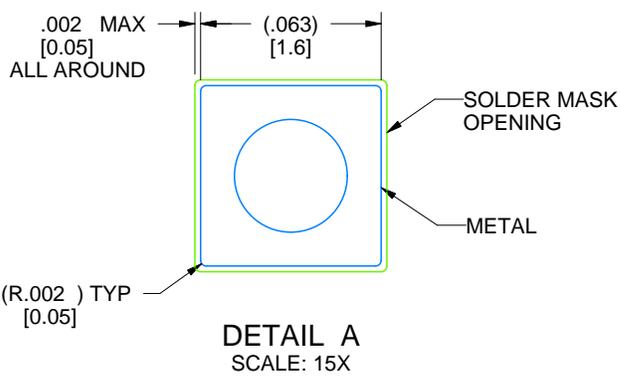SEE DETAIL A

SEE DETAIL B

1

14

12X (.100)
[2.54]

SYMM
℄

14X (∅ .039)
[1]

7

8

SYMM
℄

LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

.002 MAX
[0.05]
ALL AROUND

(.063)
[1.6]

SOLDER MASK
OPENING

METAL

METAL

(∅ .063)
[1.6]

(R.002) TYP
[0.05]

SOLDER MASK
OPENING

.002 MAX
[0.05]
ALL AROUND

DETAIL A
SCALE: 15X

DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

N (R−PDIP−T)**   **PLASTIC DUAL−IN−LINE PACKAGE**

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) △D

0.045 (1,14) / 0.030 (0,76) △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option △D

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E   12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
        △C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
        △D The 20 pin end lead shoulder width is a vendor option, either half or full width.
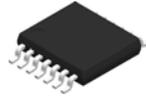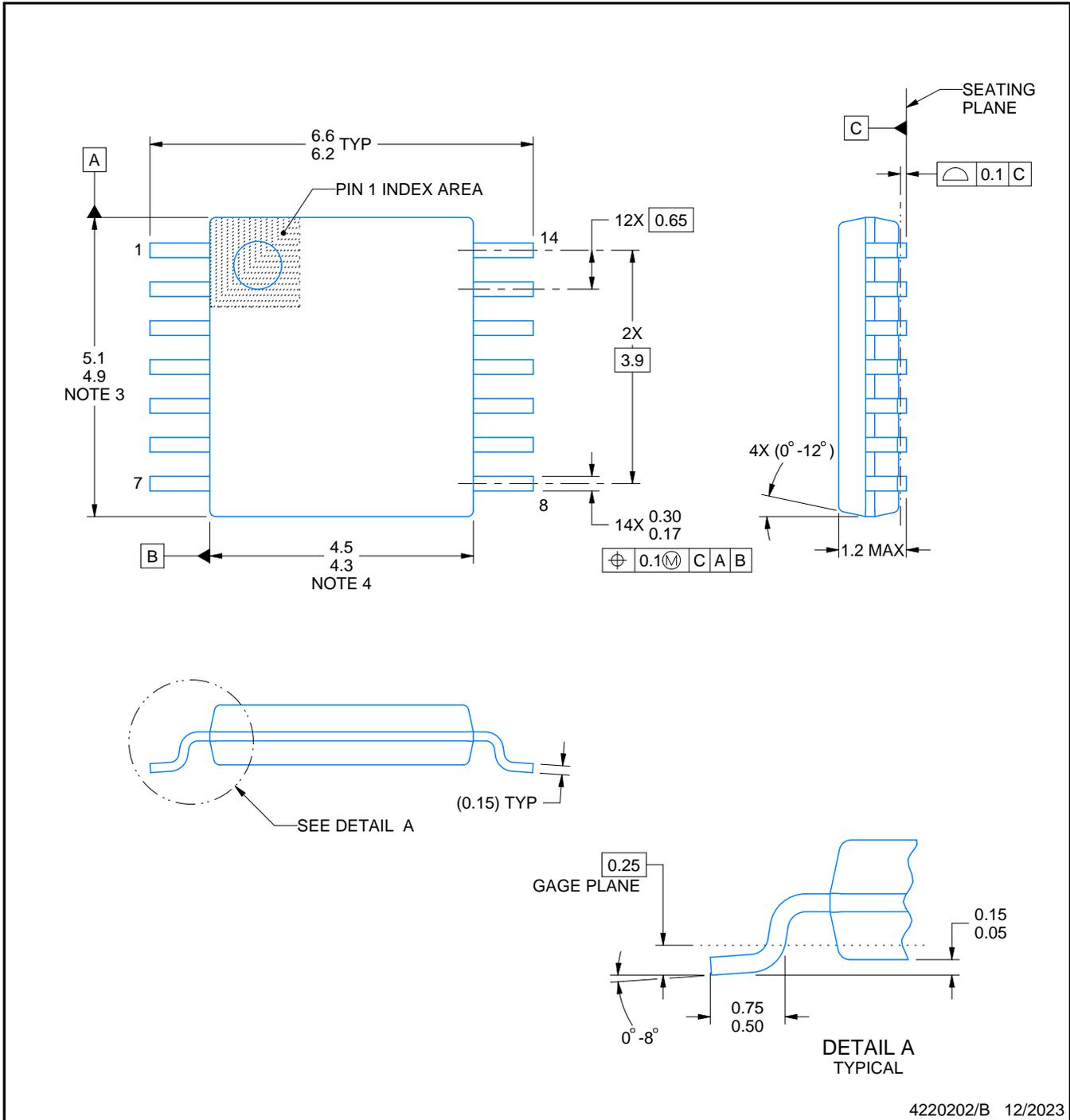
TEXAS
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6.6
6.2 TYP

A

PIN 1 INDEX AREA

1

14

12X 0.65

2X
3.9

5.1
4.9
NOTE 3

7

8

14X 0.30
0.17

⊕ 0.1 Ⓜ C A B

B

4.5
4.3
NOTE 4

SEATING PLANE

C

⌒ 0.1 C

4X (0° -12°)

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0.15
0.05

0.75
0.50

0° -8°

DETAIL A
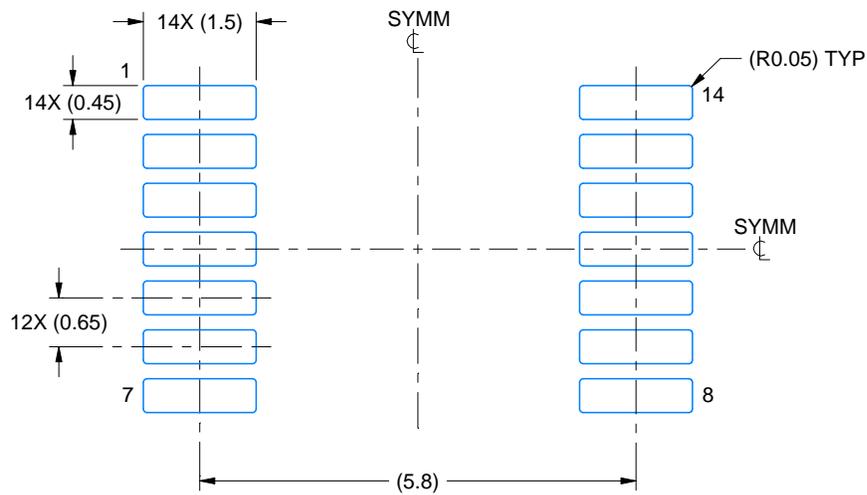TYPICAL

4220202/B   12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
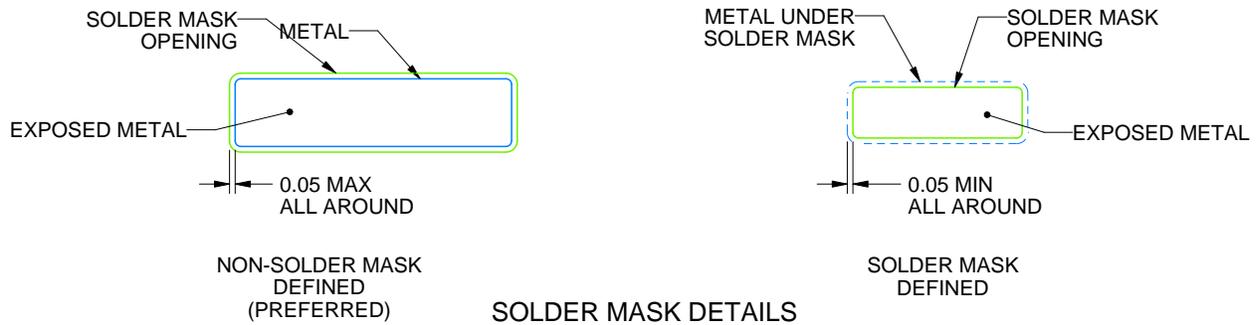5. Reference JEDEC registration MO-153.

14X (1.5)

1

14X (0.45)

SYMM
℄

(R0.05) TYP

14

SYMM
℄

12X (0.65)

7

8

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED
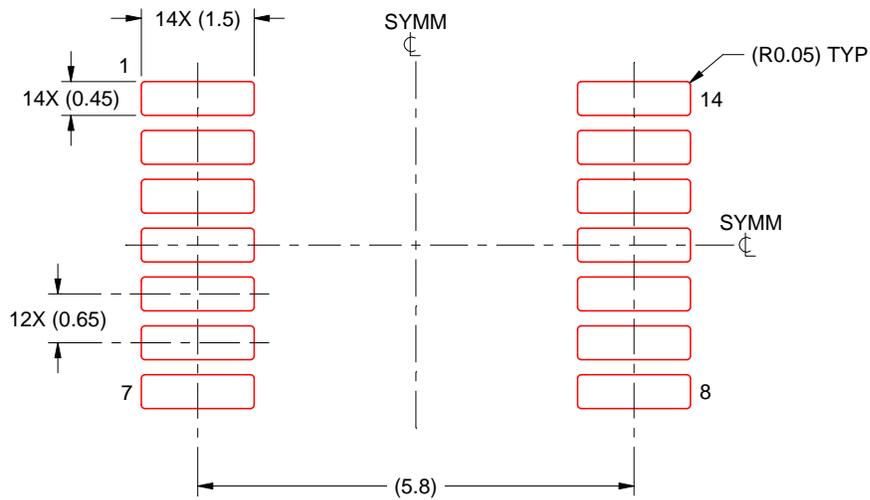
SOLDER MASK DETAILS

4220202/B   12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

14X (1.5)
SYMM
(R0.05) TYP
1
14X (0.45)
14
SYMM
12X (0.65)
7
8
(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B   12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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