

CD74HC390、CDx4HCT390 高速 CMOS 逻辑双路十进制纹波计数器

1 特性

- 2 个 BCD 十进制或二五混合进制计数器
- 该器件可配置为除以 2、除以 4、除以 5、除以 10、除以 20、除以 25、除以 50、除以 100 模式
- 2 个控制器重置输入，可分别对每个十进制计数器清零
- 扇出 (在温度范围内)
 - 标准输出：10 个 LSTTL 负载
 - 总线驱动器输出：15 个 LSTTL 负载
- 宽工作温度范围：-55°C 至 125°C
- 平衡的传播延迟及转换时间
- 与 LSTTL 逻辑 IC 相比，功耗显著降低
- HC 类型
 - 工作电压为 2V 至 6V
 - 高抗噪性：当 $V_{CC} = 5V$ 时， $N_{IL} = 30\%$ ， $N_{IH} = V_{CC}$ 的 30%
- HCT 类型
 - 工作电压为 4.5V 至 5.5V
 - 直接 LSTTL 输入逻辑兼容性， $V_{IL} = 0.8V$ (最大值)， $V_{IH} = 2V$ (最小值)
 - CMOS 输入兼容性，当电压为 V_{OL} 、 V_{OH} 时， $I_I \leq 1\mu A$

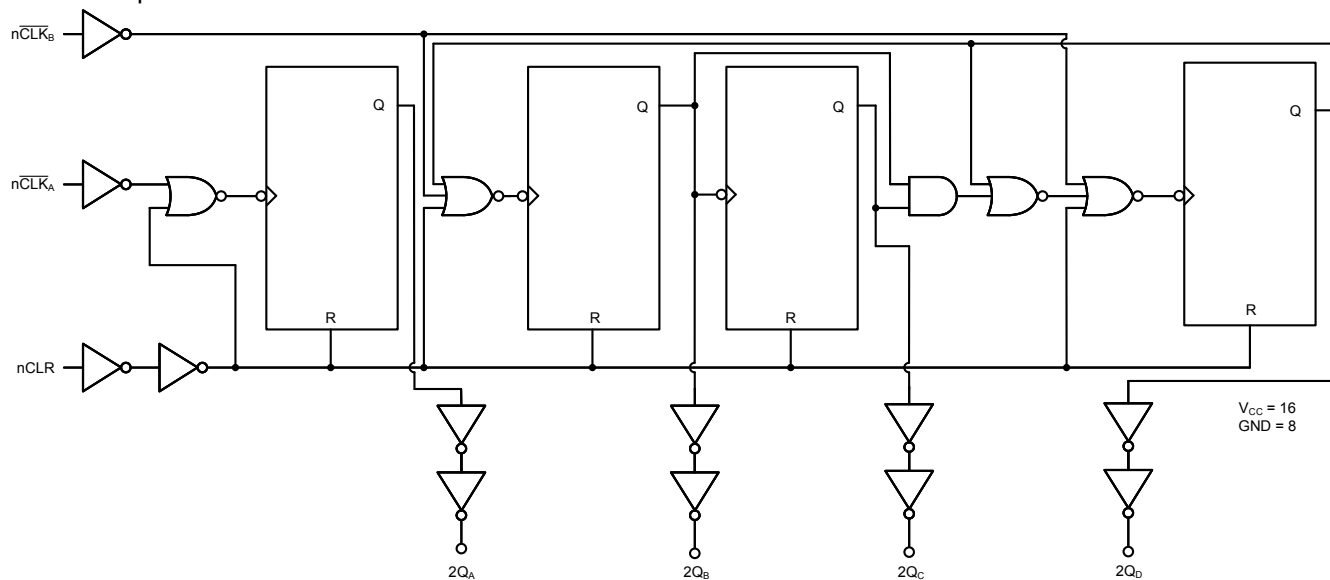
2 说明

SN74HC390 和 'HCT390 器件包含 2 个独立 4 位十进制纹波计数器，下降沿通过异步清零计时。每个计数器均分为两部分，即除以 2 计数器和除以 5 计数器，每一部分都具有独立的时钟输入。这样，就可以灵活地配置器件。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
CD54HCT390F3A	陶瓷双列直插封装 (CDIP) (16)	24.38mm × 6.92mm
CD74HC390M	SOIC (16)	9.90mm × 3.90mm
CD74HCT390M	SOIC (16)	9.90mm × 3.90mm
CD74HC390E	PDIP (16)	19.31mm × 6.35mm
CD74HCT390E	PDIP (16)	19.31mm × 6.35mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能方框图



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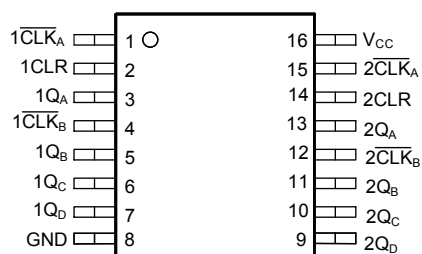
3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (November 2021) to Revision E (April 2022)	Page
• Corrected table 7-3, Q _C value 6 from H to L.....	10

Changes from Revision C (September 1997) to Revision D (November 2021)	Page
• 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准.....	1
• 更新了引脚名称，以符合现行的 TI 命名规则 1CP ₀ 现改为 1CLK _A ；1MR 现改为 1CLR；1Q ₀ 现改为 1Q _A ；1CP ₁ 现改为 1CLK _B ；1Q ₁ 现改为 1Q _B ；1Q ₂ 现改为 1Q _C ；1Q ₃ 现改为 1Q _D ；2Q ₃ 现改为 2Q _D ；2Q ₂ 现改为 2Q _C ；2Q ₁ 现改为 2Q _B ；2CP ₁ 现改为 2CLK _B ；2Q ₀ 现改为 2Q _A ；2MR 现改为 2CLR；2CP ₀ 现改为 2CLK _A	1

4 Pin Configuration and Functions



J, N or D Package
16-Pin CDIP, PDIP, or SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
I _{IK}	Input diode current ⁽²⁾	(V _I < 0 or V _I > V _{CC})		±20	mA
I _{OK}	Output diode current ⁽²⁾	(V _O < 0 or V _O > V _{CC})		±20	mA
I _O	Output source or sink current per output pin	(V _O = 0 to V _{CC})		±25	mA
	Continuous current through V _{CC} or GND			±50	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C
	Lead temperature (Soldering 10s) (SOIC - Lead tips only)			300	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range	HC Types	2	6	V
		HCT Types	4.5	5.5	
V _I , V _O	Input or output voltage		0	V _{CC}	V
t _t	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T _A	Temperature range		- 55	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating SMOS Inputs, literature number [SCBA004](#).

5.3 Thermal Information

THERMAL METRIC		CD74HC390, CD74HCT390		UNIT
		D (SOIC)	N (PDIP)	
		16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	73	67	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS ⁽¹⁾	V _{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V _{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		V
			6	4.2			4.2		4.2		V
V _{IL}	Low level input voltage		2	0.5			0.5		0.5		V
			4.5	1.35			1.35		1.35		V
			6	1.8			1.8		1.8		V
V _{OH}	High level output voltage	I _{OH} = - 20 μA	2	1.9			1.9		1.9		V
		I _{OH} = - 20 μA	4.5	4.4			4.4		4.4		V
		I _{OH} = - 20 μA	6	5.9			5.9		5.9		V
	High level output voltage	I _{OH} = - 4 mA	4.5	3.98			3.84		3.7		V
		I _{OH} = - 5.2 mA	6	5.48			5.34		5.2		V
V _{OL}	Low level output voltage	I _{OL} = 20 μA	2	0.1			0.1		0.1		V
		I _{OL} = 20 μA	4.5	0.1			0.1		0.1		V
		I _{OL} = 20 μA	6	0.1			0.1		0.1		V
	Low level output voltage	I _{OL} = 4 mA	4.5	0.26			0.33		0.4		V
		I _{OL} = 5.2 mA	6	0.26			0.33		0.4		V
I _I	Input leakage current	V _I = V _{CC} or GND	6	±0.1			±1		±1		μA
I _{CC}	Supply current	V _I = V _{CC} or GND	6	8			80		160		μA
HCT TYPES											
V _{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V _{IL}	Low level input voltage		4.5 to 5.5	0.8			0.8		0.8		V
V _{OH}	High level output voltage	I _{OH} = - 20 μA	4.5	4.4			4.4		4.4		V
	High level output voltage	I _{OH} = - 4 mA	4.5	3.98			3.84		3.7		V
V _{OL}	Low level output voltage	I _{OL} = 20 μA	4.5	0.1			0.1		0.1		V
	Low level output voltage	I _{OL} = 4 mA	4.5	0.26			0.33		0.4		V
I _I	Input leakage current	V _I = V _{CC} or GND	5.5	±0.1			±1		±1		μA
I _{CC}	Supply current	V _I = V _{CC} or GND	5.5	8			80		160		μA
Δ I _{CC} ⁽²⁾	Additional supply current per input pin	nCLK _A inputs held at V _{CC} - 2.1	4.5 to 5.5	100 162			202.5		220.5		μA
		nCLK _B , CLR inputs held at V _{CC} - 2.1	4.5 to 5.5	100 216			270		294		

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.

(2) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8mA.

5.5 Prerequisite for Switching Characteristics

PARAMETER		V _{CC} (V)	25°C	-40°C to 85°C		-55°C to 125°C		UNIT
			MIN	MIN	MAX	MIN	MAX	
HC TYPES								
f _{MAX}	Maximum Clock Frequency	2	6	5		4		MHz
		4.5	30	24		20		
		6	35	28		24		
t _W	Clock Pulse Width, n $\overline{\text{CLK}}$ _A , n $\overline{\text{CLK}}$ _B	2	80	100		120		ns
		4.5	16	20		24		
		6	14	17		20		
t _{REM}	Reset Removal Time	2	70	90		105		ns
		4.5	14	18		21		
		6	12	15		18		
t _W	Reset Pulse Width	2	50	65		75		ns
		4.5	10	13		15		
		6	9	11		13		
HCT TYPES								
f _{MAX}	Maximum Clock Frequency	4.5	27	22		18		MHz
t _W	Clock Pulse Width, n $\overline{\text{CLK}}$ _A , n $\overline{\text{CLK}}$ _B	4.5	19	24		29		ns
t _{REM}	Reset Removal Time	4.5	15	19		22		ns
t _W	Reset Pulse Width	4.5	13	16		20		ns

5.6 Switching Characteristics

Input t_r, t_f = 6 ns. Unless otherwise specified, C_L = 50pF. (see [Parameter Measurement Information](#))

PARAMETER		V _{CC} (V)	25°C		-40°C to 85°C	-55°C to 125°C	UNIT
			TYP	MAX	MAX	MAX	
HC TYPES							
t _{pd}	nCLK _A to nQ _A	2		175	220	265	ns
		4.5	14 ⁽³⁾	35	44	53	ns
		6		30	37	45	ns
	nCLK _B to nQ _B	2		185	230	280	ns
		4.5		37	46	56	ns
		6		31	39	48	ns
	nCLK _B to nQ _C	2		245	305	370	ns
		4.5		49	61	74	ns
		6		42	52	63	ns
	nCLK _B to nQ _D	2		180	225	270	ns
		4.5	15 ⁽³⁾	36	45	54	ns
		6		31	38	46	ns
	nCLK _A to nQ _D	2		365	455	550	ns
		4.5		73	91	110	ns
		6		62	77	94	ns
	CLR to Q _n	2		190	240	285	ns
		4.5	16 ⁽³⁾	38	48	57	ns
		6		32	41	48	ns

5.6 Switching Characteristics (continued)

Input t_r , t_f = 6 ns. Unless otherwise specified, C_L = 50pF. (see [Parameter Measurement Information](#))

PARAMETER		$V_{CC}(V)$	25°C		-40°C to 85°C	-55°C to 125°C	UNIT
			TYP	MAX	MAX	MAX	
t_t	Output Transition Times	2		75	95	110	ns
		4.5		15	19	22	ns
		6		13	16	19	ns
C_{IN}	Input Capacitance			10	10	10	pF
C_{PD}	Power Dissipation Capacitance ^{(1) (2)}	5	28 ⁽³⁾				pF
HCT TYPES							
t_{pd}	$n\overline{CLK}_A$ to nQ_A	4.5	17 ⁽³⁾	40	50	60	ns
	$n\overline{CLK}_B$ to nQ_B	4.5		43	51	65	ns
	$n\overline{CLK}_B$ to nQ_C	4.5		55	69	83	ns
	$n\overline{CLK}_B$ to nQ_D	4.5	18 ⁽³⁾	42	53	63	ns
	$n\overline{CLK}_A$ to nQ_C	4.5		84	105	126	ns
	CLR to Q_n	4.5	18 ⁽³⁾	42	53	63	ns
t_t	Output Transition Times	4.5		15	19	22	ns
C_{IN}	Input Capacitance			10 ⁽⁴⁾	10 ⁽⁴⁾	10 ⁽⁴⁾	pF
C_{PD}	Power Dissipation Capacitance ^{(1) (2)}	5	32 ⁽³⁾				pF

(1) C_{PD} is used to determine the dynamic power consumption, per package.

(2) $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2 + f_o)$ where f_i = Input Frequency, f_o = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

(3) C_L = 15 pF and V_{CC} = 5 V.

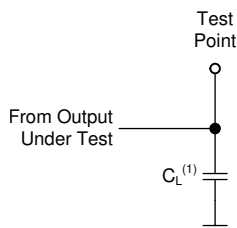
(4) C_L = 15 pF

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_f < 6 \text{ ns}$.

For clock inputs, $f_{\max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

图 6-1. Load Circuit for Push-Pull Outputs

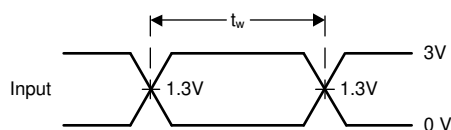


图 6-2. Voltage Waveforms, TTL-Compatible CMOS Inputs Pulse Duration

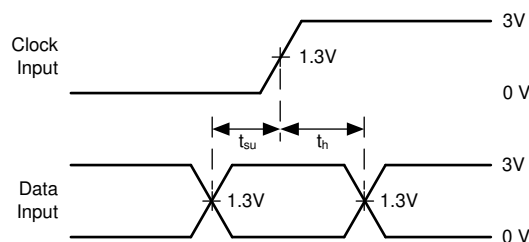
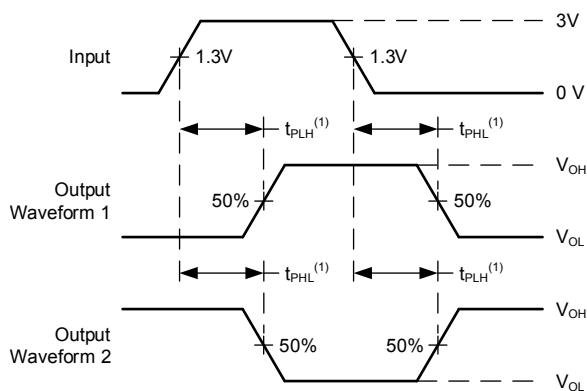


图 6-3. Voltage Waveforms, TTL-Compatible CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

图 6-4. Voltage Waveforms, TTL-Compatible CMOS Inputs Propagation Delays

7 Detailed Description

7.1 Overview

The CD74HC390 and ' HCT390 dual 4-bit decade ripple counters are high-speed silicon-gate CMOS devices and are pin compatible with low-power Schottky TTL (LSTTL). These devices are divided into four separately clocked sections. The counters have two divide-by-2 sections and two divide-by-5 sections. These sections are normally used in a BCD decade or bi-quinary configuration, since they share a common controller reset ($\overline{nCLR}$). If the two controller reset inputs ($1CLR$ and $2CLR$) are used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clock inputs ($\overline{nCLK}_A$ and $\overline{nCLK}_B$) of each section allow ripple counter or frequency division applications of divide-by-2, 4, 5, 10, 20, 25, 50, or 100. Each section is triggered by the High-to-Low transition of the input pulses ($\overline{nCLK}_A$ and $\overline{nCLK}_B$).

For BCD decade operation, the $\overline{nQ}_A$ output is connected to the $\overline{nCLK}_B$ input of the divide-by-5 section. For bi-quinary decade operation, the $\overline{nQ}_D$ output is connected to the $\overline{nCLK}_A$ input and $\overline{nQ}_A$ becomes the decade output.

The controller reset inputs ($1CLR$ and $2CLR$) are active-High asynchronous inputs to each decade counter which operates on the portion of the counter identified by the "1" and "2" prefixes in the pin configuration. A High level on the $\overline{nCLR}$ input overrides the clock and sets the four outputs Low.

7.2 Functional Block Diagram

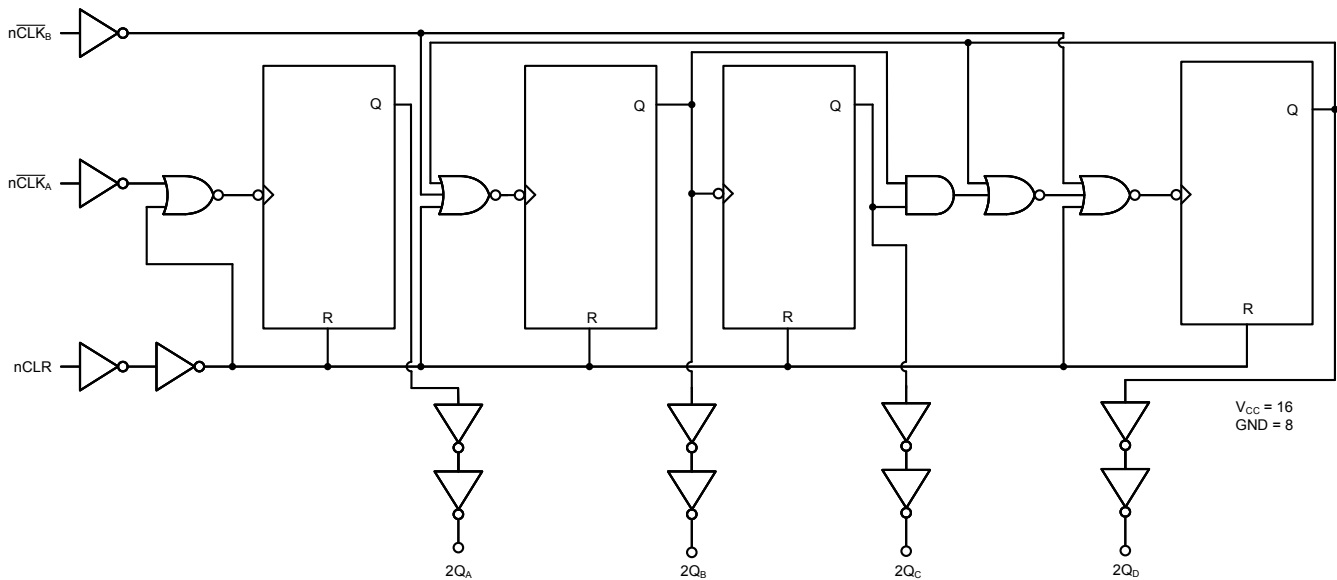


图 7-1. Functional Block Diagram

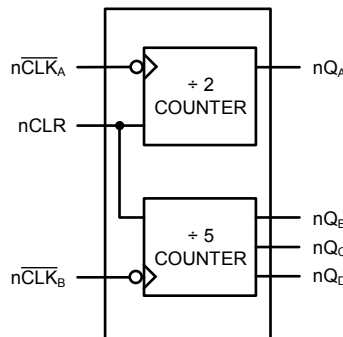


图 7-2. Functional Pinout

7.3 Device Functional Modes

表 7-1. Truth Table⁽¹⁾

INPUTS		ACTION
CLK	CLR	
↑	L	No Change
↓	L	Count
X	H	All Qs Low

- (1) H = High voltage level.
 L = Low voltage level.
 X = Dont care.
 ↑ = Transition from low to high level.
 ↓ = Transition from high to low.

表 7-2. BCD Count Sequence For ½ the 390⁽¹⁾

COUNT	OUTPUTS			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

- (1) Output nQ_A connected to nCLK_B with counter input on nCLK_A.

表 7-3. B-Quinary Count Sequence For ½ the 390⁽¹⁾

COUNT	OUTPUTS			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	H	L
2	L	H	L	L
3	L	H	H	L
4	H	L	L	L
5	L	L	L	H
6	L	L	H	H
7	L	H	L	H
8	L	H	H	H
9	H	L	L	H

- (1) Output nQ_D connected to nCLK_A with counter input on nCLK_B.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9098401MEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9098401ME A CD54HCT390F3A
CD54HCT390F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9098401ME A CD54HCT390F3A
CD54HCT390F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9098401ME A CD54HCT390F3A
CD74HC390E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC390E
CD74HC390E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC390E
CD74HC390EE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC390E
CD74HC390M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC390M
CD74HC390M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HC390M
CD74HC390M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC390M
CD74HCT390E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT390E
CD74HCT390E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT390E
CD74HCT390EE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT390E
CD74HCT390M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HCT390M
CD74HCT390M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT390M
CD74HCT390M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT390M
CD74HCT390MT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HCT390M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD54HCT390, CD74HCT390 :

- Catalog : [CD74HCT390](#)
- Military : [CD54HCT390](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC390M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT390M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC390M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HCT390M96	SOIC	D	16	2500	353.0	353.0	32.0

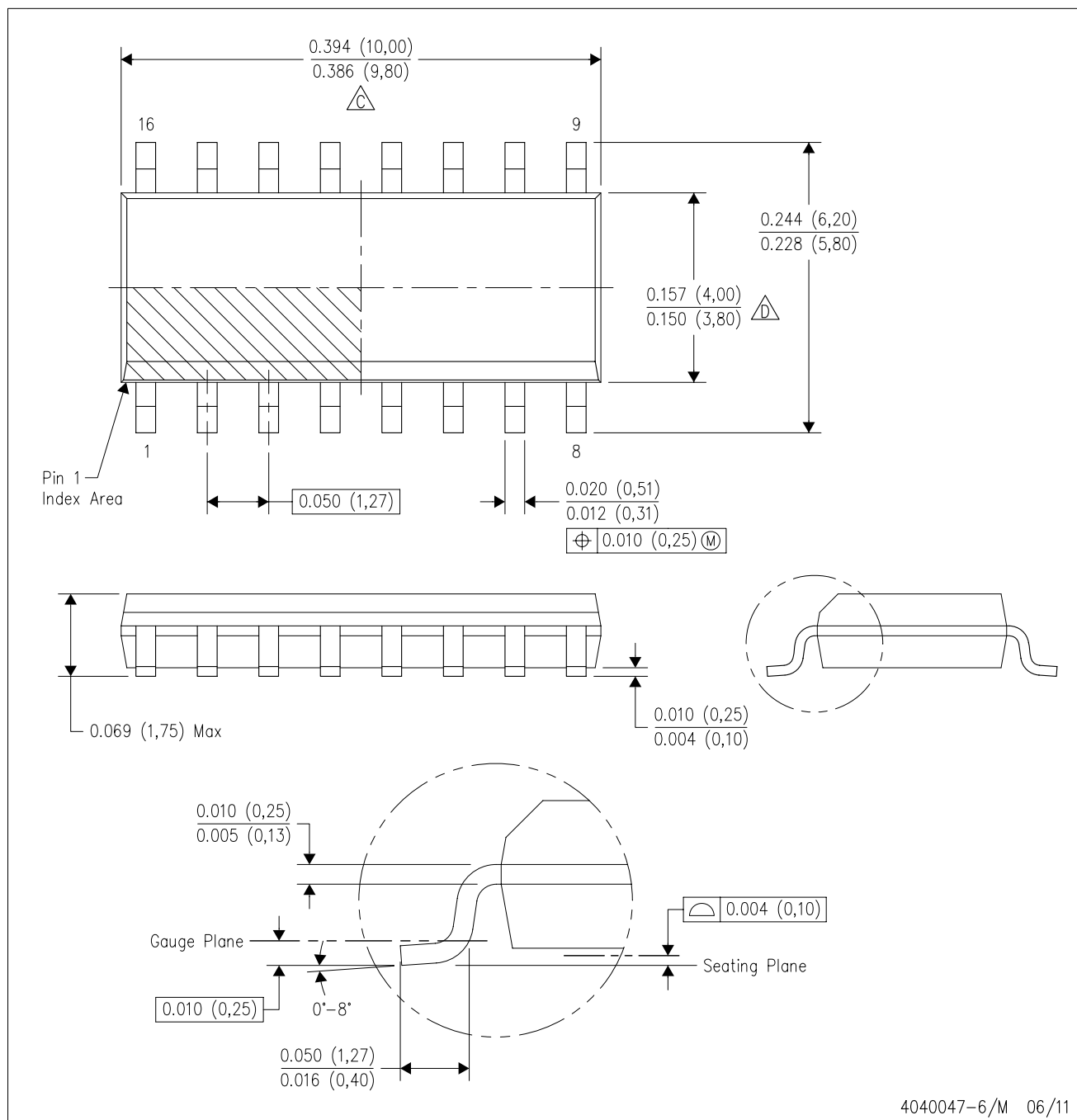
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC390E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC390E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC390E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC390E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC390EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC390EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT390E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT390E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT390E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT390E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT390EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT390EE4	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

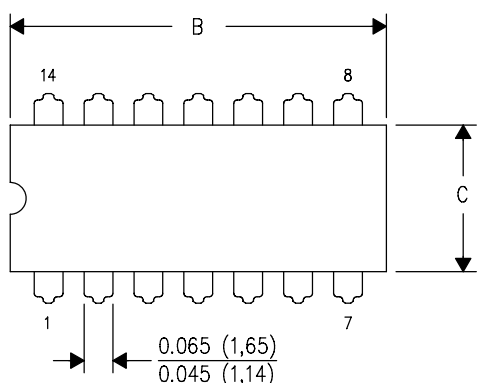
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

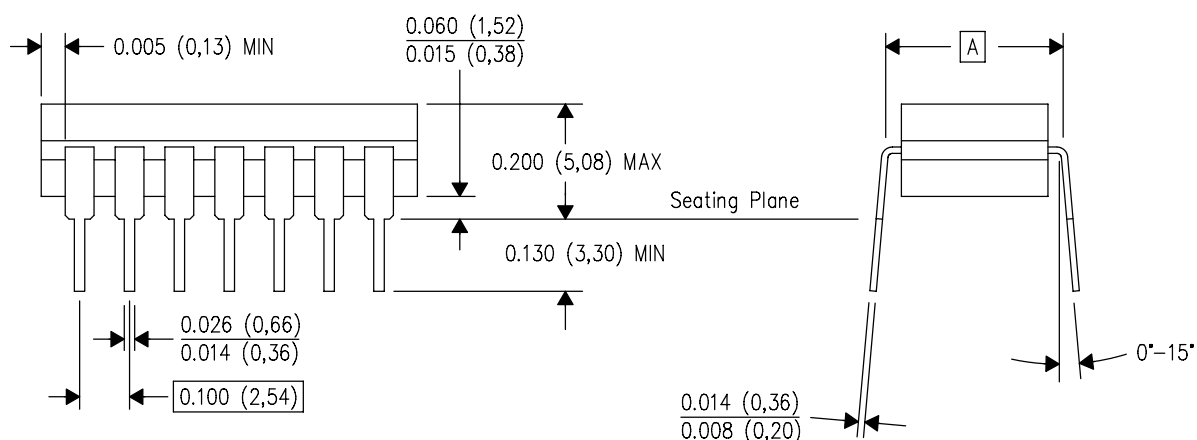
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

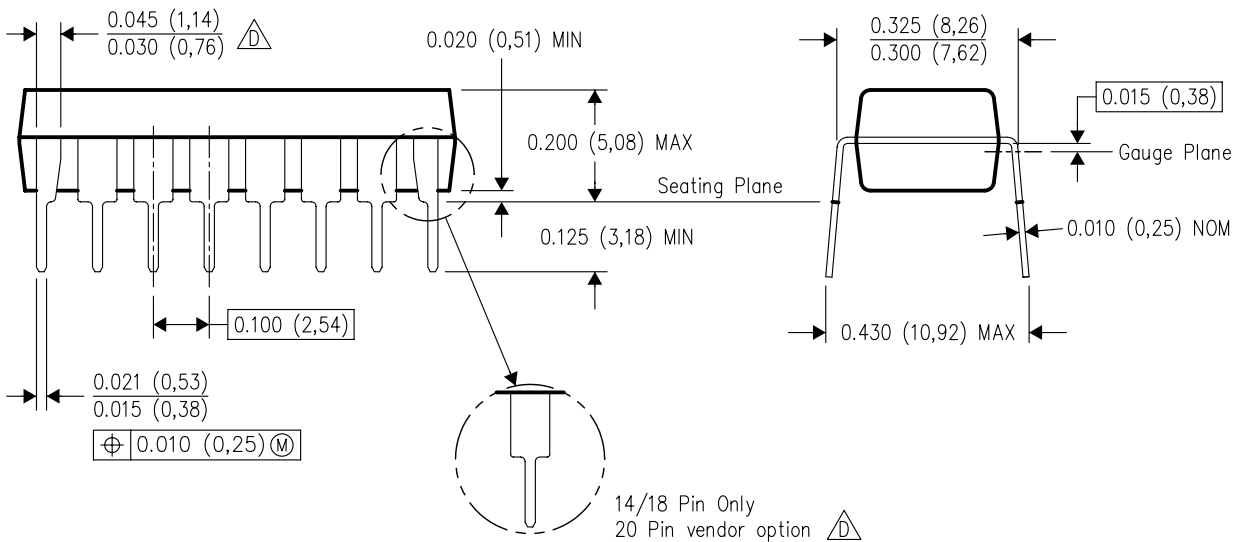
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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