

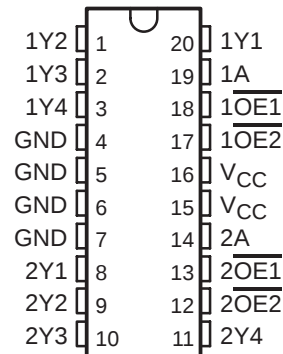
CDC208

DUAL 1-LINE TO 4-LINE CLOCK DRIVER WITH 3-STATE OUTPUTS

SCAS109F – APRIL 1990 – REVISED OCTOBER 1998

- Low-Skew Propagation Delay Specifications for Clock-Driver Applications
- TTL-Compatible Inputs and CMOS-Compatible Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise
- **EPIC™** (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline (DW)

DW PACKAGE
(TOP VIEW)



description

The CDC208 contains dual clock-driver circuits that fanout one input signal to four outputs with minimum skew for clock distribution (see Figure 2). The device also offers two output-enable ($\overline{OE1}$ and $\overline{OE2}$) inputs for each circuit that can force the outputs to be disabled to a high-impedance state or to a high- or low-logic level independent of the signal on the respective A input.

Skew parameters are specified for a reduced temperature and voltage range common to many applications.

The CDC208 is characterized for operation from -40°C to 85°C.

FUNCTION TABLES

INPUTS			OUTPUTS			
$\overline{1OE1}$	$\overline{1OE2}$	1A	1Y1	1Y2	1Y3	1Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z

INPUTS			OUTPUTS			
$\overline{2OE1}$	$\overline{2OE2}$	2A	2Y1	2Y2	2Y3	2Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

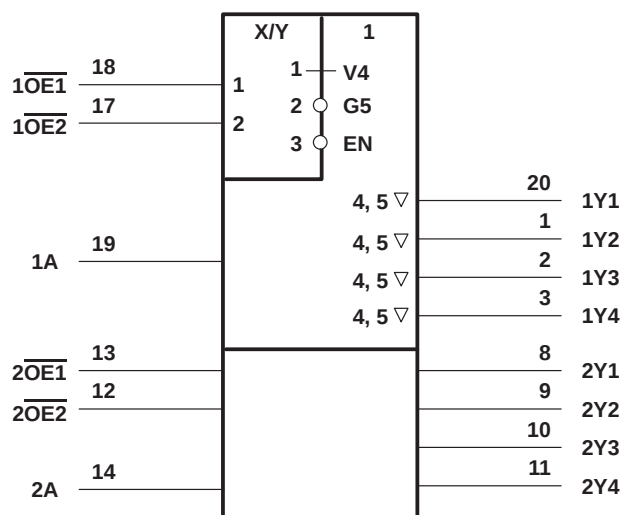
Copyright © 1998, Texas Instruments Incorporated

CDC208

DUAL 1-LINE TO 4-LINE CLOCK DRIVER WITH 3-STATE OUTPUTS

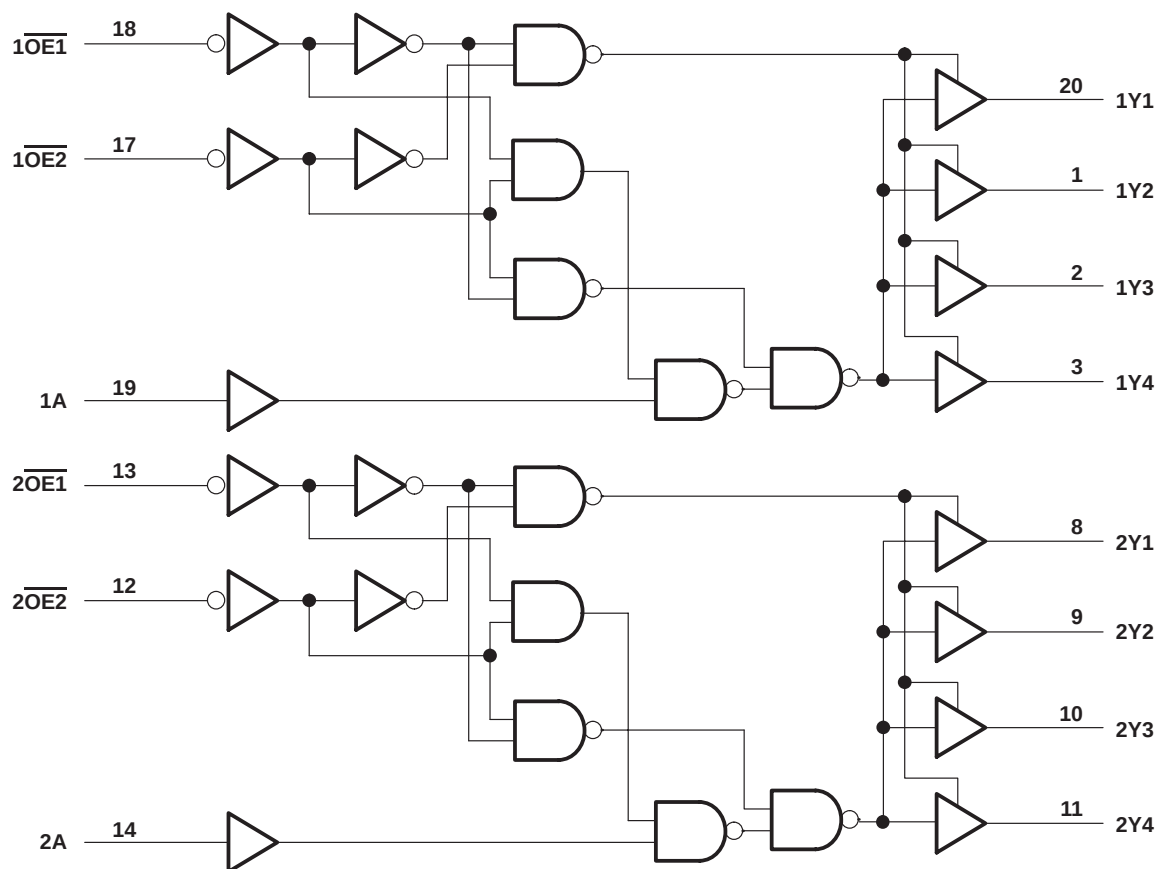
SCAS109F – APRIL 1990 – REVISED OCTOBER 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



CDC208

DUAL 1-LINE TO 4-LINE CLOCK DRIVER WITH 3-STATE OUTPUTS

SCAS109F – APRIL 1990 – REVISED OCTOBER 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±200 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2)	1.6 W
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
V_I Input voltage	0	V_{CC}		V
I_{OH} High-level output current			–24	mA
I_{OL} Low-level output current			24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0		10	ns/V
f_{clock} Input clock frequency			60	MHz
T_A Operating free-air temperature	–40		85	°C



CDC208

DUAL 1-LINE TO 4-LINE CLOCK DRIVER WITH 3-STATE OUTPUTS

SCAS109F – APRIL 1990 – REVISED OCTOBER 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 µA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I _{OH} = -75 mA [†]	5.5 V				3.85		
V _{OL}	I _{OL} = 50 µA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I _{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I _{OL} = 75 mA [†]	5.5 V					1.65	
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1	µA
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±5	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		80	µA
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			0.9		1	mA
C _i	V _I = V _{CC} or GND	5 V		4				pF
C _o	V _O = V _{CC} or GND	5 V		10				pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

CDC208
DUAL 1-LINE TO 4-LINE CLOCK DRIVER
WITH 3-STATE OUTPUTS

SCAS109F – APRIL 1990 – REVISED OCTOBER 1998

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	1A and 2A	Any Y	5.3	8.5	10.9	5.3	11.7	ns
t_{PHL}			3.6	7.7	11	3.6	11.5	
t_{PLH}	$\overline{1OE1}$, $\overline{1OE2}$, and $\overline{2OE1}$, $\overline{2OE2}$	Any Y	4.7	8.5	11.7	4.7	12.8	ns
t_{PHL}			4.4	8.4	11.3	4.4	12.4	
t_{PZH}	$\overline{1OE2}$ or $\overline{2OE2}$	Any Y	4.4	8.1	11.3	4.4	12.4	ns
t_{PZL}	$\overline{1OE1}$ or $\overline{2OE1}$		5	9.6	13.3	5	14.9	
t_{PHZ}	$\overline{1OE2}$ or $\overline{2OE2}$	Any Y	4.2	7.4	9.3	4.2	10.2	ns
t_{PLZ}	$\overline{1OE1}$ or $\overline{2OE1}$		5.4	7.5	9.2	5.4	9.9	

switching characteristics, $V_{CC} = 5\text{ V} \pm 0.25\text{ V}$, $T_A = 25^\circ\text{C}$ to 70°C (see Note 3 and Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{PLH}	1A and 2A	Any Y	6.6	10.2	ns
t_{PHL}			6.6	9.8	
$t_{sk(o)}$	1A and 2A	Any Y		1	ns

NOTE 3: All specifications are valid only for all outputs switching simultaneously and in phase.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per bank	Outputs enabled	96	pF
		Outputs disabled	12	

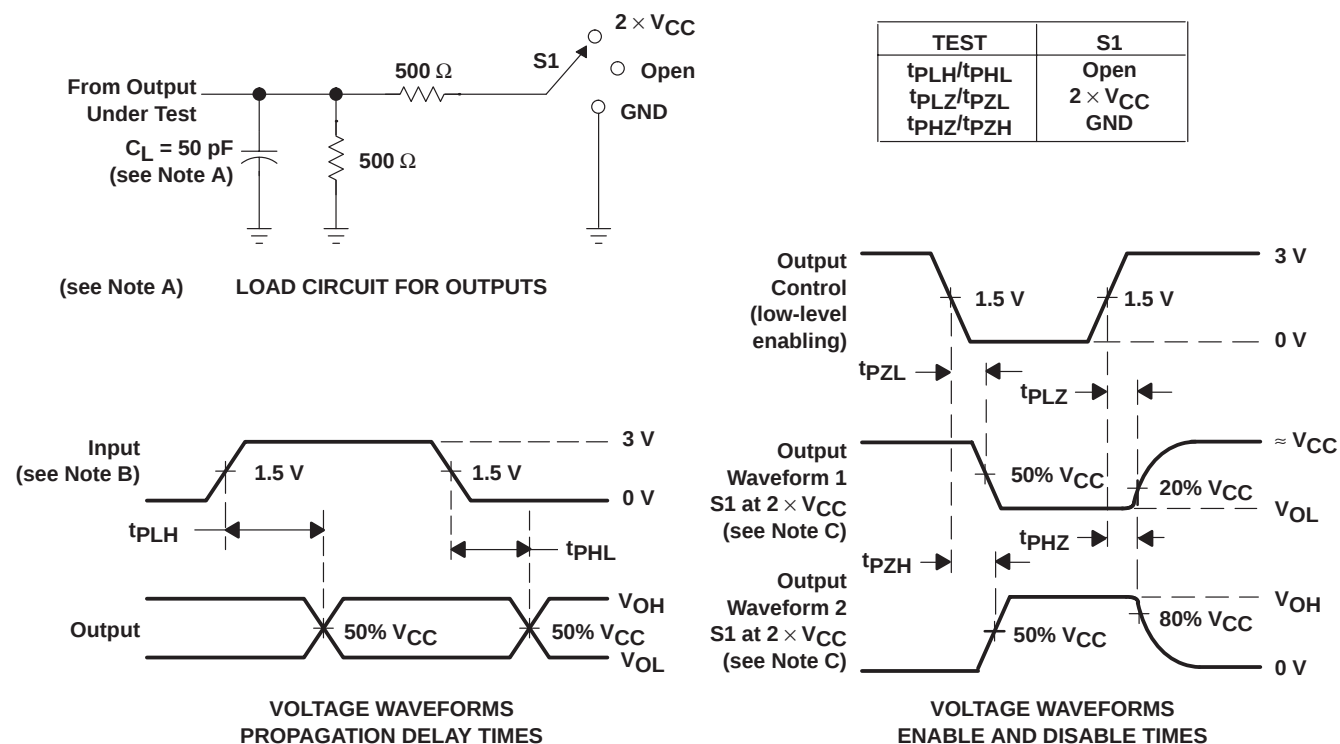


CDC208

DUAL 1-LINE TO 4-LINE CLOCK DRIVER WITH 3-STATE OUTPUTS

SCAS109F – APRIL 1990 – REVISED OCTOBER 1998

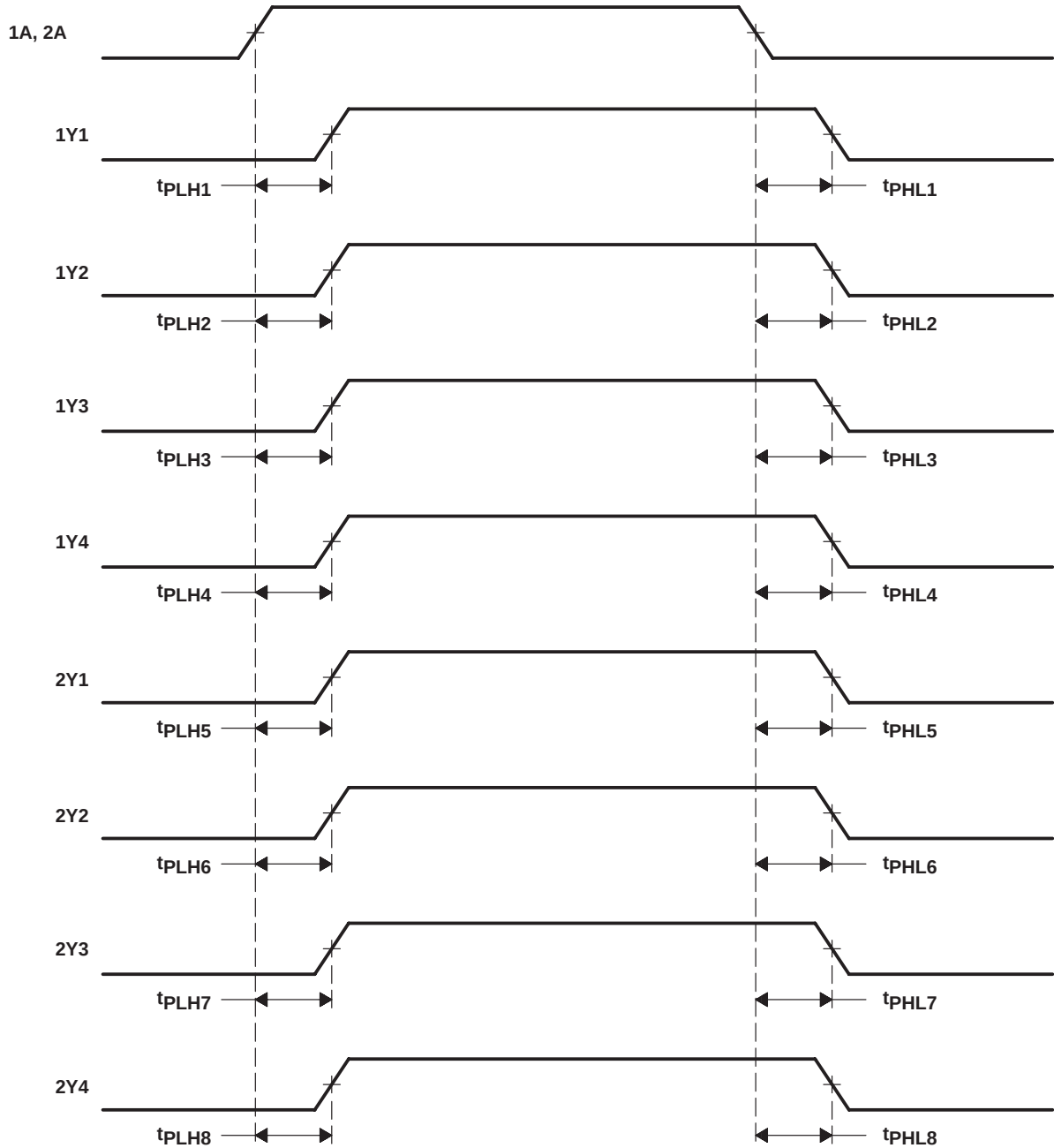
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$. For testing pulse duration: $t_r = t_f = 1 \text{ to } 3 \text{ ns}$. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:

- The difference between the fastest and slowest of t_{PLHn} ($n = 1, 2, \dots, 8$)
- The difference between the fastest and slowest of t_{PHLn} ($n = 1, 2, \dots, 8$)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDC208DW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	CDC208
CDC208DW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC208
CDC208DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	CDC208
CDC208DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC208
CDC208NS	Active	Production	SOP (NS) 20	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC208
CDC208NS.A	Active	Production	SOP (NS) 20	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC208
CDC208NSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC208
CDC208NSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC208

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

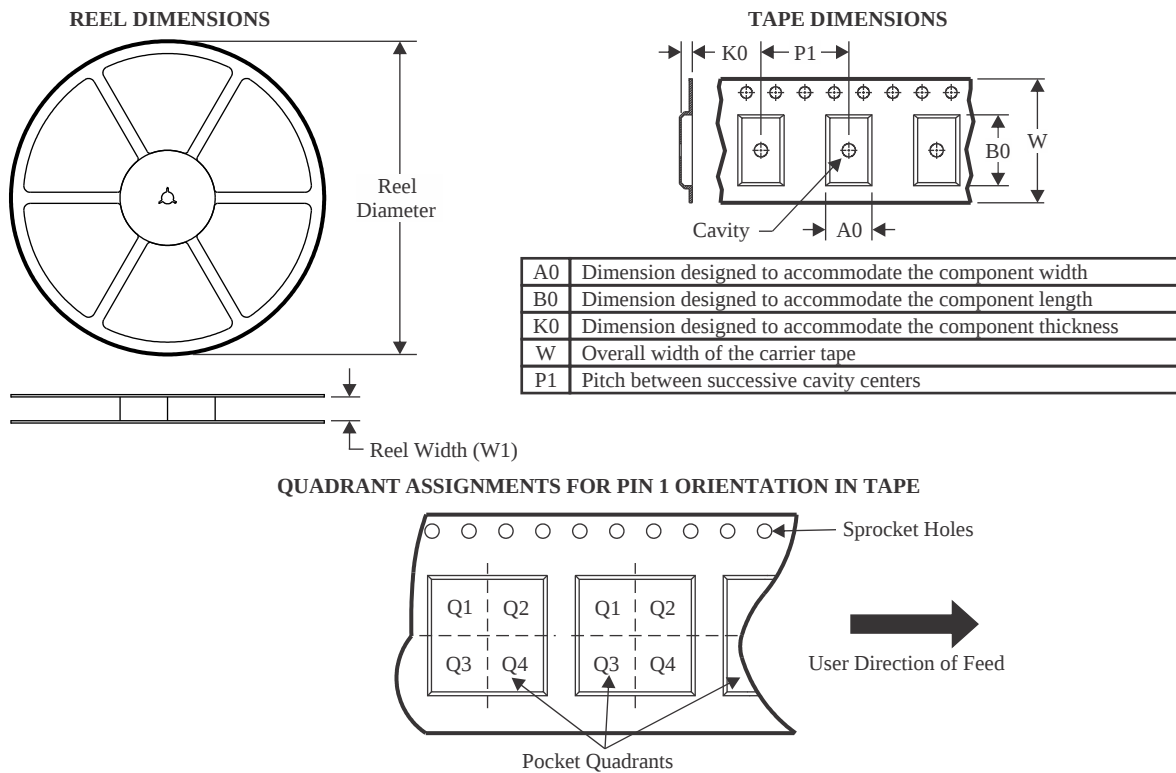
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

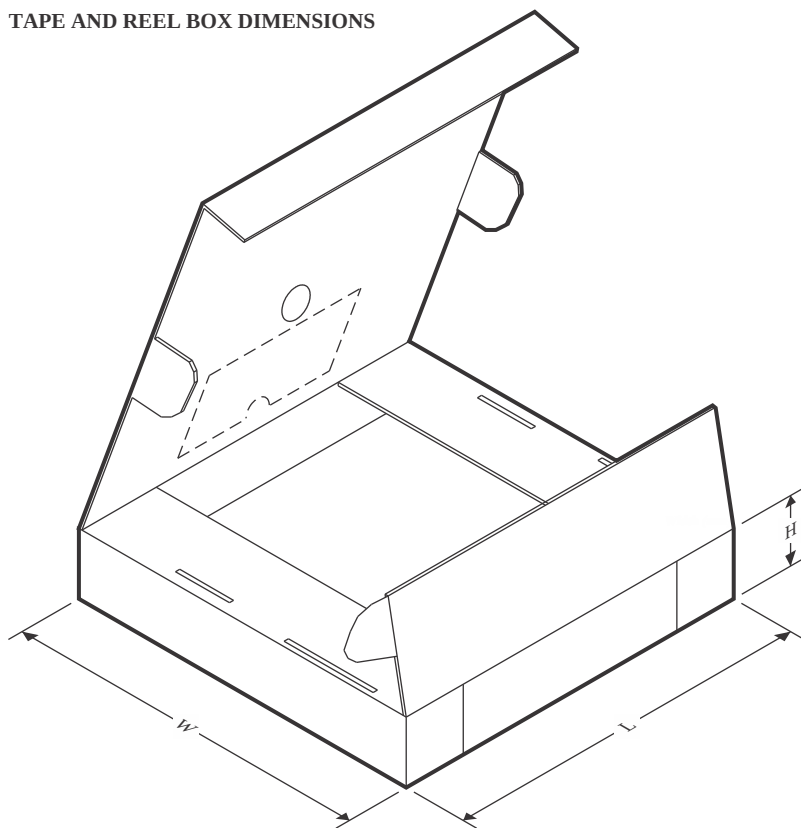
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC208DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CDC208NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC208DWR	SOIC	DW	20	2000	356.0	356.0	45.0
CDC208NSR	SOP	NS	20	2000	356.0	356.0	45.0

TUBE



*All dimensions are nominal

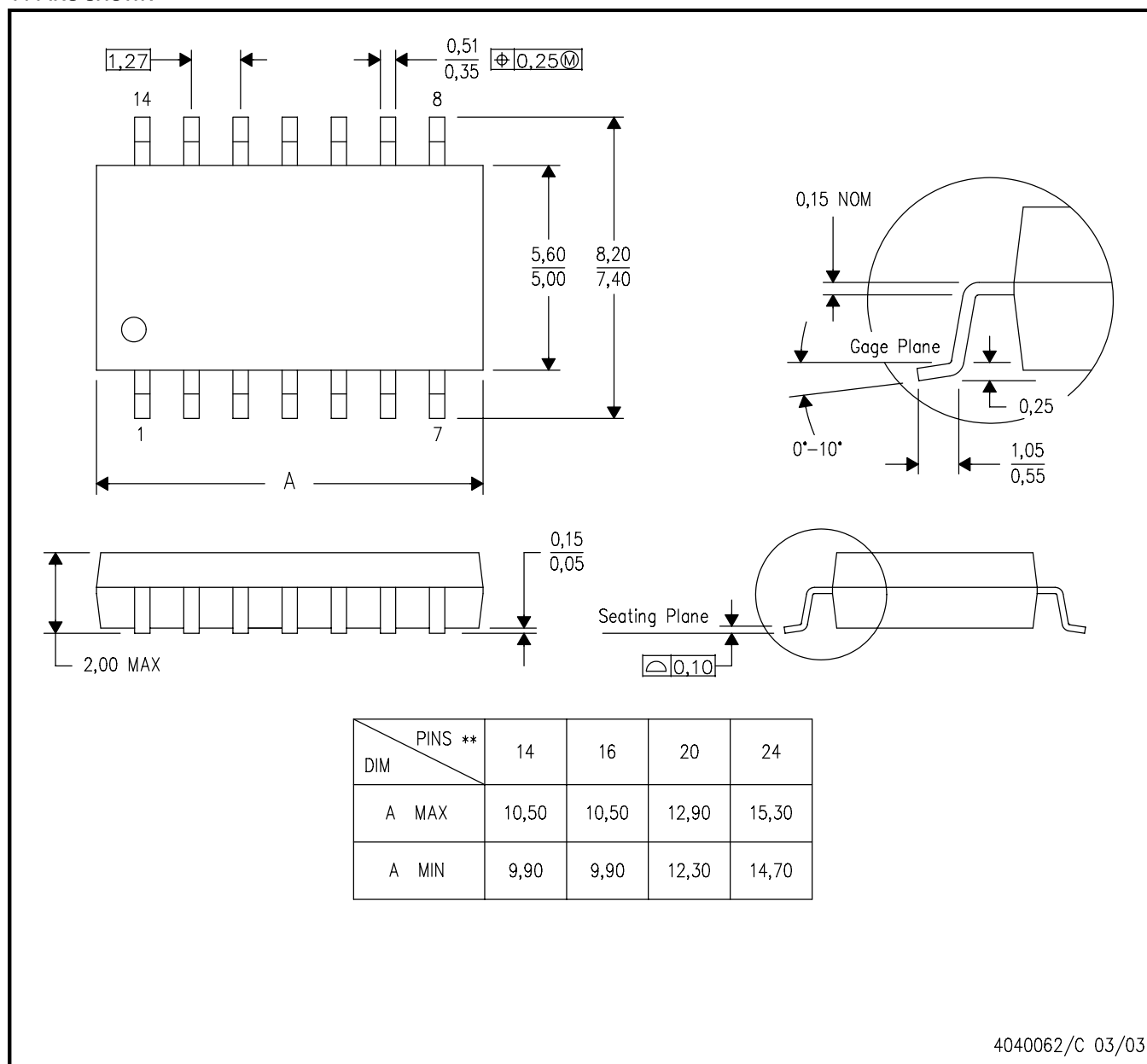
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CDC208DW	DW	SOIC	20	25	507	12.83	5080	6.6
CDC208DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
CDC208NS	NS	SOP	20	40	530	10.5	4000	4.1
CDC208NS.A	NS	SOP	20	40	530	10.5	4000	4.1

MECHANICAL DATA

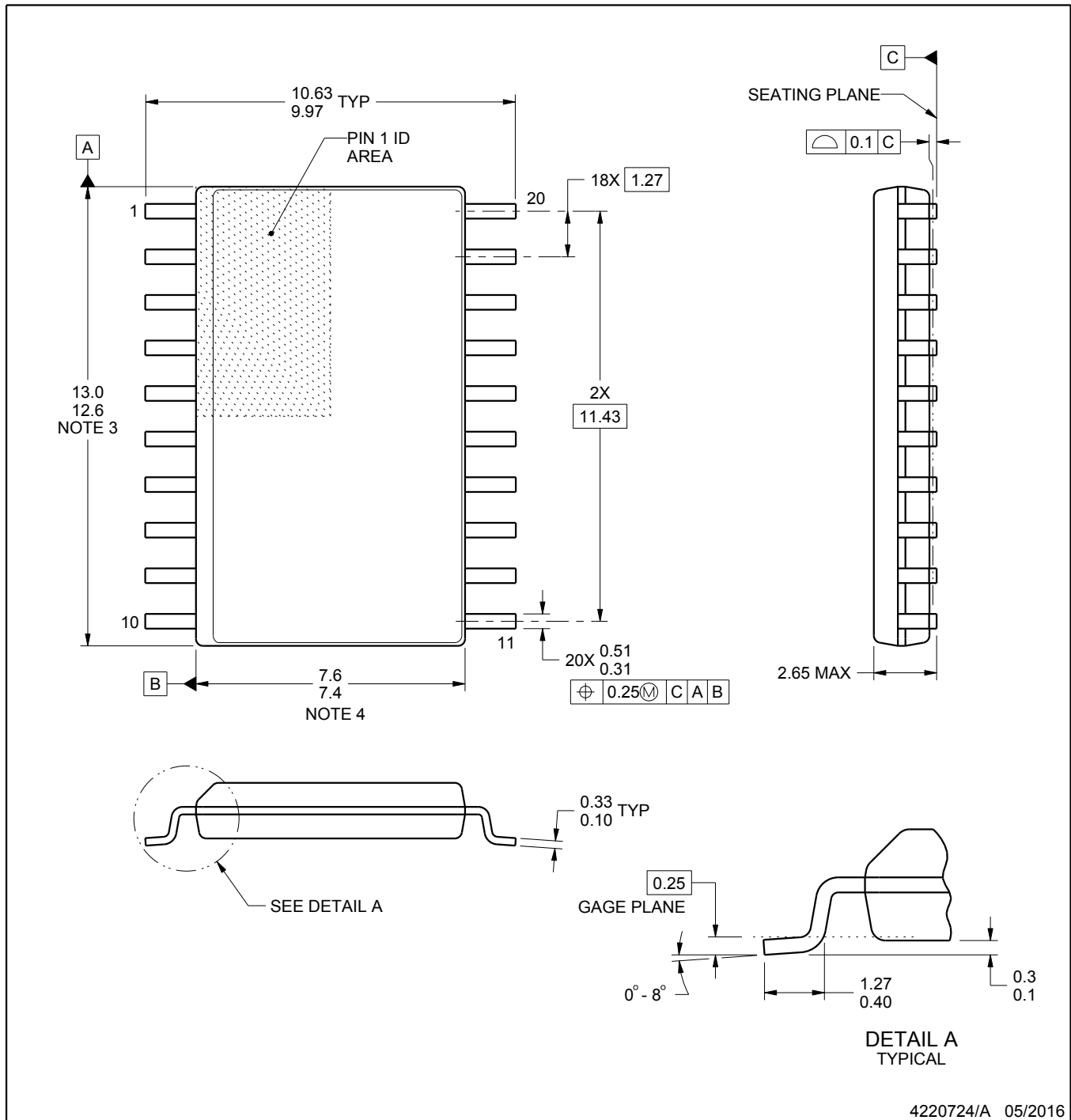
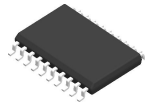
NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



4220724/A 05/2016

NOTES:

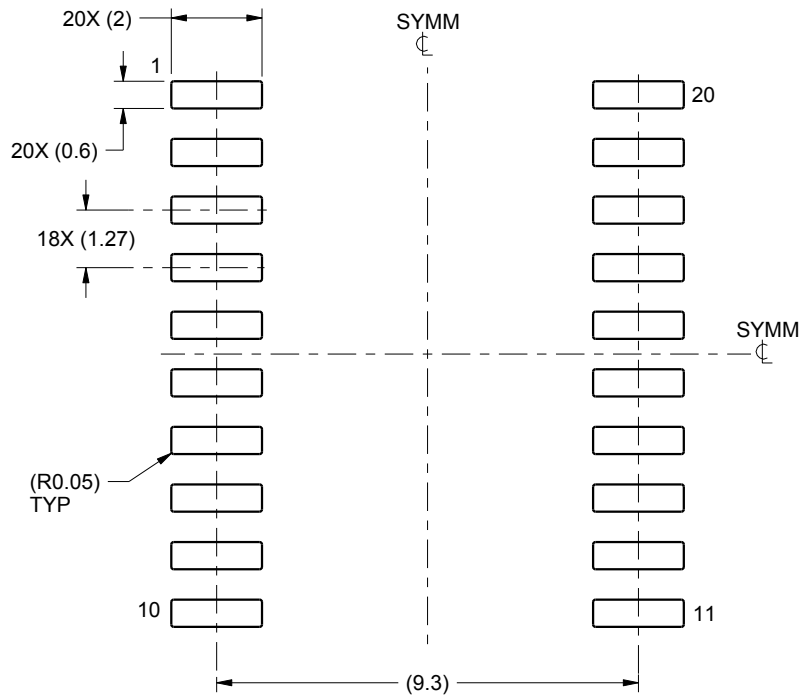
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

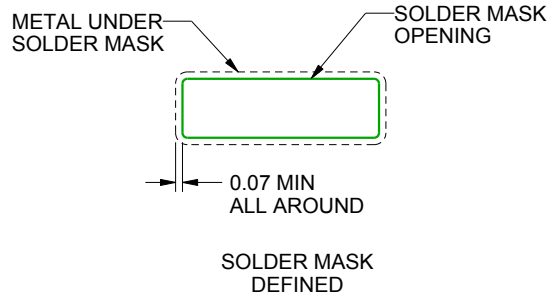
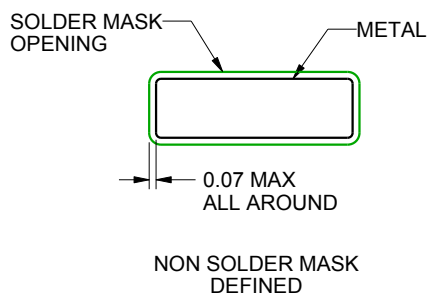
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

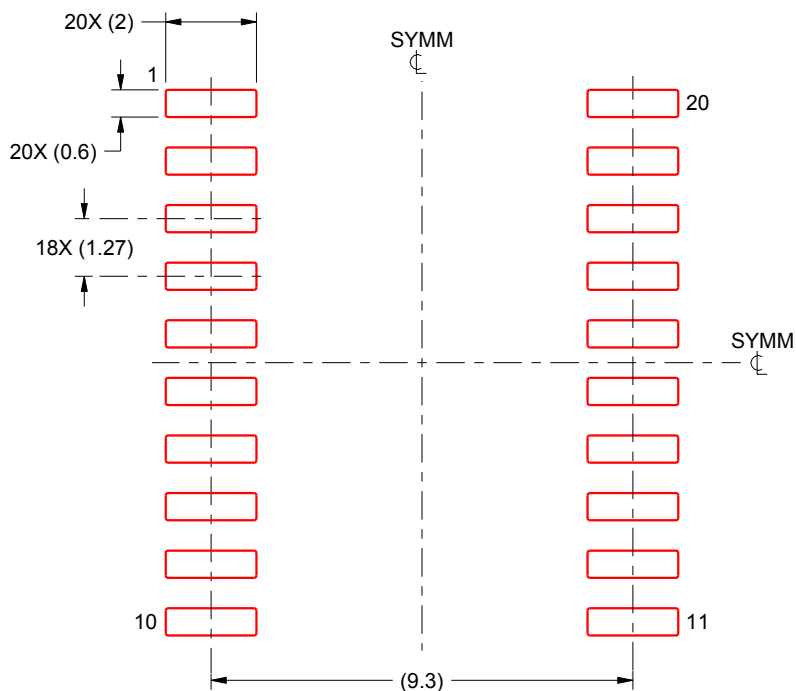
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025