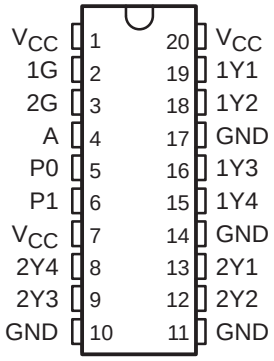
- **Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications**
- **TTL-Compatible Inputs and Outputs**
- **Distributes One Clock Input to Eight Outputs**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **High-Drive Outputs (–48-mA I_{OH}, 48-mA I_{OL})**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Packaging Options Include Plastic Small-Outline (DW) Packages**

DW PACKAGE
(TOP VIEW)



description

The CDC341 is a high-performance clock-driver circuit that distributes one (A) input signal to eight (Y) outputs with minimum skew for clock distribution. Through the use of the control pins (1G and 2G), the outputs can be placed in a low state regardless of the A input.

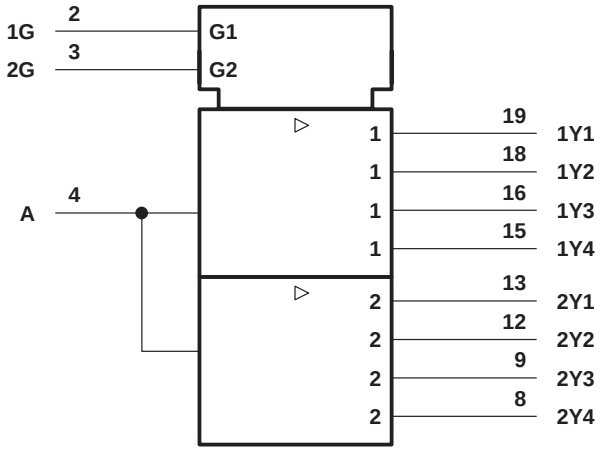
The propagation delays are adjusted at the factory using the P0 and P1 pins. These pins are not intended for customer use and should be strapped to GND.

The CDC341 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

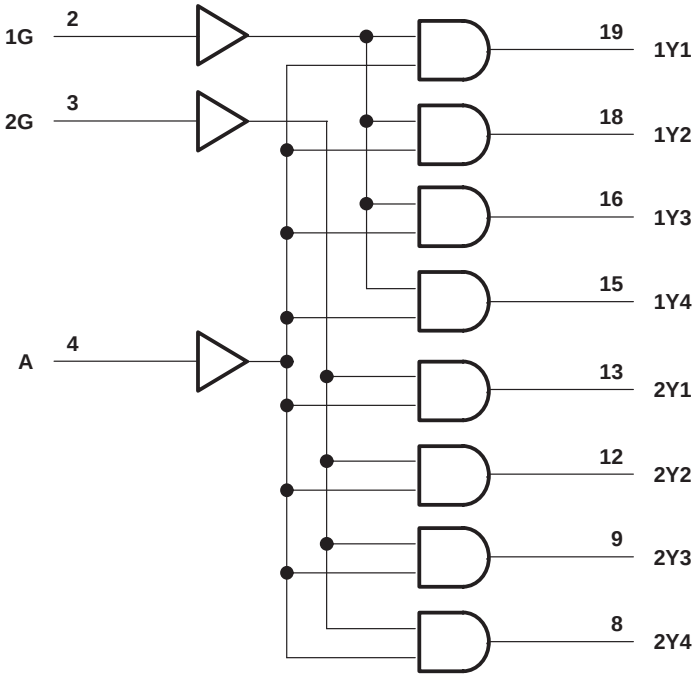
INPUTS			OUTPUTS	
1G	2G	A	1Y1–1Y4	2Y1–2Y4
X	X	L	L	L
L	L	H	L	L
L	H	H	L	H
H	L	H	H	L
H	H	H	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state,
V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O . . . . . 96 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) . . . . . 1.6 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
I_{OH}	High-level output current			–48	mA
I_{OL}	Low-level output current			48	mA
f_{clock}	Input clock frequency	One output bank loaded		80	MHz
		Both output banks loaded		40	
T_A	Operating free-air temperature		0	70	°C

NOTE 3: Unused pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP†	MAX			
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA				–1.2		–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = – 3 mA		2.5			2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		
	V_{CC} = 4.75 V,	I_{OH} = – 48 mA		2			2		
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 48 mA						0.5	V
I_I	V_{CC} = 5.25 V,	V_I = V_{CC} or GND				±1		±1	µA
I_O‡	V_{CC} = 5.25 V,	V_O = 2.5 V		–50	–100	–200	–50	–200	mA
I_{CC}	V_{CC} = 5.25 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		2			3.5	mA
			Outputs low		24			33	
C_i	V_I = 2.5 V or 0.5 V				3				pF

† All typical values are at V_{CC} = 5 V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics, C_L = 50 pF (see Figures 1 and 2)

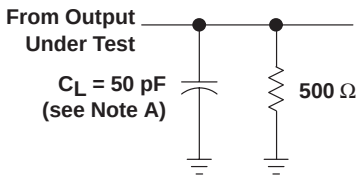
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	3.5		4.5	3.1	4.9	ns
t_{PHL}			3.5		4.3	3.1	4.9	
t_{PLH}	G	Y	2		3.8	2	4	ns
t_{PHL}			2		3.8	2	4	
$t_{sk(o)}$	A	Y		0.3	0.5		0.6	ns
$t_{sk(p)}$				0.6	0.8		0.9	
$t_{sk(pr)}$					1		1	
t_r	A	Y					1.5	ns
t_f	A	Y					1.5	ns

t_{pd} performance information relative to V_{CC} and temperature variation (see Note 4)

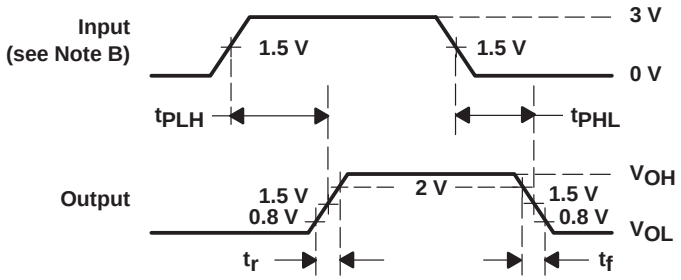
$Dt_{PLH(TA)}$†	Temperature drift of t_{PLH} from 0°C to 70°C	–41 ps/10°C
$Dt_{PHL(TA)}$†	Temperature drift of t_{PHL} from 0°C to 70°C	–52 ps/10°C
$Dt_{PLH(VCC)}$‡	V_{CC} drift of t_{PLH} from 4.75 V to 5.25 V	28 ps/100 mV
$Dt_{PHL(VCC)}$‡§	V_{CC} drift of t_{PHL} from 4.75 V to 5.25 V	20 ps/100 mV

† Virtually independent of V_{CC}
‡ Virtually independent of temperature
NOTE 4: The data extracted is from a wide range of characterization material.

PARAMETER MEASUREMENT INFORMATION



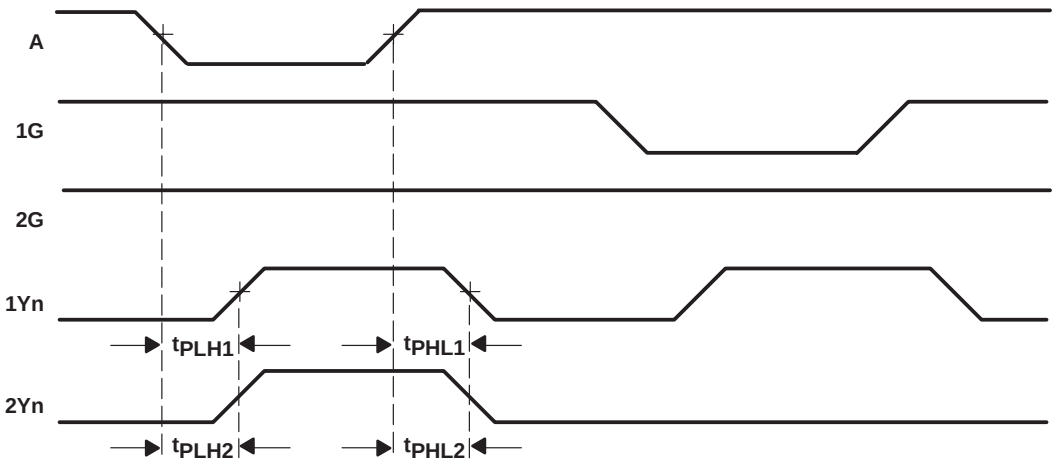
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
– The difference between the fastest and slowest of t_{PLHn} (n = 1, 2)
– The difference between the fastest and slowest of t_{PHLn} (n = 1, 2)
B. Pulse skew, $t_{sk(p)}$, is calculated as the greater of | $t_{PLHn} - t_{PHLn}$ | (n = 1, 2).
C. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
– The difference between the fastest and slowest of t_{PLHn} (n = 1, 2) across multiple devices under identical operating conditions
– The difference between the fastest and slowest of t_{PHLn} (n = 1, 2) across multiple devices under identical operating conditions

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$, $t_{sk(pr)}$

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDC341DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC341
CDC341DW.B	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC341
CDC341DWG4	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC341
CDC341DWG4.B	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC341
CDC341DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC341
CDC341DWR.B	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC341

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

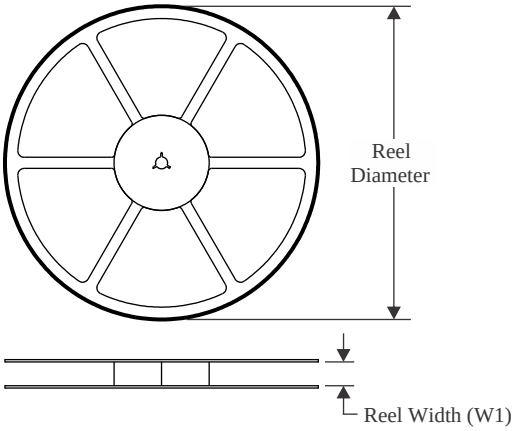
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

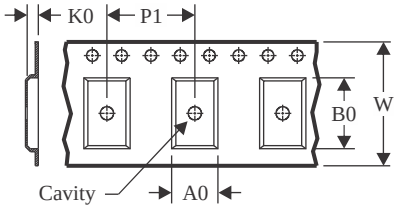
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

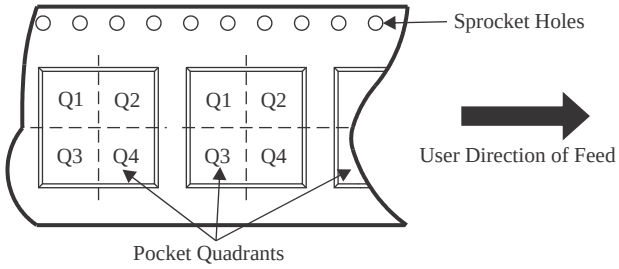


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

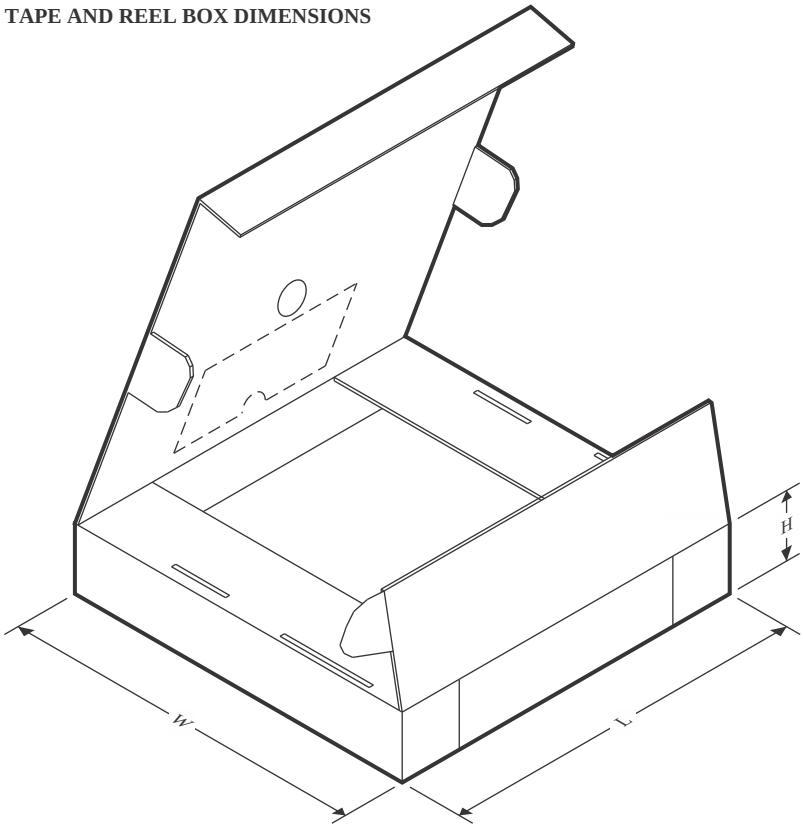
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC341DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

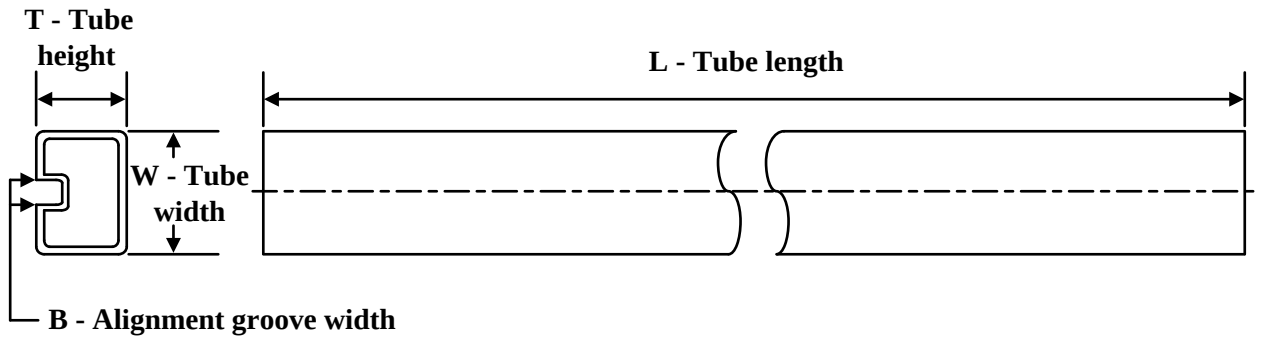
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC341DWR	SOIC	DW	20	2000	356.0	356.0	45.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CDC341DW	DW	SOIC	20	25	507	12.83	5080	6.6
CDC341DW.B	DW	SOIC	20	25	507	12.83	5080	6.6
CDC341DWG4	DW	SOIC	20	25	507	12.83	5080	6.6
CDC341DWG4.B	DW	SOIC	20	25	507	12.83	5080	6.6

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