PROGRAMMABLE 3-PLL CLOCK SYNTHESIZER / MULTIPLIER / DIVIDER

Check for Samples: CDC906

FEATURES

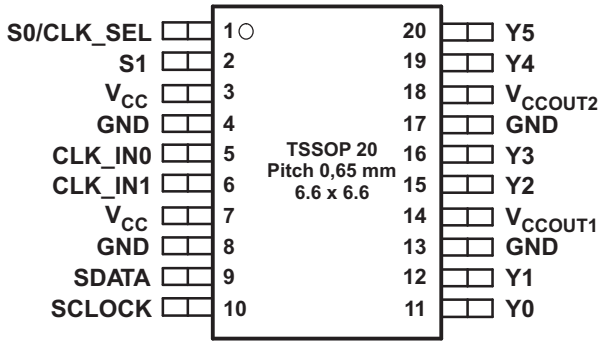
- High Performance 3:6 PLL based Clock Synthesizer / Multiplier / Divider
- User Programmable PLL Frequencies
- Easy In-Circuit Programming via SMBus Data Interface
- Wide PLL Divider Ratio Allows 0-PPM Output Clock Error
- Generates Precise Video (27 MHz or 54 MHz) and Audio System Clocks from Multiple Sampling Frequencies (f_S = 16, 22.05, 24, 32, 44.1, 48, 96 kHz)
- Clock Inputs Accept a Crystal or a Single-Ended LVCMOS or a Differential Input Signal
- Accepts Crystal Frequencies from 8 MHz up to 54 MHz
- Accepts LVCMOS or Differential Input Frequencies up to 167 MHz
- Two Programmable Control Inputs [S0/S1] for User Defined Control Signals
- Six LVCMOS Outputs with Output Frequencies up to 167 MHz
- LVCMOS Outputs can be Programmed for Complementary Signals
- Free Selectable Output Frequency via Programmable Output Switching Matrix [6x6] Including 7-Bit Post-Divider for Each Output
- PLL Loop Filter Components Integrated
- Low Period Jitter (Typical 60 ps)
- Features Spread Spectrum Clocking (SSC) for Lowering System EMI
- Programmable Center Spread SSC Modulation (±0.1%, ±0.25%, and ±0.4%) with a Mean Phase Equal to the Phase of the Non-Modulated Frequency
- Programmable Down Spread SSC Modulation (1%, 1.5%, 2%, and 3%)
- Programmable Output Slew-Rate Control (SRC) for Lowering System EMI
- 3.3-V Device Power Supply
- Commercial Temperature Range 0°C to 70°C
- Development and Programming Kit for Easy PLL Design and Programming (TI Pro-Clock™)
- Packaged in 20-Pin TSSOP
- Factory Programmable for Customized Default Settings are Available. Contact TI Sales Fordes for Further Details.

APPLICATIONS

- Digital TV
- Printer / Scanner
- Set Top Box
- Video / Audio

TERMINAL ASSIGNMENT

PW PACKAGE
(TOP VIEW)



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION

The CDC906 is one of the smallest and powerful PLL synthesizer / multiplier / divider available today. Despite its small physical outlines, the CDC906 is flexible. It has the capability to produce an almost independent output frequency from a given input frequency.

The input frequency can be derived from a LVCMOS, differential input clock, or a single crystal. The appropriate input waveform can be selected via the SMBus data interface controller.

To achieve an independent output frequency the reference divider M and the feedback divider N for each PLL can be set to values from 1 up to 511 for the M-Divider and from 1 up to 4095 for the N-Divider. The PLL-VCO (voltage controlled oscillator) frequency than is routed to the free programmable output switching matrix to any of the six outputs. The switching matrix includes an additional 7-bit post-divider (1-to-127) and an inverting logic for each output.

The deep M/N divider ratio allows the generation of zero ppm clocks from any reference input frequency (e.g., a 27 MHz).

The CDC906 includes three PLLs of those one supports SSC (spread-spectrum clocking). PLL1, PLL2, and PLL3 are designed for frequencies up to 167 MHz and optimized for zero-ppm applications with wide divider factors.

PLL2 also supports center-spread and down-spread spectrum clocking (SSC). This is a common technique to reduce electro-magnetic interference. Also, the slew-rate controllable (SRC) output edges minimize EMI noise.

Based on the PLL frequency and the divider settings, the internal loop filter components is automatically adjusted to achieve high stability and optimized jitter transfer characteristic of the PLL.

The device provides customized applications. It is preprogrammed with a factory default configuration (see Figure 13) and can be reprogrammed to a different application configuration via the serial SMBus interface.

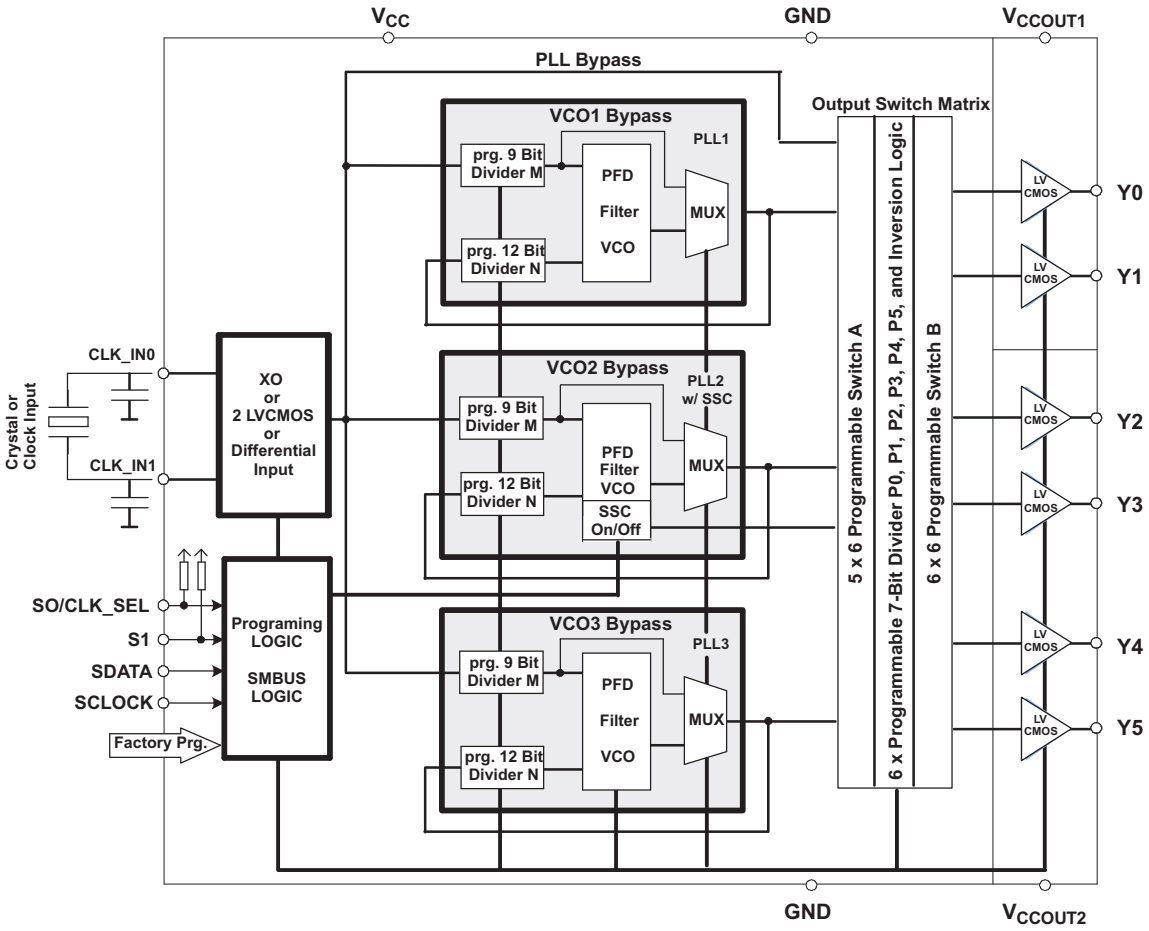
Two free programmable inputs, S0 and S1, can be used to control for each application the most demanding logic control settings (outputs disable to low, outputs 3-state, power down, PLL bypass, etc).

The CDC906 has three power supply pins, V_{CC}, V_{CCOUT1} and V_{CCOUT2}. V_{CC} is the power supply for the device. It operates from a single 3.3-V supply voltage. V_{CCOUT1} and V_{CCOUT2} are the power supply pins for the outputs. V_{CCOUT1} supplies the outputs Y0 and Y1 and V_{CCOUT2} supplies the outputs Y2, Y3, Y4, and Y5. Both outputs supplies can be 2.3 V to 3.6 V. At output voltages lower than 3.3 V, the output drive current is limited.

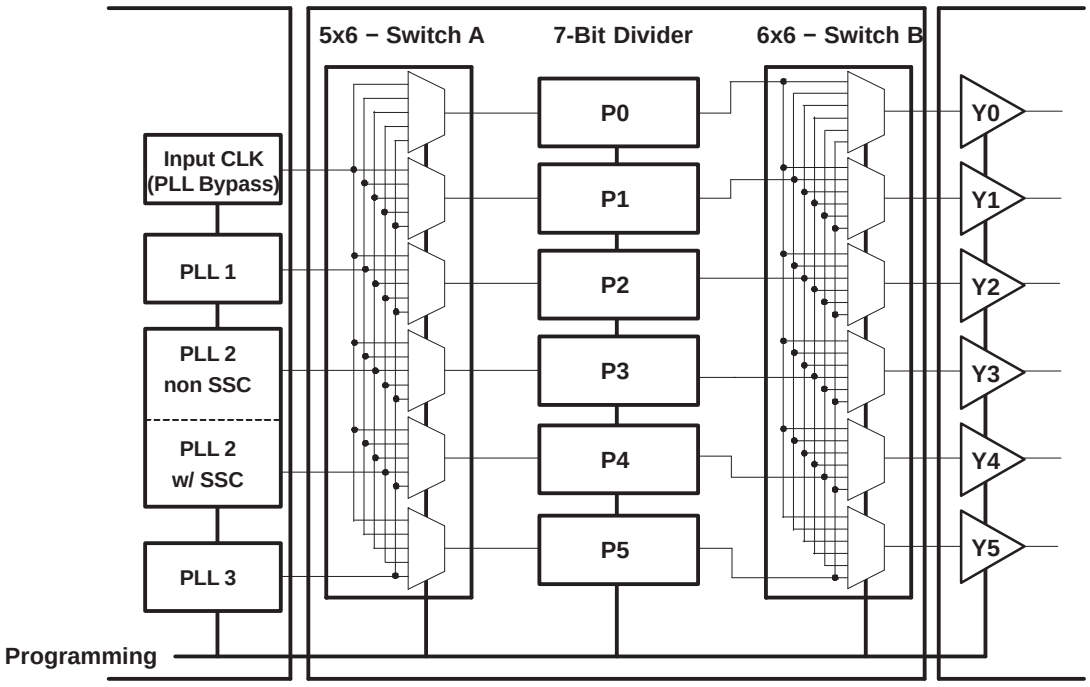
The CDC906 is characterized for operation from 0°C to 70°C.

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FUNCTIONAL BLOCK DIAGRAM



OUTPUT SWITCH MATRIX



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TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	TSSOP20 NO.		
Y0 to Y5	11, 12, 15, 16, 19, 20	O	LVCMOS outputs
CLK_IN0	5	I	Dependent on SMBus settings, CLK_IN0 is the crystal oscillator input and can also be used as LVCMOS input or as positive differential signal inputs.
CLK_IN1	6	I/O	Dependent on SMBus settings, CLK_IN1 is serving as the crystal oscillator output or can be the second LVCMOS input or the negative differential signal input.
V_{CC}	3, 7	Power	3.3-V power supply for the device.
V_{CCOUT1}	14	Power	Power supply for outputs Y0, Y1.
V_{CCOUT2}	18	Power	Power supply for outputs Y2, Y3, Y4, Y5.
GND	4, 8, 13, 17	Ground	Ground
S0, CLK_SEL	1	I	User programmable control input S0 (PLL bypass or power-down mode) or CLK_SEL (selects one of two LVCMOS clock inputs), dependent on the SMBus settings; LVCMOS inputs; internal pullup 150 kΩ.
S1	2	I	User programmable control input S1 (output enable/disable or all output low), dependent on the SMBus settings; LVCMOS inputs; internal pullup 150 kΩ
SDATA	9	I/O	Serial control data input/output for SMBus controller; LVCMOS input
SCLOCK	10	I	Serial control clock input for SMBus controller; LVCMOS input

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
V_{CC}	Supply voltage range	–0.5 to 4.6	V
V_I	Input voltage range(2)	–0.5 to V_{CC} + 0.5	V
V_O	Output voltage range(2)	–0.5 to V_{CC} + 0.5	V
I_I	Input current (V_I < 0, V_I > V_{CC})	±20	mA
I_O	Continuous output current	±50	mA
T_{stg}	Storage temperature range	–65 to 150	°C
T_J	Maximum junction temperature	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PACKAGE THERMAL RESISTANCE

for TSSOP20 (PW) Package(1) (2)

PARAMETER		AIRFLOW (LFM)	°C/W
θ_{JA}	Thermal resistance junction-to-ambient	0	66.3
		150	59.3
		250	56.3
		500	51.9
θ_{JC}	Thermal resistance junction-to-case		19.7

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Device supply voltage	3	3.3	3.6	V
V_{CCOUT1}	Output Y0, Y1 supply voltage	2.3		3.6	V
V_{CCOUT2}	Output Y2, Y3, Y4, Y5 supply voltage	2.3		3.6	V
V_{IL}	Low level input voltage LVCMOS			0.3 V_{CC}	V
V_{IH}	High level input voltage LVCMOS	0.7 V_{CC}			V
$V_{Ithresh}$	Input voltage threshold LVCMOS		0.5 V_{CC}		V
V_I	Input voltage range LVCMOS	0		3.6	V
$\|V_{ID}\|$	Differential input voltage	0.1			V
V_{IC}	Common-mode for differential input voltage	0.2		V_{CC} – 0.6	V
I_{OH} / I_{OL}	Output current (3.3 V)			±6	mA
I_{OH} / I_{OL}	Output current (2.5 V)			±4	mA
C_L	Output load LVCMOS			25	pF
T_A	Operating free-air temperature	0		70	°C

RECOMMENDED CRYSTAL SPECIFICATIONS

		MIN	NOM	MAX	UNIT
f_{Xtal}	Crystal input frequency range (fundamental mode)	8	27	54	MHz
ESR	Effective series resistance(1) (2)	15		60	Ω
C_{IN}	Input capacitance CLK_IN0 and CLK_IN1		3		pF

(1) For crystal frequencies above 50 MHz the effective series resistor should not exceed 50Ω to assure stable start-up condition.
(2) Maximum Power Handling (Drive Level) see Figure 16 .

TIMING REQUIREMENTS

over recommended ranges of supply voltage, load, and operating-free air temperature

			MIN	NOM	MAX	UNIT
CLK_IN REQUIREMENTS						
f_{CLK_IN}	CLK_IN clock input frequency (LVCMOS or Differential)	PLL mode	1		167	MHz
		PLL bypass mode	0		167	
t_r / t_f	Rise and fall time CLK_IN signal (20% to 80%)				4	ns
$duty_{REF}$	Duty cycle CLK_IN at V_{CC} / 2		40%		60%	
SMBus TIMING REQUIREMENTS (see Figure 11)						
f_{SCLK}	SCLK frequency				100	kHz
$t_{h(START)}$	START hold time		4			µs
$t_{w(SCLL)}$	SCLK low-pulse duration		4.7			µs
$t_{w(SCLH)}$	SCLK high-pulse duration		4		50	µs
$t_{su(START)}$	START setup time		0.6			µs
$t_{h(SDATA)}$	SDATA hold time		0.3			µs
$t_{su(SDATA)}$	SDATA setup time		0.25			µs
t_r	SCLK / SDATA input rise time				1000	ns
t_f	SCLK / SDATA input fall time				300	ns
$t_{su(STOP)}$	STOP setup time		4			µs
t_{BUS}	Bus free time		4.7			µs
t_{POR}	Time in which the device must be operational after power-on reset				500	ms

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DEVICE CHARACTERISTICS

over recommended operating free-air temperature range and test load (unless otherwise noted), see **Figure 1**

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
OVERALL PARAMETER							
I_{CC}	Supply current (2)	All PLLs on, all outputs on, f_{OUT} = 80 MHz, f_{CLK_IN} = 27 MHz, $f_{(VCO)}$ = 160 MHz			90	115	mA
I_{CCPD}	Power down current. Every circuit powered down except SMBus	f_{IN} = 0 MHz, V_{CC} = 3.6 V			50		µA
V_{PUC}	Supply voltage V_{CC} threshold for power up control circuit				2.1		V
$f_{(VCO)}$	VCO frequency of internal PLL (any of three PLLs)	Normal speed-mode (3)	All PLLs	80		200	MHz
			PLL2 with SSC	80		167	
		High-speed mode (3)		180		300	
f_{OUT}	LVCMOS output frequency range (4), See Figure 4	V_{CC} = 2.5 V				250	MHz
		V_{CC} = 3.3 V				300	
LVCMOS PARAMETER							
V_{IK}	LVCMOS input voltage	V_{CC} = 3 V, I_I = –18 mA				–1.2	V
I_I	LVCMOS input current (CLK_IN0 / CLK_IN1)	V_I = 0 V or V_{CC}, V_{CC} = 3.6 V				±5	µA
I_{IH}	LVCMOS input current (For S1/S0)	V_I = V_{CC}, V_{CC} = 3.6 V				5	µA
I_{IL}	LVCMOS input current (For S1/S0)	V_I = 0 V, V_{CC} = 3.6 V		-35		–10	µA
C_I	Input capacitance at CLK_IN0 and CLK_IN1	V_I = 0 V or V_{CC}			3		pF
LVCMOS PARAMETER FOR V_{CCOUT} = 3.3-V Mode							
V_{OH}	LVCMOS high-level output voltage	V_{CCOUT} = 3 V, I_{OH} = –0.1 mA		2.9			V
		V_{CCOUT} = 3 V, I_{OH} = –4 mA		2.4			
		V_{CCOUT} = 3 V, I_{OH} = –6 mA		2.1			
V_{OL}	LVCMOS low-level output voltage	V_{CCOUT} = 3 V, I_{OL} = 0.1 mA				0.1	V
		V_{CCOUT} = 3 V, I_{OL} = 4 mA				0.5	
		V_{CCOUT} = 3 V, I_{OL} = 6 mA				0.85	
t_{PLH}, t_{PHL}	Propagation delay	All PLL bypass			9		ns
		VCO bypass			11		
t_{r0}/t_{f0}	Rise and fall time for output slew rate 0	V_{CCOUT} = 3.3 V (20%–80%)		1.7	3.3	4.8	ns
t_{r1}/t_{f1}	Rise and fall time for output slew rate 1	V_{CCOUT} = 3.3 V (20%–80%)		1.5	2.5	3.2	ns
t_{r2}/t_{f2}	Rise and fall time for output slew rate 2	V_{CCOUT} = 3.3 V (20%–80%)		1.2	1.6	2.1	ns
t_{r3}/t_{f3}	Rise and fall time for output slew rate 3 (Default Configuration)	V_{CCOUT} = 3.3 V (20%–80%)		0.4	0.6	1	ns
$t_{jit(cc)}$	Cycle-to-cycle jitter (5) (6)	1 PLL, 1 Output	f_{OUT} = 24.576 MHz		65	95	ps
		3 PLLs, 3 Outputs	f_{OUT} = 24.576 MHz		85	135	
$t_{jit(per)}$	Peak-to-peak period jitter (5) (6)	1 PLL, 1 Output	f_{OUT} = 24.576 MHz		90	115	ps
		3 PLLs, 3 Outputs	f_{OUT} = 24.576 MHz		100	150	
$t_{sk(o)}$	Output skew (see (7) and Table 5)	1.6-ns rise/fall time at $f_{(VCO)}$ = 150 MHz, Pdiv = 3				200	ps

(1) All typical values are at respective nominal V_{CC}.
(2) For calculating total supply current, add the current from Figure 2 , Figure 3 , and Figure 4 . Using high-speed mode of the VCO reduces the current consumption significantly. See Figure 3
(3) Normal-speed mode or high-speed mode must be selected by the VCO frequency selection bit in Byte 6, Bit [7:5]. The min $f_{(VCO)}$ can be lower but impacts jitter-performance.
(4) The maximum output frequency may be exceeded, but specifications under the Recommended Operating Condition may change and are no longer assured. Do not exceed the maximum power dissipation of the 20-pin TSSOP package (600 mW at no air flow). See Figure 5 .
(5) 50000 cycles.
(6) Jitter depends on configuration. Jitter data is for normal t_r/t_f, input frequency = 27 MHz, $f_{(VCO)}$ = 147 MHz output.
(7) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

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DEVICE CHARACTERISTICS (continued)

over recommended operating free-air temperature range and test load (unless otherwise noted), see **Figure 1**

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
odc	Output duty cycle (8)	$f_{(VCO)}$ = 100 MHz, Pdiv = 1		45%		55%	
LVCMOS PARAMETER FOR V_{CCOUT} = 2.5-V Mode (9)							
V_{OH}	LVCMOS high-level output voltage	V_{CCOUT} = 2.3 V, I_{OH} = 0.1 mA		2.2			V
		V_{CCOUT} = 2.3 V, I_{OH} = –3 mA		1.7			
		V_{CCOUT} = 2.3 V, I_{OH} = –4 mA		1.5			
V_{OL}	LVCMOS low-level output voltage	V_{CCOUT} = 2.3 V, I_{OL} = 0.1 mA				0.1	V
		V_{CCOUT} = 2.3 V, I_{OL} = 3 mA				0.5	
		V_{CCOUT} = 2.3 V, I_{OL} = 4 mA				0.85	
t_{PLH}, t_{PHL}	Propagation delay	All PLL bypass			9		ns
		VCO bypass			11		
t_{r0}/t_{f0}	Rise and fall time for output slew rate 0	V_{CCOUT} = 2.5 V (20%–80%)		2	3.9	5.6	ns
t_{r1}/t_{f1}	Rise and fall time for output slew rate 1	V_{CCOUT} = 2.5 V (20%–80%)		1.8	2.9	4.4	ns
t_{r2}/t_{f2}	Rise and fall time for output slew rate 2	V_{CCOUT} = 2.5 V (20%–80%)		1.3	2	3.2	ns
t_{r3}/t_{f3}	Rise and fall time for output slew rate 3 (Default Configuration)	V_{CCOUT} = 2.5 V (20%–80%)		0.4	0.8	1.1	ns
$t_{jit(cc)}$	Cycle-to-cycle jitter (10) (11)	1 PLL, 1 Output	f_{OUT} = 24.576 MHz		85	120	ps
		3 PLLs, 3 Outputs	f_{OUT} = 24.576 MHz		95	155	
$t_{jit(per)}$	Peak-to-peak period jitter (10) (11)	1 PLL, 1 Output	f_{OUT} = 24.576 MHz		110	135	ps
		3 PLLs, 3 Outputs	f_{OUT} = 24.576 MHz		110	175	
$t_{sk(o)}$	Output skew (see (12) and Table 5)	2-ns rise/fall time at $f_{(VCO)}$ = 150 MHz, Pdiv = 3				250	ps
odc	Output duty cycle (13)	$f_{(VCO)}$ = 100 MHz, Pdiv = 1		45%		55%	
SMBus PARAMETER							
V_{IK}	SCLK and SDATA input clamp voltage	V_{CC} = 3 V, I_I = –18 mA				–1.2	V
I_I	SCLK and SDATA input current	V_I = 0 V or V_{CC}, V_{CC} = 3.6 V				±5	µA
V_{IH}	SCLK input high voltage			2.1			V
V_{IL}	SCLK input low voltage					0.8	V
V_{OL}	SDATA low-level output voltage	I_{OL} = 4 mA, V_{CC} = 3 V				0.4	V
C_I	Input capacitance at SCLK	V_I = 0 V or V_{CC}			3	10	pF
	Input capacitance at SDATA	V_I = 0 V or V_{CC}			3	10	pF

(8) odc depends on output rise and fall time (t_r/t_f); above limits are for normal t_r/t_f.
(9) There is a limited drive capability at output supply voltage of 2.5 V. For proper termination, see application report SCAA080.
(10) 50000 cycles.
(11) Jitter depends on configuration. Jitter data is for normal t_r/t_f, input frequency = 27 MHz, $f_{(VCO)}$ = 147 MHz output.
(12) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.
(13) odc depends on output rise and fall time (t_r/t_f); above limits are for normal t_r/t_f.

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PARAMETER MEASUREMENT INFORMATION

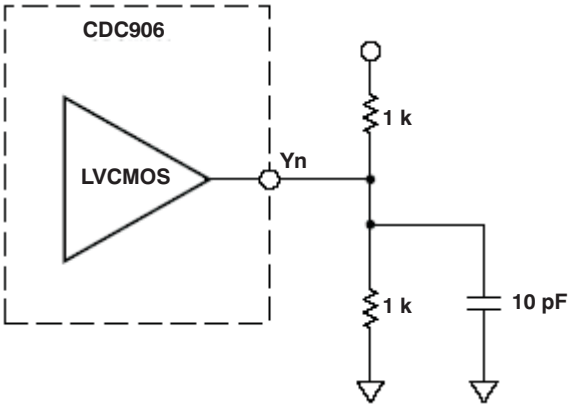


Figure 1. Test Load

TYPICAL CHARACTERISTICS

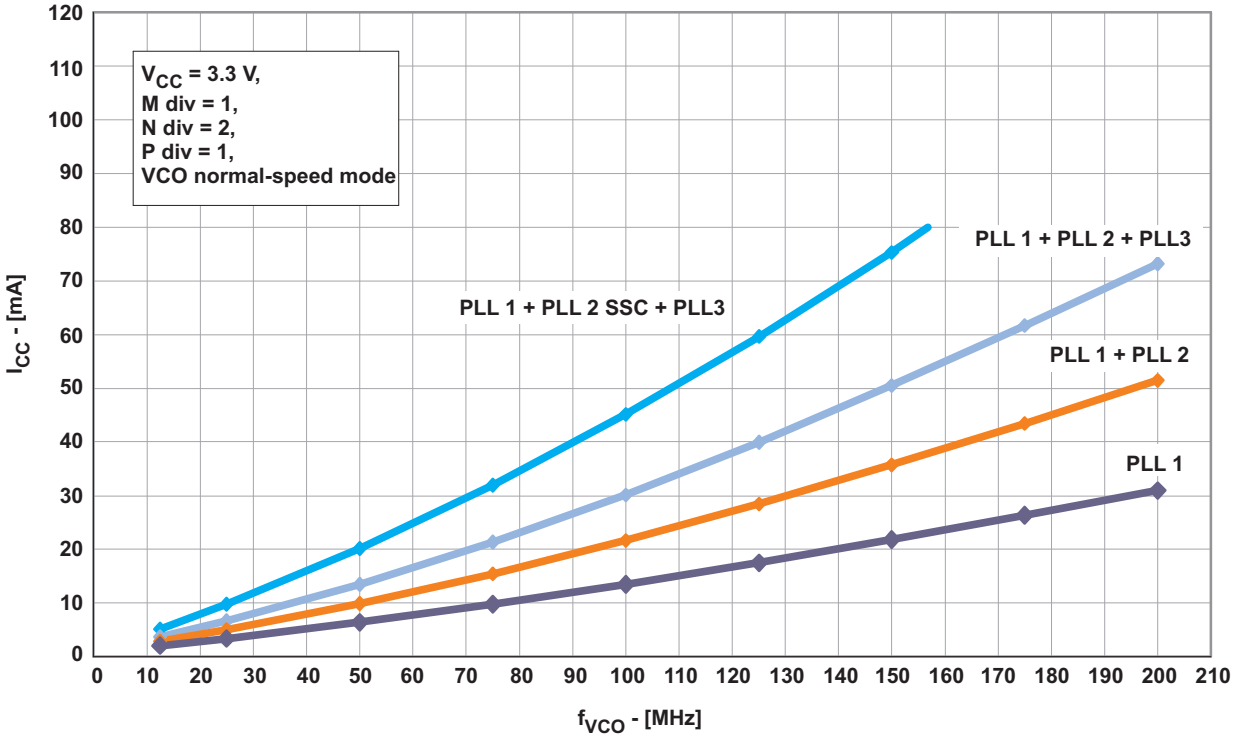


Figure 2. I_{CC} vs Number of PLLs and VCO Frequency (VCO at Normal-Speed Mode, Byte 6 Bit [7:5])

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TYPICAL CHARACTERISTICS (continued)

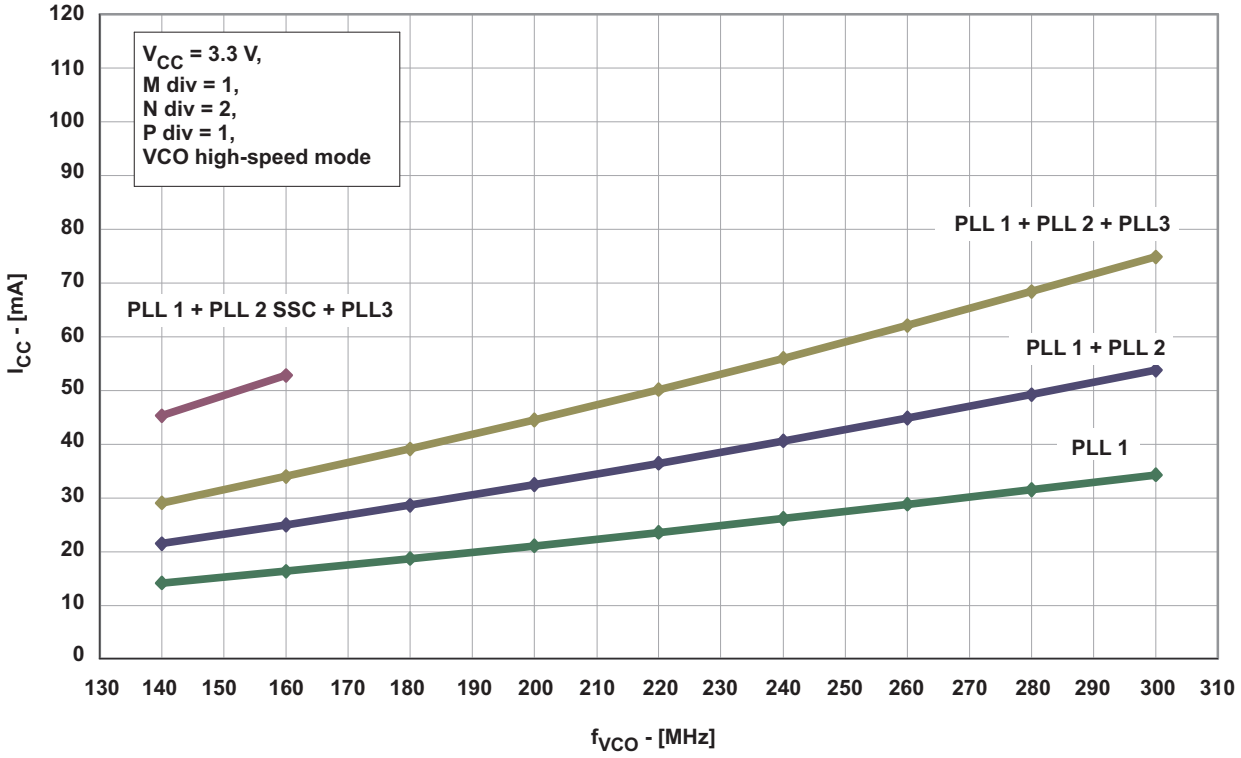


Figure 3. I_{CC} vs Number of PLLs and VCO Frequency (VCO at High-Speed Mode, Byte 6 Bit [7:5])

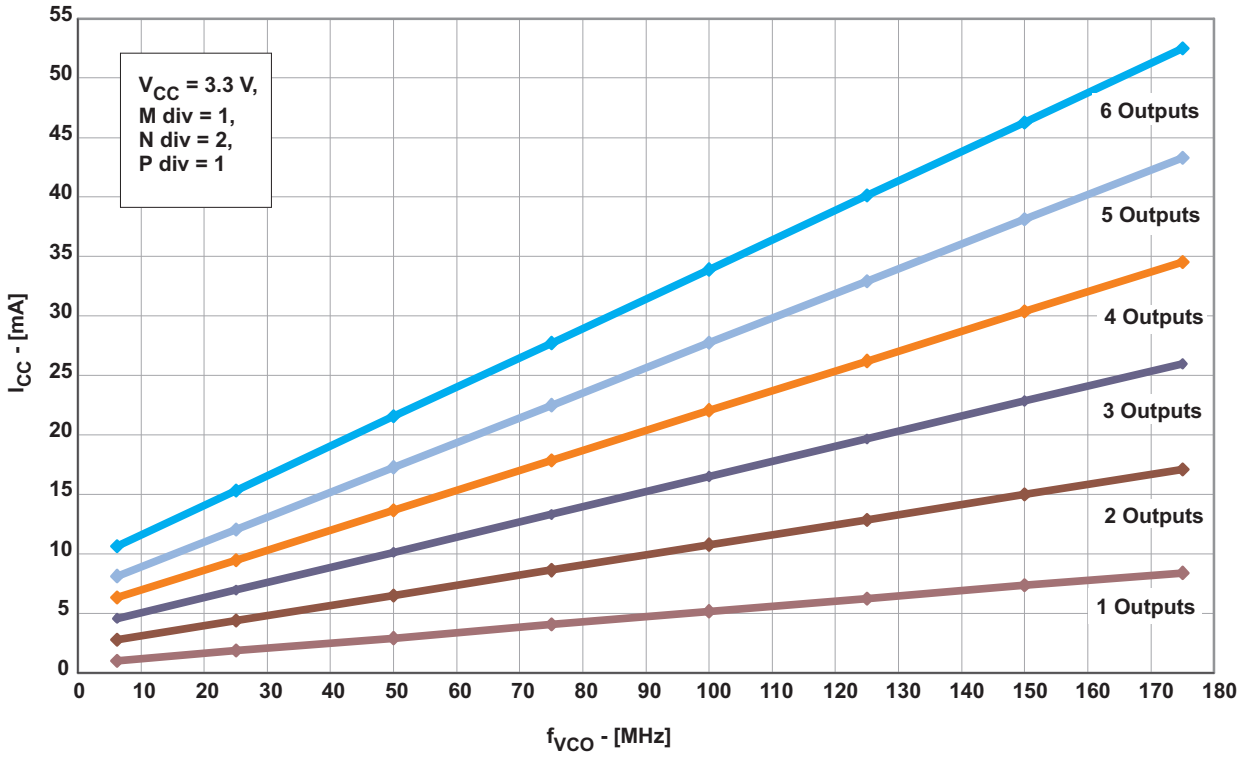


Figure 4. I_{CCOUT} vs Number of Outputs and VCO Frequency

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TYPICAL CHARACTERISTICS (continued)

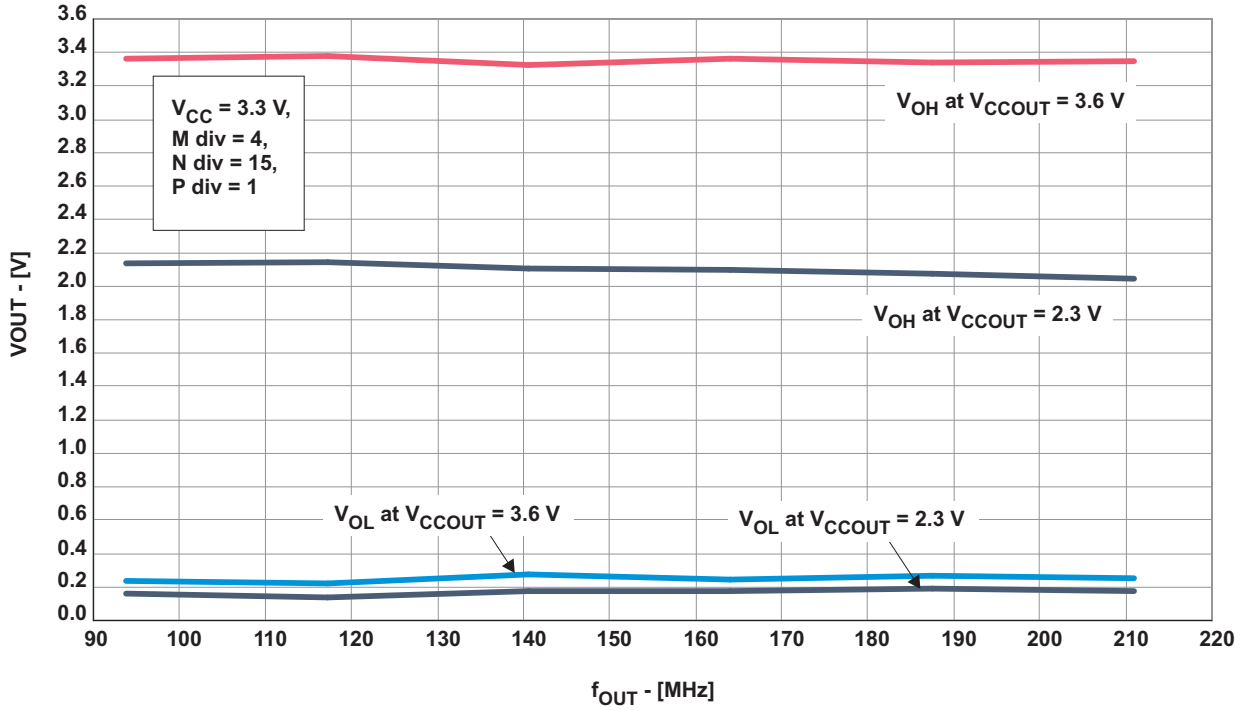


Figure 5. Output Swing vs Output Frequency

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APPLICATION INFORMATION

SMBus Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. It follows the SMBus specification Version 2.0, which is based upon the principals of operation of I^2C. More details of the SMBus specification can be found at http://http://www.smbus.org.

Through the SMBus, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the SMBus data interface initialize to their default setting upon power-up; therefore, using this interface is optional. The clock device register changes are normally made upon system initialization, if any are required.

Data Protocol

The clock driver serial protocol accepts Byte Write, Byte Read, Block Write, and Block Read operations from the controller.

For Block Write/Read operations, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For Byte Write and Byte Read operations, the system controller can access individually addressed bytes.

Once a byte has been sent, it is written into the internal register and effective immediately. With the rising edge of the ACK bit, this applies to each transferred byte, independent of whether this is a Byte Write or a Block Write sequence.

The offset of the indexed byte is encoded in the command code, as described in Table 1.

The Block Write and Block Read protocol is outlined in Figure 9 and Figure 10, while Figure 7 and Figure 8 outlines the corresponding Byte Write and Byte Read protocol.

Slave Receiver Address (7 bits)

A6	A5	A4	A3	A2	A1	A0	$\overline{R}$/W
1	1	0	1	0	0	1	0

Table 1. Command Code Definition

Bit	Description
7	0 = Block Read or Block Write operation 1 = Byte Read or Byte Write operation
(6:0)	Byte Offset for Byte Read and Byte Write operation.

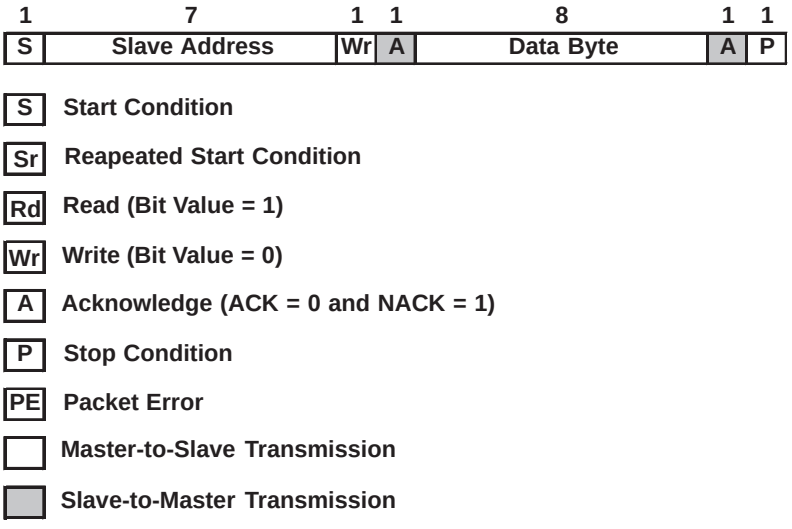


Figure 6. Generic Programming Sequence

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Byte Write Programming Sequence

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	CommandCode	A	Data Byte	A	P

Figure 7. Byte Write Protocol

Byte Read Programming Sequence

1	7	1	1	8	1	1	7	1	1
S	Slave Address	Wr	A	CommandCode	A	S	Slave Address	Rd	A

8	1	1
Data Byte	A	P

Figure 8. Byte Read Protocol

Block Write Programming Sequence(1)

1	7	1	1	8	1	8	1
S	Slave Address	Wr	A	CommandCode	A	Byte Count N	A

8	1	8	1		8	1	1
Data Byte 0	A	Data Byte 1	A	- - - - -	Data Byte N–1	A	P

(1) Data Byte 0 is reserved for revision code and vendor identification. However, this byte is used for internal test. Do not write into it other than 0000 0000.

Figure 9. Block Write Protocol

Block Read Programming Sequence

1	7	1	1	8	1	1	7	1	1
S	Slave Address	Wr	A	CommandCode	A	Sr	Slave Address	Rd	A

8	1	8	1		8	1	1
Byte Count N	A	Data Byte 0	A	- - - - -	Data Byte N–1	A	P

Figure 10. Block Read Protocol

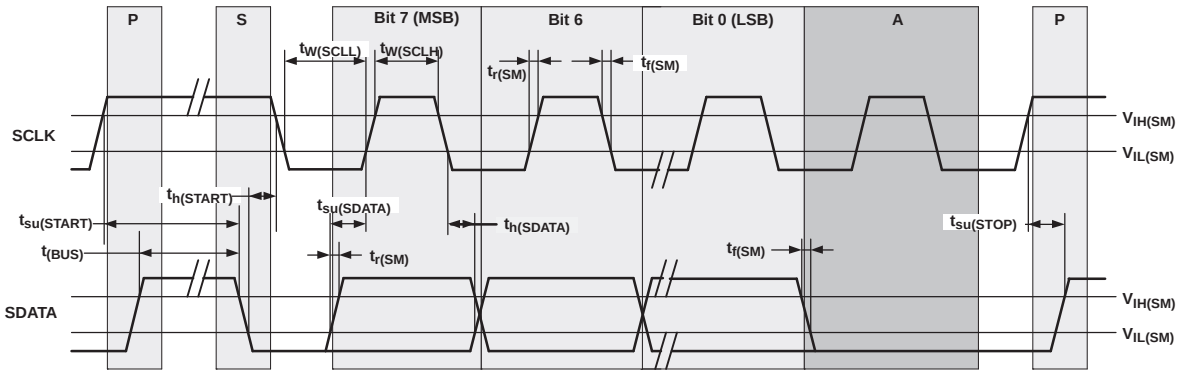


Figure 11. Timing Diagram Serial Control Interface

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SMBus Hardware Interface

The following diagram shows how the CDC906 clock synthesizer is connected to the SMBus. Note that the current through the pullup resistors (R_p) must meet the SMBus specifications (min 100 µA, max 350 µA). If the CDC906 is not connected to the SMBus, then SDATA and SCLK inputs have to be connected with 10-kΩ pullup resistors to V_{CC} to avoid floating input conditions.

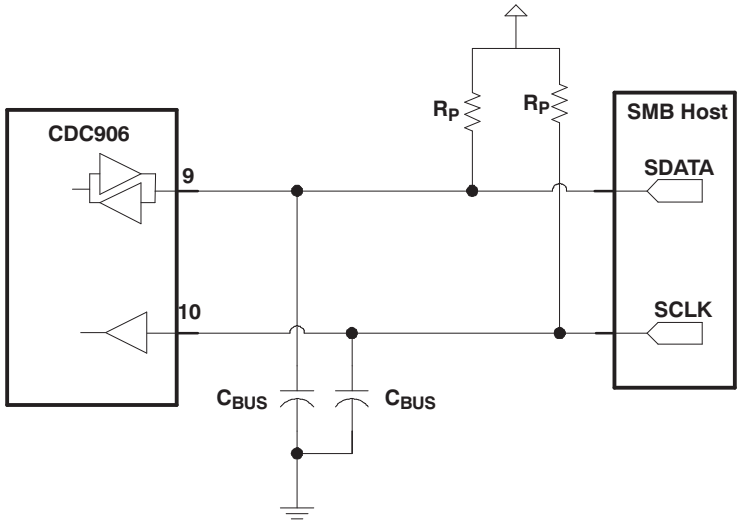


Figure 12. SMBus Hardware Interface

Table 2. Register Configuration Command Bitmap

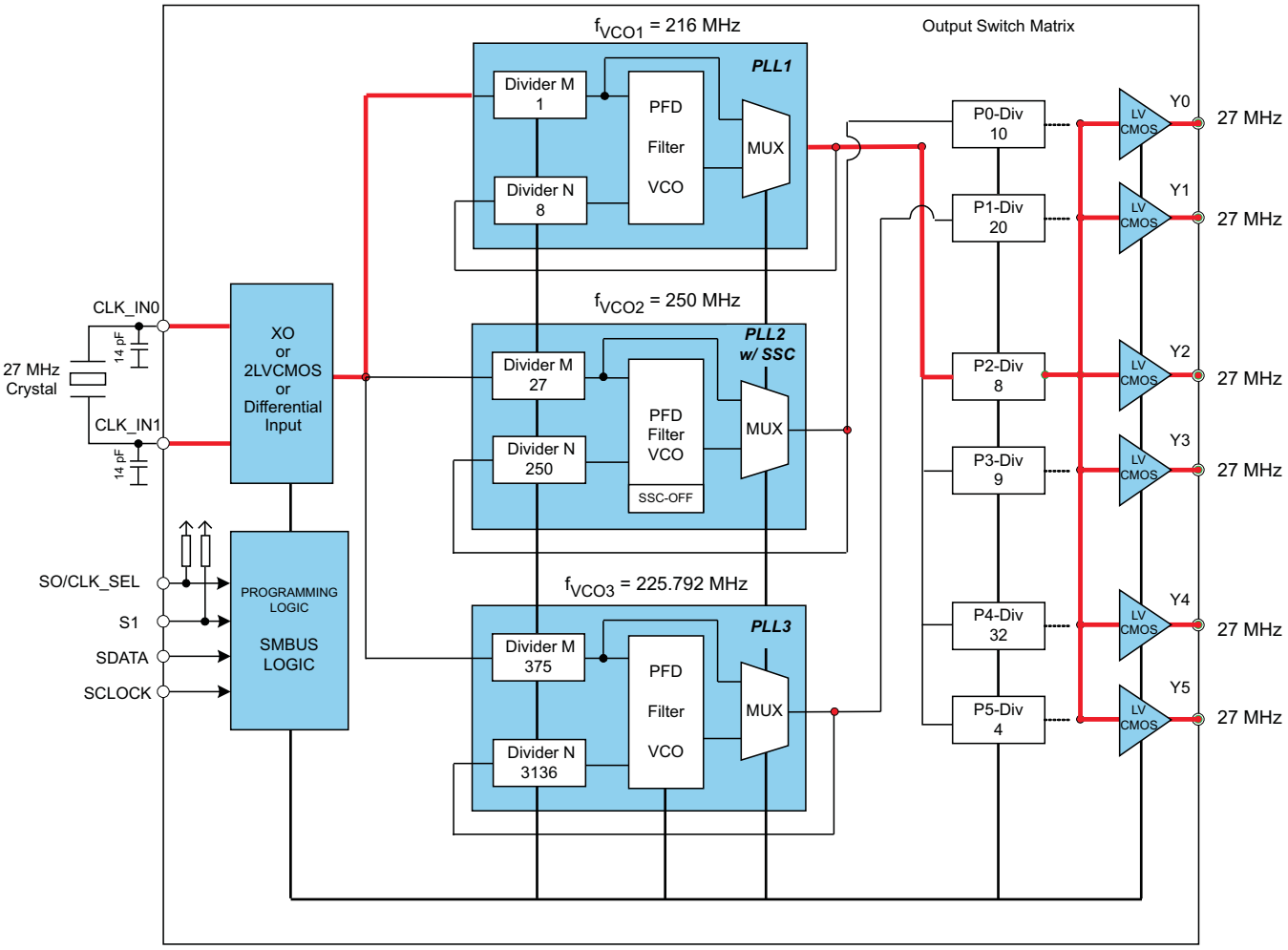
Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0	Revision Code				Vendor Identification			
Byte 1	PLL1 Reference Divider M 9-Bit [7:0]							
Byte 2	PLL1 Feedback Divider N 12-Bit [7:0]							
Byte 3	PLL1 Mux	PLL2 Mux	PLL3 Mux	PLL1 Feedback Divider N 12-Bit [11:8]				PLL1 Ref Dev M [8]
Byte 4	PLL2 Reference Divider M 9-Bit [7:0]							
Byte 5	PLL2 Feedback Divider N 12-Bit [7:0]							
Byte 6	PLL1 fvco Selection	PLL2 fvco Selection	PLL3 fvco Selection	PLL2 Feedback Divider N 12-Bit [11:8]				PLL2 Ref Dev M [8]
Byte 7	PLL3 Reference Divider 9-Bit M [7:0]							
Byte 8	PLL3 Feedback Divider N [12-Bit 7:0]							
Byte 9	PLL Selection for P0 (Switch A)			PLL3 Feedback Divider N 12-Bit [11:8]				PLL3 Ref Dev M [8]
Byte 10	PLL Selection for P1 (Switch A)			Inp. Clock Selection	Configuration Inputs S1		Configuration Inputs S0	
Byte 11	Input Signal Source		PLL Selection for P3 (Switch A)			PLL Selection for P2 (Switch A)		
Byte 12	Reserved	Power Down	PLL Selection for P5 (Switch A)			PLL Selection for P4 (Switch A)		
Byte 13	Reserved	7-Bit Divider P0 [6:0]						
Byte 14	Reserved	7-Bit Divider P1 [6:0]						
Byte 15	Reserved	7-Bit Divider P2 [6:0]						
Byte 16	Reserved	7-Bit Divider P3 [6:0]						
Byte 17	Reserved	7-Bit Divider P4 [6:0]						
Byte 18	Reserved	7-Bit Divider P5 [6:0]						
Byte 19	Reserved	Y0 Inv. or Non-Inv	Y0 Slew-Rate Control		Y0 Enable or Low	Y0 Divider Selection (Switch B)		
Byte 20	Reserved	Y1 Inv. or Non-Inv	Y1 Slew-Rate Control		Y1 Enable or Low	Y1 Divider Selection (Switch B)		
Byte 21	Reserved	Y2 Inv. or Non-Inv	Y2 Slew-Rate Control		Y2 Enable or Low	Y2 Divider Selection (Switch B)		
Byte 22	Reserved	Y3 Inv. or Non-Inv	Y3 Slew-Rate Control		Y3 Enable or Low	Y3 Divider Selection (Switch B)		
Byte 23	Reserved	Y4 Inv. or Non-Inv	Y4 Slew-Rate Control		Y4 Enable or Low	Y4 Divider Selection (Switch B)		
Byte 24	Reserved	Y5 Inv or Non-Inv	Y5 Slew-Rate Control		Y5 Enable or Low	Y5 Divider Selection (Switch B)		
Byte 25	Reserved	Spread Spectrum (SSC) Modulation Selection			Frequency Selection for SSC			
Byte 26	Reserved	7-Bit Byte Count						

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Default Device Setting

The CDC906 is pre-programmed with a factory default configuration as shown below. This puts the device in an operating mode without the need to program it first. The default setting appears after power is switched on or after a power-down/up sequence until it is re-programmed by the user to a different application configuration. A new register setting is programmed via the serial SMBUS Interface.

A different default setting can be programmed upon customer request. Contact a Texas Instruments sales or marketing representative for more information.



NOTE: All outputs are enabled and in non-inverting mode. S0, S1, and SSC comply according the default setting described in Byte 10 and Byte 25 respectively.

Figure 13. Default Device Setting

The output frequency can be calculated:

$$\text{fout} = \frac{\text{fin} \times N}{M \times P}, \text{ i.e. fout} = \frac{27\ \text{MHz} \times 8}{(1 \times 8)} = 27\ \text{MHz} \quad (1)$$

Functional Description of the Logic

All Bytes are read-/write-able, unless otherwise expressly mentioned.

Byte 0 (read only): Vendor Identification Bits [3:0]; Revision Code Bit [7:4]								
Revision Code (1)				Vendor Identification				
X	X	X	X	0	0	0	1	

(1) Byte 0 is readable by "Byte Read sequency" only.

Byte 1 to 9: Reference Divider M of PLL1, PLL2, PLL3 (1)										
M8	M7	M6	M5	M4	M3	M2	M1	M0	Div by	Default (2) (3)
0	0	0	0	0	0	0	0	0	Not allowed	
0	0	0	0	0	0	0	0	1	1	
0	0	0	0	0	0	0	1	0	2	
0	0	0	0	0	0	0	1	1	3	
				• • •						
1	1	1	1	1	1	1	0	1	509	
1	1	1	1	1	1	1	1	0	510	
1	1	1	1	1	1	1	1	1	511	

(1) By selecting the PLL divider factors, M ≤ N and 80 MHz ≤ fvco ≤ 300 MHz.
(2) Unless customer specific setting.
(3) Default setting of divider M for PLL1 = 1, for PLL2 = 27 and for PLL3 = 375.

Byte 1 to 9: Feedback Divider N of PLL1, PLL2, PLL3 (1)													
N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	Div by	Default (2) (3)
0	0	0	0	0	0	0	0	0	0	0	0	Not allowed	
0	0	0	0	0	0	0	0	0	0	0	1	1	
0	0	0	0	0	0	0	0	0	0	1	0	2	
0	0	0	0	0	0	0	0	0	0	1	1	3	
							• • •						
1	1	1	1	1	1	1	1	1	1	0	1	4093	
1	1	1	1	1	1	1	1	1	1	1	0	4094	
1	1	1	1	1	1	1	1	1	1	1	1	4095	

(1) By selecting the PLL divider factors, M ≤ N and 80 MHz ≤ fvco ≤ 300 MHz.
(2) Unless customer specific setting.
(3) Default setting of divider N for PLL1 = 8, for PLL2 = 250 and for PLL3 = 3136.

Byte 3 Bit [7:5]: PLL (VCO) Bypass Multiplexer		
PLLxMUX	PLL (VCO) MUX Output	Default (1)
0	PLLx	Yes
1	VCO bypass	

(1) Unless customer specific setting.

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Byte 6 Bit [7:5]: VCO Frequency Selection Mode for each PLL (1)		
PLLxFVCO	**VCO Frequency Range**	**Default (2)**
0	80-200 MHz	
1	180-300 MHz	Yes

(1) This bit selects the normal-speed mode or the high-speed mode for the dedicated VCO in PLL1, PLL2 or PLL3. At power-up, the high-speed mode is selected, f_{VCO} is 180-300 MHz. In case of higher f_{VCO}, this bit has to be set to [1].
(2) Unless customer specific setting.

Byte 9 to 12: Outputs Switch Matrix (5x6 Switch A) PLL Selection for P-Divider P0-P5				
SWAPx2	**SWAPx1**	**SWAPx0**	**Any Output Px**	**Default (1)**
0	0	0	PLL bypass (input clock)	
0	0	1	PLL1	P2, P3, P4, P5
0	1	0	PLL2 non-SSC	P0
0	1	1	PLL2 w/ SSC (2)	
1	0	0	PLL3	P1
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

(1) Unless customer specific setting.
(2) PLL2 has a SSC output and non-SSC output. If SSC bypass is selected (see Byte 25, Bit [6:4]), the SSC circuitry of PLL2 is powered-down and the SSC output is reset to logic low. The non-SSC output of PLL2 is not affected by this mode and can still be used.

Byte 10, Bit [1:0]: Configuration Settings of Input S0/CLK_SEL			
S01	**S00**	**Function**	**Default (1)**
0	0	If S0 is low, the PLLs and the clock-input stage are going into power-down mode, outputs are in 3-state, all actual register settings will be maintained, SMBus stays active (2)	Yes
0	1	If S0 is low, the PLL and all dividers (M-Div and P-Div) are bypassed and PLL is in power-down, all outputs are active (inv. or non-inv.), actual register settings will be maintained, SMBus stays active; this mode is useful for production test;	
1	0	CLK_SEL (input clock selection — overwrites the CLK_SEL setting in Byte 10, Bit [4]) (3) — CLK_SEL is set low selects CLK_IN_IN0 — CLK_SEL is set high selects CLK_IN_IN1	
1	1	Reserved	

(1) Unless customer specific setting.
(2) Power-down mode overwrites 3-state or low-state of S1 setting in Byte 10, Bit [3:2].
(3) If the clock input (CLK_IN0/CLK_IN1) is selected as crystal input or differential clock input (Byte 11, Bit [7:6]) then this setting is not relevant.

Byte 10, Bit [3:2]: Configuration Settings of Input S1			
S11	**S10**	**Function**	**Default (1)**
0	0	If S1 is set low, all outputs are switched to a low-state (non-inv.) or high-state (inv.);	Yes
0	1	If S1 is set low, all outputs are switched to a 3-state	
1	0	Reserved	
1	1	Reserved	

(1) Unless customer specific setting.

Byte 10, Bit [4]: Input Clock Selection (1)		
CLKSEL	**Input Clock**	**Default (2)**
0	CLK_IN0	Yes
1	CLK_IN1	

(1) This bit is not relevant, if crystal input or differential clock input is selected, Byte 11, Bit [7:6].
(2) Unless customer specific setting.

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Byte 11, Bit [7:6]: Input Signal Source (1)			
IS1	IS0	Function	Default (2)
0	0	CLK_IN0 is Crystal Oscillator Input and CLK_IN1 is serving as Crystal Oscillator Output.	Yes
0	1	CLK_IN0 and CLK_IN1 are two LVCMOS Inputs. CLK_IN0 or CLK_IN1 are selectable via CLK_SEL control pin.	
1	0	CLK_IN0 and CLK_IN1 serve as differential signal inputs.	
1	1	Reserved	

(1) In case the crystal input or differential clock input is selected, the input clock selection, Byte 10, Bit [4], is not relevant.
(2) Unless customer specific setting.

Byte 12, Bit [6]: Power-Down Mode (except SMBus)		
PD	Power-Down Mode	Default (1)
0	Normal Device Operation	Yes
1	Power Down (2)	

(1) Unless customer specific setting.
(2) In power down, all PLLs and the Clock-Input-Stage are going into power-down mode, all outputs are in 3-State, all actual register settings will be maintained and SMBus stays active. Power-Down Mode overwrites 3-State or Low-State of S0 and S1 setting in Byte 10.

Byte 13 to 18, Bit [6:0]: Outputs Switch Matrix - 6x7-Bit Divider P0-P5								
DIVYx6	DIVYx5	DIVYx4	DIVYx3	DIVYx2	DIVYx1	DIVYx0	Div by	Default (1) (2)
0	0	0	0	0	0	0	Not allowed	
0	0	0	0	0	0	1	1	
0	0	0	0	0	1	0	2	
		• • •						
1	1	1	1	1	0	1	125	
1	1	1	1	1	1	0	126	
1	1	1	1	1	1	1	127	

(1) Unless customer specific setting.
(2) Default setting of divider P0 = 10, P1 = 20, P2 = 8, P3 = 9, P4 = 32, and P5 = 4

Byte 19 to 24, Bit [5:4]: LVCMOS Output Rise/Fall Time Setting at Y0-Y5			
SRCYx1	SRCYx0	Yx	Default (1)
0	0	Nominal +3 ns (t_{r0}/t_{f0})	
0	1	Nominal +2 ns (t_{r1}/t_{f1})	
1	0	Nominal +1 ns (t_{r2}/t_{f2})	
1	1	Nominal (t_{r3}/t_{f3})	Yes

(1) Unless customer specific setting.

Byte 19 to 24, Bit [2:0]: Outputs Switch Matrix (6 x 6 Switch B) Divider (P0-P5) Selection for Outputs Y0-Y5				
SWBYx2	SWBYx1	SWBYx0	Any Output Yx	Default (1)
0	0	0	Divider P0	
0	0	1	Divider P1	
0	1	0	Divider P2	Y0, Y1, Y2, Y3, Y4, Y5
0	1	1	Divider P3	
1	0	0	Divider P4	
1	0	1	Divider P5	
1	1	0	Reserved	
1	1	1	Reserved	

(1) Unless customer specific setting.

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Byte 19 to 24, Bit [3]: Output Y0-Y5 Enable or Low-State		
ENDISYx	**Output Yx**	**Default (1)**
0	Disable to low	
1	Enable	Yes

(1) Unless customer specific setting.

Byte 19 to 24, Bit [6]: Output Y0-Y5 Non-Inverting/Inverting		
INVYx	**Output Yx Status**	**Default (1)**
0	Non-inverting	Yes
1	Inverting	

(1) Unless customer specific setting.

Byte 25, Bit [3:0]: SSC Modulation Frequency Selection in the Range of 30 kHz 60 kHz (1)														
FSSC3	**FSSC2**	**FSSC1**	**FSSC0**	**Modulation Factor**		f_{vco} [MHz]								**Default (2)**
						100	**110**	**120**	**130**	**140**	**150**	**160**	**167**	
0	0	0	0	5680	f_{mod} [kHz]	17.6	19.4	21.1	22.9	24.6	26.4	28.2	29.4	
0	0	0	1	5412		18.5	20.3	22.2	24.0	25.9	27.7	29.6	30.9	
0	0	1	0	5144		19.4	21.4	23.3	25.3	27.2	29.2	31.1	32.5	
0	0	1	1	4876		20.5	22.6	24.6	26.7	28.7	30.8	32.8	34.2	
0	1	0	0	4608		21.7	23.9	26.0	28.2	30.4	32.6	34.7	36.2	
0	1	0	1	4340		23.0	25.3	27.6	30.0	32.3	34.6	36.9	38.5	
0	1	1	0	4072		24.6	27.0	29.5	31.9	34.4	36.8	39.3	41.0	
0	1	1	1	3804		26.3	28.9	31.5	34.2	36.8	39.4	42.1	43.9	
1	0	0	0	3536		28.3	31.1	33.9	36.8	39.6	42.4	45.2	47.2	
1	0	0	1	3286		30.4	33.5	36.5	39.6	42.6	45.6	48.7	50.8	Yes
1	0	1	0	3000		33.3	36.7	40.0	43.3	46.7	50.0	53.3	55.7	
1	0	1	1	2732		36.6	40.3	43.9	47.6	51.2	54.9	58.6	61.1	
1	1	0	0	2464		40.6	44.6	48.7	52.8	56.8	60.9	64.9	67.8	
1	1	0	1	2196		45.5	50.1	54.6	59.2	63.8	68.3	72.9	76.0	
1	1	1	0	1928		51.9	57.1	62.2	67.4	72.6	77.8	83.0	86.6	
1	1	1	1	1660		60.2	66.3	72.3	78.3	84.3	90.4	96.4	100.6	

(1) The PLL has to be bypassed (turned off) when changing *SSC Modulation Frequency Factor* on-the-fly. This can be done by following programming sequence: bypass PLL2 (Byte 3, Bit 6 = 1); write new *Modulation Factor* (Byte 25); re-activate PLL2 (Byte 3, Bit 6 = 0).
(2) Unless customer specific setting.

Byte 25, Bit [6:4]: SSC Modulation Amount (1)				
SSC2	**SSC1**	**SSC0**	**Function**	**Default (2)**
0	0	0	SSC Modulation Amount 0% = SSC bypass for PLL (3)	Yes
0	0	1	SSC Modulation Amount ±0.1% (center spread)	
0	1	0	SSC Modulation Amount ±0.25% (center spread)	
0	1	1	SSC Modulation Amount ±0.4% (center spread)	
1	0	0	SSC Modulation Amount 1% (down spread)	
1	0	1	SSC Modulation Amount 1.5% (down spread)	
1	1	0	SSC Modulation Amount 2% (down spread)	
1	1	1	SSC Modulation Amount 3% (down spread)	

(1) The PLL has to be bypassed (turned off) when changing *SSC Modulation Amount* on-the-fly. This can be done by following programming sequence: bypass PLL2 (Byte 3, Bit 6 = 1); write new *Modulation Amount* (Byte 25); re-activate PLL2 (Byte 3, Bit 6 = 0).
(2) Unless customer specific setting.
(3) If SSC bypass is selected, SSC circuitry of PLL2 is powered-down and the SSC output is reset to logic low. The non-SSC output of PLL2 is not affected by this mode and can still be used.

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Byte 26, Bit [6:0]: Byte Count (1)								
BC6	**BC5**	**BC4**	**BC3**	**BC2**	**BC1**	**BC0**	**No. of Bytes**	**Default (2)**
0	0	0	0	0	0	0	Not allowed	
0	0	0	0	0	0	1	1	
0	0	0	0	0	1	0	2	
0	0	0	0	0	1	1	3	
			• • •					
0	0	1	1	0	1	1	27	Yes
			• • •					
1	1	1	1	1	0	1	125	
1	1	1	1	1	1	0	126	
1	1	1	1	1	1	1	127	

(1) Defines the number of Bytes, which will be sent from this device at the next Block Read protocol.
(2) Unless customer specific setting.

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FUNCTIONAL DESCRIPTION

Zero ppm Audio and Video System Clock Generation and Divider Setting

The CDC906 is ideally suited for audio and video applications. It consists of a triple PLL clock generator which generates up to six audio, video and system clocks from i.e. a 27-MHz master clock. The output frequencies are programmable to meet different application requirements. The master clock can be either a crystal oscillator or an external input clock signal. The CDC906 provides a very low jitter, high accuracy clock with zero ppm for the common audio and video clocks. The following table shows the system clocks versus the standard sampling frequency and the corresponding divider settings.

Audio Rate [kHz]	fs x 256 [MHz]	Divider			Error ppm	fs x 384 [MHz]	Divider			Error ppm
		M	N	P			M	N	P	
16	4.096	375	2048	36	0	6.144	125	768	27	0
22.05	5.6448	75	392	25	0	8.4672	125	588	15	0
24	6.144	125	768	27	0	9.216	125	768	18	0
32	8.192	375	2048	18	0	12.288	375	2048	12	0
44.1	11.2896	375	1568	10	0	16.9344	125	784	10	0
48	12.288	375	2048	12	0	18.432	125	768	9	0
96	24.576	375	2048	6	0	36.864	375	2048	4	0

Audio Rate [kHz]	fs x 512 [MHz]	Divider			Error ppm	fs x 768 [MHz]	Divider			Error ppm
		M	N	P			M	N	P	
16	8.192	375	2048	18	0	12.288	375	2048	12	0
22.05	11.2896	375	1568	10	0	16.9344	125	784	10	0
24	12.288	375	2048	12	0	18.432	125	768	9	0
32	16.384	375	2048	9	0	24.576	375	2048	6	0
44.1	22.5792	375	1568	5	0	33.8688	125	784	5	0
48	24.576	375	2048	6	0	36.864	375	2048	4	0
96	49.152	375	2048	3	0	73.728	375	2048	2	0

NOTE: Input frequency is 27 MHz.

Video Rate [MHz]	2 [MHz]	Divider			Error ppm	1 [MHz]	Divider			Error ppm	0.5 [MHz]	Divider			Error ppm
		M	N	P			M	N	P			M	N	P	
27	54	1	8	4	0	27	-	-	1	0	13.5	-	-	2	0

Typical applications for the CDC906 are digital HDTV systems, gaming consoles, DVD players, DVD add-on cards for multimedia PCs, and step-top boxes.

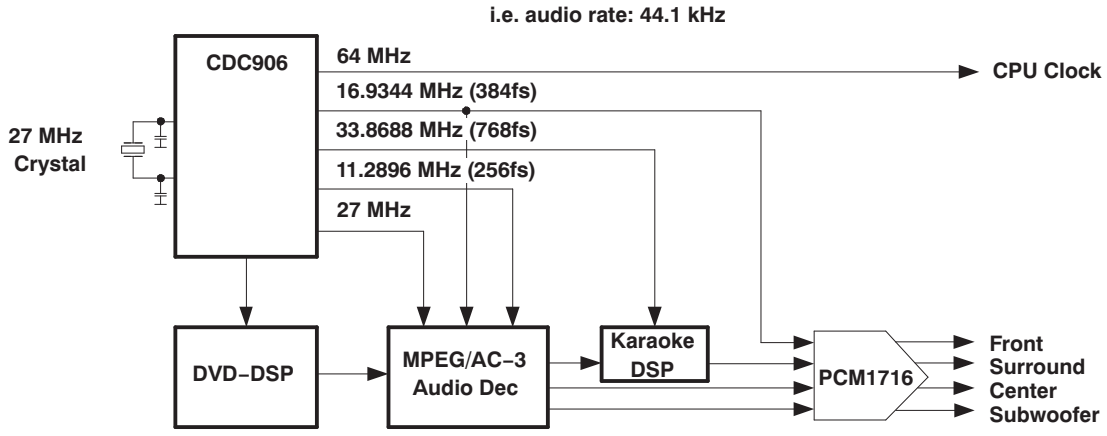


Figure 14. CDC906 System Application Block Diagram

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Clock Inputs (CLK_IN0 and CLK_IN1)

The CDC906 features two clock inputs which can be used as:

- Crystal oscillator input (default setting)
- Two independent single-ended LVCMOS inputs
- Differential signal input

The dedicated clock input can be selected by the *input signal source* Bit [7:6] of Byte 11.

Crystal Oscillator Inputs

The input frequency range in crystal mode is 8 MHz to 54 MHz. The CDC906 uses a Pierce-type oscillator circuitry with included feedback resistance for the inverting amplifier. The user, however, has to add external capacitors C_{X0}, C_{X1}) to match the input load capacitor from the crystal (see Figure 15). The required values can be calculated:

$$C_{X0} = C_{X1} = 2 \times C_L - C_{ICB},$$

where C_L is the crystal load capacitor as specified for the crystal unit and C_{ICB} is the input capacitance of the device including the board capacitance (stray capacitance of PCB).

For example, for a fundamental 27-MHz crystal with C_L of 9 pF and C_{ICB} of 4 pF,

$$C_{X0} = C_{X1} = (2 \times 9\ pF) - 3\ pF = 15\ pF.$$

It is important to use a short PCB trace from the device to the crystal unit to keep the stray capacitance of the oscillator loop to a minimum.

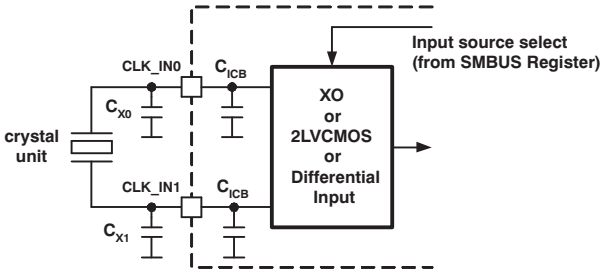


Figure 15. Crystal Input Circuitry

In order to ensure a stable oscillating, a certain drive power must be applied. The CDC906 features an input oscillator with adaptive gain control which relieves the user to manually program the gain. The drive level is the amount of power dissipated by the oscillating crystal unit and is usually specified in terms of power dissipated by the resonator (equivalent series resistance (ESR)). Figure 16 gives the resulting drive level vs crystal frequency and ESR.

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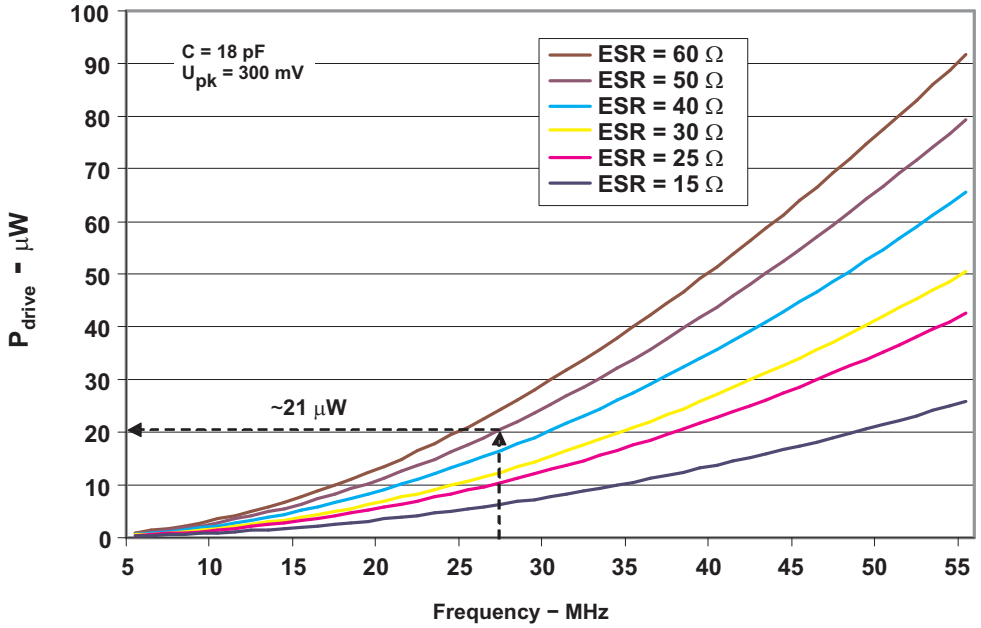


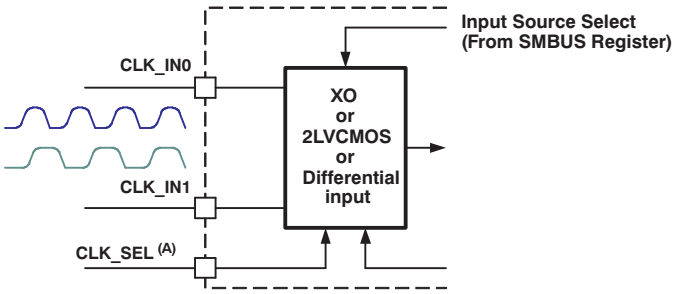
Figure 16. Crystal Drive Power

For example, if a 27-MHz crystal with ESR of 50 Ω is used and 2 × C_L is 18 pF, the drive power is 21 µW. Drive level should be held to a minimum to avoid over driving the crystal. The maximum power dissipation is specified for each type of crystal in the oscillator specifications, i.e., 100 µW for the example above.

Single-Ended LVCMOS Clock Inputs

When selecting the LVCMOS clock mode, CLK_IN0 and CLK_IN1 act as regular clock inputs pins and can be driven up to 167 MHz. Both clock inputs circuitry are equal in design and can be used independently to each other (see Figure 17). The internal clock select bit, Byte 10, Bit [4], selects one of the two input clocks. CLK_IN0 is the default selection. There is also the option to program the external control pin S0/CLK_SEL as clock select pin, Byte 10, Bit [1:0].

The two clock inputs can be used for redundancy switching, i.e. to switch between a primary clock and secondary clock. Note a phase difference between the clock inputs may require PLL correction. Also in case of different frequencies between the primary and secondary clock, the PLL has to re-lock to the new frequency.



A. CLK_SEL is optional and can be configured by SMBus setting.

Figure 17. LVCMOS Clock Input Circuitry

Differential Clock Inputs

The CDC906 supports differential signaling as well. In this mode, CLK_IN0 and CLK_IN1 pin serve as differential signal inputs and can be driven up to 167 MHz.

The minimum magnitude of the differential input voltage is 100 mV over a differential common-mode input voltage range of 200 mV to V_{CC} – 0.6. If LVDS or LVPECL signal levels are applied, ac-coupling and a biasing structure is recommended to adjust the different physical layers (see Figure 18). The capacitor removes the dc component of the signal (common-mode voltage), while the ac component (voltage swing) is passed on. A resistor pull-up and/or pull-down network represents the biasing structure used to set the common-mode voltage on the receiver side of the ac-coupling capacitor. DC coupling is also possible.

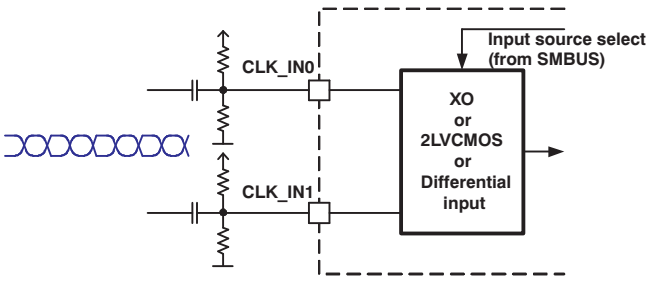


Figure 18. Differential Clock Input Circuitry

PLL Configuration and Setting

The CDC906 includes three PLLs which are equal in function and performance. Except PLL2 which in addition supports spread spectrum clocking (SSC) generation. Figure 19 shows the block diagram of the PLL.

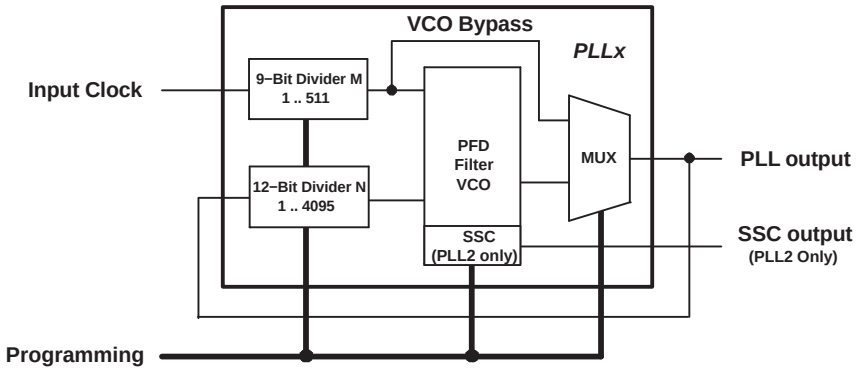


Figure 19. PLL Architecture

All three PLLs are designed for easiest configuration. The user just has to define the input and output frequencies or the divider (M, N, P) setting respectively. All other parameters, such as charge-pump current, filter components, phase margin, or loop bandwidth are controlled and set by the device itself. This assures optimized jitter attenuation and loop stability.

The PLL support normal-speed mode (80 MHz ≤ f_{VCO} ≤ 200 MHz) and high-speed mode (180 MHz ≤ f_{VCO} ≤ 300 MHz) which can be selected by PLLxFVCO (Bit [7:5] of Byte 6). The respective speed option assures stable operation and lowest jitter.

The divider M and divider N operates internally as fractional divider for f_{VCO} up to 250 MHz. This allows fractional divider ratio for zero ppm output clock error.

In case of f_{VCO} > 250 MHz, it is recommended that integer factors of N/M are used only.

For optimized jitter performance, keep divider M as small as possible. Also, the fractional divider concept requires a PLL divider configuration, M ≤ N (or N/M ≥ 1).

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Additionally, each PLL supports two bypass options:

- PLL Bypass and
- VCO Bypass

In PLL bypass mode, the PLL completely is bypassed, so that the input clock is switched directly to the Output-Switch-A (SWAPxx of Byte 9 to12). In the VCO bypass mode, only the VCO of the respective PLL is bypassed by setting PLLxMUX to 1 (Bit [7:5] of Byte 3). But the divider M still is useable and expands the output divider by additional 9-bits. This gives a total divider range of M x P = 511 × 127 = 64897. In VCO bypass mode the respective PLL block is powered down and minimizes current consumption.

Table 3. Example for Divide, Multiplication, and Bypass Operation

Function	Equation (1)	f_{IN} [MHz]	$f_{OUT\text{-}desired}$ [MHz]	$f_{OUT\text{-}actual}$ [MHz]	Divider				f_{VCO} [MHz]
					M	N	P	N/M	
Fractional (2)	$f_{OUT} = f_{IN}$ x (N/M)/P	30.72	155.52	155.52	16	81	1	5.0625	155.52
Integer Factor (3)	$f_{OUT} = f_{IN}$ x (N/M)/P	27	162	162	1	6	1	6	162
VCO bypass	$f_{OUT} = f_{IN}/(M \times P)$	30.72	0.06	0.06	8	—	64	—	—

(1) P-divider of Output-Switch-Matrix is included in the calculation.
(2) Fractional operation for $f_{VCO} \leq 250$ MHz.
(3) Integer operation for $f_{VCO} > 250$ MHz.

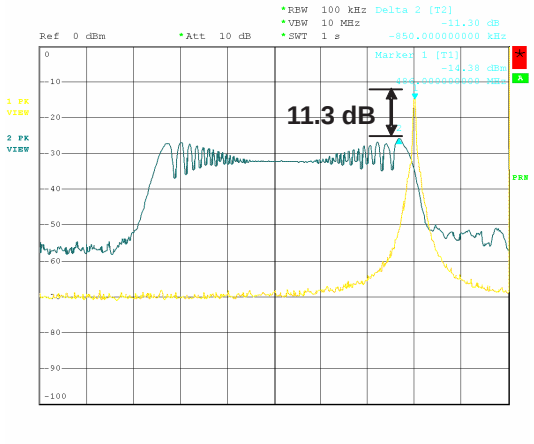
Spread Spectrum Clocking and EMI Reduction

In addition to the basic PLL function, PLL2 supports spread spectrum clocking (SSC) as well. Thus, PLL 2 features two outputs, a SSC output and a non-SSC output. Both outputs can be used in parallel. The mean phase of the Center Spread SSC modulated signal is equal to the phase of the non-modulated input frequency. SSC is selected by Output-Switch-A (SWAPxx of Byte 9 to 12).

SSC also is bypass-able (Byte 25, Bit [6:4]), which powers-down the SSC output and set it to logic low state. The non-SSC output of PLL2 is not affected by this mode and can still be used.

SSC is an effective method to reduce electro-magnetic interference (EMI) noise in high-speed applications. It reduces the RF energy peak of the clock signal by modulating the frequency and spread the energy of the signal to a broader frequency range. Because the energy of the clock signal remains constant, a varying frequency that broadens the overtones necessarily lowers their amplitudes. Figure 20 shows the effect of SSC on a 54-MHz clock signal for DSP

Down Spread 3%
9th Harmonic, fm = 60 kHz



Center Spread ± 0.4%
9th Harmonic, fm = 60 kHz

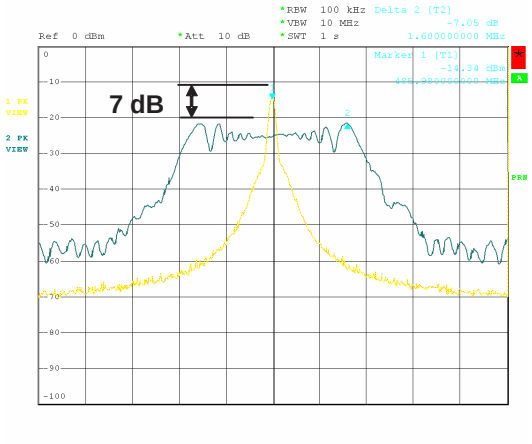


Figure 20. Spread Spectrum Clocking With Center Spread and Down Spread

The peak amplitude of the modulated clock is 11.3 dB lower than the non-modulated carrier frequency for down spread and radiated less electro-magnetic energy.

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In SSC mode, the user can select the SSC modulation amount and SSC modulation frequency. The modulation amount is the frequency deviation based to the carrier (min/max frequency), whereas the modulation frequency determines the speed of the frequency variation. In SSC mode, the maximum VCO frequency is limited to 167 MHz.

SSC Modulation Amount

The CDC906 supports center spread modulation and down spread modulation. In center spread, the clock is symmetrically shifted around the carrier frequency and can be ±0.1%, ±0.25%, and ±0.4%. At down spread, the clock frequency is always lower than the carrier frequency and can be 1%, 1.5%, 2%, and 3%. The down spread is preferred if a system can not tolerate an operating frequency higher than the nominal frequency (over-clocking problem).

Example:

	Modulation Type	Minimum Frequency	Center Frequency	Maximum Frequency
A	±0.25% center spread	53.865 MHz	54 MHz	54.135 MHz
B	1% down spread	53.46 MHz	—	54 MHz
C	0.5% down spread (1)	53.73 MHz	53.865 MHz	54 MHz

(1) A down spread of 0.5% of a 54-MHz carrier is equivalent to 59.865 MHz at a center spread of ±0.25%.

SSC Modulation Frequency

The modulation frequency (sweep rate) can be selected between 30 kHz and 60 kHz. It is also based on the VCO frequency as shown in the *SSC Modulation Frequency Selection*. As shown in Figure 21, the damping increases with higher modulation frequencies. It may be limited by the tracking skew of a downstream PLL. The CDC906 uses a triangle modulation profile which is one of the common profiles for SSC.

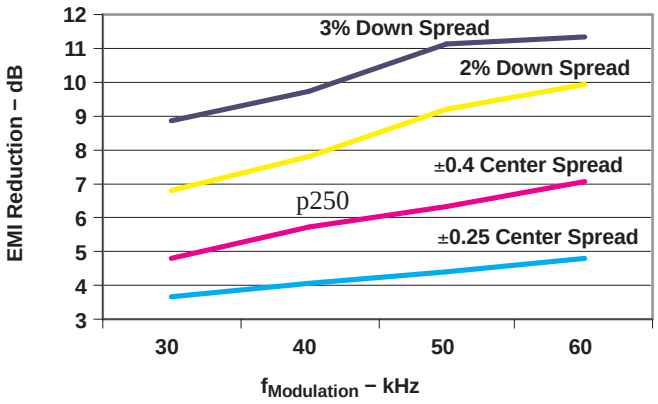


Figure 21. EMI Reduction vs $f_{Modulation}$ and f_{Amount}

Further EMI Reduction

The optimum damping is a combination of modulation amount, modulation frequency and the harmonics which are considered. Note that higher order harmonic frequencies results in stronger EMI reduction because of respective higher frequency deviation.

As seen in Figure 22 and Figure 23, a slower output slew rate and/or smaller output signal amplitude helps to reduce EMI emission even more. Both measures reduce the RF energy of clock harmonics. The CDC906 allows slew rate control in four steps between 0.6 ns and 3.3 ns (Byte 19-24, Bit [5:4]). The output amplitude is set by the two independent output supply voltage pins, V_{CCOUT1} and V_{CCOUT2}, and can vary from 2.3 V to 3.6 V. Even a lower output supply voltage down to 1.8 V works, but the maximum frequency has to be considered.

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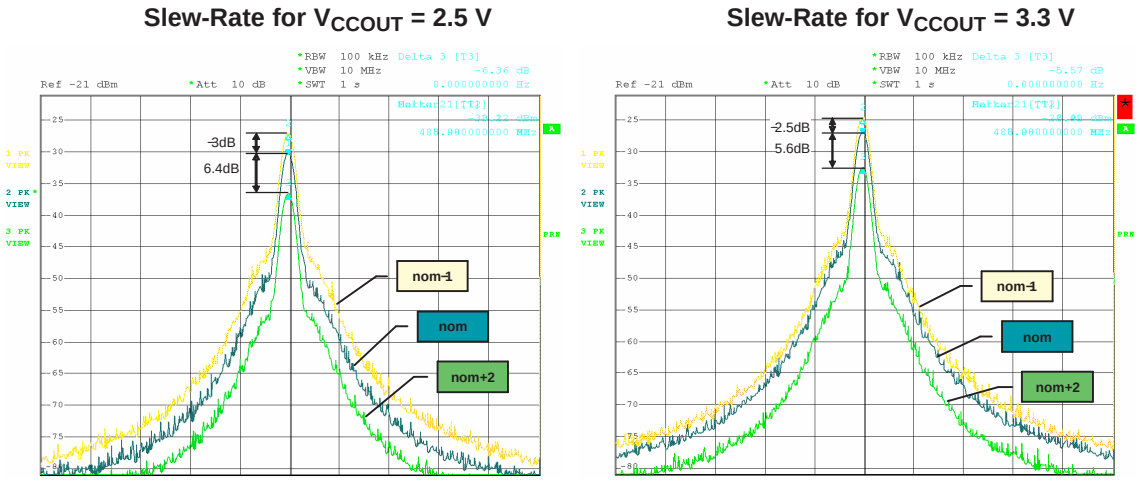


Figure 22. EMI Reduction vs Slew-Rate and V_{ccout}

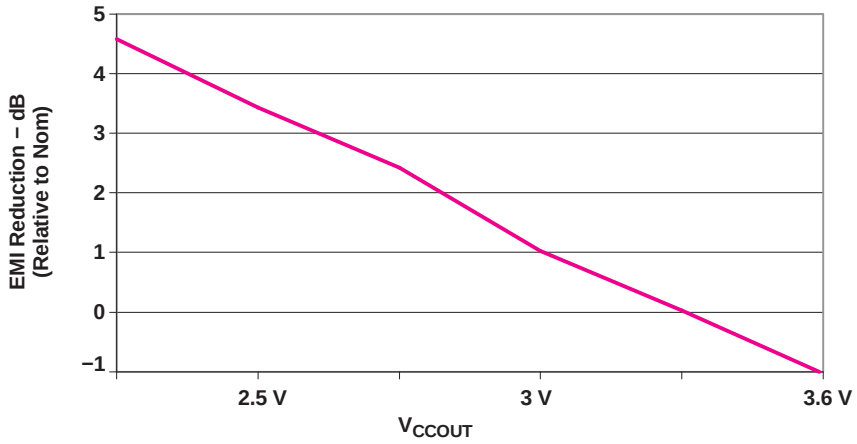


Figure 23. EMI Reduction vs V_{ccout}

Multi-Function Control Inputs S0 and S1

The CDC906 features two user definable inputs pins which can be used as external control pins or address pins. When programmed as control pins, they can function as clock select pin, enable/disable pin or device power-down pin. If both pins used as address-bits, up to four devices can be connected to the same SMBus. The respective function is set in Byte 10; Bit [3:0]. Table 4 shows the possible setting for the different output conditions, clock select and device addresses.

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Table 4. Configuration Setting of Control Inputs

Configuration Bits				External Control Pins		Device Function			
Byte 10, Bit [3:2]		Byte 10, Bit [1:0]							
S11	S10	S01	S00	S1 (Pin 2)	S0 (Pin 1)	Yx Outputs	Power Down	Pin 2	Pin 1
0	X	0	X	1	1	Active	No	Output ctrl	Output ctrl
0	0	0	X	0	1	Low/High(1)	No	Output ctrl	Output ctrl
0	1	0	X	0	1	3-State	Outputs only	Output ctrl	Output ctrl
0	X	0	0	X	0	3-State	PLL, inputs and outputs	Output ctrl	Output ctrl and pd
0	X	0	1	0	0	*S10*=0: low/high(1) *S10*=1: 3-State	PLL only	Output ctrl	PLL and Div bypass
0	X	0	1	1	0	Active	PLL only	Output ctrl	PLL and Div bypass
0	X	1	0	0	0/1(2)	*S10*=0: Low/High(1) *S10*=1: 3-State	No	Output ctrl	CLK_SEL
0	X	1	0	1	0/1(2)	Active	No	Output ctrl	CLK_SEL

(1) A non-inverting output will be set to low and an inverting output will be set to high.
(2) If S0 is 0, CLK_IN0 is selected; if S0 is 1, CLK_IN1 is selected.

As shown in Table 4, there is a specific order of the different output condition: Power-down mode overwrites 3-state, 3-state overwrites low-state, and low-state overwrites active-state.

Output Switching Matrix

The flexible architecture of the output switch matrix allows the user to switch any of the internal clock signal sources via a free-selectable post-divider to any of the six outputs.

As shown in Figure 24, the CDC906 is based on two banks of switches and six post-dividers. Switch A comprises six *5-Input-Muxes* which selects one of the four PLL clock outputs or directly selects the input clock and feed it to one of the 7-bit post-divider (P-Divider). Switch B is made up of six 6-Input-Muxes which takes any post-divider and feeds it to one of the six outputs, Yx.

Switch B was added to the output switch matrix to ensure that outputs frequencies derive from one P-divider are 100% phase aligned. Also, the P-divider is built in a way that every divide factor is automatically duty-cycle corrected. Changing the divider value on the fly may cause a glitch on the output.

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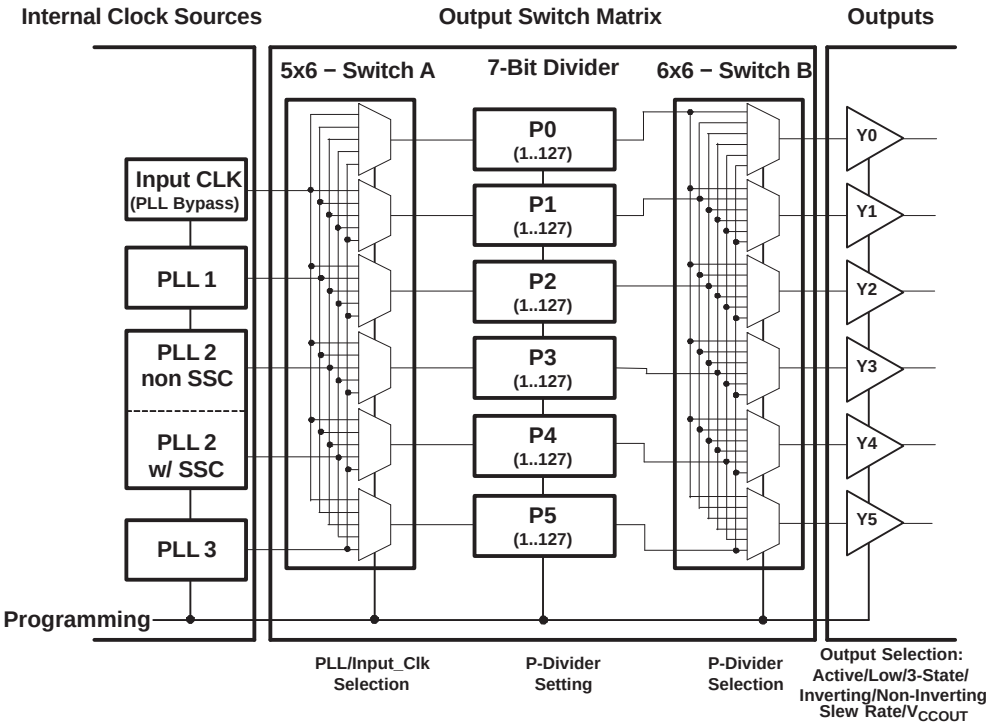


Figure 24. CDC906 Output Switch Matrix

In addition, the outputs can be switched active, low or 3-state and/or 180 degree phase shifted. Also the outputs slew-rate and the output-voltage is user selectable.

LVCMOS Output Configuration

The output stage of the CDC906 supports all common output setting, such as enable, disable, low-state and signal inversion (180 degree phase shift). It further features slew-rate control (0.6 ns to 3.3 ns) and variable output supply voltage (2.3 V to 3.6 V).

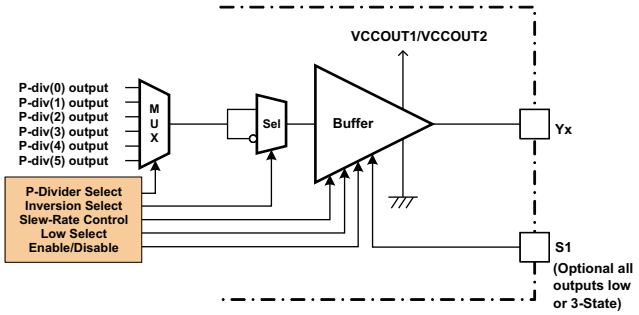


Figure 25. Block Diagram of Output Architecture

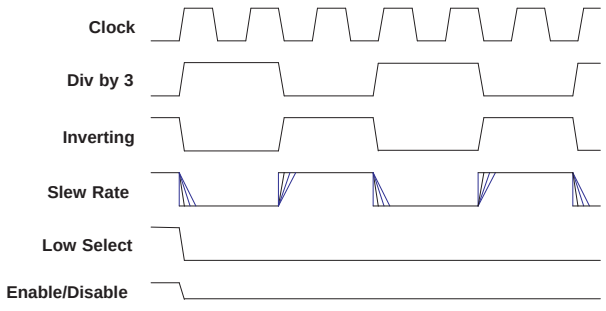


Figure 26. Example for Output Waveforms

All output settings are programmable via SMBus:

- enable, disable, low-state via external control pins S0 and S1 → Byte 10, Bit[3:0]
- enable or disable-to-low → Byte 19 to 24, Bit[3]
- inverting/non-inverting → Byte 19 to 24, Bit[6]
- slew-rate control → Byte 19 to 24, Bit[5:4]
- output swing → external pins V_{CCOUT1} (Pin 14) and V_{CCOUT2} (Pin 18)

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Performance Data: Output Skew, Jitter, Cross Coupling, Noise Rejection (Spur-Suppression), and Phase Noise

Output Skew

Skew is an important parameter for clock distribution circuits. It is defined as the time difference between outputs that are driven by the same input clock. Table 5 shows the output skew ($t_{sk(o)}$) of the CDC906 for high-to-low and low-to-high transitions over the entire range of supply voltages, operating temperature and output voltage swing.

Table 5. Output Skew

PARAMETER	V_{ccout}	TYP	MAX	UNIT
$t_{sk(o)}$	2.5 V	130	250	ps
	3.3 V	130	200	ps

Jitter Performance

Jitter is a major parameter for PLL-based clock driver circuits. This becomes important as speed increases and timing budget decreases. The PLL and internal circuits of CDC906 are designed for lowest jitter. The peak-to-peak period jitter is only 60 ps (typical). Table 6 gives the peak-to-peak and rms deviation of cycle-to-cycle jitter, period jitter and phase jitter as taken during characterization.

Table 6. Jitter Performance of CDC906

PARAMETER	f_{out}	TYP (1)		MAX (1)		UNIT
		Peak-Peak	rms (one sigma)	Peak-Peak	rms (one sigma)	
$t_{jit(cc)}$	50 MHz	55	–	75	–	ps
	133 MHz	50	–	85	–	
$t_{jit(per)}$	50 MHz	60	4	76	7	ps
	133 MHz	55	5	84	11	
$t_{jit(phase)}$	50 MHz	730	90	840	115	ps
	133 MHz	930	130	1310	175	

(1) All typical and maximum values are at V_{CC} = 3.3 V, temperature = 25°C, V_{ccout} = 3.3 V; one output is switching, data taken over several 10000 cycles.

Figure 27, Figure 28, and Figure 29 show the relationship between cycle-to-cycle jitter, period jitter, and phase jitter over 10000 samples. The jitter varies with a smaller or wider sample window. The cycle-to-cycle jitter and period jitter show the measured value whereas the phase jitter is the accumulated period jitter.

Cycle-to-Cycle jitter ($t_{jit(cc)}$) is the variation in cycle time of a clock signal between adjacent cycles, over a random sample of adjacent cycle pairs. Cycle-to-cycle jitter will never be greater than the period jitter. It is also known as adjacent cycle jitter.

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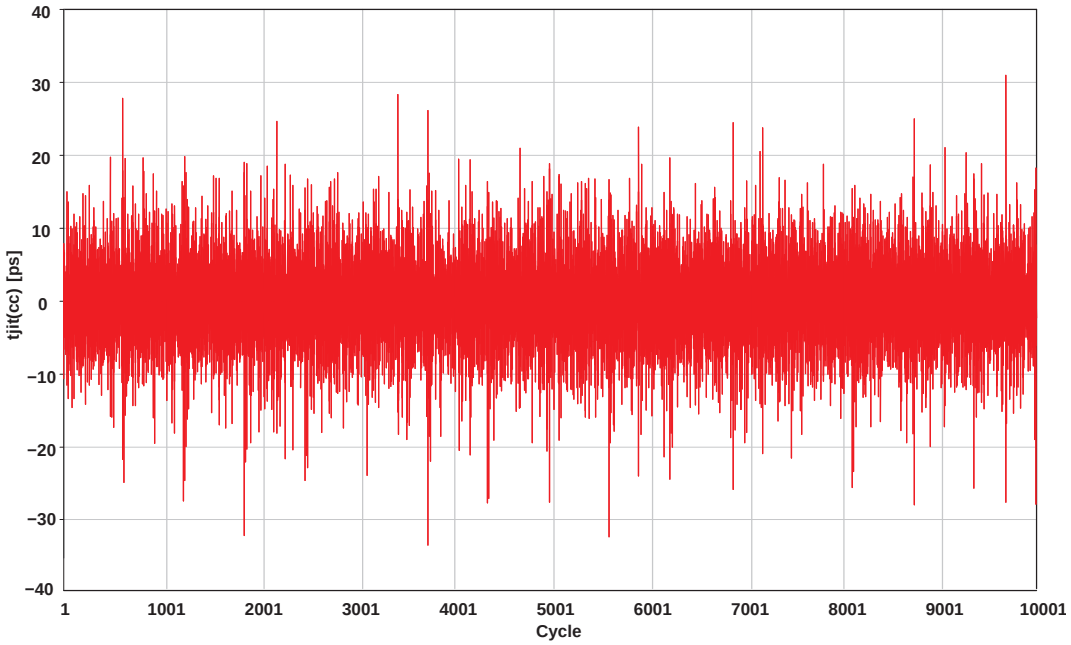


Figure 27. Snapshot of Cycle-to-Cycle Jitter

Period jitter ($t_{jit(per)}$) is the deviation in cycle time of a clock signal with respect to the ideal period (1/fo) over a random sample of cycles. In reference to a PLL, period jitter is the worst-case period deviation from the ideal that would ever occur on the PLLs outputs. This is also referred to as short-term jitter.

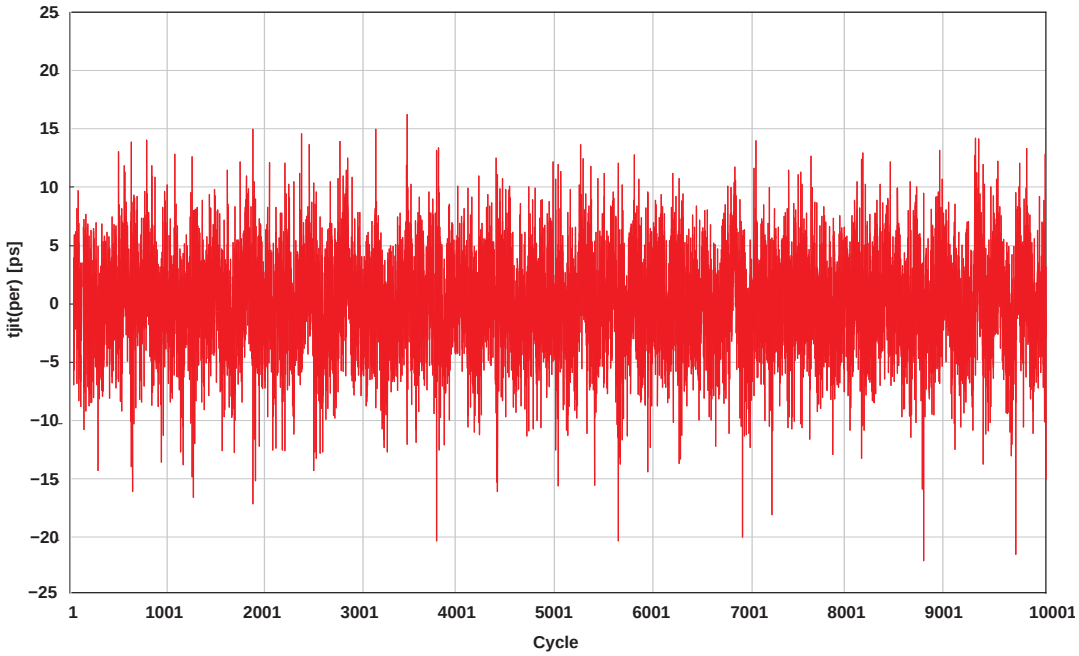


Figure 28. Snapshot of Period Jitter

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Phase jitter ($t_{jit(phase)}$) is the long-term variation of the clock signal. It is the cumulative deviation in t(Θ) for a controlled edge with respect to a t(Θ) mean in a random sample of cycles. Phase jitter, Time Interval Error (TIE), or Wander are used in literature to describe long-term variation in frequency. As of ITU-T: G.810, wander is defined as phase variation at rates less than 10 Hz while jitter is defined as phase variation greater than 10 Hz. The measurement interval must be long enough to gain a meaningful result. Wander can be caused by temperature drift, aging, supply voltage drift, etc.

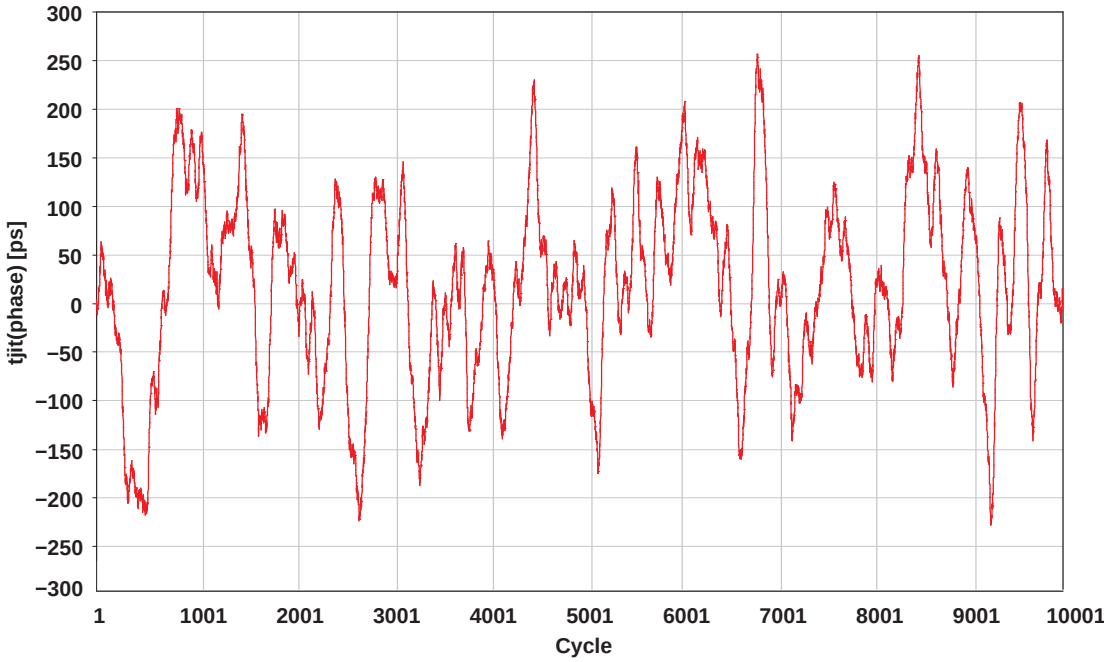


Figure 29. Snapshot of Phase Jitter

Jitter also depends on the VCO frequency (f_{VCO}) of the PLL. A higher f_{VCO} results in better jitter performance compared to a lower f_{VCO}. The VCO frequency can be defined via the M- and N-divider of the PLL.

As the CDC906 supports a pretty wide frequency range, the device offers a VCO Frequency Selection Bit, Bit [7:5] of Byte 6. This bit defines the jitter-optimized frequency range of each PLL. The user can select between the normal-speed mode (80 MHz to 200 MHz) and the high-speed mode (180 MHz to 300 MHz). Figure 30 shows the jitter performance over f_{VCO} for the two frequency ranges.

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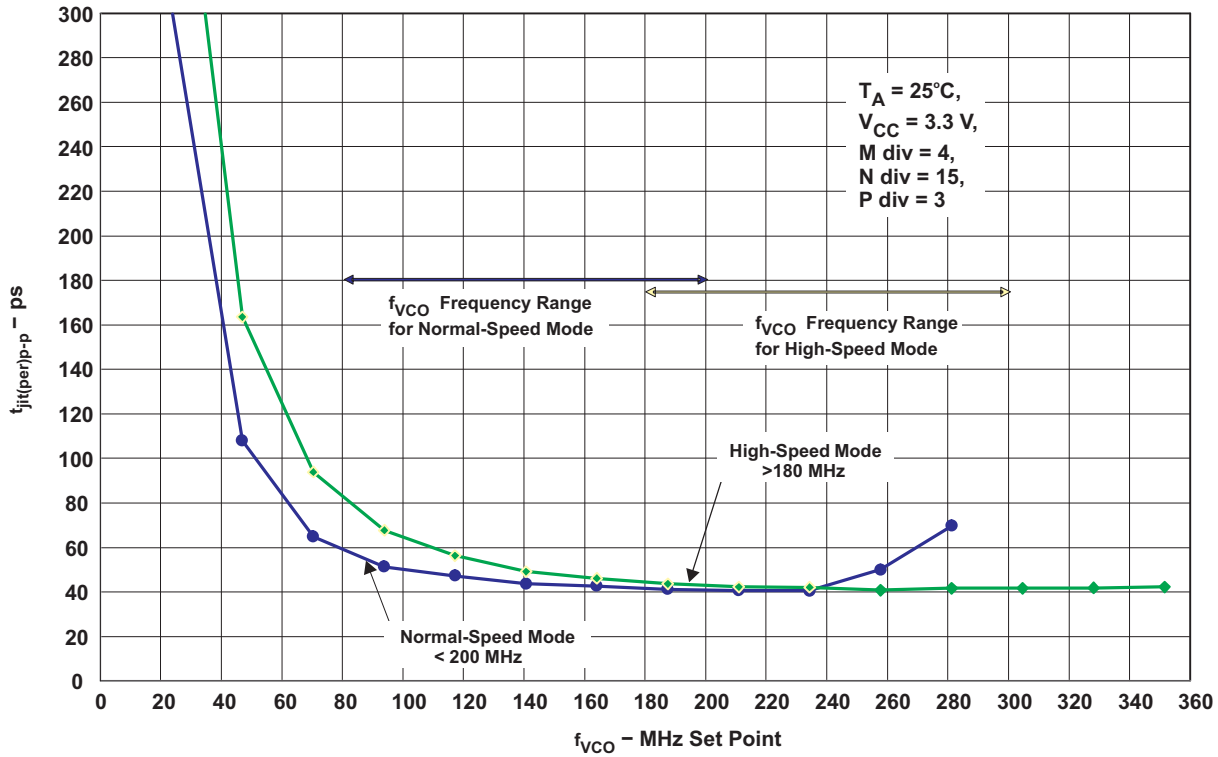


Figure 30. Period Jitter vs f_{VCO} for Normal-Speed Mode and High-Speed Mode

The TI Pro Clock software automatically calculates the PLL parameter for jitter-optimized performance.

Cross Coupling, Spur Suppression, and Noise Rejection

Cross-Coupling in ICs occurs through interactions between several parts of the chip such as between output stages, metal lines, bond wires, substrate, etc. The coupling can be capacitive, inductive and resistive (ohmic) induced by output switching, leakage current, ground bouncing, power supply transients, etc.

The CDC906 is designed in a RFSiGe process technology. This process gives excellent performance in linearity, low power consumption, best-in-class noise performance and good isolation characteristic between the on-chip components.

The good isolation was a major criteria to use the RFSiGe process as it minimizes the coupling effect. Even if all three PLLs are active and all outputs are on, the noise suppression is clearly above 50 dB. Figure 31 and Figure 32 show an example of noise coupling, spur-suppression, and power supply noise rejection of CDC906. Die respective measurement conditions are shown in Figure 31 and Figure 32.

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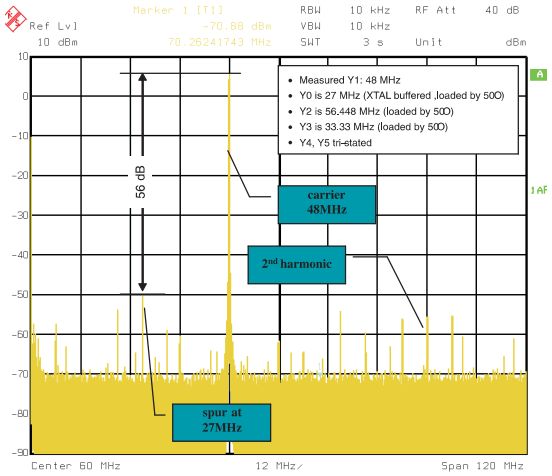


Figure 31. Noise Coupling and Spur Suppression

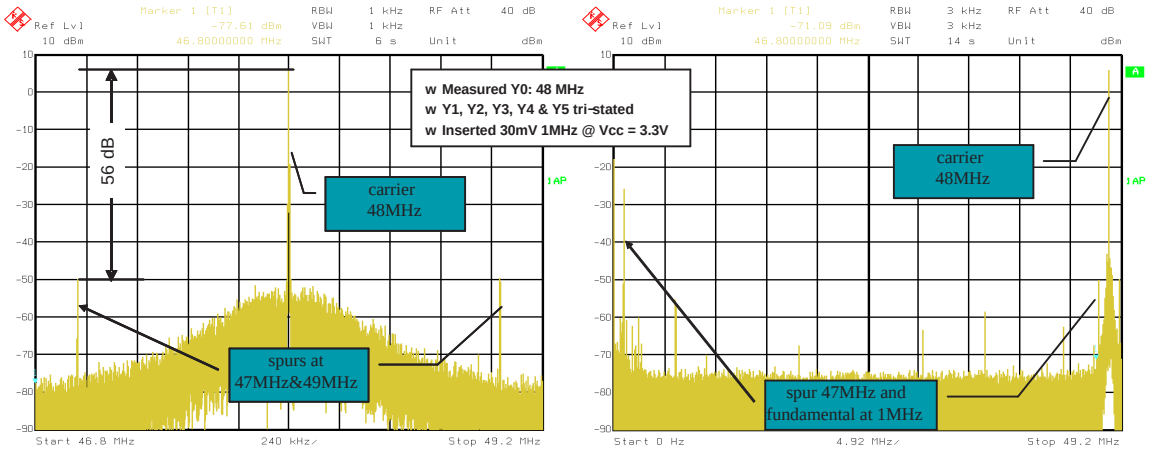


Figure 32. Power Supply Noise Rejection

Phase Noise Characteristic

In high-speed communication systems, the phase noise characteristic of the PLL frequency synthesizer is of high interest. Phase noise describes the stability of the clock signal in the frequency domain, similar to the jitter specification in the time domain.

Phase noise is a result of random and discrete noise causing a broad slope and spurious peaks. The discrete spurious components could be caused by known clock frequencies in the signal source, power line interference, and mixer products. The broadening caused by random noise fluctuation is due to phase noise. It can be the result of thermal noise, shot noise and/or flicker noise in active and passive devices.

Important factor for PLL synthesizer is the loop bandwidth (–3 dB cut-off frequency) — large loop bandwidth (LBW) results in fast transient response but have less reference spur attenuation. The LBW of the CDC906 is about 100 kHz to 250 kHz, dependent on selected PLL parameter.

For the CDC906, two phase noise characteristics are of interest: The phase noise of the crystal-input stage and the phase noise of the internal PLL (VCO). Figure 33 shows the respective phase noise characteristic.

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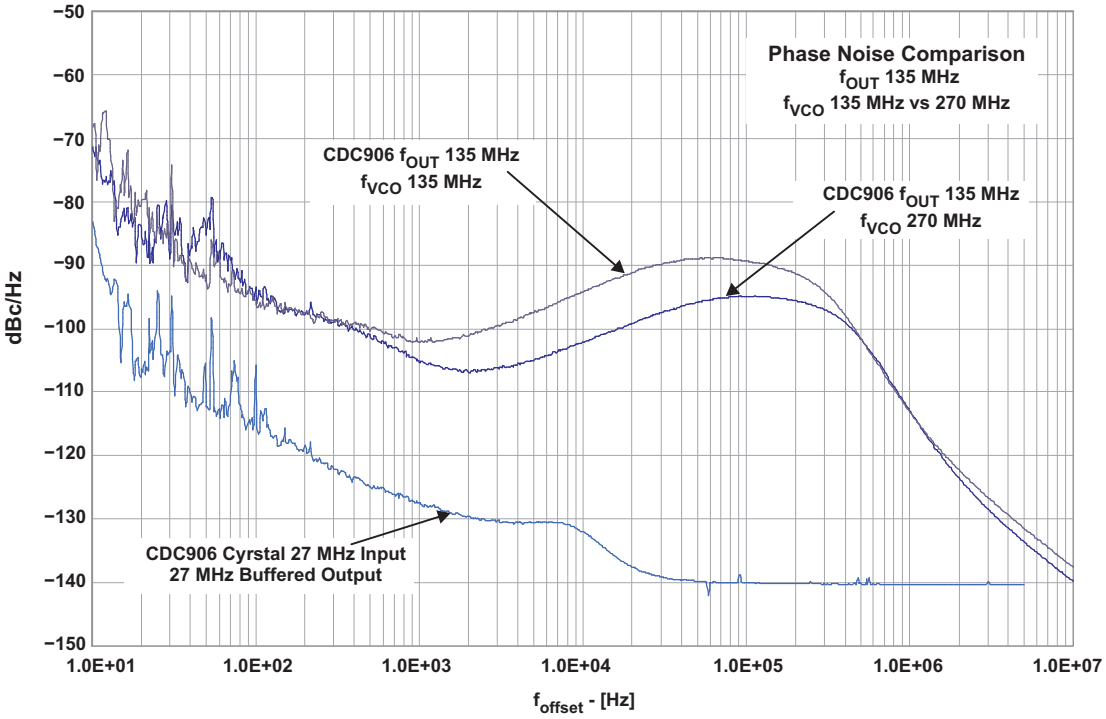


Figure 33. Phase Noise Characteristic

PLL Lock-Time

Some applications use frequency switching, i.e. to change frequency in TV application (switching between channels) or change the PCI-X frequency in computers. The time spent by the PLL in achieving the new frequency is of main interest. The lock time is the time it takes to jump from one specified frequency to another specified frequency within a given frequency tolerance (Figure 34). It should be low, because a long lock time impacts the data rate of the system.

The PLL Lock Time depends on the device configuration and can be changed by the VCO frequency, i.e. by changing the M/N divider values. Table 7 gives the typical lock times of the CDC906 and Figure 34 shows a snapshot of a frequency switch.

Table 7. CDC906 PLL Lock-Times

Description	Lock Time (Typical)	Unit
Frequency change via reprogramming of N/M counter	100	µs
Frequency change via CLK_SEL pin (switching between CLK_IN0 and CLK_IN1)	100	µs
Power-up lock time with system clock	50	µs
Power-up lock time with 27-MHz Crystal at CLK_IN0 and CLK_IN1	300(1)	µs

(1) Is the result of crystal power up (200 µs) and PLL Lock Time (100 µs).

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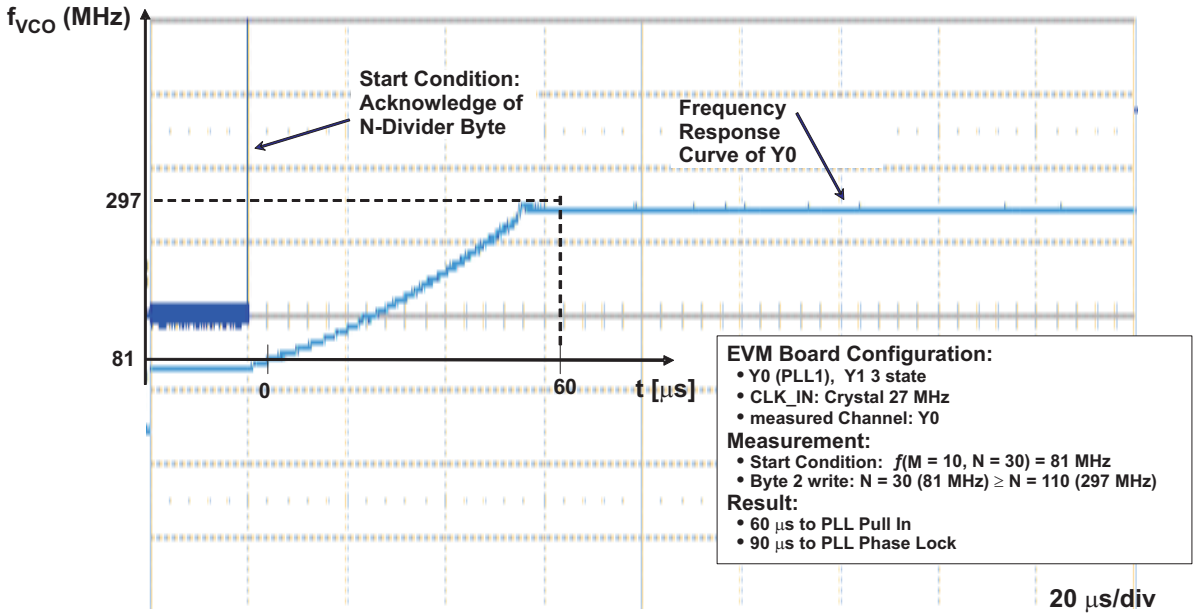


Figure 34. Snapshot of the PLL Lock-Time

Power Supply Sequence

The CDC906 includes the following three power supply pins: V_{CC}, V_{CCOUT1}, and V_{CCOUT2}. There are no power supply sequencing requirements, as the three power nodes are separated from each other. So, power can be supplied in any order to the three nodes.

Also, the part has a power-up circuitry which switches the device on if V_{CC} exceeds 2.1 V (typical) and switches the device off at V_{CC} < 1.7 V (typical). In power-down mode, all outputs and clock inputs are switched off.

Device Behavior During Supply Voltage Drops

The CDC906 has a Power-Up-Circuit, which activates the device function at V_{PUC_ON} (typical 2.1 V). At the same time, the ROM information is loaded into the register. This mechanism ensures that there is a pre-defined default after Power-Up and no need to reprogram the CDC906 in the application.

In the event of a supply-voltage-drop, the Power-Up-Circuit assures that there is always a defined setup within the register. Figure 35 shows possible voltage drops with different amplitudes.

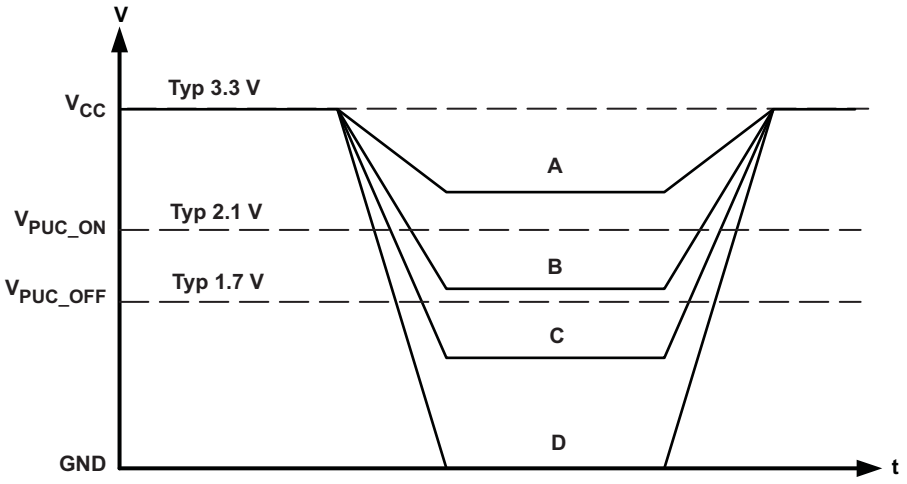


Figure 35. Different Voltage Drops on V_{CC} During Operation

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The CDC906 Power-Up-Circuit has an inbuilt hysteresis. If the voltage stays above V_{PUC_OFF}, which is typically at 1.7 V, the register content stays unchanged. If the voltage drops below V_{PUC_OFF}, the internal register is reloaded by the ROM after V_{PUC_ON} is crossed again. V_{PUC_ON} is typically 2.1 V. Table 8 show the content of the ROM and the Register after above voltage drops scenarios.

Table 8. ROM and Register Content After V_{CC} Drop

Power Drop	ROM Content	Register Content
A	Unchanged	Unchanged
B	Unchanged	Unchanged
C	Unchanged	Reloaded from ROM
D	Unchanged	Reloaded from ROM

EVM and Programming SW

The CDC906 EVM is a development kit consisting of a performance evaluation module, the TI Pro Clock software, and the User's Guide. Contact Texas Instruments sales or marketing representative for more information.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDC906PW	NRND	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	CDC906
CDC906PW.B	NRND	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	See CDC906PW	CDC906
CDC906PWG4	NRND	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	See CDC906PW	CDC906
CDC906PWR	NRND	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	CDC906
CDC906PWR.B	NRND	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See CDC906PWR	CDC906
CDC906PWRG4	NRND	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See CDC906PWR	CDC906

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

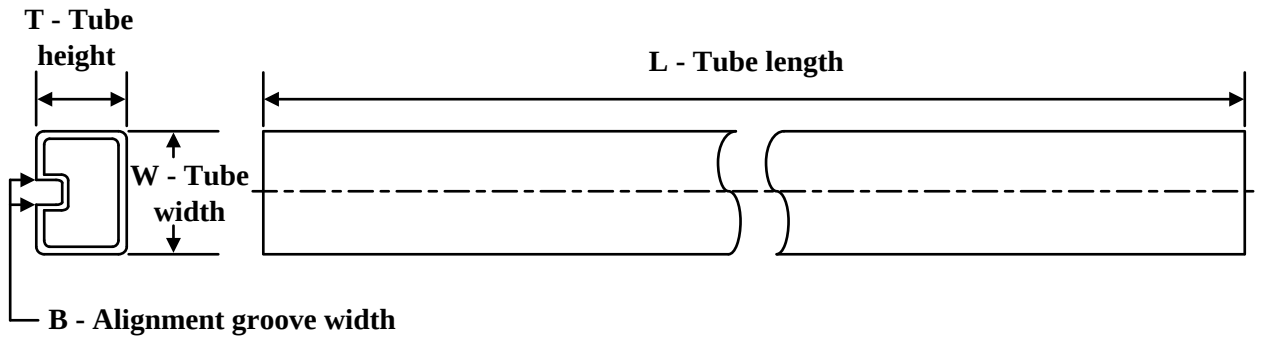
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE



*All dimensions are nominal

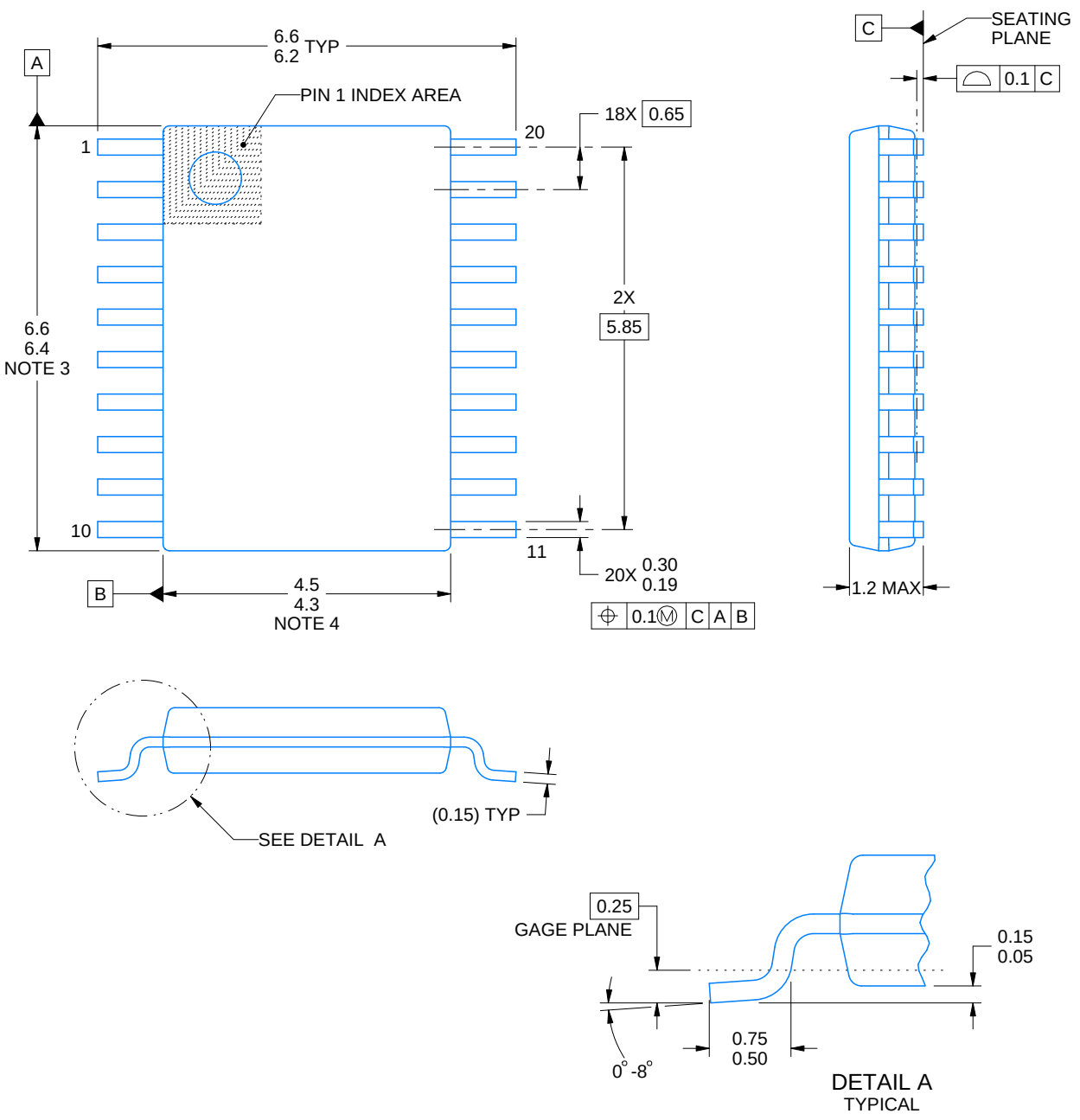
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CDC906PW	PW	TSSOP	20	70	530	10.2	3600	3.5
CDC906PW.B	PW	TSSOP	20	70	530	10.2	3600	3.5
CDC906PWG4	PW	TSSOP	20	70	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0020A

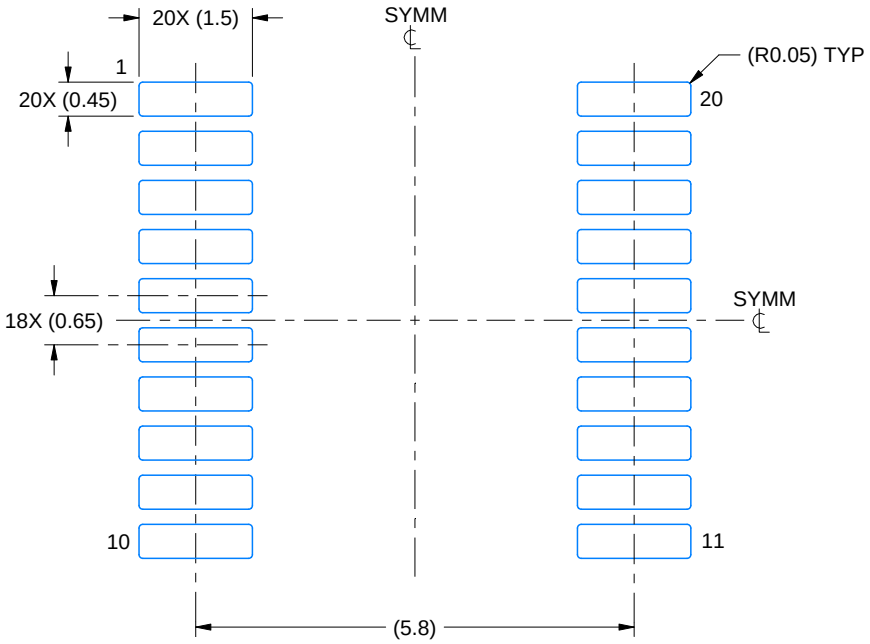
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

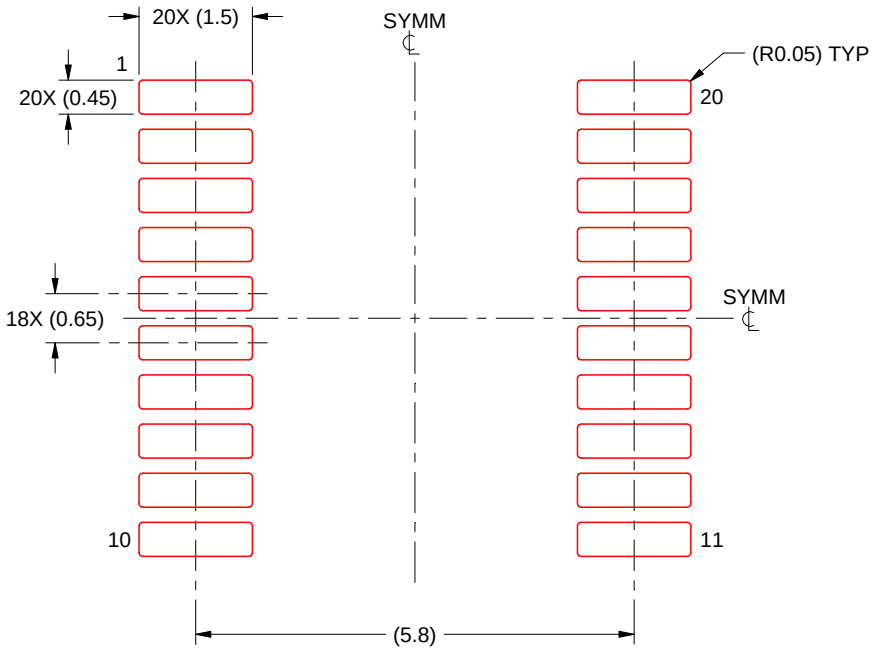


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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