CDCLVD1204 2:4 Low Additive Jitter LVDS Buffer

1 Features

- 2:4 differential buffer
- Low additive jitter: <300fs RMS in 10kHz to 20MHz
- Low output skew of 20ps (maximum)
- Universal inputs accept LVDS, LVPECL, and LVCMOS
- Selectable clock inputs through control pin
- 4 LVDS outputs, ANSI EIA/TIA-644A standard compatible
- Clock frequency: up to 800MHz
- Device power supply: 2.375V to 2.625V
- LVDS reference voltage, V_{AC_REF}, available for capacitive coupled inputs
- Industrial temperature range: –40°C to 85°C
- Packaged in 3mm × 3mm, 16-Pin VQFN (RGT)
- ESD protection exceeds 3kV HBM, 1kV CDM

2 Applications

- Telecommunications and networking
- Medical imaging
- Test and measurement equipment
- Wireless communications
- General purpose clocking

3 Description

The CDCLVD1204 clock buffer distributes one of two selectable clock inputs (IN0 and IN1) to 4 pairs of differential LVDS clock outputs (OUT0 through OUT3) with minimum skew for clock distribution. The CDCLVD1204 can accept two clock sources into an input multiplexer. The inputs can either be LVDS, LVPECL, or LVCMOS.

The CDCLVD1204 is specifically designed for driving 50Ω transmission lines. In case of driving the inputs in single ended mode, the appropriate bias voltage, V_{AC_REF}, must be applied to the unused negative input pin.

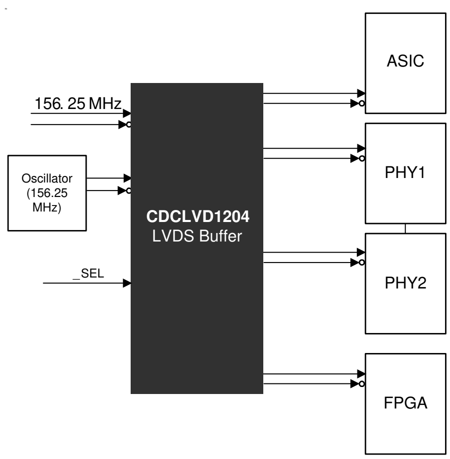
The IN_SEL pin selects the input which is routed to the outputs. If this pin is left open, it disables the outputs (static). The part supports a fail safe function. The device incorporates an input hysteresis which prevents random oscillation of the outputs in the absence of an input signal.

The device operates in 2.5V supply environment and is characterized from –40°C to 85°C (ambient temperature). The CDCLVD1204 is packaged in small, 16-pin, 3mm × 3mm VQFN package.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
CDCLVD1204	VQFN (16)	3.00mm × 3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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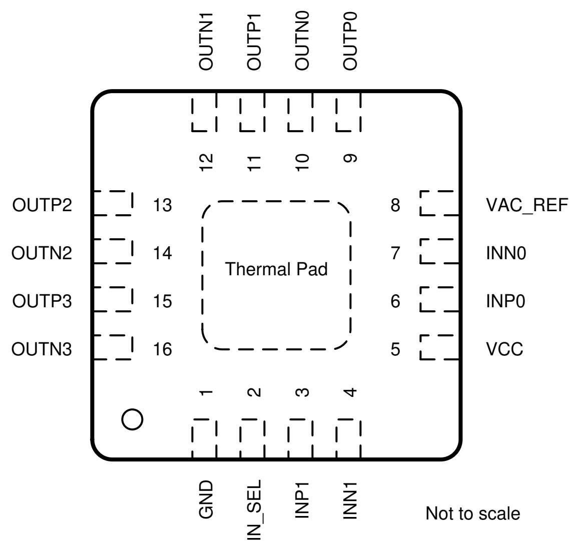


Figure 4-1. RGT Package 16-Pin VQFN Top View

Table 4-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NO.	NAME		
1	GND	G	Device ground
2	IN_SEL	I	Input selection with an internal 200-kΩ pullup and pulldown; selects input port (see Table 7-1)
3, 4	INP1, INN1	I	Differential redundant input pair or single-ended input
5	V_{CC}	P	2.5-V supply for the device
6, 7	INP0, INN0	I	Differential input pair or single-ended input
8	V_{AC_REF}	O	Bias voltage output for capacitive coupled inputs. If used, TI recommends using a 0.1-µF to GND on this pin.
9, 10	OUTP0, OUTN0	O	Differential LVDS output pair number 0
11,12	OUTP1, OUTN1	O	Differential LVDS output pair number 1
13,14	OUTP2, OUTN2	O	Differential LVDS output pair number 2
15,16	OUTP3, OUTN3	O	Differential LVDS output pair number 3

(1) G = Ground, I = Input, O = Output, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

	MIN	MAX	UNIT
Supply voltage, V_{CC}	–0.3	2.8	V
Input voltage, V_I	–0.2	V_{CC} + 0.2	V
Output voltage, V_O	–0.2	V_{CC} + 0.2	V
Driver short circuit current , I_{OSD}	See[(2)]		
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The output can handle the permanent short.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	>3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	>1000	

(1) Human Body Model, 1.5 kΩ, 100 pF
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Device supply voltage	2.375	2.5	2.625	V
T_A	Ambient temperature	–40		85	°C

5.4 Thermal Information

THERMAL METRIC[(1)]		CDCLVD1204 RGT (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	85.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

V_{CC} = 2.375 V to 2.625 V and T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IN_SEL CONTROL						
Vd_{I3}	3-state input	Open		0.5 × V_{CC}		V
Vd_{IH}	Input high voltage		0.7 × V_{CC}			V
Vd_{IL}	Input low voltage				0.2 × V_{CC}	V
Id_{IH}	Input high current	V_{CC} = 2.625 V, V_{IH} = 2.625 V			30	µA
Id_{IL}	Input low current	V_{CC} = 2.625 V, V_{IL} = 0 V			–30	µA
$R_{pull(IN\_SEL)}$	Input pullup or pulldown resistor			200		kΩ
2.5-V LVCMOS INPUT (See Figure 6-3)						
f_{IN}	Input frequency				200	MHz
V_{th}	Input threshold voltage	External threshold voltage applied to complementary input	1.1		1.5	V
V_{IH}	Input high voltage		V_{th} + 0.1		V_{CC}	V
V_{IL}	Input low voltage		0		V_{th} – 0.1	V
I_{IH}	Input high current	V_{CC} = 2.625 V, V_{IH} = 2.625 V			10	µA
I_{IL}	Input low current	V_{CC} = 2.625 V, V_{IL} = 0 V			–10	µA
ΔV/ΔT	Input edge rate	20% to 80%	1.5			V/ns
C_{IN}	Input capacitance			2.5		pF
DIFFERENTIAL INPUT						
f_{IN}	Input frequency	Clock input			800	MHz
$V_{IN, DIFF}$	Differential input voltage peak-to-peak	V_{ICM} = 1.25 V	0.3		1.6	V_{PP}
V_{ICM}	Input common mode voltage	$V_{IN, DIFF, PP}$ > 0.4 V	1		V_{CC} – 0.3	V
I_{IH}	Input high current	V_{CC} = 2.625 V, V_{IH} = 2.625 V			10	µA
I_{IL}	Input low current	V_{CC} = 2.625 V, V_{IL} = 0 V			–10	µA
ΔV/ΔT	Input edge rate	20% to 80%	0.75			V/ns
C_{IN}	Input capacitance			2.5		pF
LVDS OUTPUT						
$\|V_{OD}\|$	Differential output voltage magnitude	$V_{IN, DIFF, PP}$ = 0.3 V,R_L = 100 Ω	250		450	mV
ΔV_{OD}	Change in differential output voltage magnitude	$V_{IN, DIFF, PP}$ = 0.3 V,R_L = 100 Ω	–15		15	mV
$V_{OC(SS)}$	Steady-state common mode output voltage	$V_{IN, DIFF, PP}$ = 0.3 V,R_L = 100 Ω	1.1		1.375	V
$\Delta V_{OC(SS)}$	Steady-state common mode output voltage	$V_{IN, DIFF, PP}$ = 0.6 V,R_L = 100 Ω	–15		15	mV
V_{ring}	Output overshoot and undershoot	Percentage of output amplitude V_{OD}			10%	
V_{OS}	Output AC common mode	$V_{IN, DIFF, PP}$ = 0.6 V, R_L = 100 Ω		25	70	mV_{PP}
I_{OS}	Short-circuit output current	V_{OD} = 0 V			±24	mA
t_{PD}	Propagation delay	$V_{IN, DIFF, PP}$ = 0.3 V		1.5	2.5	ns
$t_{SK, PP}$	Part-to-part skew				600	ps
$t_{SK, O}$	Output skew				20	ps
$t_{SK,P}$	Pulse skew	50% duty cycle input, crossing-point-to-crossing-point distortion	–50		50	ps
t_{RJIT}	Random additive jitter	50% duty cycle input, edge speed = 0.75 V/ns, 10 kHz to 20 MHz			0.3	ps, RMS

5.5 Electrical Characteristics (continued)

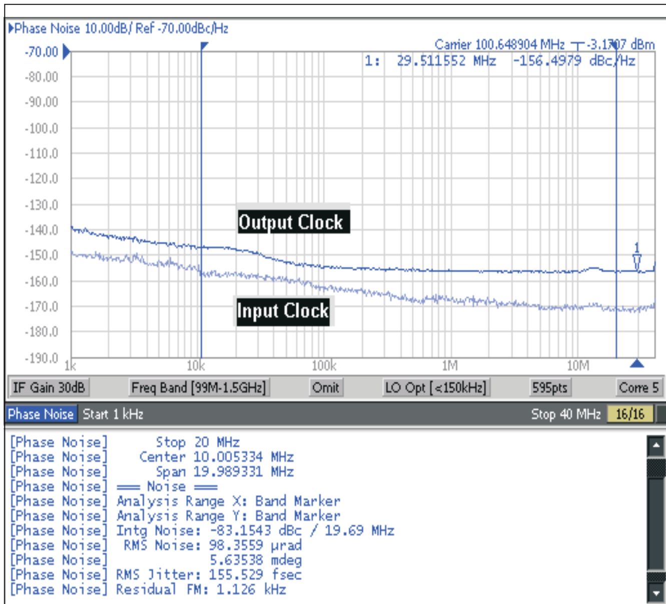
V_{CC} = 2.375 V to 2.625 V and T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R/t_F	Output rise and fall time	20% to 80%,100 Ω, 5 pF	50		300	ps
I_{CCSTAT}	Static supply current	Outputs unterminated, f = 0 Hz		17	28	mA
I_{CC100}	Supply current	All outputs, R_L = 100 Ω, f = 100 MHz		40	58	mA
I_{CC800}	Supply current	All outputs, R_L = 100 Ω, f = 800 MHz		60	80	mA
V_{AC_REF}	Reference output voltage	V_{CC} = 2.5 V, I_{load} = 100 µA	1.1	1.25	1.35	V

5.6 Timing Requirements

		MIN	NOM	MAX	UNIT
ADDITIVE PHASE NOISE FOR 100-MHZ CLOCK					
phn_{100}	Phase noise at 100 Hz offset		–132.9		dBc/Hz
phn_{1k}	Phase noise at 1 kHz offset		–138.8		dBc/Hz
phn_{10k}	Phase noise at 10 kHz offset		–147.4		dBc/Hz
phn_{100k}	Phase noise at 100 kHz offset		–153.6		dBc/Hz
phn_{1M}	Phase noise at 1 MHz offset		–155.2		dBc/Hz
phn_{10M}	Phase noise at 10 MHz offset		–156.2		dBc/Hz
phn_{20M}	Phase noise at 20 MHz offset		–156.6		dBc/Hz
t_{RJIT}	Random additive jitter from 10 kHz to 20 MHz		171		fs, RMS
ADDITIVE PHASE NOISE FOR 737.27-MHZ CLOCK					
phn_{100}	Phase noise at 100 Hz offset		–80.2		dBc/Hz
phn_{1k}	Phase noise at 1 kHz offset		–114.3		dBc/Hz
phn_{10k}	Phase noise at 10 kHz offset		–138		dBc/Hz
phn_{100k}	Phase noise at 100 kHz offset		–143.9		dBc/Hz
phn_{1M}	Phase noise at 1 MHz offset		–145.2		dBc/Hz
phn_{10M}	Phase noise at 10 MHz offset		–146.5		dBc/Hz
phn_{20M}	Phase noise at 20 MHz offset		–146.6		dBc/Hz
t_{RJIT}	Random additive jitter from 10 kHz to 20 MHz		65		fs, RMS

5.7 Typical Characteristics



Input clock RMS jitter is 32 fs from 10 kHz to 20 MHz and additive RMS jitter is 152 fs, T_A = 25°C, and V_{CC} = 2.5 V

Figure 5-1. 100-MHz Input and Output Phase Noise Plot

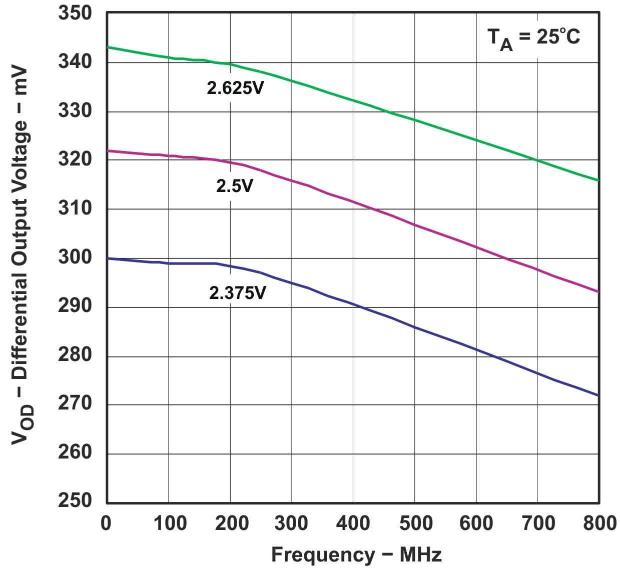


Figure 5-2. Differential Output Voltage vs Frequency

6 Parameter Measurement Information

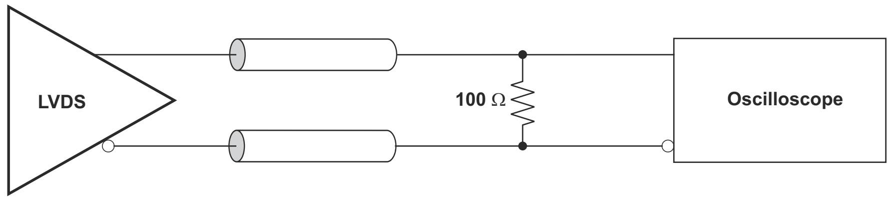


Figure 6-1. LVDS Output DC Configuration During Device Test

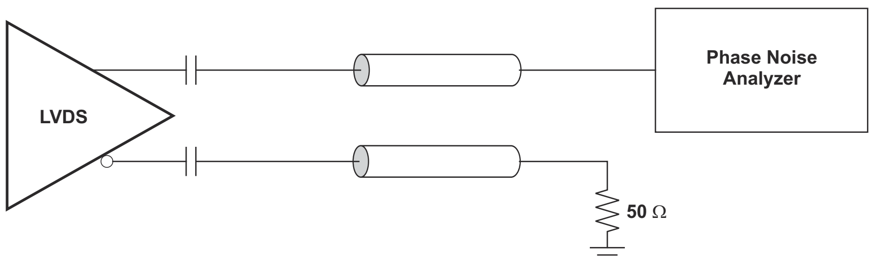


Figure 6-2. LVDS Output AC Configuration During Device Test

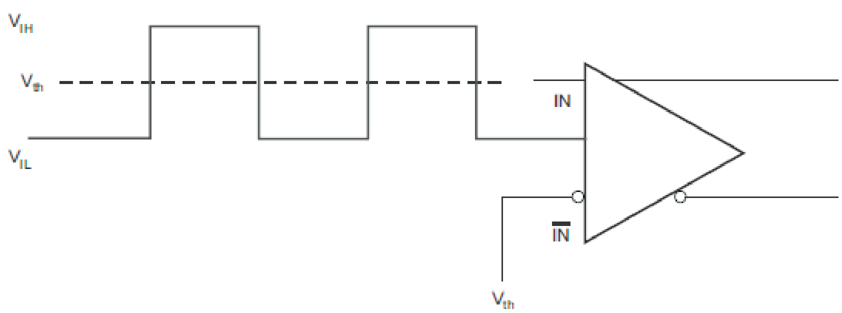


Figure 6-3. DC Coupled LVCMOS Input During Device Test

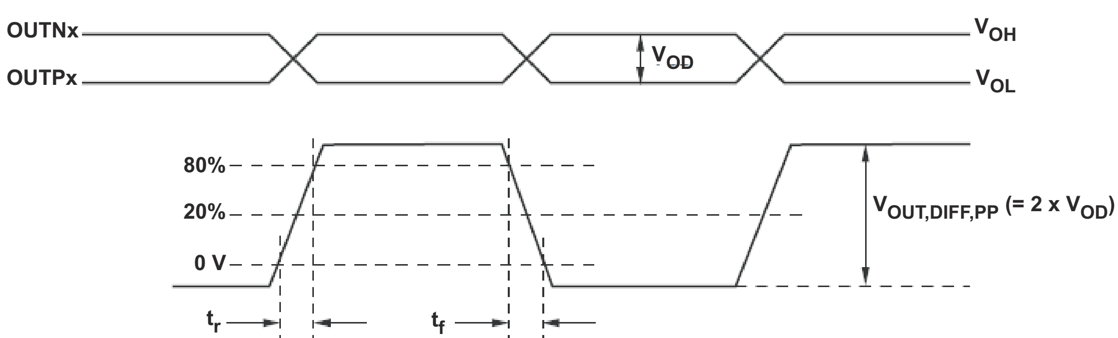
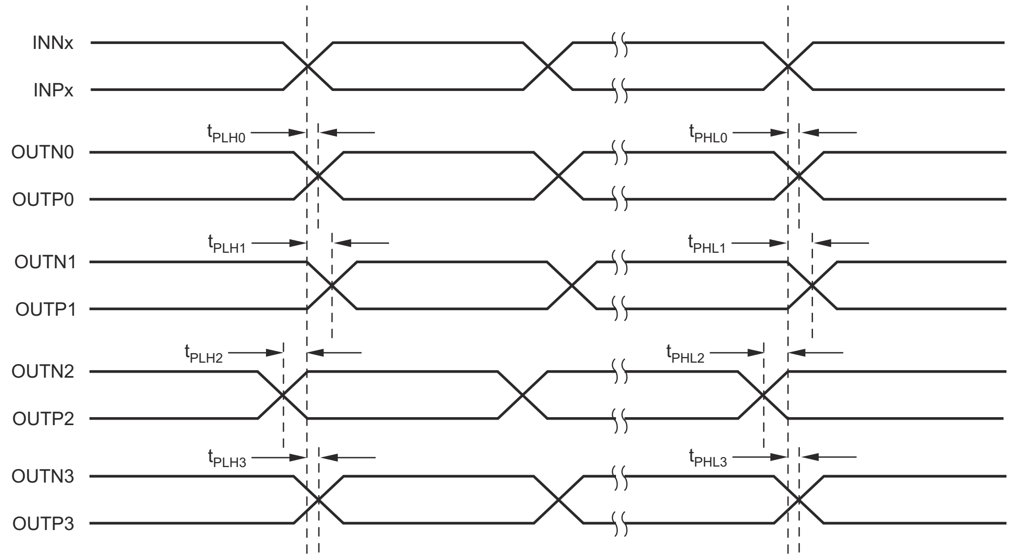


Figure 6-4. Output Voltage and Rise/Fall Time



1. Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1, 2, 3).
2. Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} across multiple devices (n = 0, 1, 2, 3).

Figure 6-5. Output Skew and Part-to-Part Skew

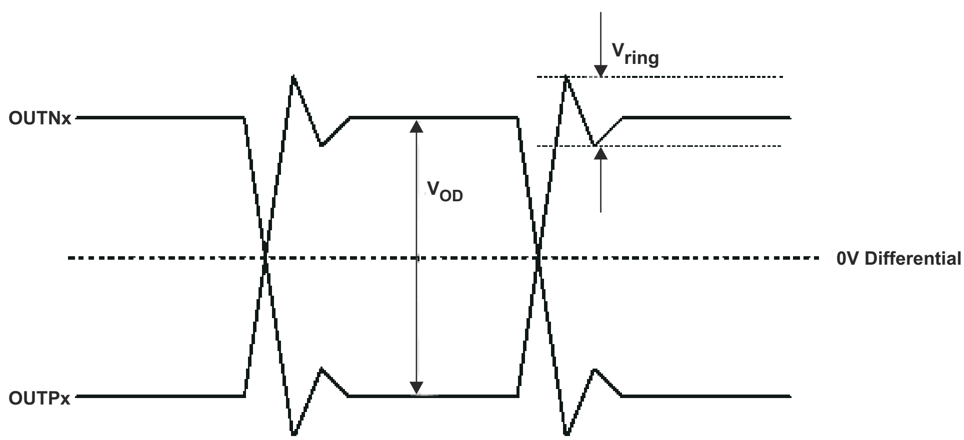


Figure 6-6. Output Overshoot and Undershoot

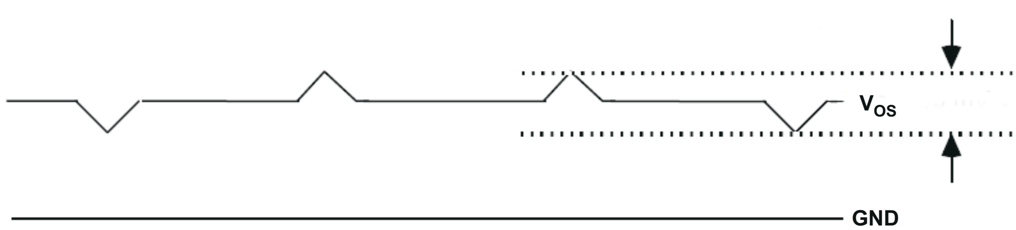


Figure 6-7. Output AC Common Mode

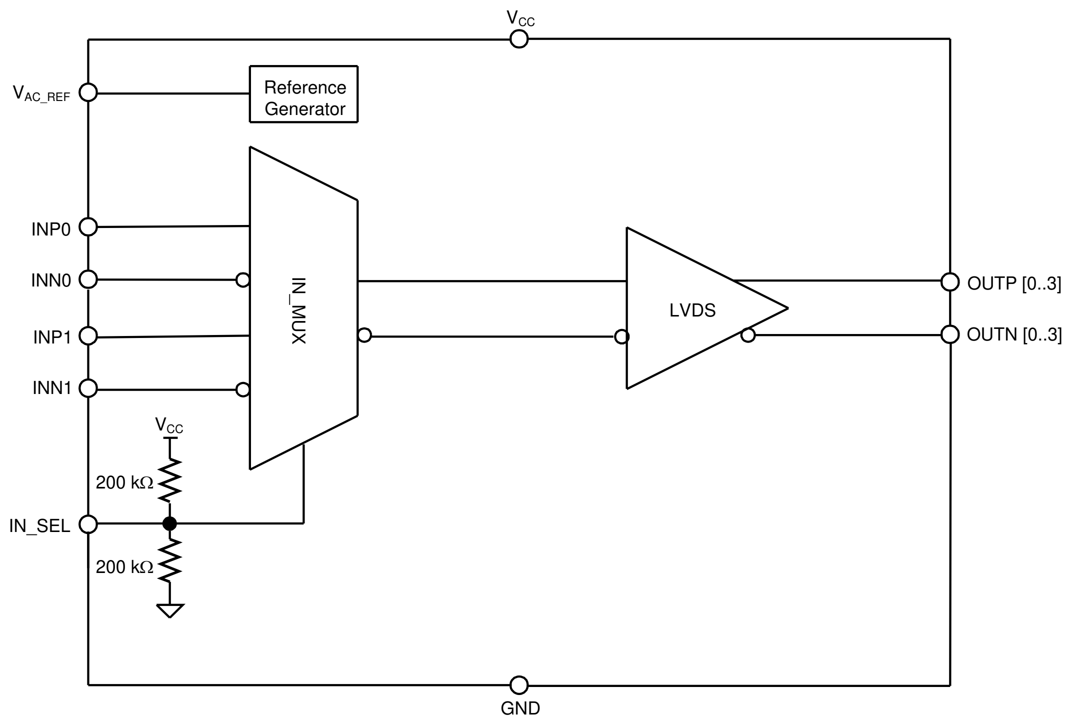
7 Detailed Description

7.1 Overview

The CDCLVD1204 LVDS drivers use CMOS transistors to control the output current. Therefore, proper biasing and termination are required to ensure correct operation of the device and to maximize signal integrity.

The proper LVDS termination for signal integrity over two 50-Ω lines is 100 Ω between the outputs on the receiver end. Either DC-coupled termination or AC-coupled termination can be used for LVDS outputs. TI recommends placing a termination resistor close to the receiver. If the receiver is internally biased to a voltage different than the output common mode voltage of the CDCLVD1204, AC-coupling must be used. If the LVDS receiver has internal 100-Ω termination, external termination must be omitted.

7.2 Functional Block Diagram



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7.3 Feature Description

The CDCLVD1204 is a low additive jitter LVDS fan-out buffer that can generate four copies of two selectable LVPECL, LVDS, or LVCMOS inputs. The CDCLVD1204 can accept reference clock frequencies up to 800 MHz while providing low output skew.

7.4 Device Functional Modes

The two inputs of the CDCLVD1204 are internally muxed together and can be selected through the control pin (see Table 7-1). Unused inputs and outputs can be left floating to reduce overall component cost. Both AC- and DC-coupling schemes can be used with the CDCLVD1204 to provide greater system flexibility.

Table 7-1. Input Selection Table

IN_SEL	ACTIVE CLOCK INPUT
0	INP0, INN0
1	INP1, INN1
Open	None(1)

(1) The input buffers are disabled and the outputs are static.

7.4.1 LVDS Output Termination

Unused outputs can be left open without connecting any trace to the output pins.

The CDCLVD1204 can be connected to LVDS receiver inputs with DC- and AC-coupling as shown in Figure 7-1 and Figure 7-2 (respectively).

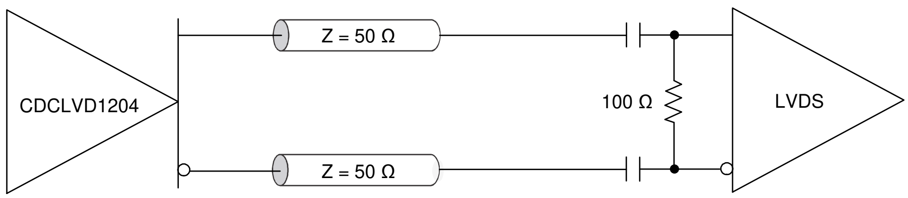


Figure 7-1. Output DC Termination

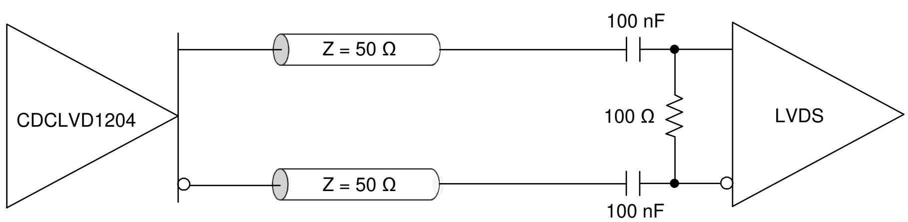


Figure 7-2. Output AC Termination (With the Receiver Internally Biased)

7.4.2 Input Termination

The CDCLVD1204 inputs can be interfaced with LVDS, LVPECL, or LVCMOS drivers.

LVDS drivers can be connected to CDCLVD1204 inputs with AC- and DC-coupling as shown in Figure 7-3 and Figure 7-4 (respectively).

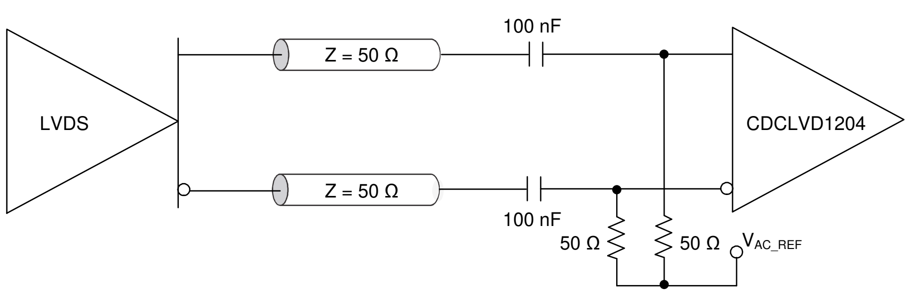


Figure 7-3. LVDS Clock Driver Connected to CDCLVD1204 Input (AC-Coupled)

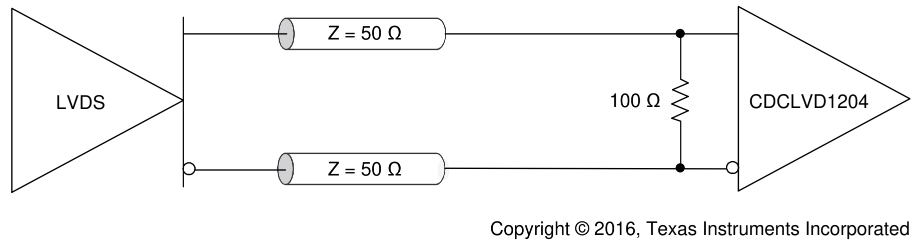


Figure 7-4. LVDS Clock Driver Connected to CDCLVD1204 Input (DC-Coupled)

Figure 7-5 shows how to connect LVPECL inputs to the CDCLVD1204. The series resistors are required to reduce the LVPECL signal swing if the signal swing is >1.6 Vpp.

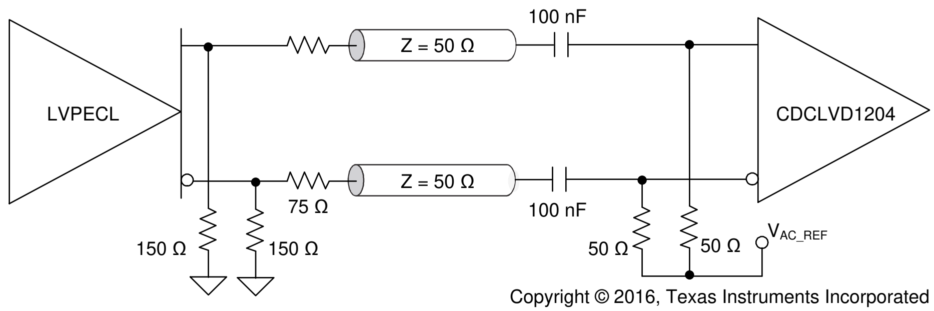


Figure 7-5. LVPECL Clock Driver Connected to CDCLVD1204 Input

Figure 7-6 illustrates how to couple a 2.5-V LVCMOS clock input to the CDCLVD1204 directly. The series resistance, R_S, must be placed close to the LVCMOS driver if required. 3.3-V LVCMOS clock input swing must be limited to $V_{IH} \le V_{CC}$.

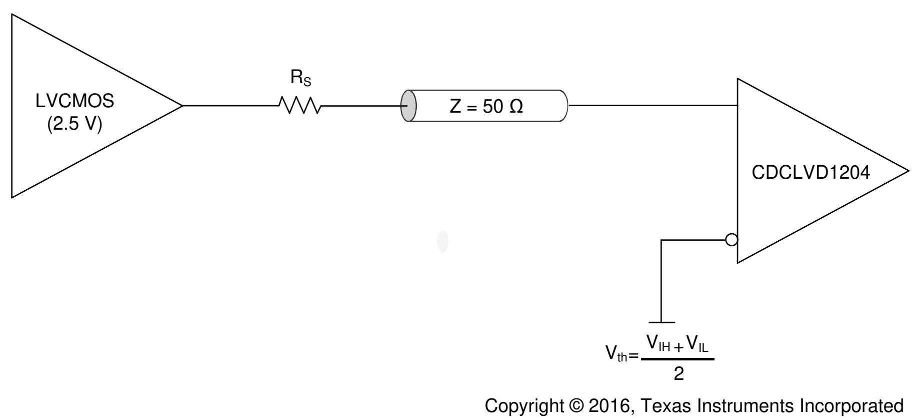


Figure 7-6. 2.5-V LVCMOS Clock Driver Connected to CDCLVD1204 Input

For unused input, TI recommends grounding both input pins (INP, INN) using 1-kΩ resistors.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The CDCLVD1204 is a low additive jitter universal to LVDS fan-out buffer with 2 selectable inputs. The small package, low output skew, and low additive jitter make for a flexible device in demanding applications.

8.2 Typical Application

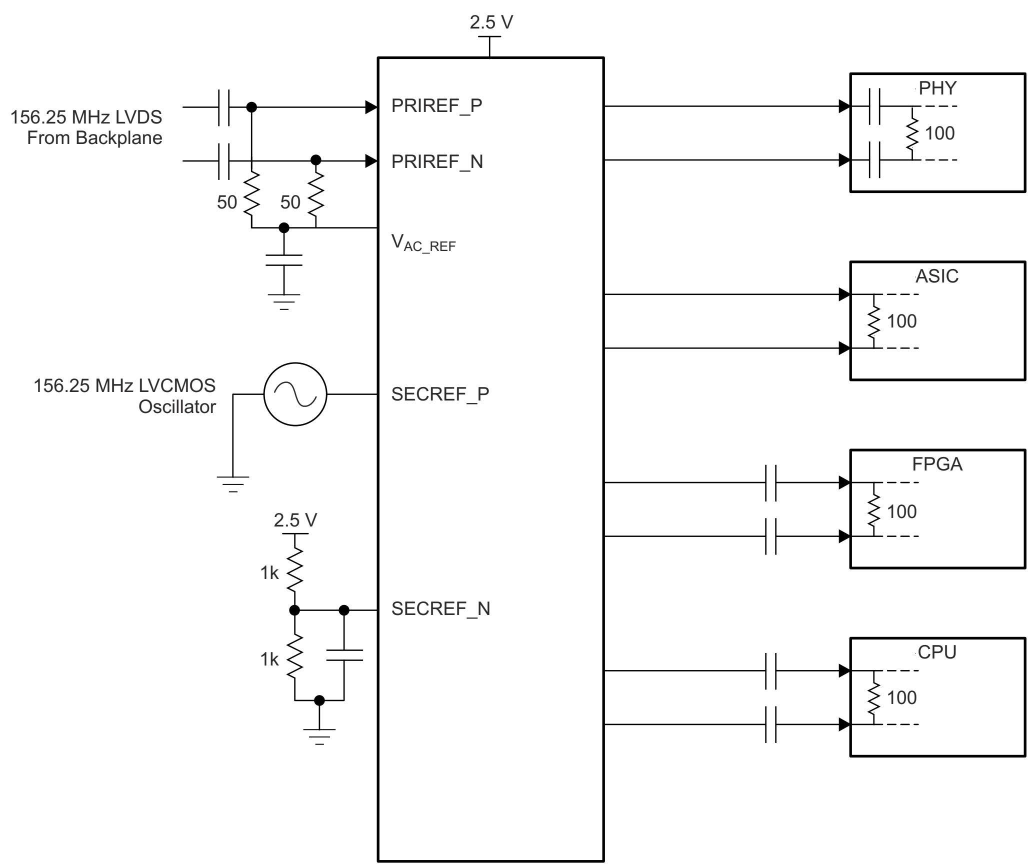


Figure 8-1. Fan-Out Buffer for Line Card Application

8.2.1 Design Requirements

The CDCLVD1204 shown in Figure 8-1 is configured to select two inputs: a 156.25-MHz LVDS clock from the backplane, or a secondary 156.25-MHz LVCMOS 2.5-V oscillator. The LVDS clock is AC-coupled and biased using the integrated reference voltage generator. A resistor divider is used to set the threshold voltage correctly for the LVCMOS clock. 0.1-µF capacitors are used to reduce noise on both V_{AC_REF} and SECREF_N. Either input signal can be then fanned out to desired devices, as shown. The configuration example is driving 4 LVDS receivers in a line card application with the following properties:

- The PHY device is capable of DC-coupling with an LVDS driver such as the CDCLVD1204. This PHY device features internal termination so no additional components are required for proper operation.
- The ASIC LVDS receiver features internal termination and operates at the same common mode voltage as the CDCLVD1204. Again, no additional components are required.
- The FPGA requires external AC-coupling, but has internal termination. 0.1-µF capacitors are placed to provide AC-coupling. Similarly, the CPU is internally terminated, and requires only external AC-coupling capacitors.

8.2.2 Detailed Design Procedure

See *Input Termination* for proper input terminations, dependent on single ended or differential inputs.

See *LVDS Output Termination* for output termination schemes depending on the receiver application.

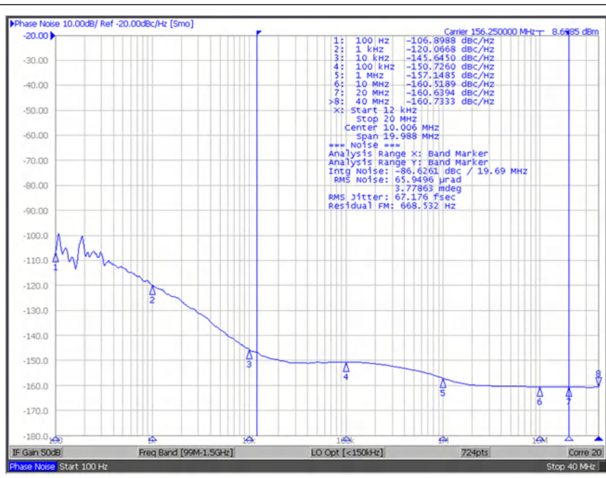
Unused outputs can be left floating.

In this example, the PHY, ASIC, and FPGA or CPU require different schemes. Power supply filtering and bypassing is critical for low-noise applications.

See *Power Supply Recommendations* for recommended filtering techniques. A reference layout is provided in *Low-Additive Jitter, Four LVDS Outputs Clock Buffer Evaluation Board* (SCAU043).

8.2.3 Application Curves

The CDCLVD12xx's low additive noise is shown in this line card application. The low noise 156.25 MHz source with 67 fs RMS jitter drives the CDCLVD12xx, resulting in 80 fs RMS when integrated from 12 kHz to 20 MHz. The resultant additive jitter is a low 44 fs RMS for this configuration.



Reference signal is low-noise Rohde & Schwarz SMA100A

Figure 8-2. CDCLVD12xx Reference Phase Noise, 67 fs rms (12 kHz to 20 MHz)

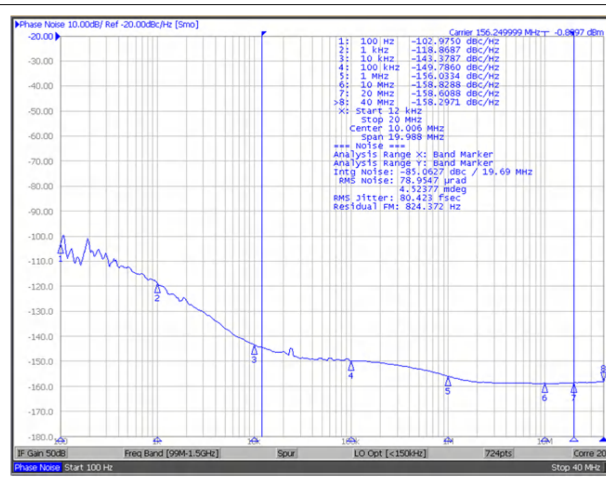


Figure 8-3. CDCLVD12xx Output Phase Noise, 80 fs rms (12 kHz to 20 MHz)

9 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and must have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed close to the power-supply pins and laid out with short loops to minimize inductance. It is recommended to add as many high-frequency (for example, 0.1 µF) bypass capacitors as there are supply pins in the package. It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with low DC-resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

Figure 9-1 shows this recommended power-supply decoupling method.

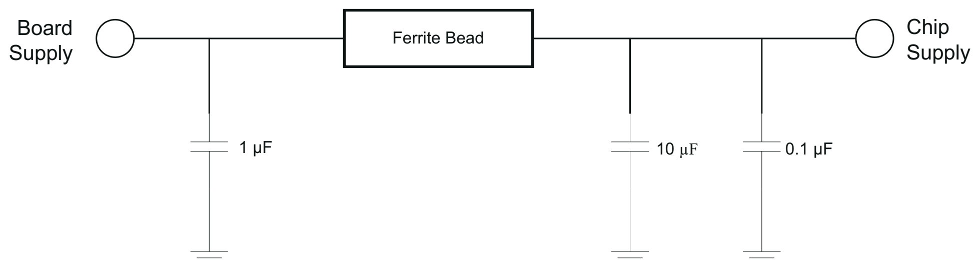


Figure 9-1. Power-Supply Decoupling

10 Layout

10.1 Layout Guidelines

For reliability and performance reasons, the die temperature must be limited to a maximum of 125°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The thermal pad must be soldered down to ensure adequate heat conduction to of the package. Figure 10-1 shows a recommended land and via pattern.

10.2 Layout Example

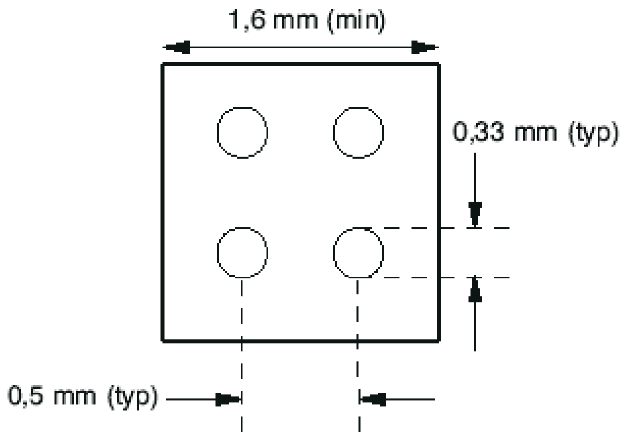


Figure 10-1. Recommended PCB Layout

10.3 Thermal Considerations

The CDCLVD1204 supports high temperatures on the printed circuit board (PCB) measured at the thermal pad. The system designer must ensure that the maximum junction temperature is not exceeded. Ψ_{JB} can allow the system designer to measure the board temperature with a fine gauge thermocouple and back calculate the junction temperature using Equation 1. Note that Ψ_{JB} is close to $R_{\theta JB}$ as 75% to 95% of a device's heat is dissipated by the PCB.

$$T_J = T_{PCB} + (\Psi_{JB} \times Power) \quad (1)$$

Example:

Calculation of the junction-lead temperature with a 4-layer JEDEC test board using four thermal vias:

T_{PCB} = 105°C

Ψ_{JB} = 19.4°C/W

$Power_{inclTerm} = I_{max} \times V_{max}$ = 80 mA × 2.625 V = 210 mW (maximum power consumption including termination resistors)

$Power_{exclTerm}$ = 202 mW (maximum power consumption excluding termination resistors, see *Power Consumption of LVPECL and LVDS* (SLYT127) for further details)

$\Delta T_J = \Psi_{JB} \times Power_{exclTerm}$ = 19.4°C/W × 202 mW = 3.92°C

$T_J = \Delta T_J + T_{Chassis}$ = 3.92°C + 105°C = 108.92°C (maximum junction temperature of 125°C is not violated)

Further information can be found at *Semiconductor and IC Package Thermal Metrics* (SPRA953) and *Using Thermal Calculation Tools for Analog Components* (SLUA566).

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Low-Additive Jitter, Four LVDS Outputs Clock Buffer Evaluation Board* (SCAU043)
- *Power Consumption of LVPECL and LVDS* (SLYT127)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- *Using Thermal Calculation Tools for Analog Components* (SLUA566)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2016) to Revision C (May 2026) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1

Changes from Revision A (June 2010) to Revision B (October 2016) — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section................... 1

Changes from Revision * (May 2010) to Revision A (June 2010) **Page**

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDCLVD1204RGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D1204
CDCLVD1204RGTR.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D1204
CDCLVD1204RGTT	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D1204
CDCLVD1204RGTT.A	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D1204
CDCLVD1204RGTTG4	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D1204
CDCLVD1204RGTTG4.A	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D1204

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

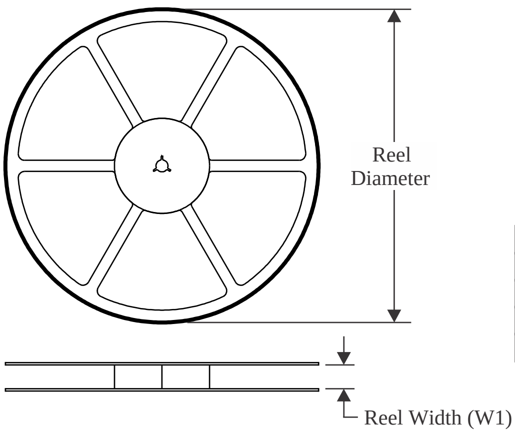
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

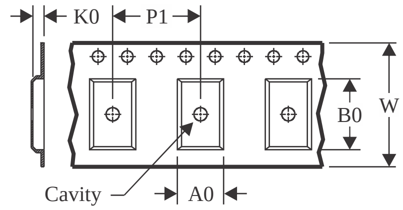
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

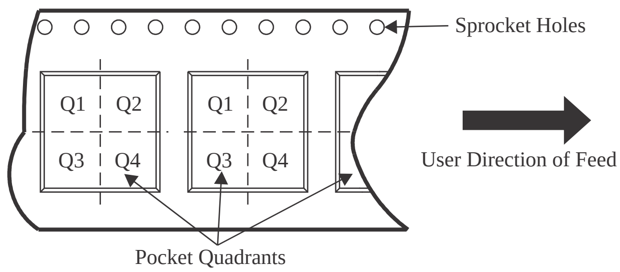


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

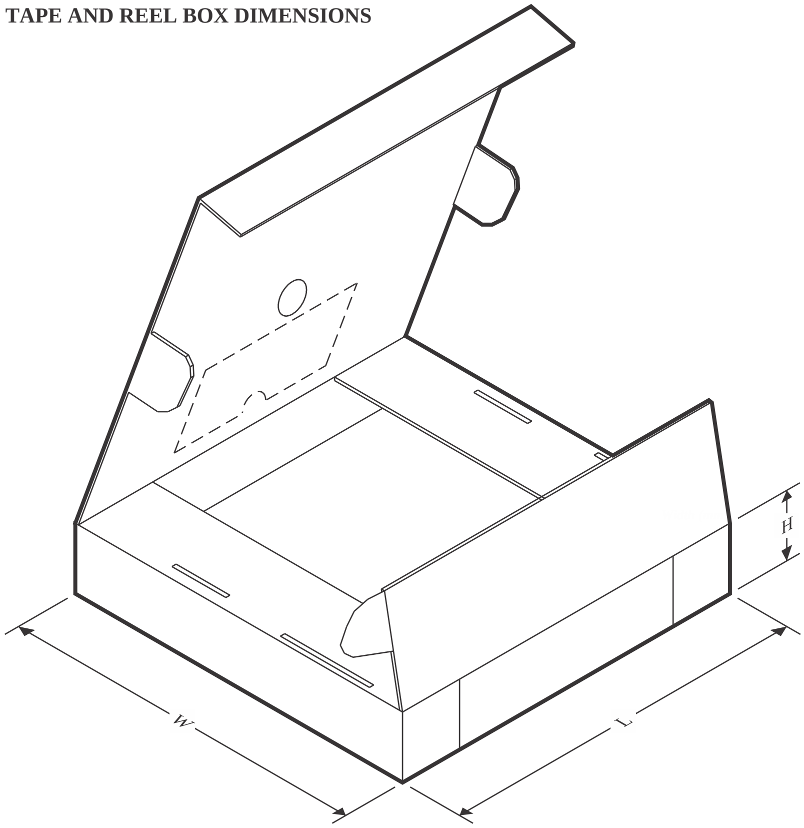
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVD1204RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
CDCLVD1204RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
CDCLVD1204RGTTG4	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

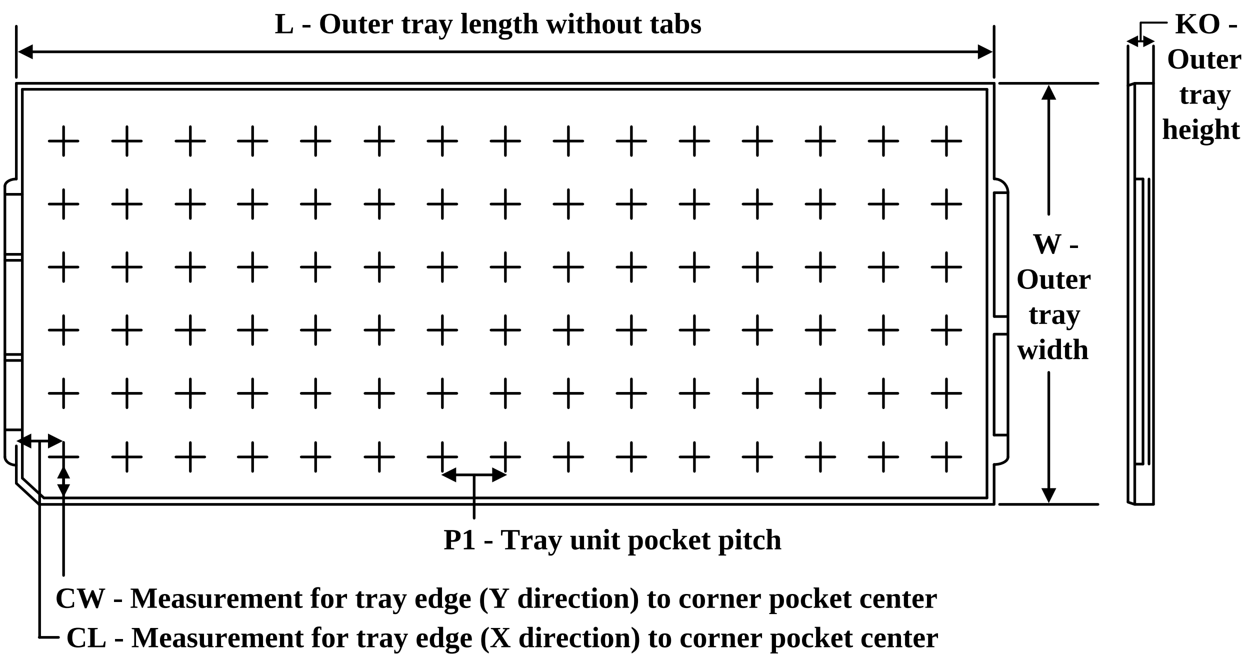
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVD1204RGTR	VQFN	RGT	16	3000	350.0	350.0	43.0
CDCLVD1204RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
CDCLVD1204RGTTG4	VQFN	RGT	16	250	210.0	185.0	35.0

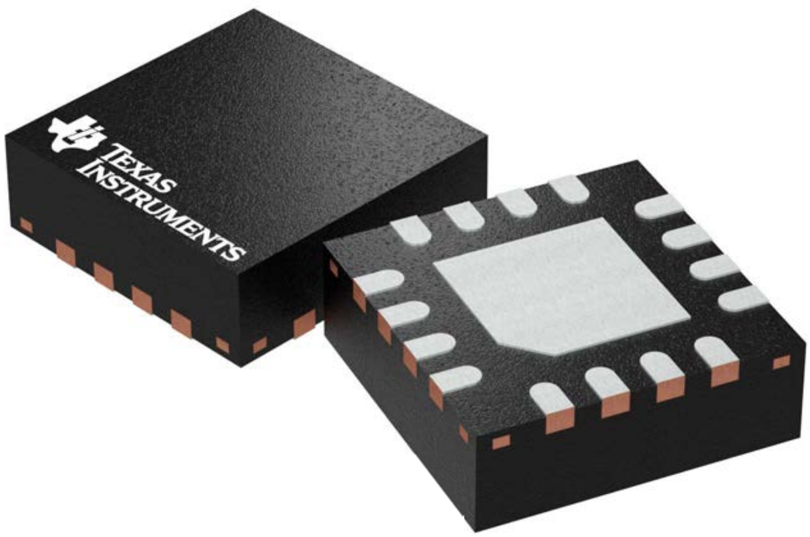
TRAY



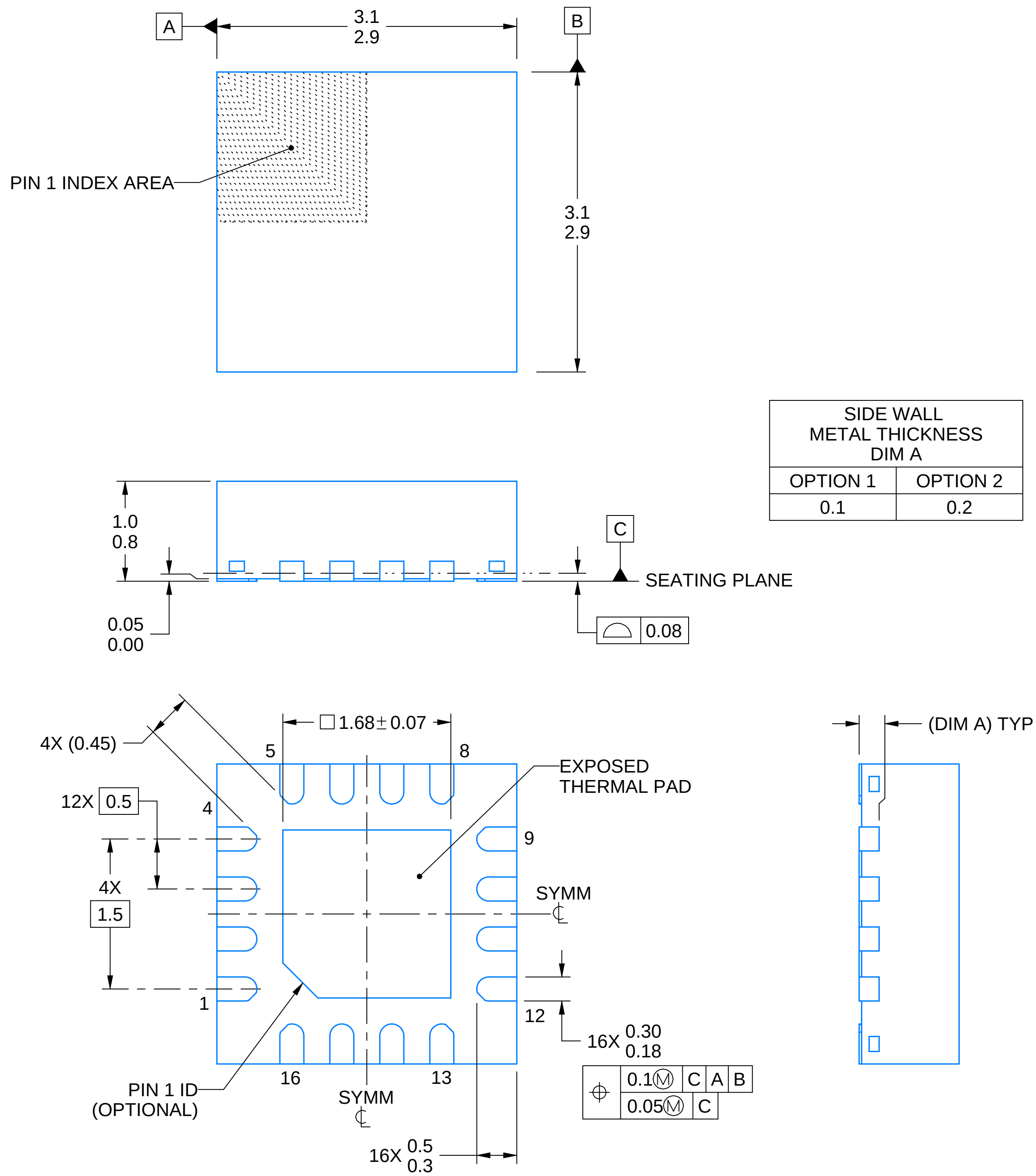
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
CDCLVD1204RGTR	RGT	VQFN	16	3000	35 X 14	150	315	135.9	7620	8.8	7.9	8.15
CDCLVD1204RGTR.A	RGT	VQFN	16	3000	35 X 14	150	315	135.9	7620	8.8	7.9	8.15
CDCLVD1204RGTT	RGT	VQFN	16	250	35 X 14	150	315	135.9	7620	8.8	7.9	8.15
CDCLVD1204RGTT.A	RGT	VQFN	16	250	35 X 14	150	315	135.9	7620	8.8	7.9	8.15



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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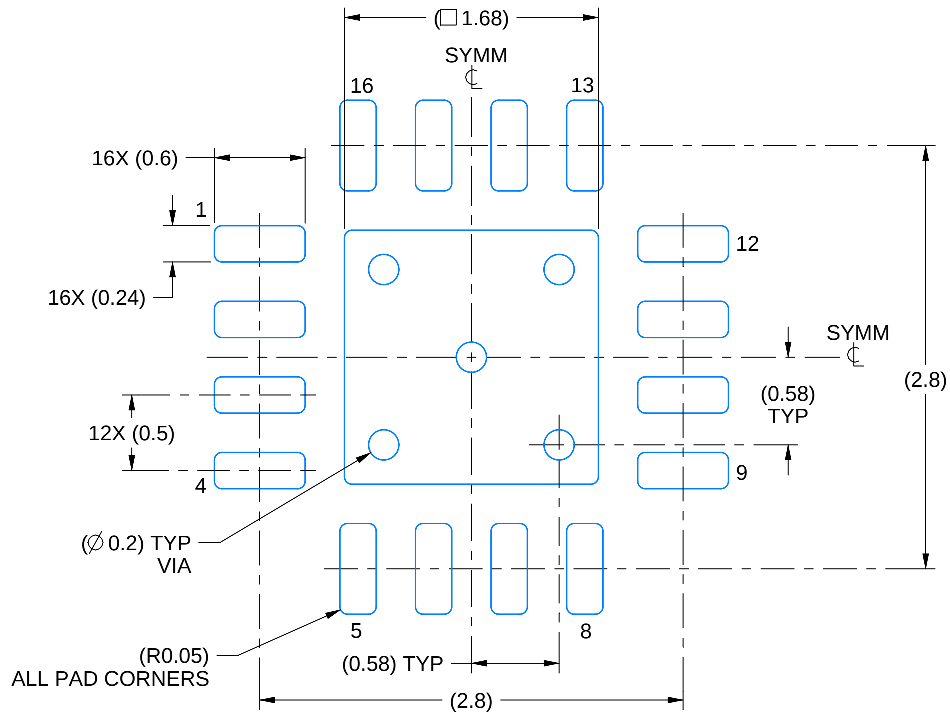
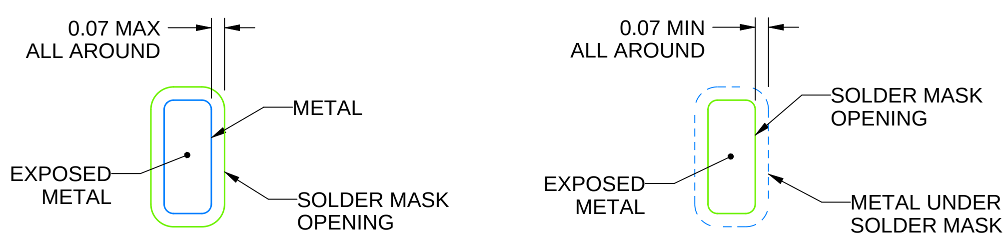
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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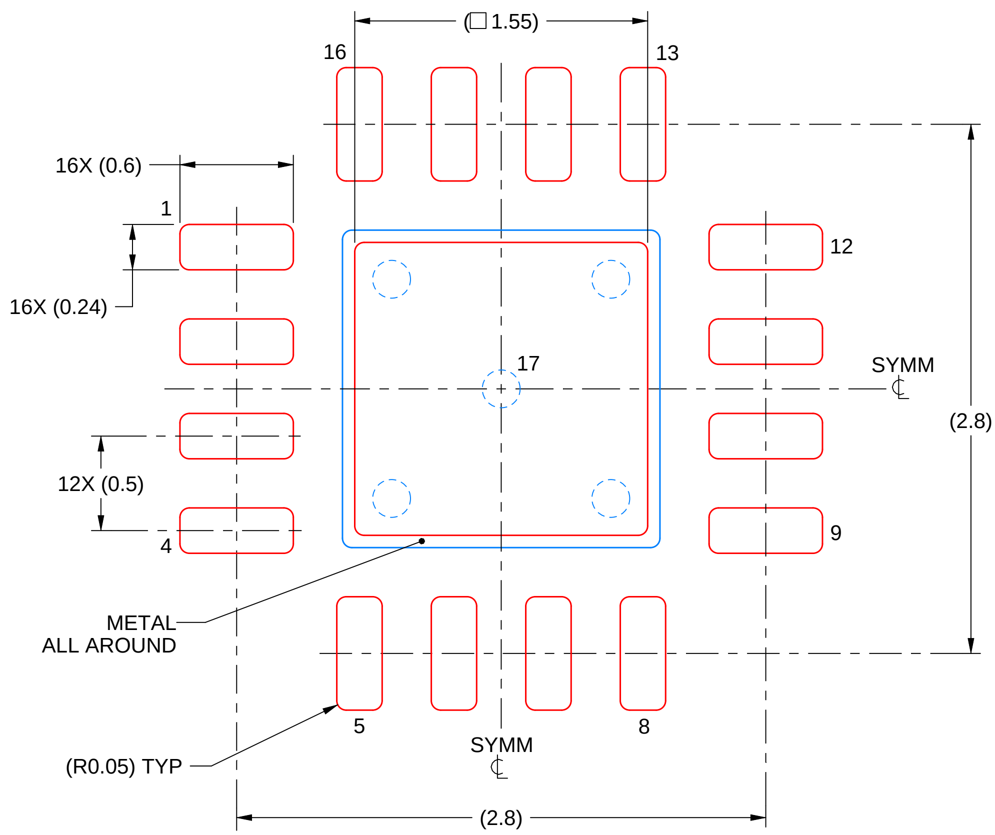
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.