CSD13380F3 12V N 沟道 FemtoFET™ MOSFET

1 特性

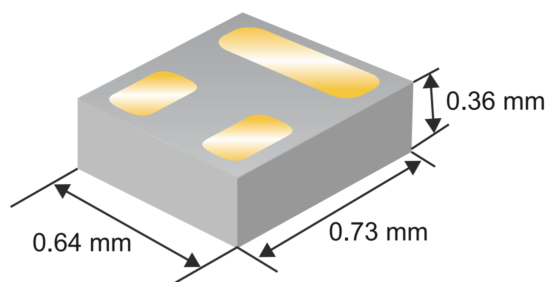
- 低导通电阻
- 超低 Q_g 和 Q_{gd}
- 高漏极工作电流
- 超小尺寸
  - 0.73mm × 0.64mm
- 薄型封装
  - 最大厚度为 0.36mm
- 集成型 ESD 保护二极管
  - 额定值 > 3kV 人体放电模型 (HBM)
  - 额定值 > 2kV 充电器件模型 (CDM)
- 无铅且无卤素
- 符合 RoHS

2 应用

- 针对负载开关应用进行了优化
- 针对通用开关应用进行了优化
- 电池应用
- 手持式和移动类应用

3 说明

该 63mΩ、12V N 沟道 FemtoFET™ MOSFET 经过设计和优化，能够最大限度地减小在许多手持式和移动应用中占用的空间。这项技术能够在替代标准小信号 MOSFET 的同时大幅减小封装尺寸。



典型器件尺寸

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	12		V
Q_g	栅极电荷总量 (4.5V)	0.91		nC
Q_{gd}	栅极电荷（栅极到漏极）	0.15		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 1.8V	96	mΩ
		V_{GS} = 2.5V	73	
		V_{GS} = 4.5V	63	
$V_{GS(th)}$	阈值电压	0.85		V

器件信息(1)

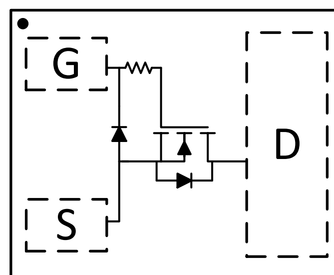
器件	数量	介质	封装	配送
CSD13380F3	3000	7 英寸卷带	Femto 0.73mm × 0.64mm 基板栅格阵列 (LGA)	卷带包装
CSD13380F3T	250			

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

T_A = 25°C（除非另外注明）		值	单位
V_{DS}	漏源电压	12	V
V_{GS}	栅源电压	8	V
I_D	持续漏极电流(1)	3.6	A
	持续漏极电流(2)	2.1	
I_{DM}	脉冲漏极电流(2) (3)	13.5	A
P_D	功率耗散(1)	1.4	W
	功率耗散(2)	0.5	
$V_{(ESD)}$	人体放电模型 (HBM)	3	kV
	充电器件模型 (CDM)	2	
T_J、T_{stg}	工作结温、贮存温度	–55 至 150	°C

(1) 覆铜面积最大时的典型 $R_{\theta JA}$ = 90°C/W（在 0.06 英寸 (1.52mm) 厚的 FR4 PCB 上安装 1 平方英寸 (6.45cm²)、2oz、0.071mm 厚的铜焊盘时）
(2) 覆铜面积最小时的典型 $R_{\theta JA}$ = 255°C/W。
(3) 脉冲持续时间 ≤ 100μs，占空比 ≤ 1%。



顶视图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。
English Data Sheet: SLPS593

Table of Contents

1 特性.......... 1
2 应用.......... 1
3 说明.......... 1
4 Revision History.......... 2
5 Specifications.......... 3
  5.1 Electrical Characteristics.......... 3
  5.2 Thermal Information.......... 3
  5.3 Typical MOSFET Characteristics.......... 4
6 Device and Documentation Support.......... 7
  6.1 Receiving Notification of Documentation Updates.......... 7
  6.2 Trademarks.......... 7
7 Mechanical, Packaging, and Orderable Information.......... 8
  7.1 Mechanical Dimensions.......... 8
  7.2 Recommended Minimum PCB Layout.......... 9
  7.3 Recommended Stencil Pattern.......... 9

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (October 2016) to Revision A (February 2022) **Page**

- 将超薄型封装要点中的厚度从 0.35mm 更改为 0.36mm.......... 1
- 将超薄型封装图片中的厚度从 0.35mm 更新为 0.36mm.......... 1
- Changed ultra-low profile image height from 0.35 mm to 0.36 mm.......... 8
- Added FemtoFET Surface Mount Guide note.......... 9

Copyright © 2022 Texas Instruments Incorporated

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 μA	12			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 9.6 V			50	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 8 V			25	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	0.55	0.85	1.30	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 1.8 V, I_{DS} = 0.1 A		96	135	mΩ
		V_{GS} = 2.5 V, I_{DS} = 0.4 A		73	92	
		V_{GS} = 4.5 V, I_{DS} = 0.4 A		63	76	
g_{fs}	Transconductance	V_{DS} = 1.2 V, I_{DS} = 0.4 A		4.3		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 6 V, *f* = 1 MHz		120	156	pF
C_{oss}	Output capacitance			81	105	pF
C_{rss}	Reverse transfer capacitance			9.6	12.5	pF
R_G	Series gate resistance			16		Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 6 V, I_{DS} = 0.4 A		0.91	1.2	nC
Q_{gd}	Gate charge gate-to-drain			0.15		nC
Q_{gs}	Gate charge gate-to-source			0.19		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.15		nC
Q_{oss}	Output charge	V_{DS} = 6 V, V_{GS} = 0 V		0.81		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 6 V, V_{GS} = 4.5 V, I_{DS} = 0.4 A, R_G = 2 Ω		4		ns
t_r	Rise time			4		ns
$t_{d(off)}$	Turnoff delay time			11		ns
t_f	Fall time			3		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 0.4 A, V_{GS} = 0 V		0.71	1	V
Q_{rr}	Reverse recovery charge	V_{DS}= 6 V, I_F = 0.4 A, di/dt = 100 A/μs		2.1		nC
t_{rr}	Reverse recovery time			8		ns

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)		90		°C/W
	Junction-to-ambient thermal resistance(2)		255		

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

Copyright © 2022 Texas Instruments Incorporated

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

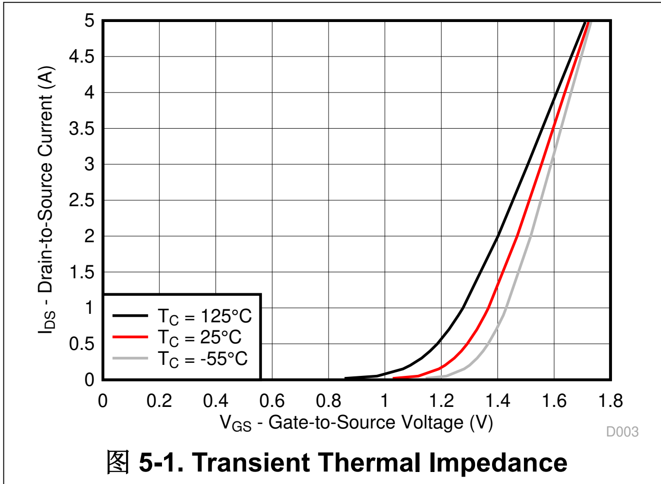


图 5-1. Transient Thermal Impedance

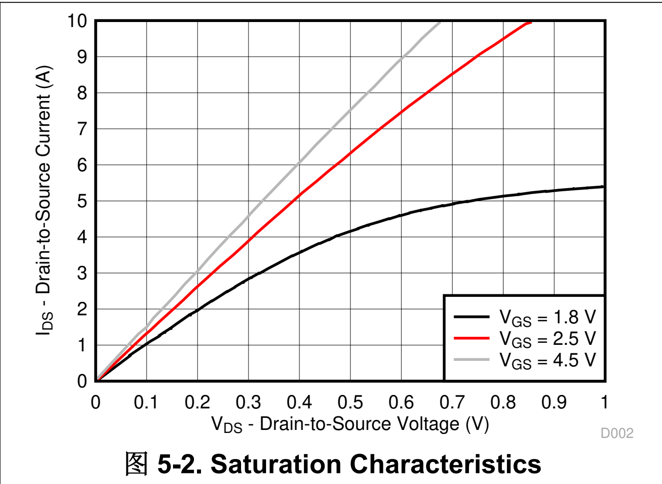
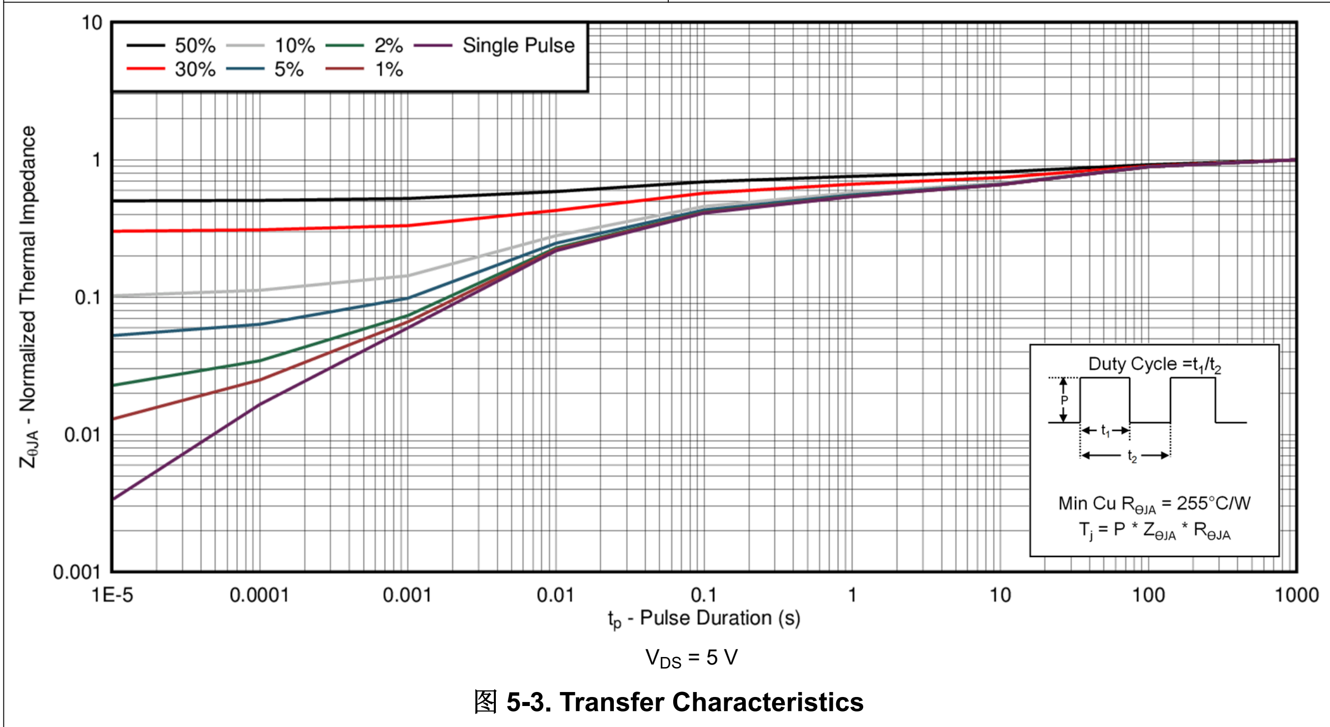


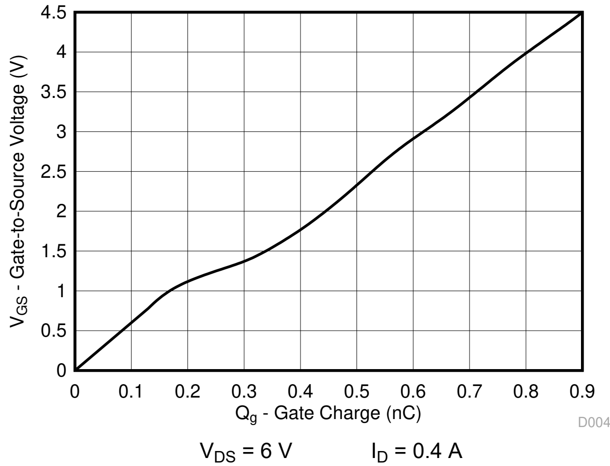
图 5-2. Saturation Characteristics



V_{DS} = 5 V

图 5-3. Transfer Characteristics

Copyright © 2022 Texas Instruments Incorporated



V_{DS} = 6 V　　I_D = 0.4 A

图 5-4. Gate Charge

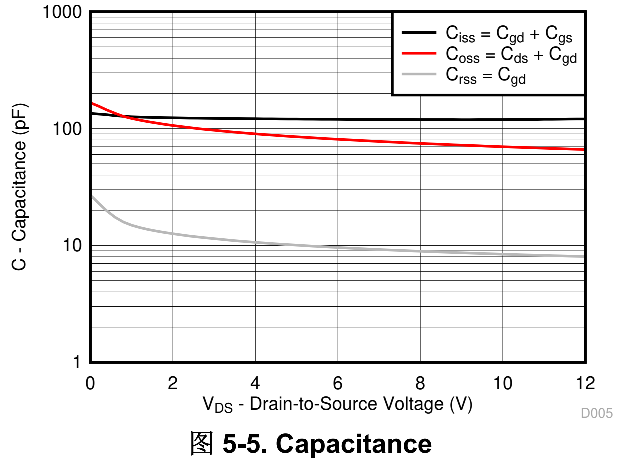
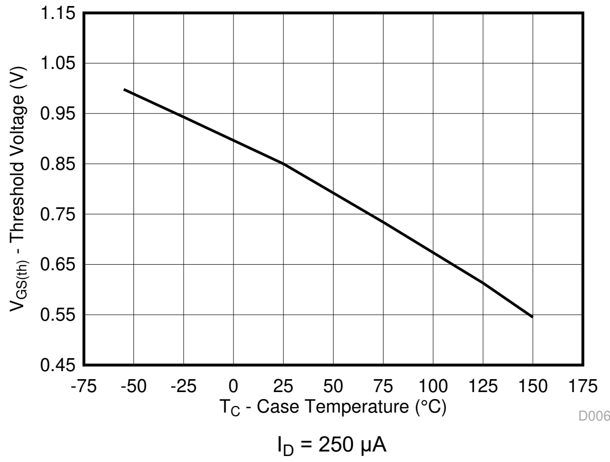


图 5-5. Capacitance



I_D = 250 µA

图 5-6. Threshold Voltage vs Temperature

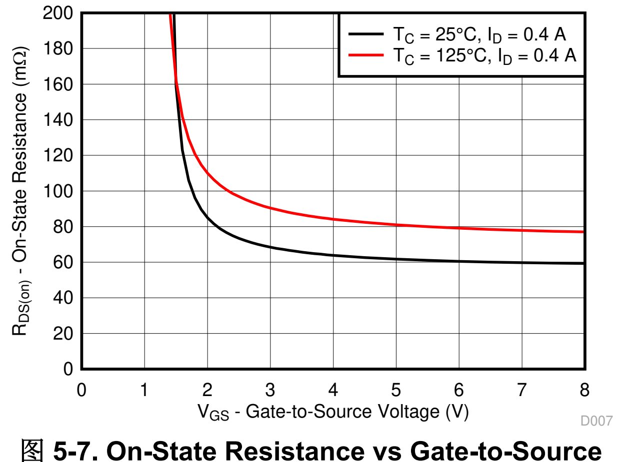
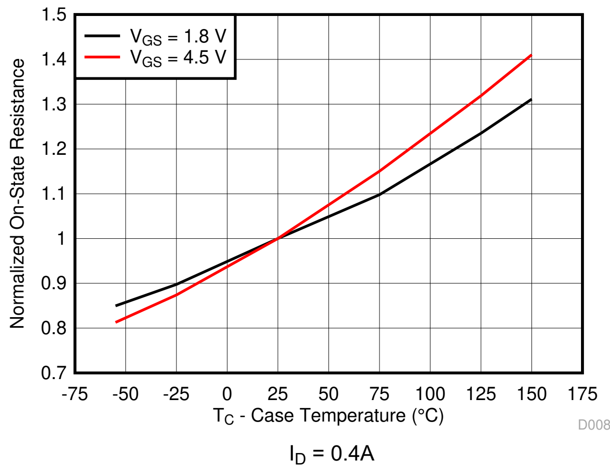


图 5-7. On-State Resistance vs Gate-to-Source Voltage



I_D = 0.4A

图 5-8. Normalized On-State Resistance vs Temperature

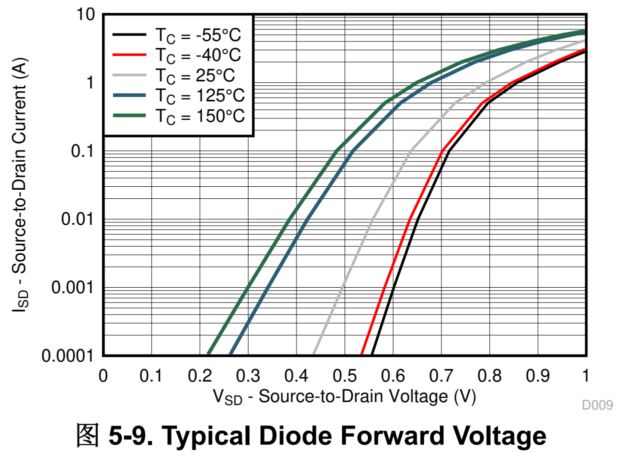
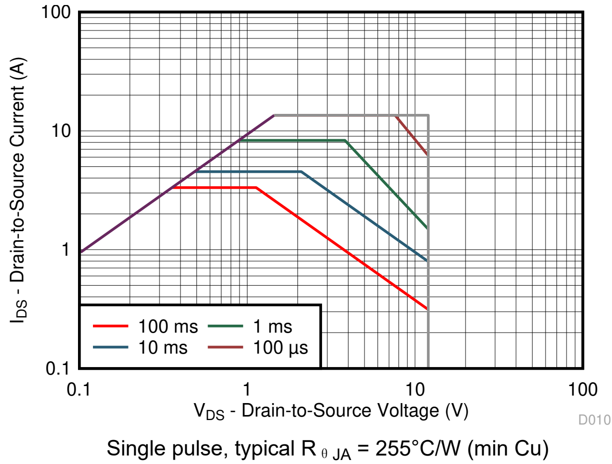


图 5-9. Typical Diode Forward Voltage



Single pulse, typical $R_{\theta JA}$ = 255°C/W (min Cu)

图 5-10. Maximum Safe Operating Area

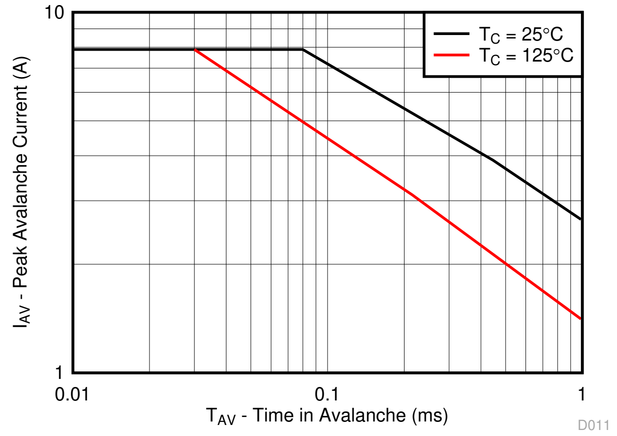
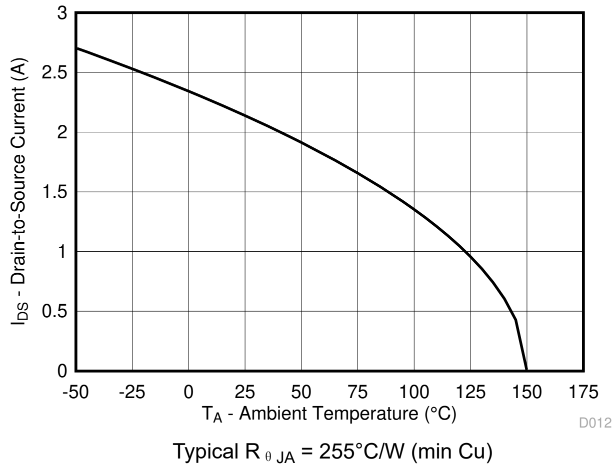


图 5-11. Single Pulse Unclamped Inductive Switching



Typical $R_{\theta JA}$ = 255°C/W (min Cu)

图 5-12. Maximum Drain Current vs Temperature

Copyright © 2022 Texas Instruments Incorporated

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

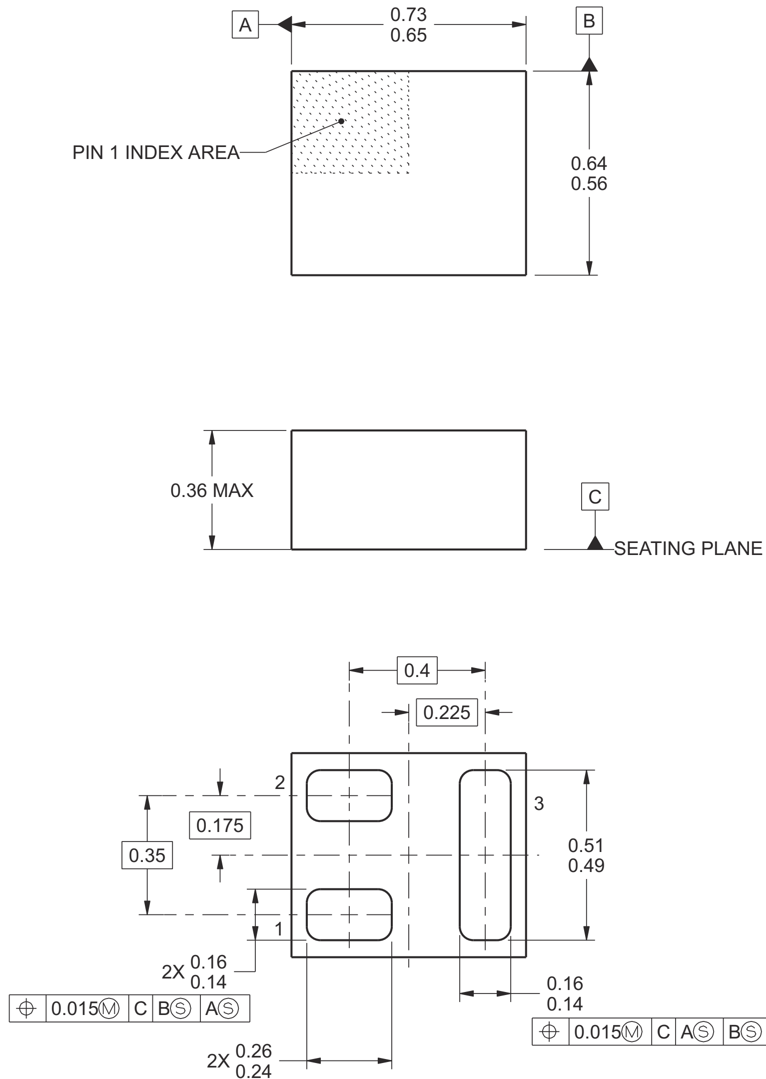
6.2 Trademarks

FemtoFET™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



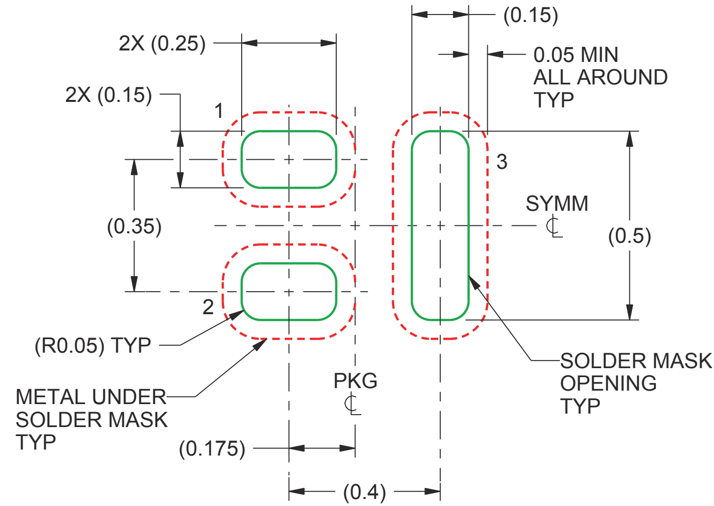
A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
B. This drawing is subject to change without notice.
C. This package is a PB-free solder land design.

表 7-1. Pin Configuration

POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

Copyright © 2022 Texas Instruments Incorporated

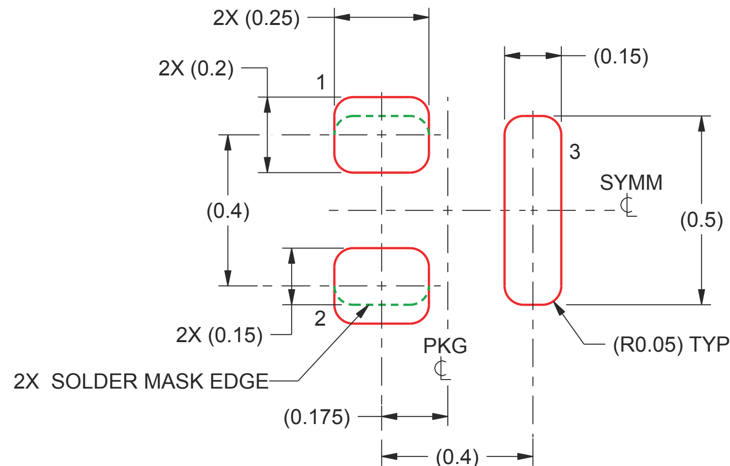
7.2 Recommended Minimum PCB Layout



A. All dimensions are in millimeters.

A. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

7.3 Recommended Stencil Pattern



A. All dimensions are in millimeters.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD13380F3	Active	Production	PICOSTAR (YJM) | 3	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	D
CSD13380F3.B	Active	Production	PICOSTAR (YJM) | 3	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	D
CSD13380F3T	Active	Production	PICOSTAR (YJM) | 3	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	D
CSD13380F3T.B	Active	Production	PICOSTAR (YJM) | 3	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	D

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

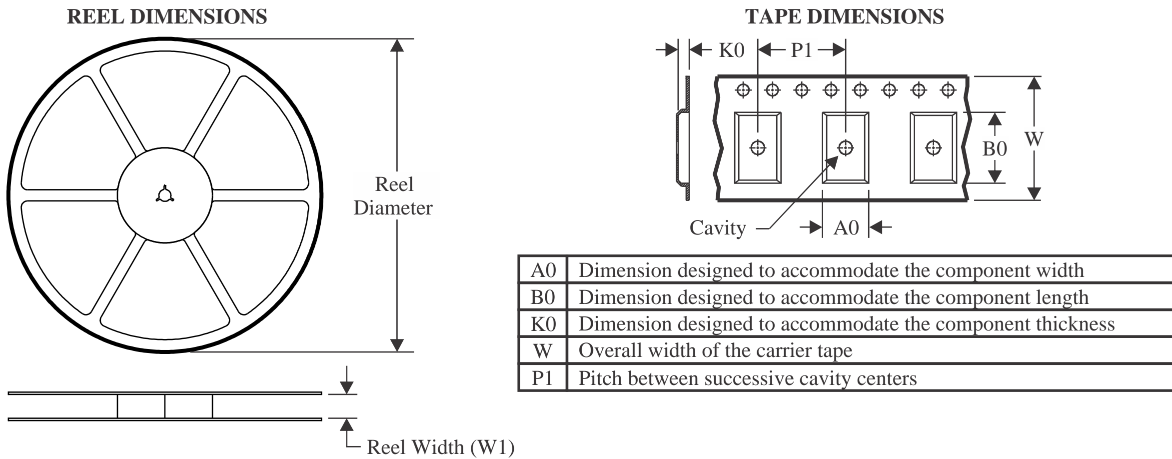
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

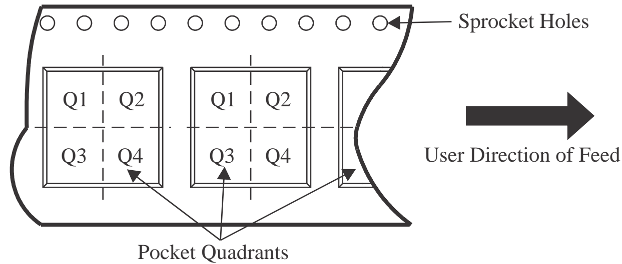
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

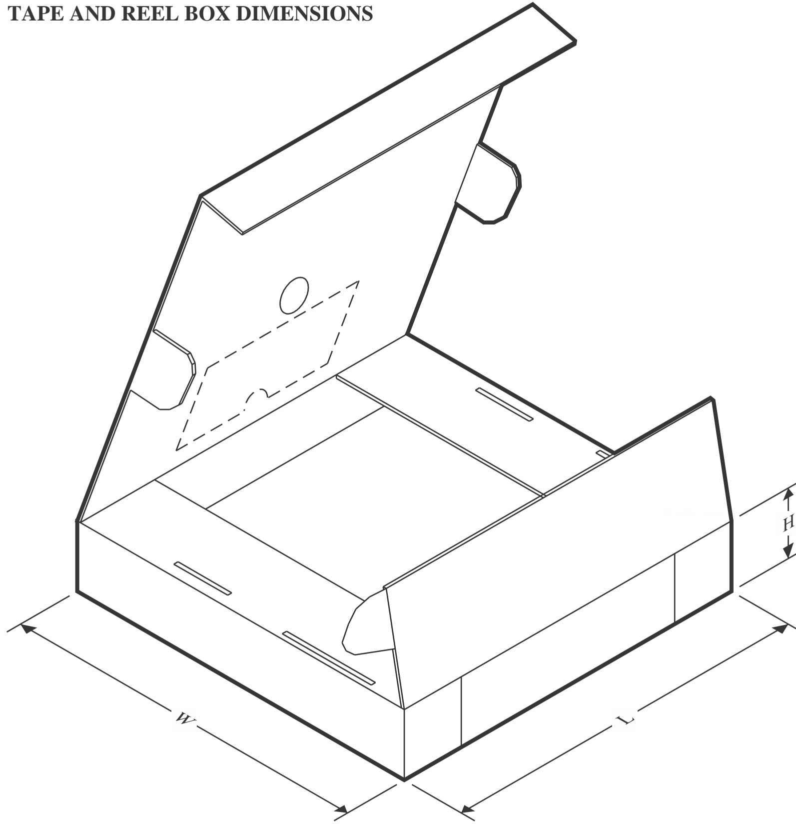
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD13380F3	PICOSTAR	YJM	3	3000	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2
CSD13380F3T	PICOSTAR	YJM	3	250	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



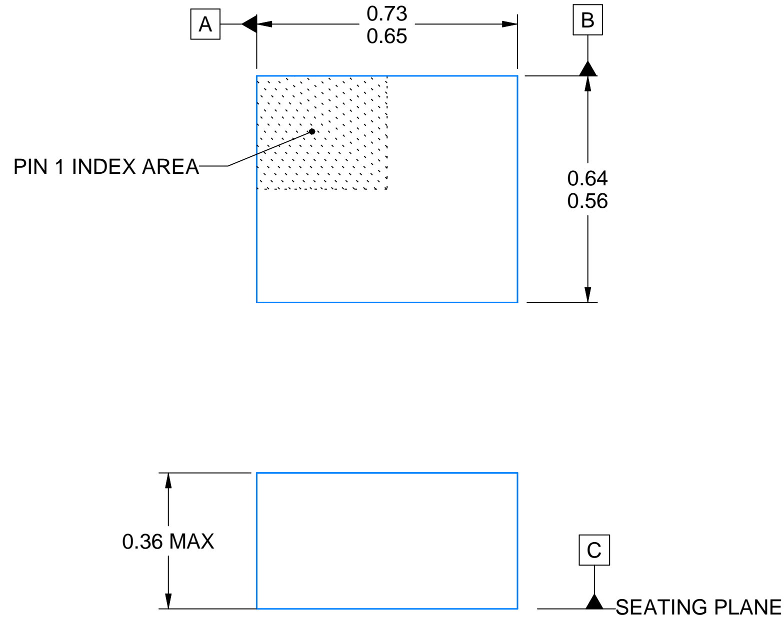
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD13380F3	PICOSTAR	YJM	3	3000	182.0	182.0	20.0
CSD13380F3T	PICOSTAR	YJM	3	250	182.0	182.0	20.0

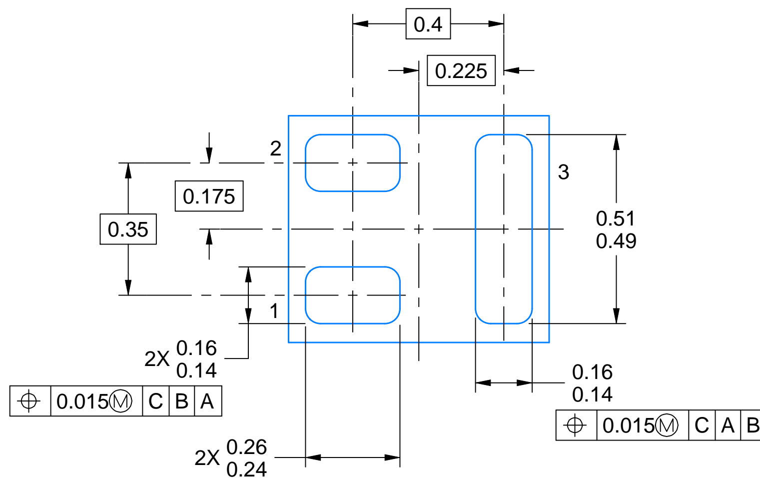
PACKAGE OUTLINE

PicoStar ™ - 0.36 mm max height

PicoStar ™



0.36 MAX
C
SEATING PLANE

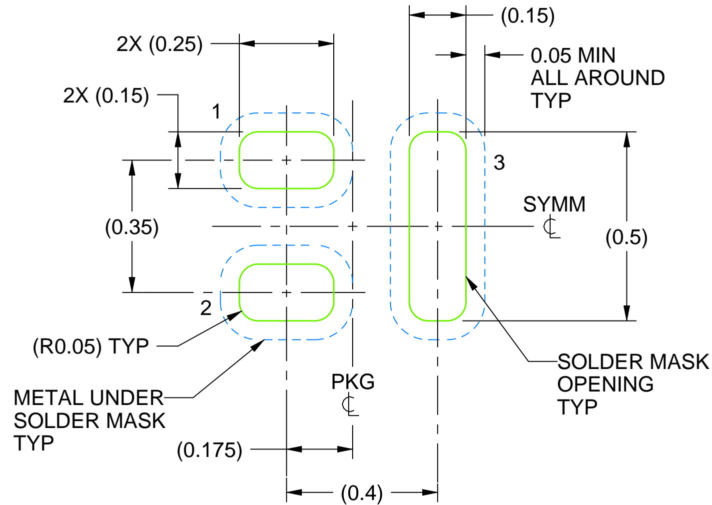


4222304/B 03/2022

NOTES:

PicoStar is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.

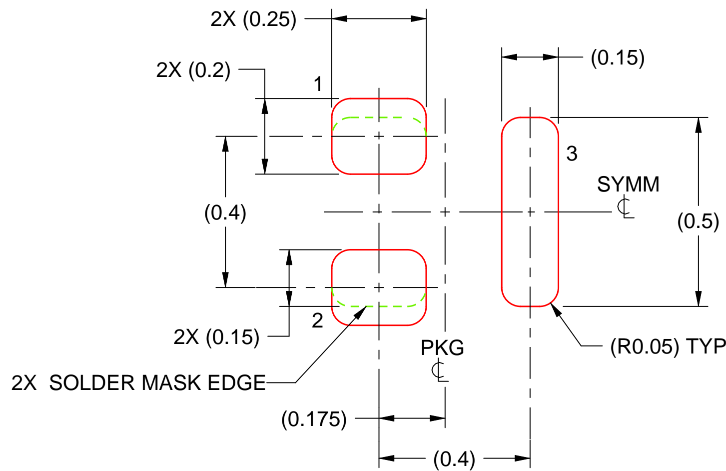


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

4222304/B 03/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:50X

4222304/B 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月