

20V N 通道 NexFET™ 功率金属氧化物场效应晶体管 (MOSFET)

 查询样品: **CSD15571Q2**

特性

- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅端子镀层
- 符合 RoHS 标准
- 无卤素
- 小外形尺寸无引线 (SON) 2mm x 2mm 塑料封装

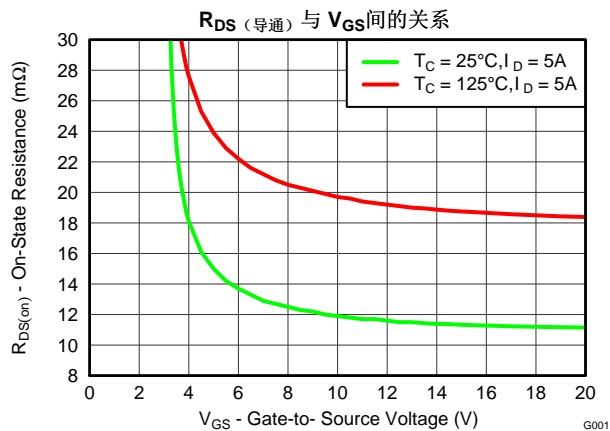
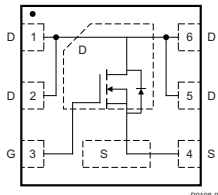
应用范围

- 针对负载开关应用进行了优化
- 存储、平板电脑和手持类器件
- 针对控制场效应晶体管 (FET) 应用进行了优化
- 负载点同步降压转换器

说明

此 NexFET™ 功率 MOSFET 被设计成在功率转换和负载管理应用中大大降低功率损耗。小外形尺寸无引线 (SON) 2mm x 2mm 封装提供针对封装尺寸的出色散热性能。

顶视图



产品概述

V_{DS}	漏源电压	20	V
Q_g	栅极电荷总量 (4.5V)	2.5	nC
Q_{gd}	栅漏栅极电荷	0.66	nC
$R_{DS(on)}$ (导通)	漏源导通电阻	$V_{GS}=4.5\text{V}$	16 mΩ
		$V_{GS}=10\text{V}$	12 mΩ
$V_{GS(th)}$	阈值电压	1.45	V

订购信息

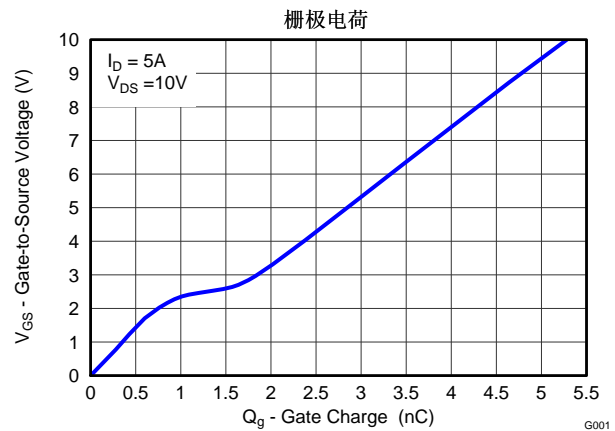
器件	封装	介质	数量	出货
CSD15571Q2	SON 2mm x 2mm 塑料封装	7 英寸卷带	3000	卷带封装

绝对最大额定值

$T_A=25^\circ\text{C}$ 时测得, 除非另外注明		值	单位
V_{DS}	漏源电压	20	V
V_{GS}	栅源电压	± 20	V
I_D	持续漏极电流 (受封装限制)	22	A
	持续漏极电流 ⁽¹⁾	10	A
I_{DM}	脉冲漏极电流, $T_A=25^\circ\text{C}$ 时测得 ⁽²⁾	52	A
P_D	功率耗散 ⁽¹⁾	2.5	W
T_J, T_{STG}	运行结温和储存温度范围	-55 至 150	$^\circ\text{C}$
E_{AS}	雪崩能量, 单脉冲 $I_D=19\text{A}, L=0.1\text{mH}, R_G=25\Omega$	18	mJ

(1) $R_{\theta JA} = 50$, 这是在 1 平方英寸纯铜 (2 盎司), 厚度为 .060" 的环氧板 (FR4) 印刷电路板 (PCB) 上测得的值。

(2) 脉冲持续时间 10 μs , 占空比 $\leq 2\%$



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise specified

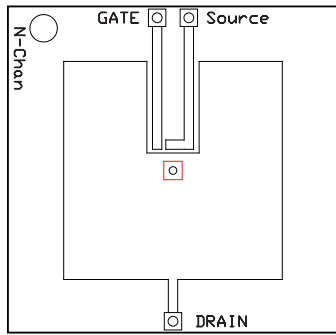
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	20			V
I_{DSS}	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 20V$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = 20V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\mu A$	1.10	1.45	1.90	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5V, I_{DS} = 5A$		16.0	19.2	m Ω
		$V_{GS} = 10V, I_{DS} = 5A$		12.0	15.0	m Ω
g_{fs}	Transconductance	$V_{DS} = 16V, I_{DS} = 5A$		25		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	$V_{GS} = 0V, V_{DS} = 10V, f = 1MHz$		320	419	pF
C_{OSS}	Output Capacitance			184	239	pF
C_{RSS}	Reverse Transfer Capacitance			32	42	pF
R_g	Series Gate Resistance			3.8	7.6	Ω
Q_g	Gate Charge Total (4.5V)	$V_{DS} = 10V, I_{DS} = 5A$		2.5	3.3	nC
Q_g	Gate Charge Total (10V)			5.1	6.7	nC
Q_{gd}	Gate Charge – Gate to Drain			0.66		nC
Q_{gs}	Gate Charge Gate to Source			0.93		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.52		nC
Q_{OSS}	Output Charge		$V_{DS} = 10V, V_{GS} = 0V$		4.1	
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 10V, V_{GS} = 4.5V, I_{DS} = 5A$ $R_G = 2\Omega$		4.7		ns
t_r	Rise Time			17.2		ns
$t_{d(off)}$	Turn Off Delay Time			9.9		ns
t_f	Fall Time			4.1		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_{DS} = 5A, V_{GS} = 0V$		0.82	1	V
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 10V, I_F = 5A, di/dt = 300A/\mu s$		10.7		nC
t_{rr}	Reverse Recovery Time			19		ns

THERMAL CHARACTERISTICS

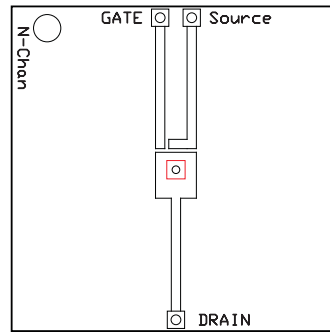
($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case ⁽¹⁾			4.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			65	$^\circ\text{C}/\text{W}$

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch x 1.5-inch (3.81-cm x 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA} = 65$ when mounted on 1 inch² (6.45 cm²) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA} = 235$ when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

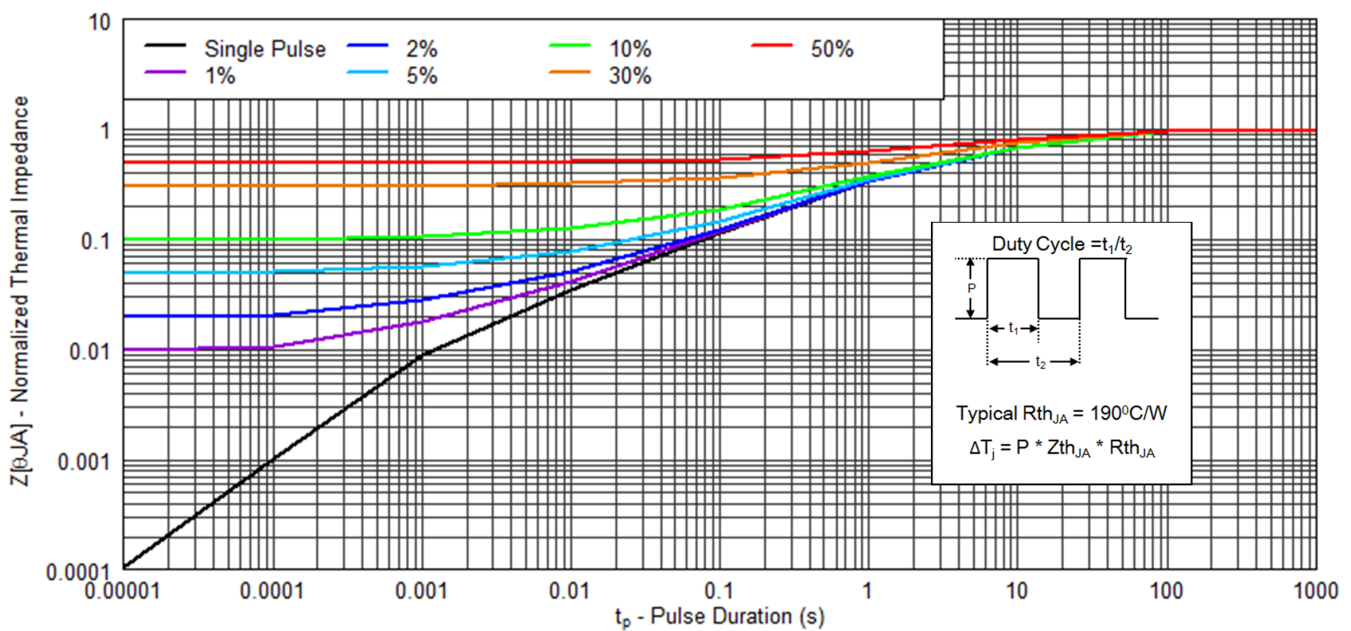


Figure 1. Transient Thermal Impedance

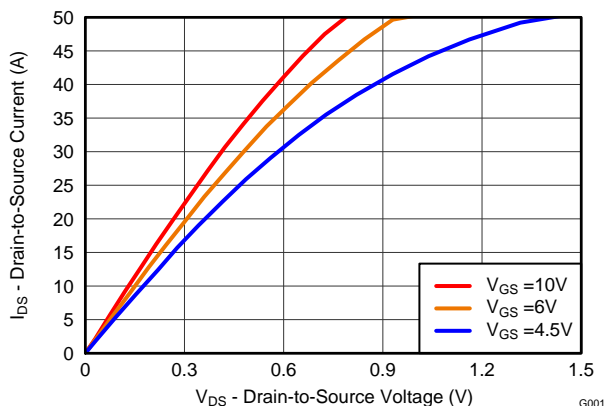


Figure 2. Saturation Characteristics

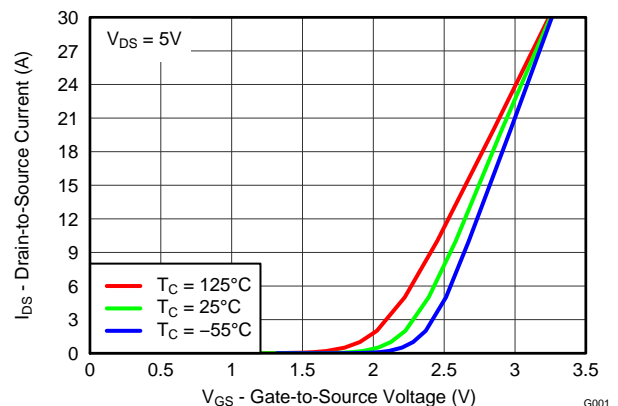


Figure 3. Transfer Characteristics

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

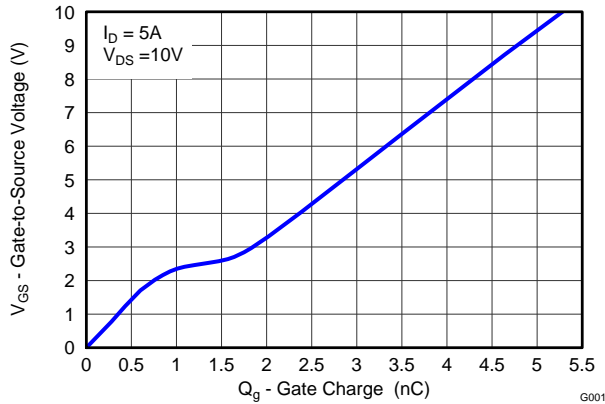


Figure 4. Gate Charge

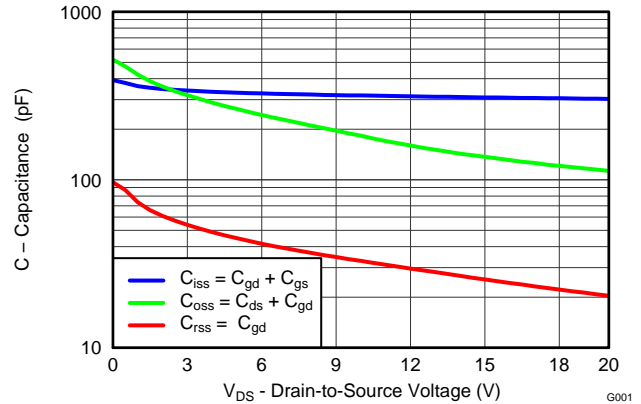


Figure 5. Capacitance

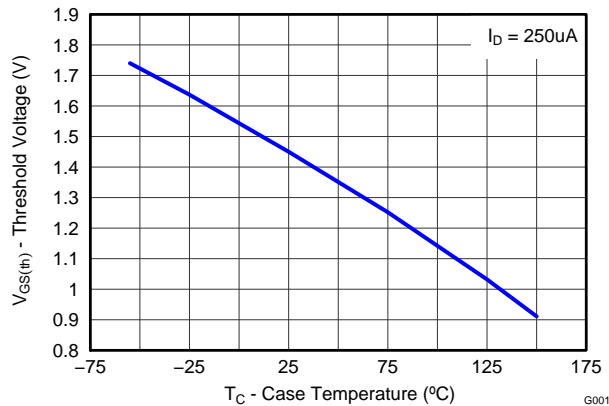


Figure 6. Threshold Voltage vs. Temperature

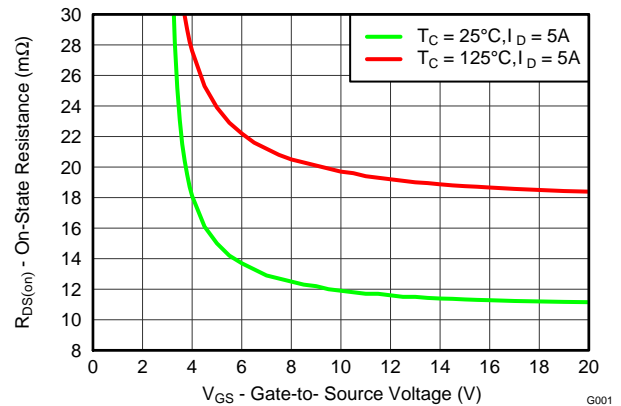


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

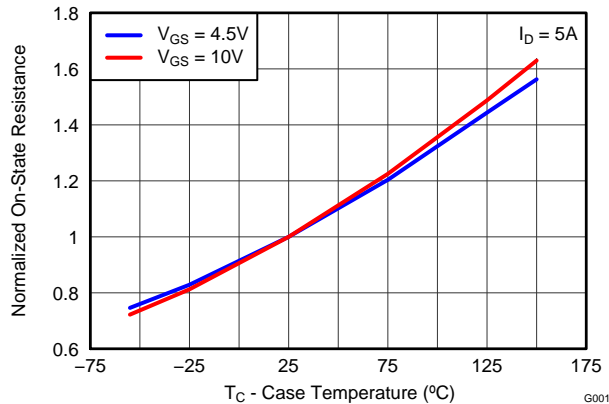


Figure 8. Normalized On-State Resistance vs. Temperature

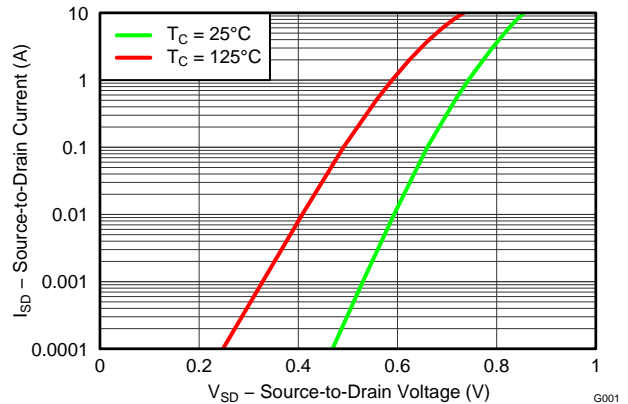


Figure 9. Typical Diode Forward Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

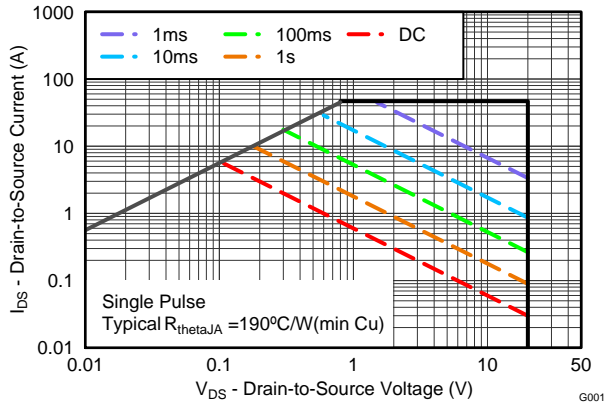


Figure 10. Maximum Safe Operating Area

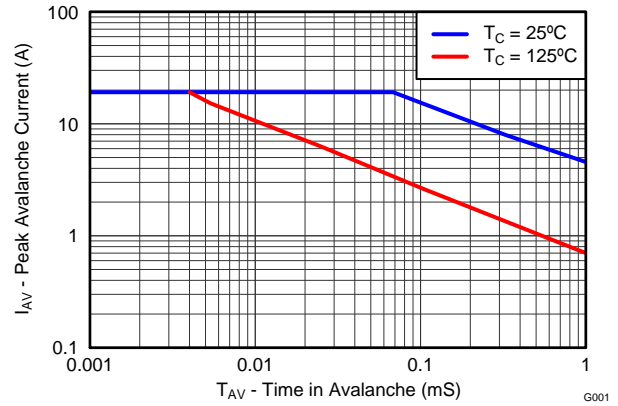


Figure 11. Single Pulse Unclamped Inductive Switching

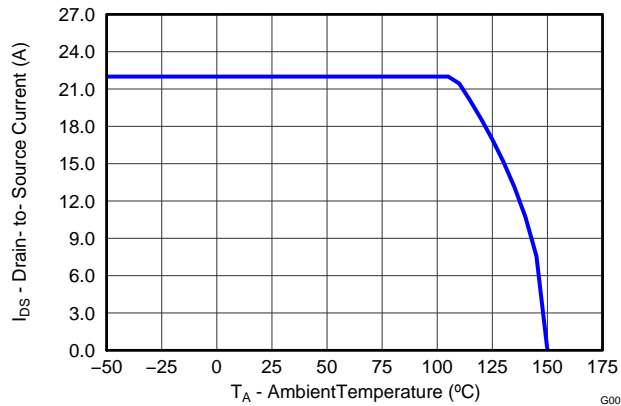
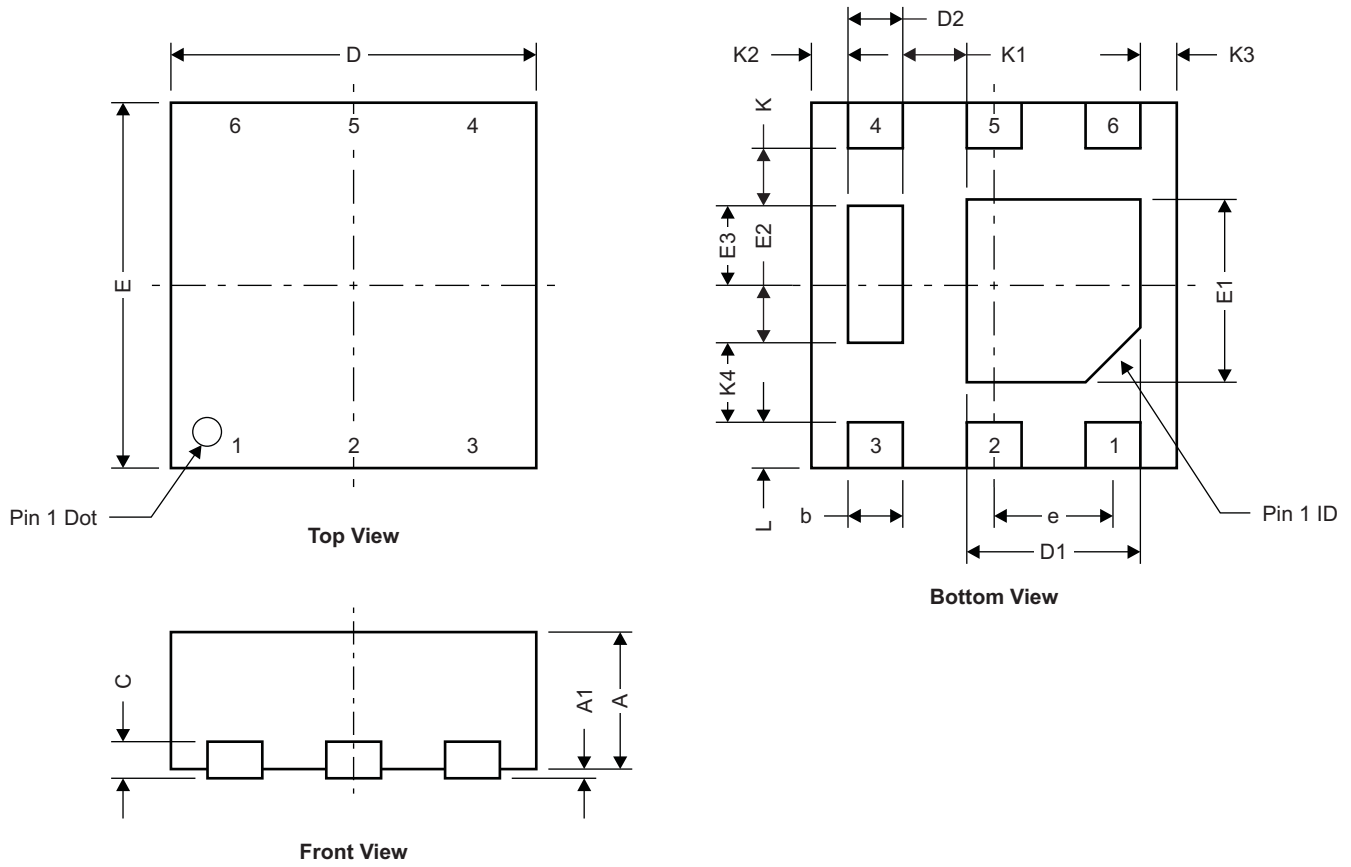


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

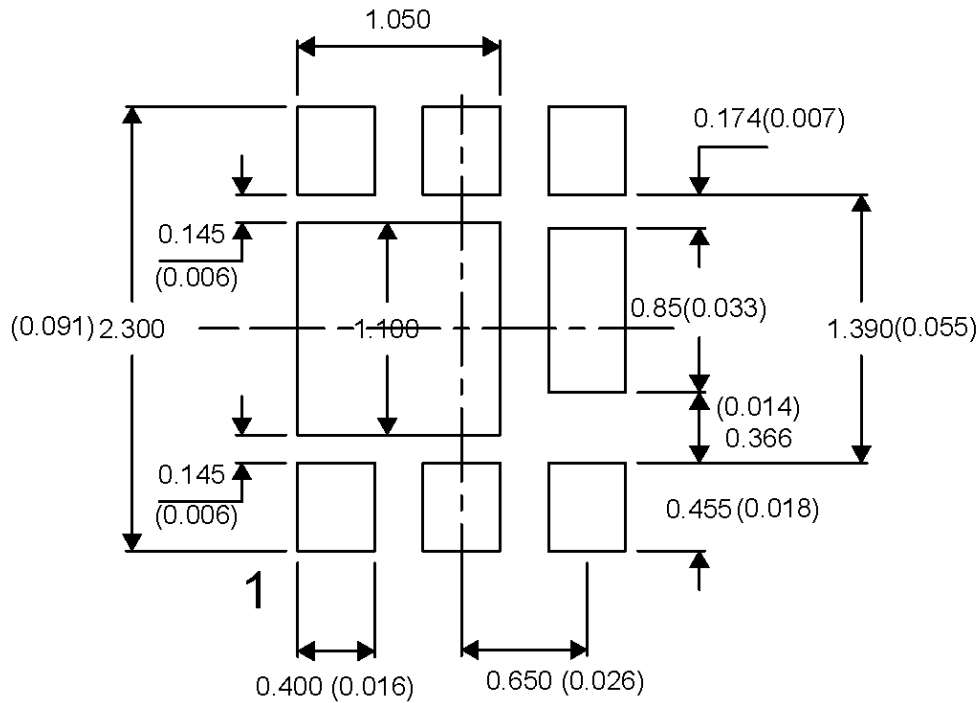
Q2 Package Dimensions



M0165-01

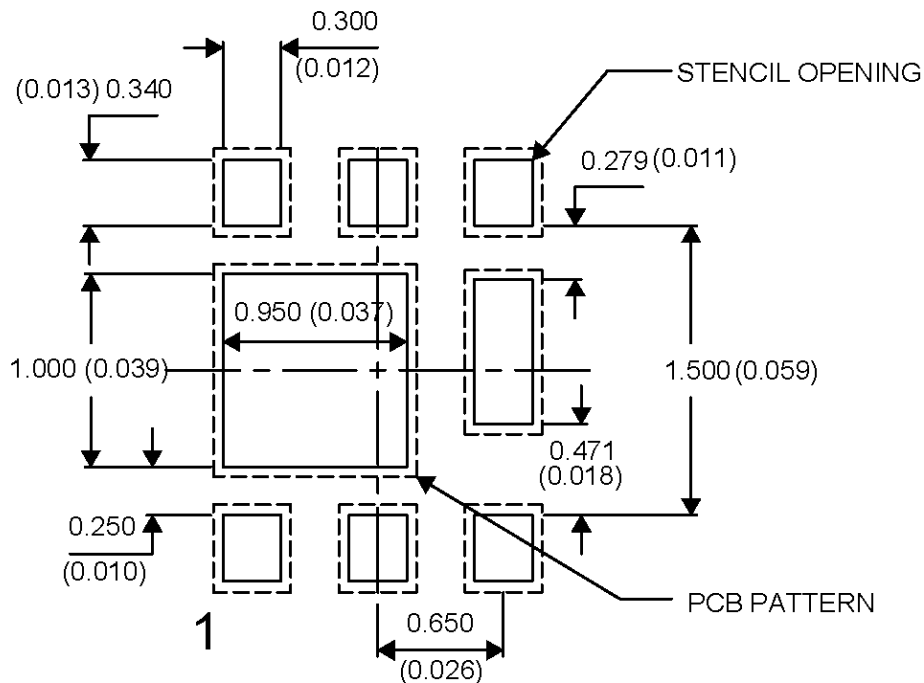
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.032
A1	0.000		0.050	0.000		0.002
b	0.250	0.300	0.350	0.010	0.012	0.014
C	0.203 TYP			0.008 TYP		
D	2.000 TYP			0.080 TYP		
D1	0.900	0.950	1.000	0.036	0.038	0.040
D2	0.300 TYP			0.012 TYP		
E	2.000 TYP			0.080 TYP		
E1	0.900	1.000	1.100	0.036	0.040	0.044
E2	0.280 TYP			0.0112 TYP		
E3	0.470 TYP			0.0188 TYP		
e	0.650 BSC			0.026 TYP		
K	0.280 TYP			0.0112 TYP		
K1	0.350 TYP			0.014 TYP		
K2	0.200 TYP			0.008 TYP		
K3	0.200 TYP			0.008 TYP		
K4	0.470 TYP			0.0188 TYP		
L	0.200	0.25	0.300	0.008	0.010	0.012

Recommended PCB Pattern



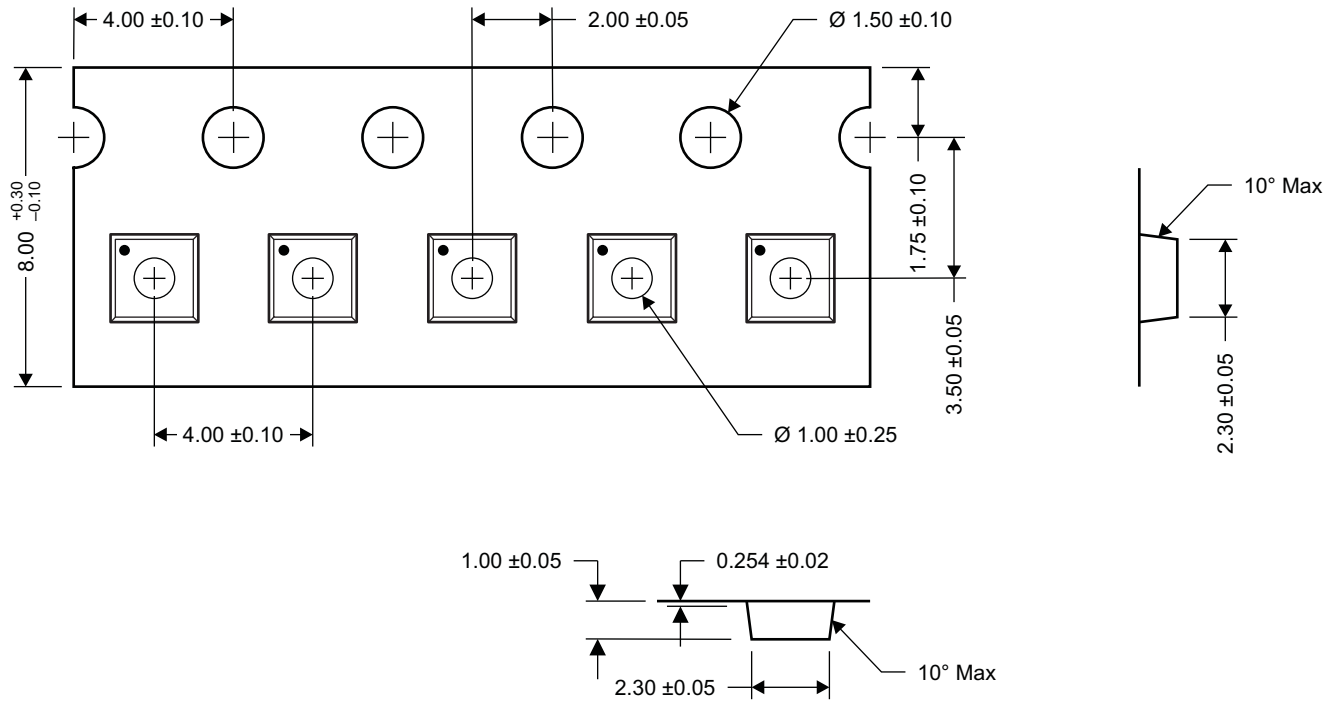
For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

Recommended Stencil Pattern



Note: All dimensions are in mm, unless otherwise specified.

Q2 Tape and Reel Information



- Notes:
1. Measured from centerline of sprocket hole to centerline of pocket
 2. Cumulative tolerance of 10 sprocket holes is ±0.20
 3. Other material available
 4. Typical SR of form tape Max 10⁹ OHM/SQ
 5. All dimensions are in mm, unless otherwise specified.

M0168-01

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD15571Q2	Active	Production	WSON (DQK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1551
CSD15571Q2.B	Active	Production	WSON (DQK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1551
CSD15571Q2G4.B	Active	Production	WSON (DQK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1551

(1) Status: For more details on status, see our [product life cycle](#).

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

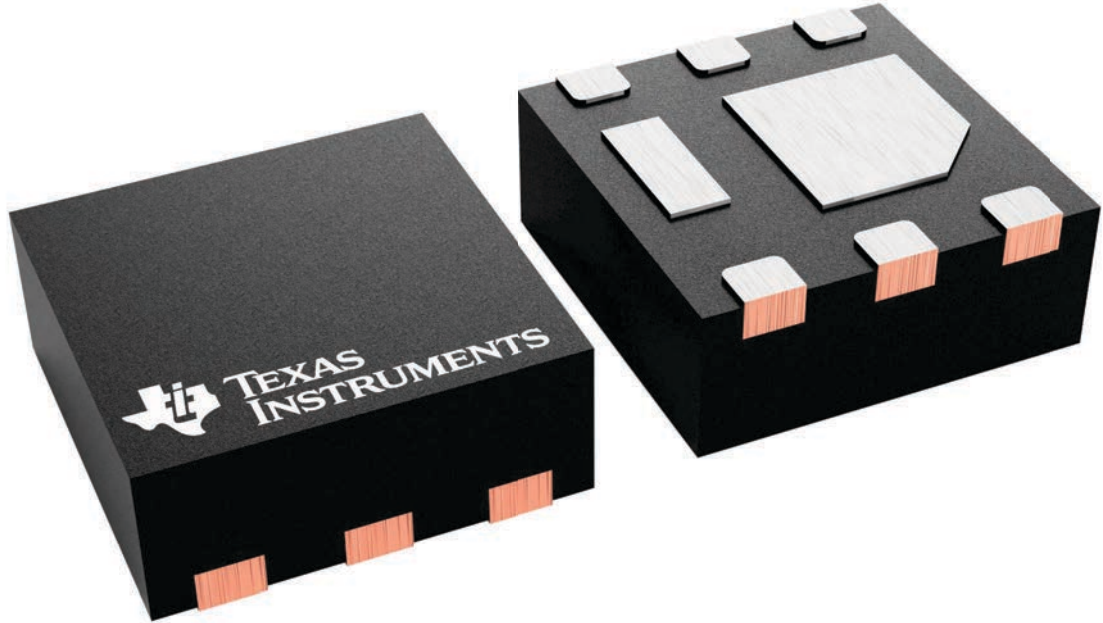
DQK 6

WSON - 0.8 mm max height

2 x 2, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

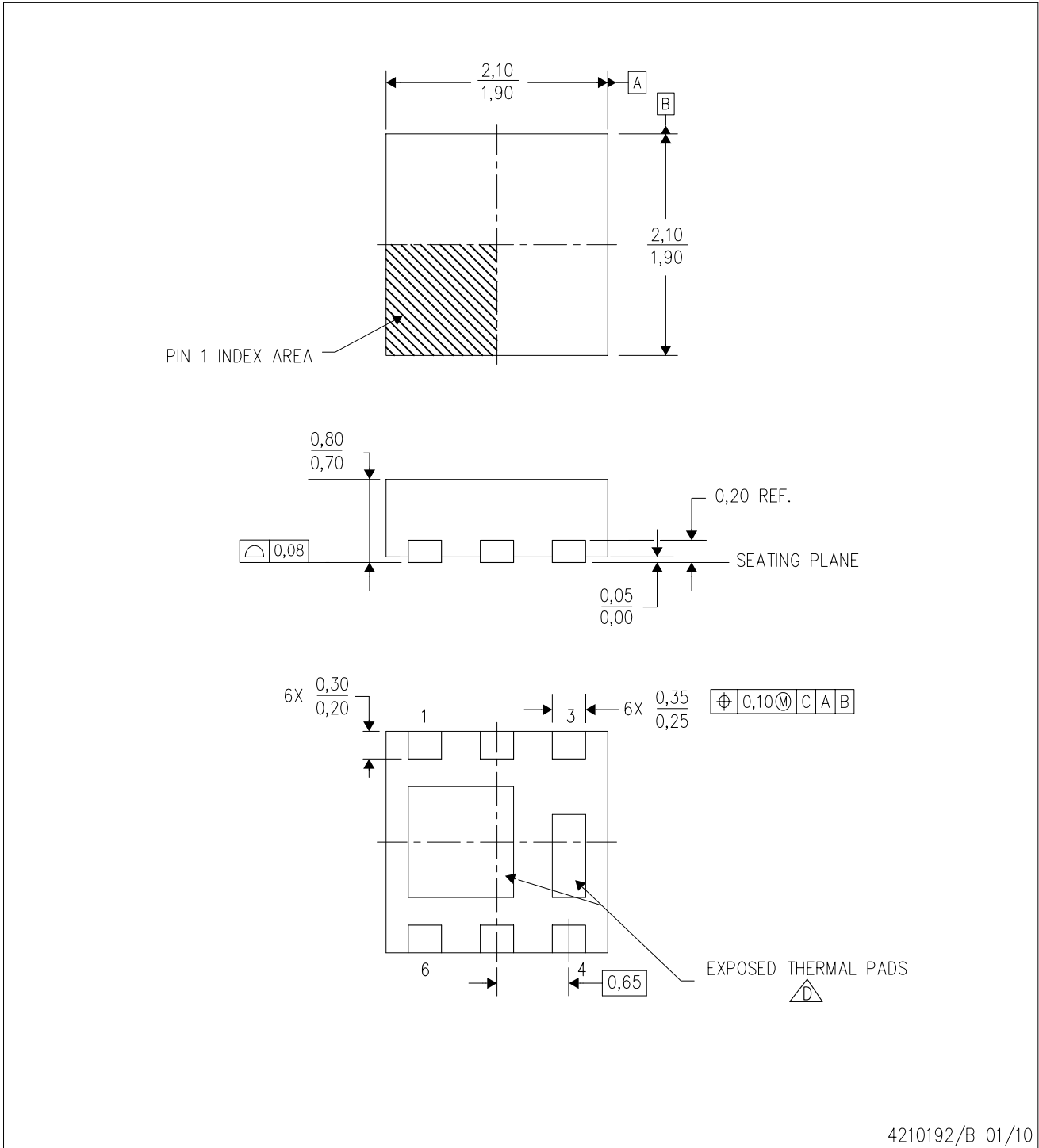
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4229807/A

DQK (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



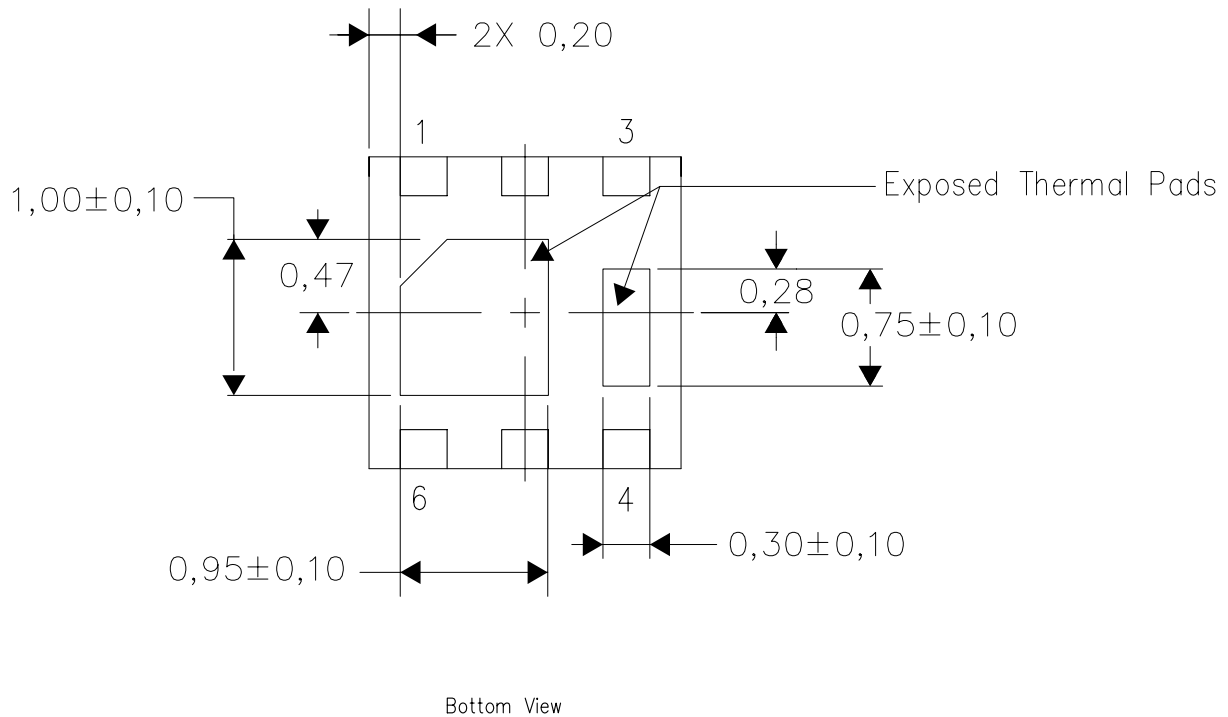
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.
 -  D. The package thermal pads must be soldered to the board for thermal and mechanical performance.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

重要通知和免责声明

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