CSD17522Q5A

30V、N 沟道 NexFET™ 功率 MOSFET

查询样品：CSD17522Q5A

特性

- 针对 **5V** 栅极驱动而优化
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩额定
- 无铅终端镀层
- 符合 **RoHS** 标准
- 无卤素
- **SON 5** 毫米 **×** **6** 毫米塑料封装

应用

- 笔记本电脑负载点
- 网络、电信和计算系统中的负载点同步降压

说明

此 NexFET™ 功率 MOSFET 专为最大限度地减少功率转换应用中的损耗而设计，并针对 5V 栅极驱动应用进行了优化。

产品汇总

V_{DS}	漏极至源极电压	30		V
Q_g	总栅极电荷 (4.5V)	3.6		nC
Q_{gd}	栅极电荷（栅极至漏极）	1.1		nC
$R_{DS(on)}$	漏极至源极导通电阻	V_{GS} = 4.5V	10	mΩ
		V_{GS} = 10V	6.7	mΩ
$V_{GS(th)}$	门限电压	1.6		V

订购信息

器件	封装	介质	数量	出货
CSD17522Q5A	SON 5-mm × 6-mm 塑料封装	13 英寸卷带	2500	卷带封装

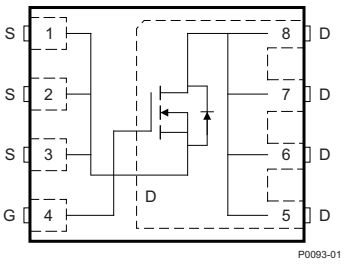
最大绝对额定值

T_A = 25°C，除非另有说明。		数值	单位
V_{DS}	漏极至源极电压	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	连续漏极电流，T_C = 25°C	87	A
	连续漏极电流(1)	16	A
I_{DM}	脉冲漏极电流，T_A = 25°C(2)	104	A
P_D	功耗(1)	3	W
T_J, T_{STG}	工作结温及存储温度范围	–55 至 150	°C
E_{AS}	雪崩能量，单脉冲 I_D = 33A，L = 0.1mH，R_G = 25Ω	54	mJ

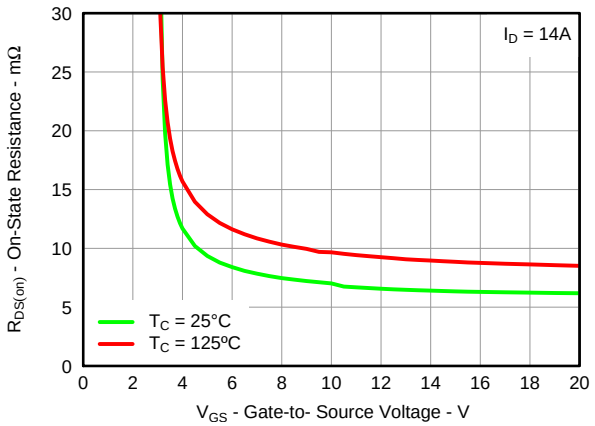
(1) 典型 $R_{\theta JA}$ = 41°C/W，在一块 1 英寸^2 (6.45-cm^2)、2 盎司（0.071-mm 厚）铜焊盘上，该焊盘位于一块厚度为 0.06 英寸 (1.52-mm) 的 FR4 PCB 之上。

(2) 脉冲持续时间 ≤300μs，占空比 ≤2%

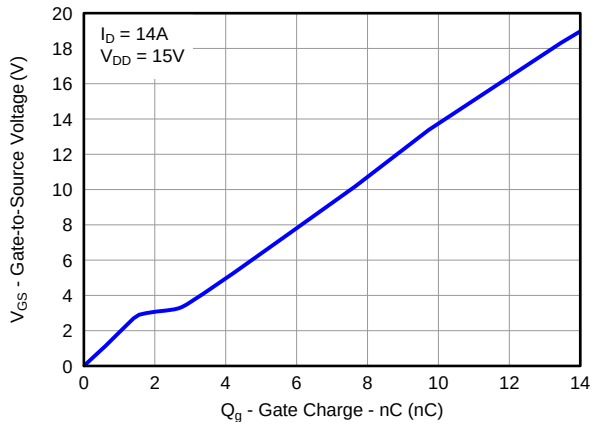
图 **1.** 顶视图



$R_{DS(on)}$ 与 **V_{GS}** 的关系曲线



栅极电荷



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = 250µA	30			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 24V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = ±20V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	1.1	1.6	2.0	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V, I_D = 14A		10	12.4	mΩ
		V_{GS} = 10V, I_D = 14A		6.7	8.1	mΩ
g_{fs}	Transconductance	V_{DS} = 15V, I_D = 14A		37		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		580	695	pF
C_{oss}	Output Capacitance			390	470	pF
C_{rss}	Reverse Transfer Capacitance			35	44	pF
R_G	Series Gate Resistance			4.7		Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 15V, I_D = 14A		3.6	4.3	nC
Q_{gd}	Gate Charge Gate to Drain			1.1		nC
Q_{gs}	Gate Charge Gate to Source			1.6		nC
$Q_{g(th)}$	Gate Charge at Vth			0.9		nC
Q_{oss}	Output Charge	V_{DS} = 13V, V_{GS} = 0V		8.6		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15V, V_{GS} = 4.5V, I_{DS} = 14A, R_G = 2Ω		6.7		ns
t_r	Rise Time			12		ns
$t_{d(off)}$	Turn Off Delay Time			10.5		ns
t_f	Fall Time			3.7		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD} = 14A, V_{GS} = 0V		0.85	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD}= 13V, I_F = 14A, di/dt = 300A/µs		19.6		nC
t_{rr}	Reverse Recovery Time			17.8		ns

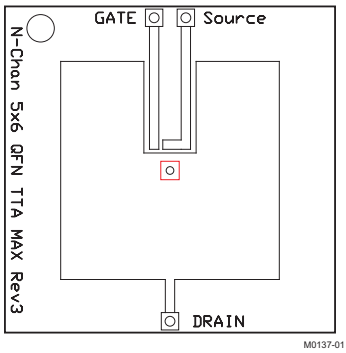
THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

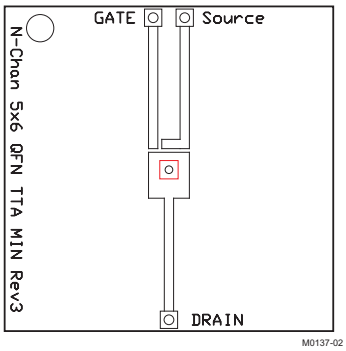
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case(1)			1.8	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1)(2)			51	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.

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Max $R_{\theta JA}$ = 51°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

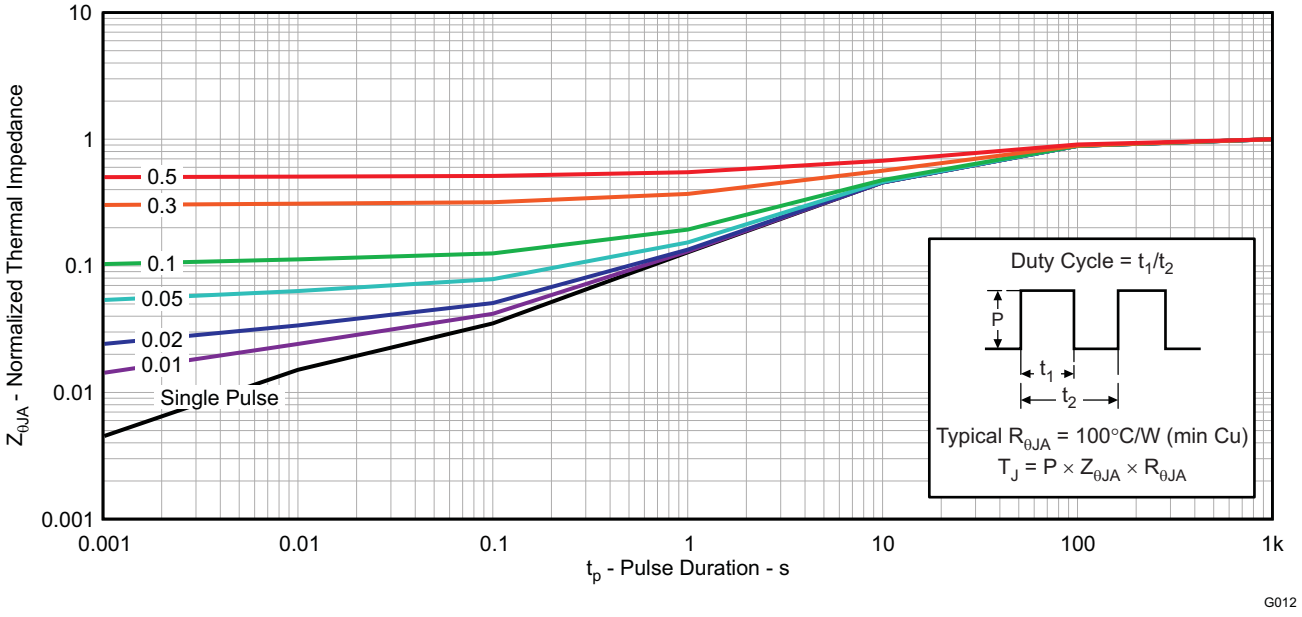


Figure 2. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

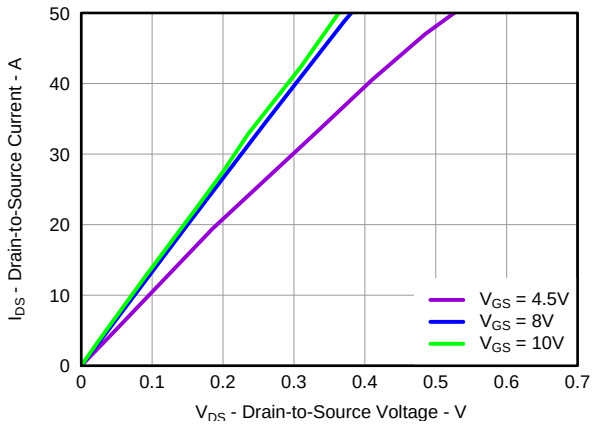


Figure 3. Saturation Characteristics

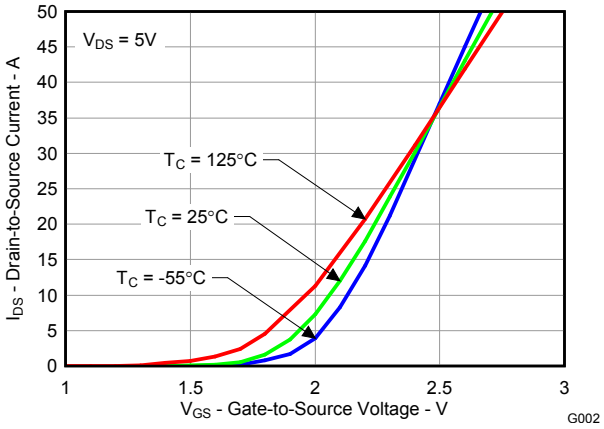


Figure 4. Transfer Characteristics

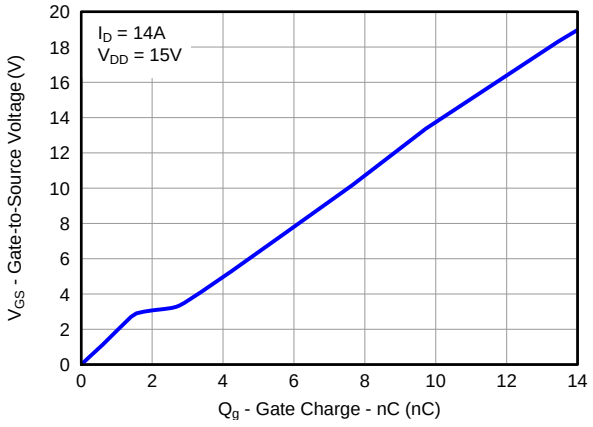


Figure 5. Gate Charge

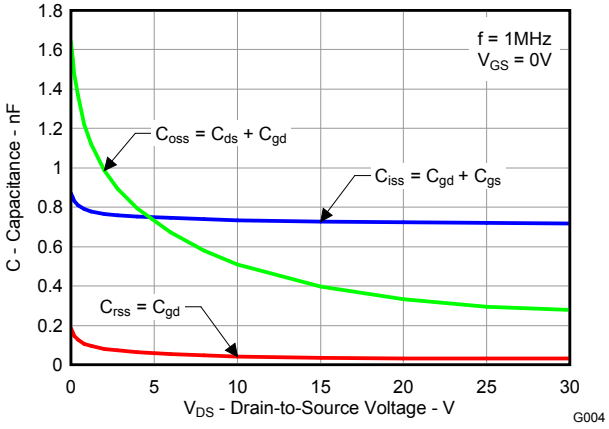


Figure 6. Capacitance

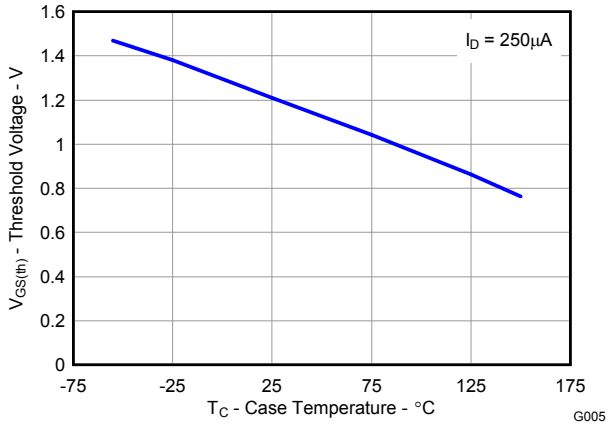


Figure 7. Threshold Voltage vs. Temperature

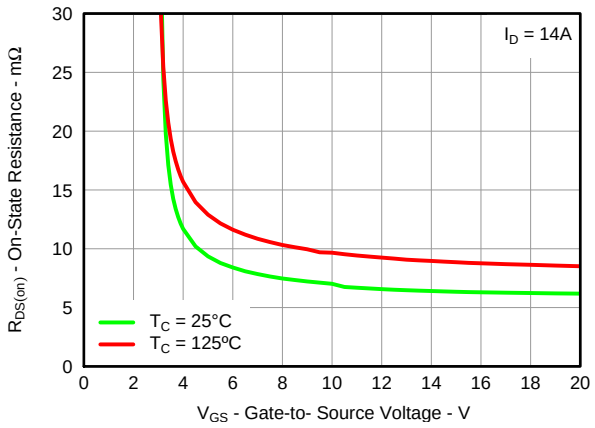


Figure 8. On-State Resistance vs. Gate-to-Source Voltage

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TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

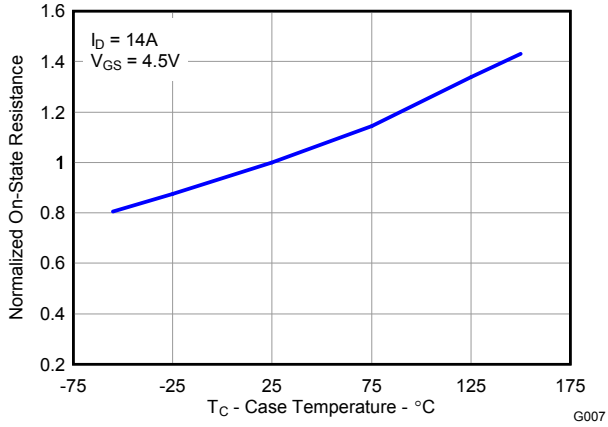


Figure 9. Normalized On-State Resistance vs. Temperature

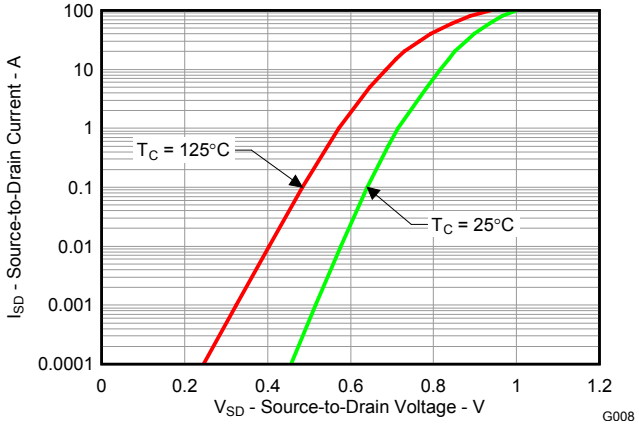


Figure 10. Typical Diode Forward Voltage

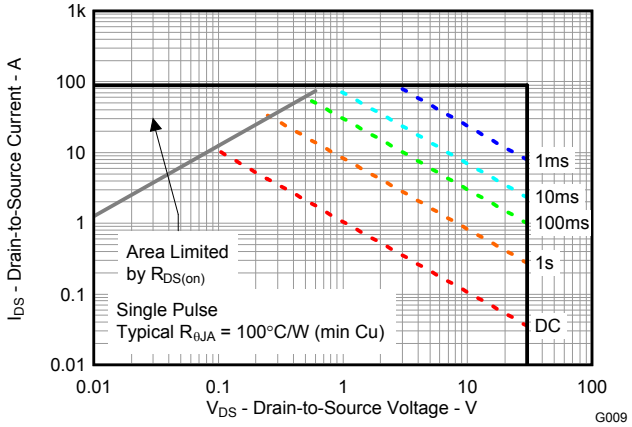


Figure 11. Maximum Safe Operating Area

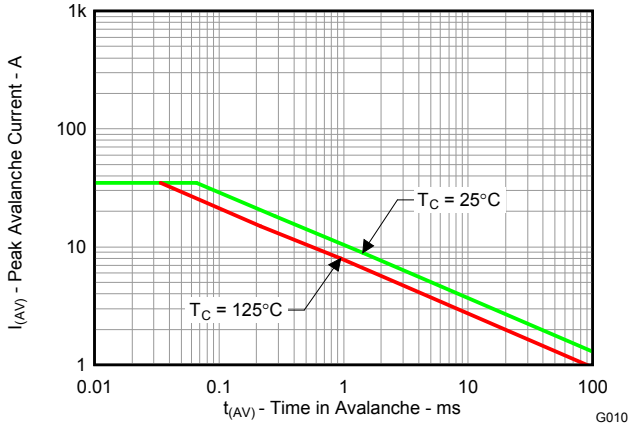


Figure 12. Single Pulse Unclamped Inductive Switching

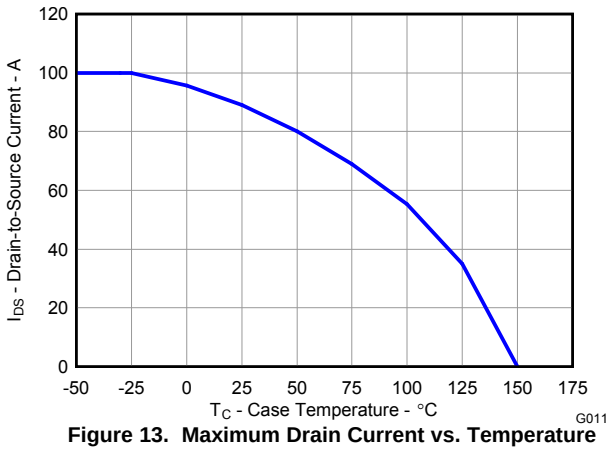
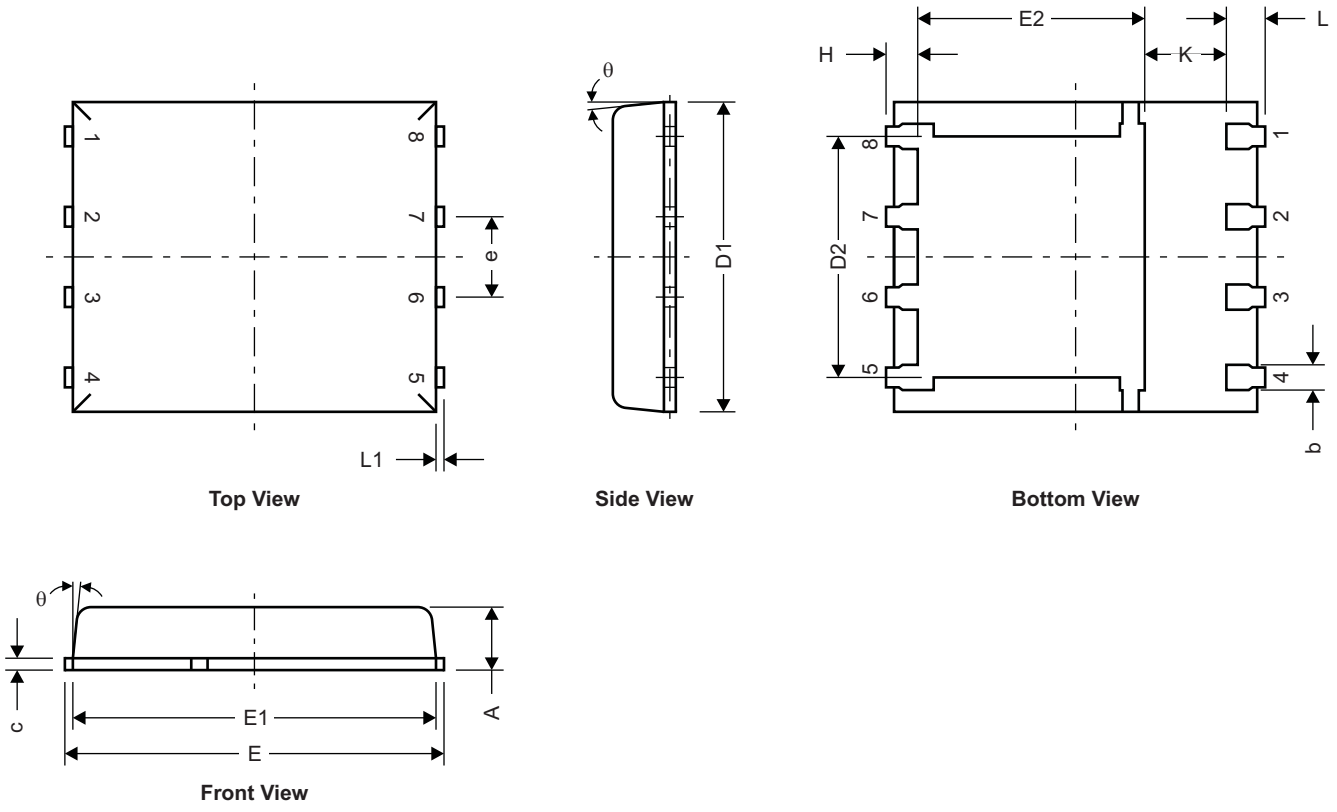


Figure 13. Maximum Drain Current vs. Temperature

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MECHANICAL DATA

Q5A Package Dimensions

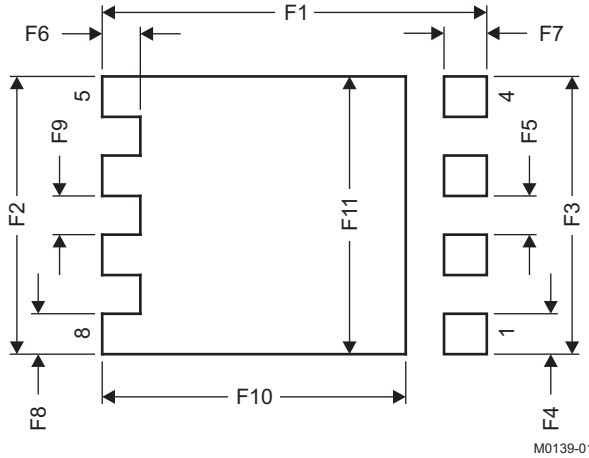


M0135-01

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.17	1.27	1.37
H	0.41	0.56	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°		12°

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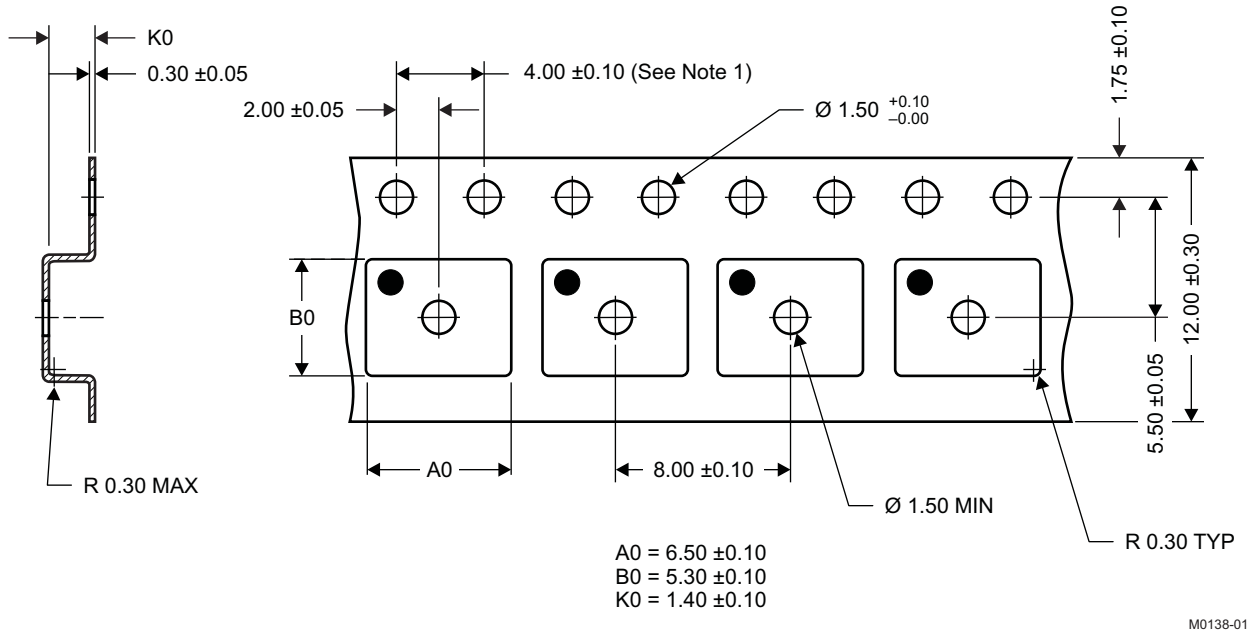
Figure 14. Recommended PCB Pattern



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Q5A Tape and Reel Information



Notes:

1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

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REVISION HISTORY

Changes from Original (June 2011) to Revision A **Page**

- Changed V_{GS} From: +20 / –12V To: ±20V in the Abs Max Ratings table 1
- Changed I_{GSS} the Test Conditions From: V_{DS} = 0V, V_{GS} = +20/-12V To: V_{DS} = 0V, V_{GS} = ±20V 2

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17522Q5A	Active	Production	VSONP (DQJ) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17522
CSD17522Q5A.B	Active	Production	VSONP (DQJ) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17522

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

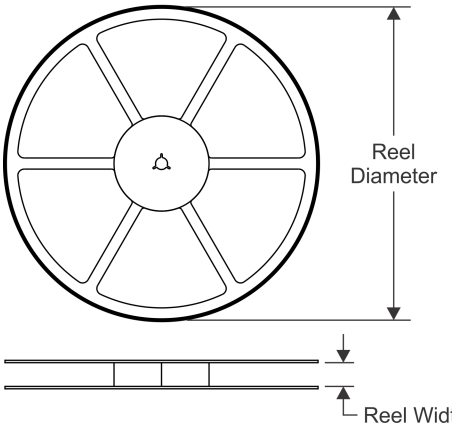
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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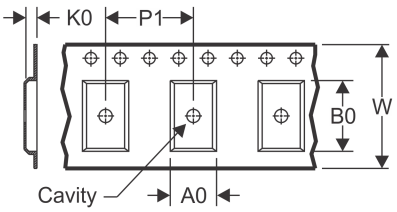
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

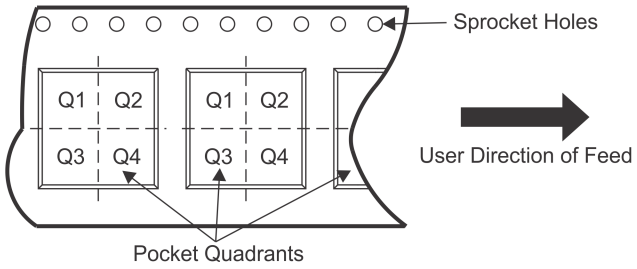


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

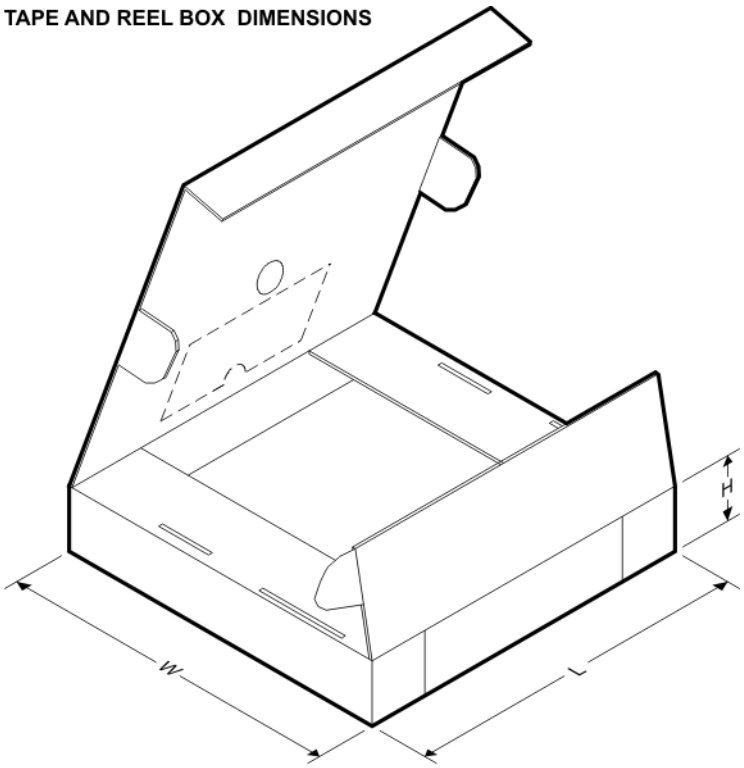
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

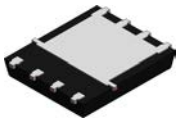
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17522Q5A	VSONP	DQJ	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17522Q5A	VSONP	DQJ	8	2500	340.0	340.0	38.0

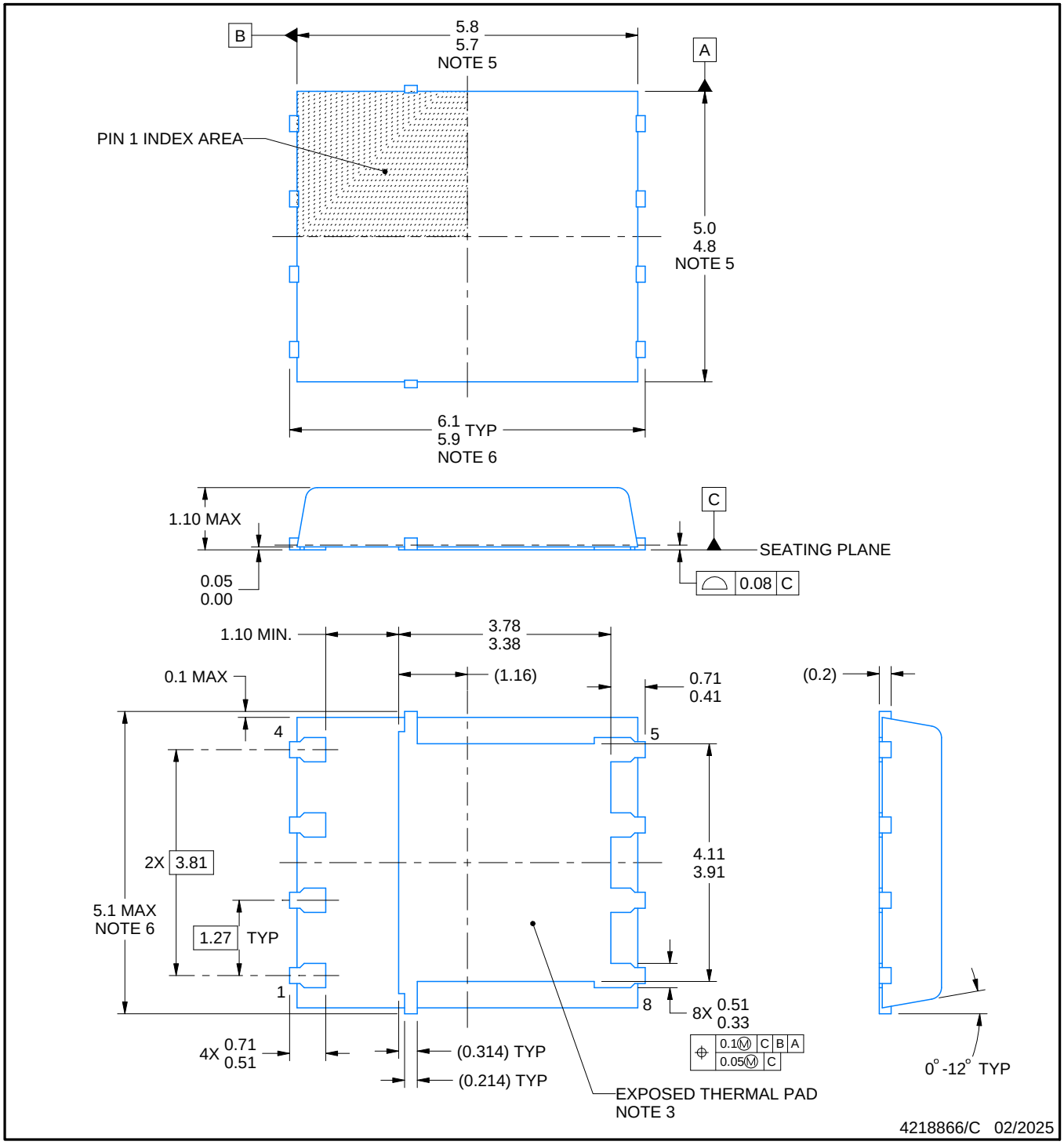


PACKAGE OUTLINE

DQJ0008A

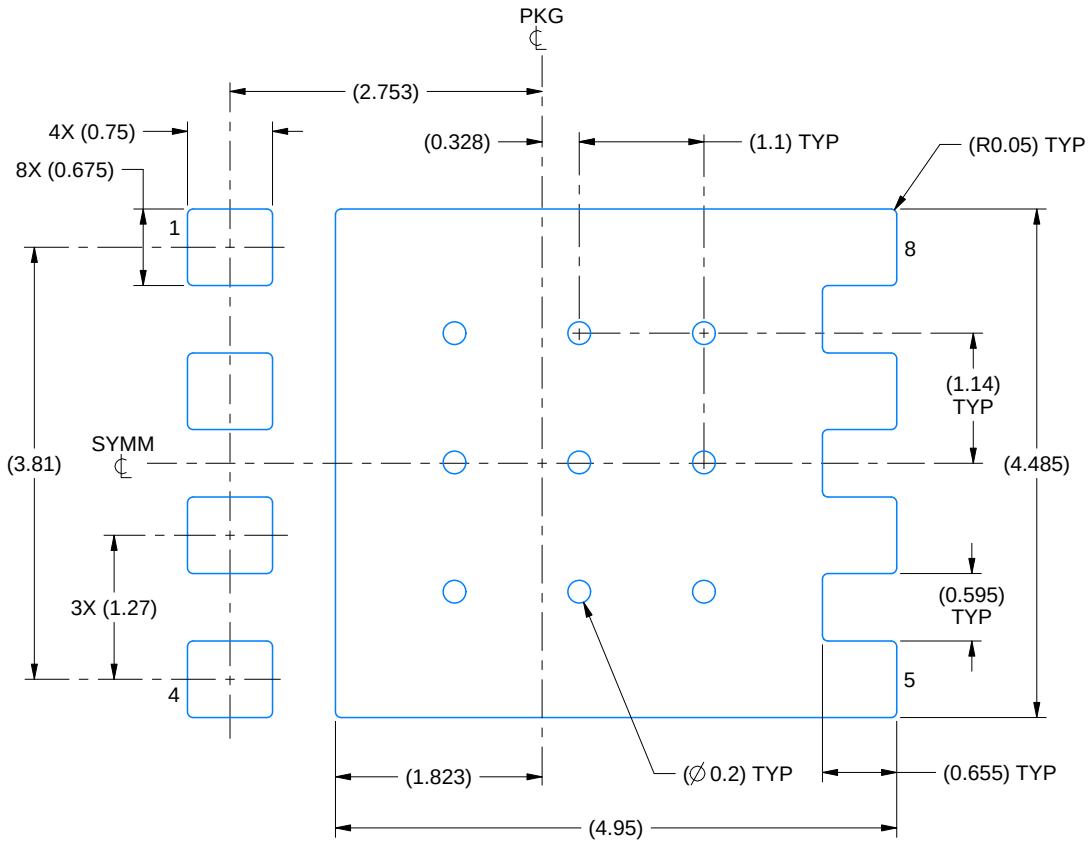
VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

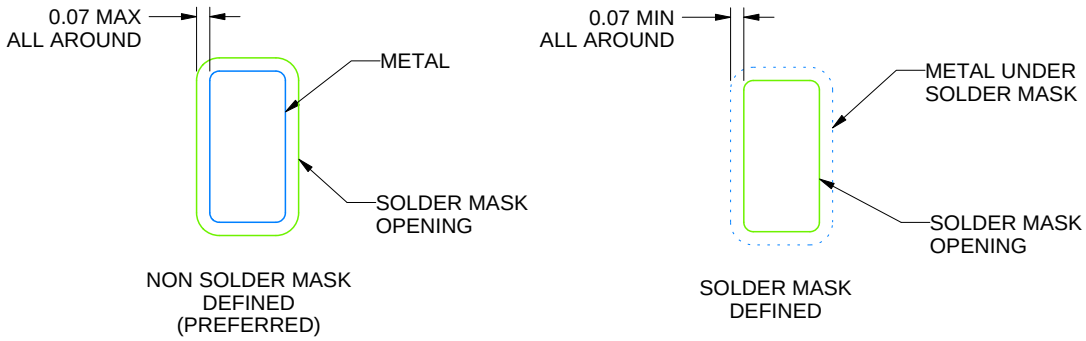


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. These dimensions do not include mold flash protrusions or gate burrs.
6. These dimensions include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 15X

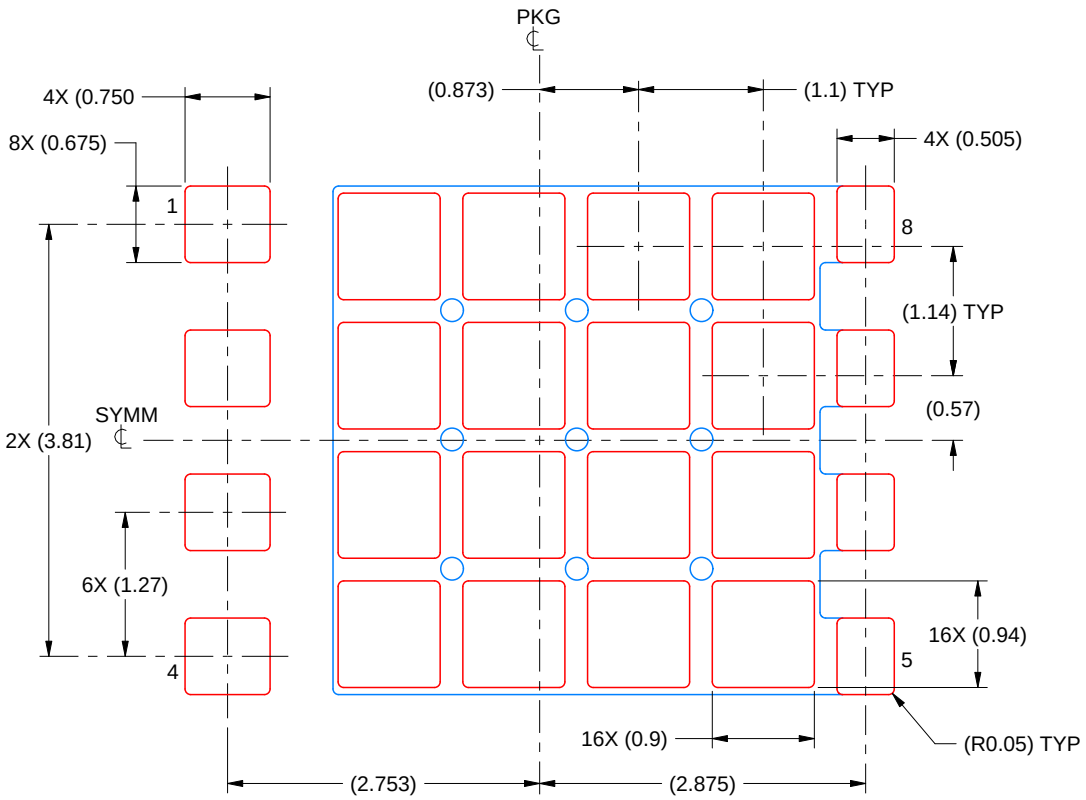


SOLDER MASK DETAILS

4218866/C 02/2025

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD:
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 15X

4218866/C 02/2025

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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