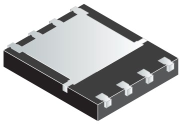


30V N 通道 NexFET™ 功率金属氧化物场效应晶体管 (MOSFET)

查询样品: **CSD17555Q5A**

特性

- 超低 Q_g和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅端子镀层
- 符合 **RoHS** 标准
- 无卤素
- 小外形无引线 **(SON) 5mm × 6mm** 塑料封装

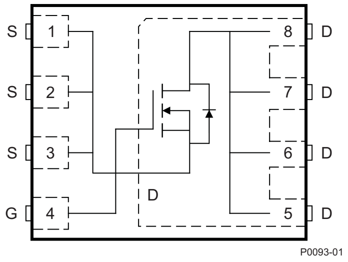
应用范围

- 在网络互联、电信、和计算系统中的负载点同步降压
- 针对控制和同步 **FET** 应用进行了优化

说明

此 NexFET™ 功率 MOSFET 被设计用于在功率转换应用中大大降低功率损失。

顶视图



产品概述

T_A=25°C 时测得，除非另外注明		典型值		单位
V_{DS}	漏源电压	30		V
Q_g	栅极电荷总量 (4.5V)	23		nC
Q_{gd}	栅漏栅极电荷	5		nC
R_{DS}（接通）	漏源导通电阻	V_{GS}=4.5V	2.8	mΩ
		V_{GS}=10V	2.3	mΩ
$V_{GS(th)}$	阀值电压	1.5		V

订购信息

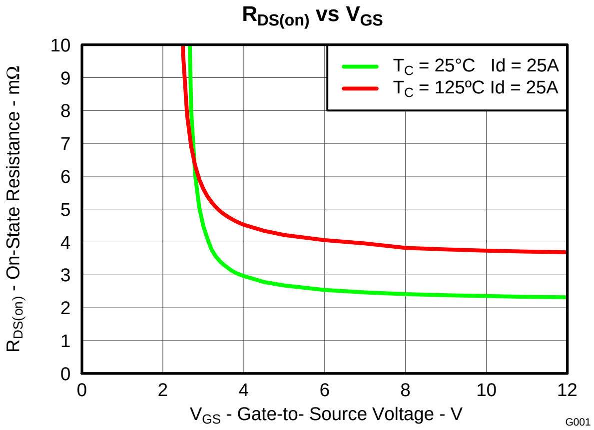
器件	封装	介质	数量	出货
CSD17555Q5A	5mm x 6mm SON 塑料封装	13 英寸卷带	2500	卷带封装

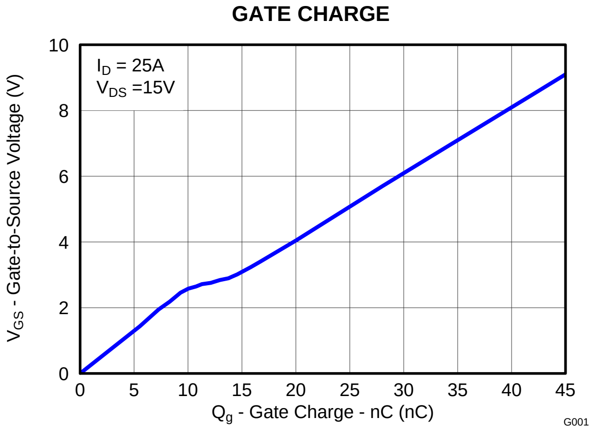
绝对最大额定值

T_A=25°C 时测得，除非另外注明		值	单位
V_{DS}	漏源电压	30	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制），T_C=25°C 时测得	100	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	116	
	持续漏极电流$^{(1)}$	24	A
I_{DM}	脉冲漏极电流，T_A=25°C 时测得$^{(2)}$	153	A
P_D	功率耗散$^{(1)}$	3	W
T_J，T_{STG}	运行结温和储存温度范围	-55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D=60A，L=0.1mH，R_G=25Ω	180	mJ

(1) $R_{\theta JA}$=42°C/W，这是在一块厚度为 0.06 英寸 (1.52mm) 的 FR4 印刷电路板 (PCB) 上的一英寸^2(6.45cm^2)，2 盎司（厚度 0.071mm）铜过渡垫片上测得的典型值。

(2) 脉冲持续时间 ≤ 300μs，占空比 ≤ 2%





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NexFET is a trademark of Texas Instruments.

English Data Sheet: SLPS353

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_{DS} = 250μA	30			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 24V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = 20V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250μA	1	1.5	1.9	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V, I_{DS} = 25A		2.8	3.4	mΩ
		V_{GS} = 10V, I_{DS} = 25A		2.3	2.7	mΩ
g_{fs}	Transconductance	V_{DS} = 15V, I_{DS} = 25A		109		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		3875	4650	pF
C_{oss}	Output Capacitance			949	1139	pF
C_{rss}	Reverse Transfer Capacitance			70	87	pF
R_G	Series Gate Resistance			0.8	1.6	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 15V, I_{DS} = 25A		23	28	nC
Q_{gd}	Gate Charge Gate to Drain			5		nC
Q_{gs}	Gate Charge Gate to Source			7.5		nC
$Q_{g(th)}$	Gate Charge at Vth			5		nC
Q_{oss}	Output Charge	V_{DS} = 14V, V_{GS} = 0V		25		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15V, V_{GS} = 4.5V, I_{DS} = 25A,R_G = 2Ω		14		ns
t_r	Rise Time			18		ns
$t_{d(off)}$	Turn Off Delay Time			20		ns
t_f	Fall Time			5.3		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD} = 25A, V_{GS} = 0V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD}= 14V, I_F = 25A, di/dt = 300A/μs		31		nC
t_{rr}	Reverse Recovery Time			25		ns

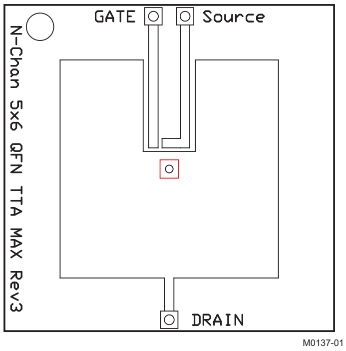
THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

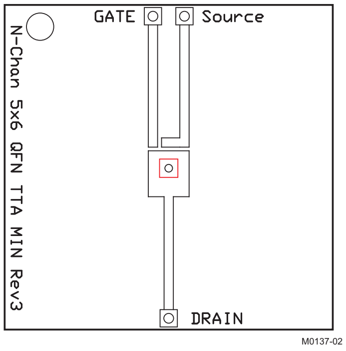
PARAMETER		MIN	TYP	MAX	UNIT
$R_{θJC}$	Thermal Resistance Junction to Case (1)			2.2	°C/W
$R_{θJA}$	Thermal Resistance Junction to Ambient (1) (2)			52	°C/W

(1) $R_{θJC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{θJC}$ is specified by design, whereas $R_{θJA}$ is determined by the user's board design.

(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 52°C/W when mounted on 1 $inch^2$ (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 128°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

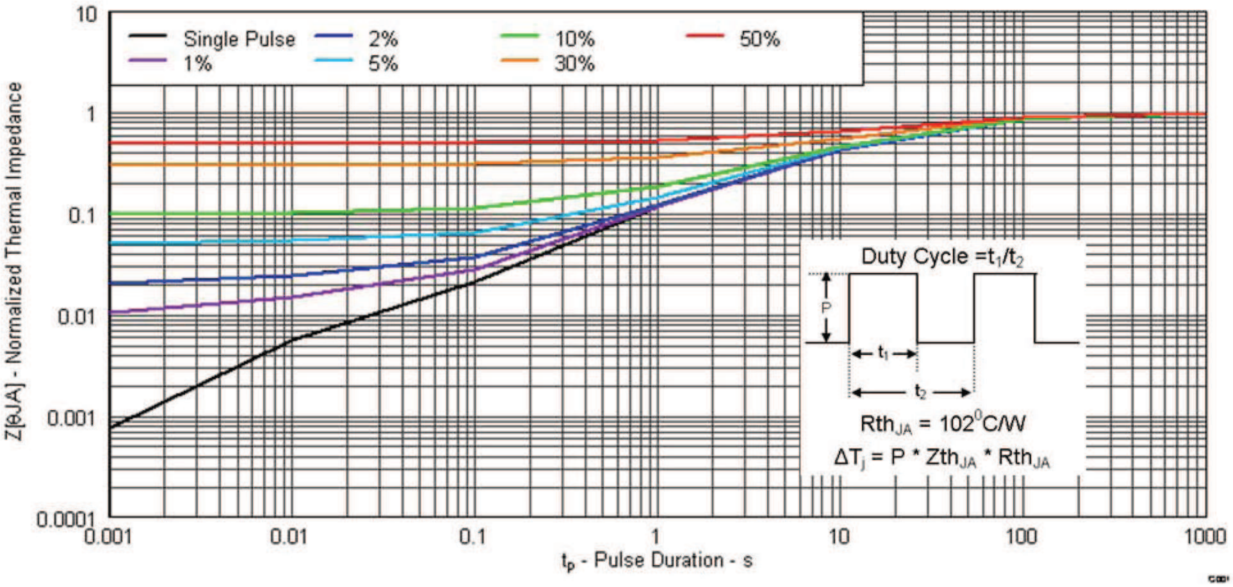


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

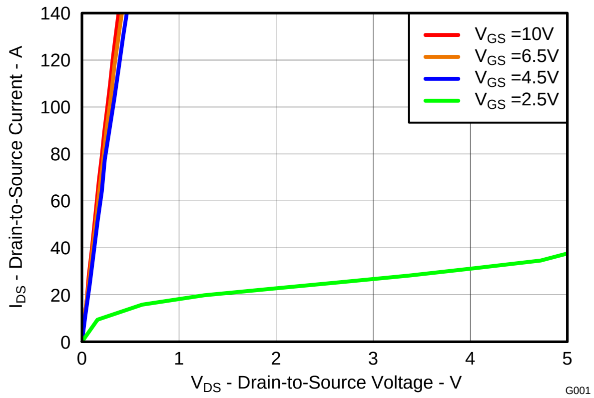


Figure 2. Saturation Characteristics

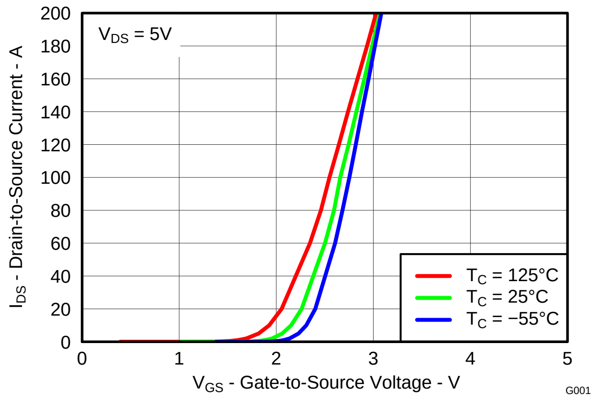


Figure 3. Transfer Characteristics

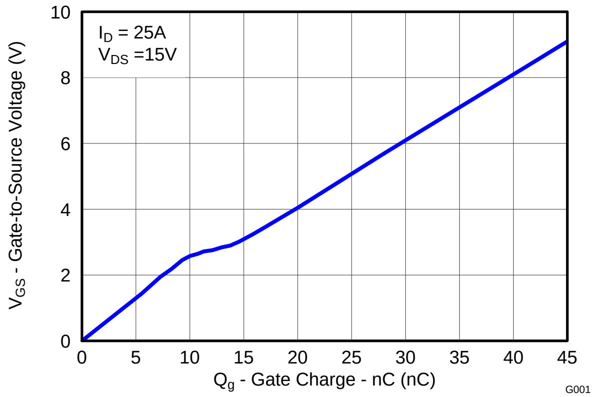


Figure 4. Gate Charge

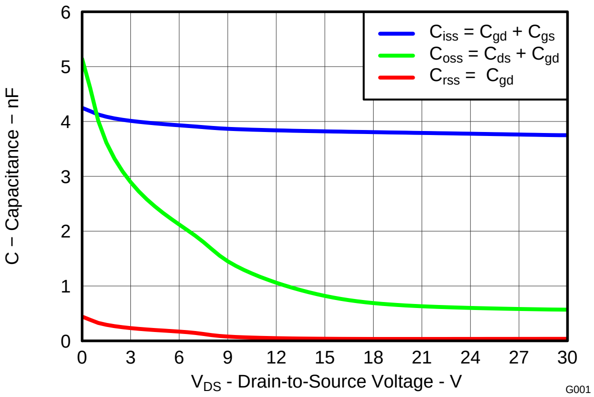


Figure 5. Capacitance

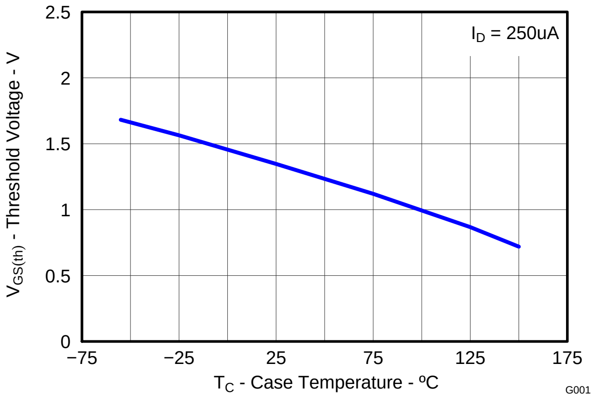


Figure 6. Threshold Voltage vs. Temperature

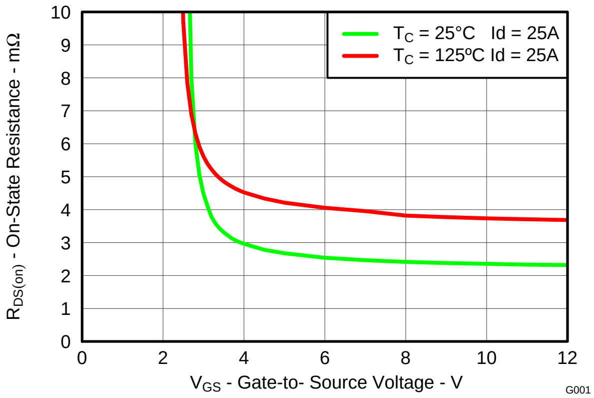


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

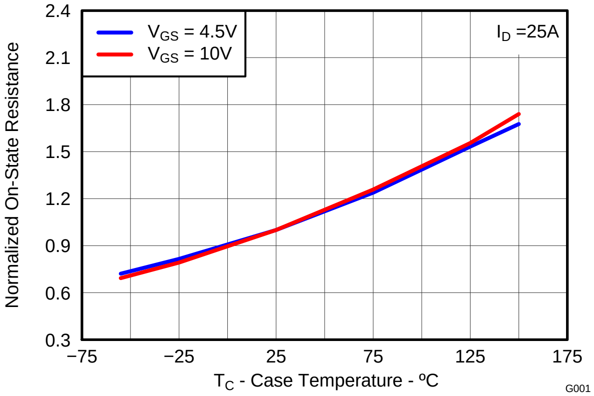


Figure 8. Normalized On-State Resistance vs. Temperature

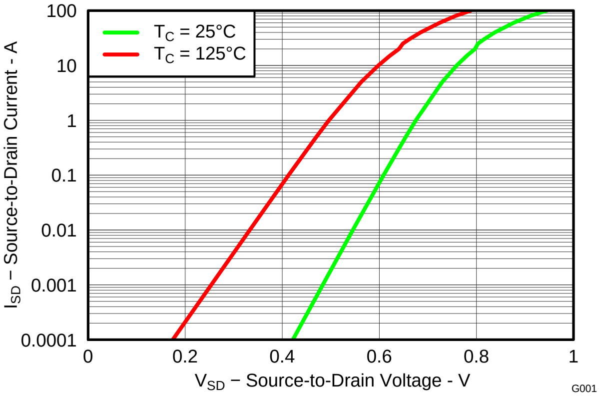


Figure 9. Typical Diode Forward Voltage

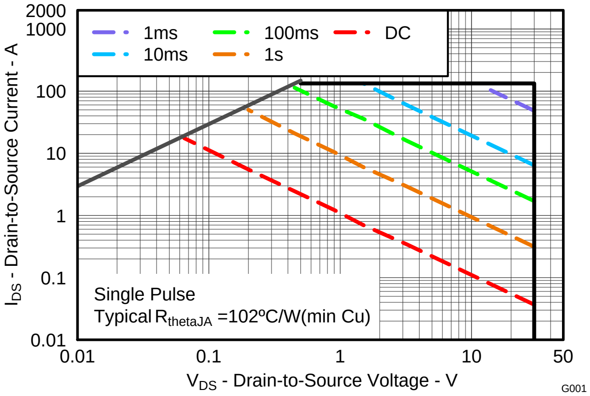


Figure 10. Maximum Safe Operating Area

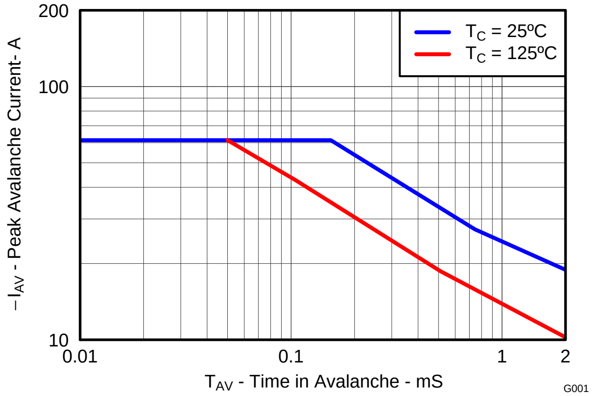


Figure 11. Single Pulse Unclamped Inductive Switching

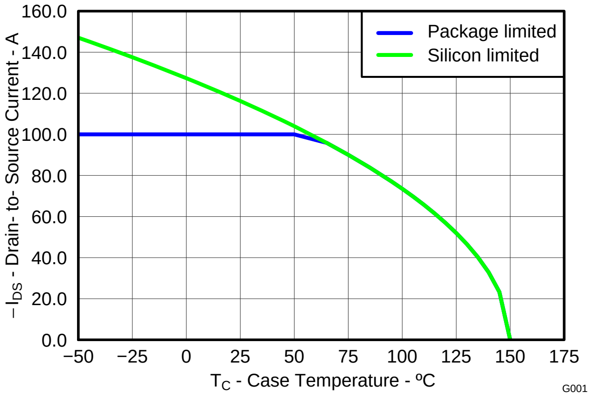
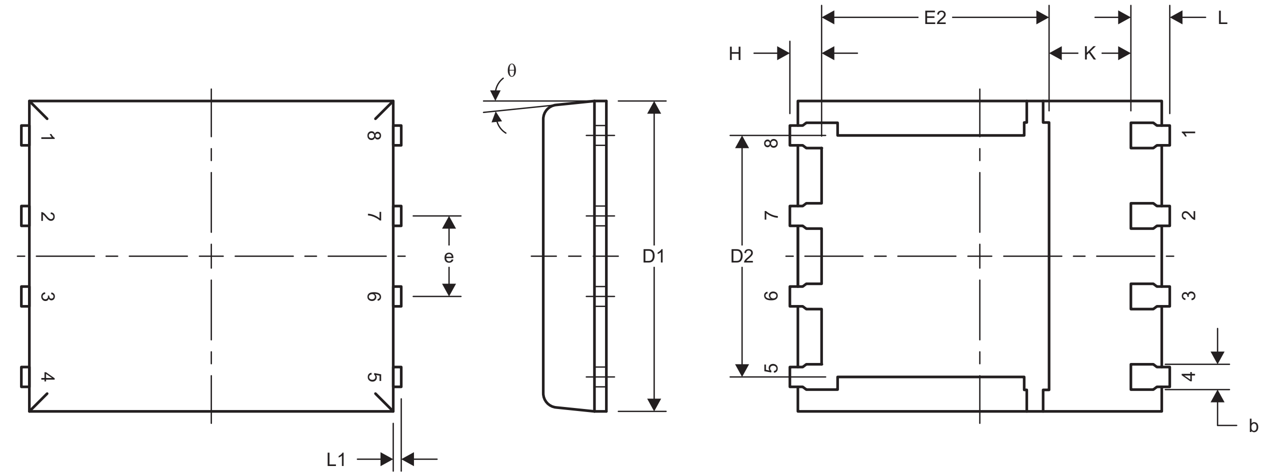


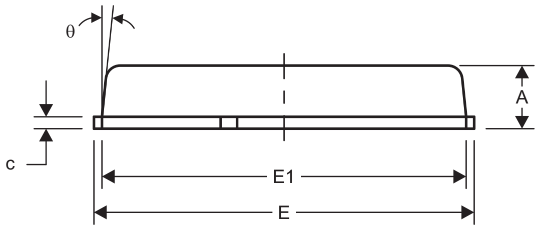
Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

Q5A Package Dimensions



Top View **Side View** **Bottom View**

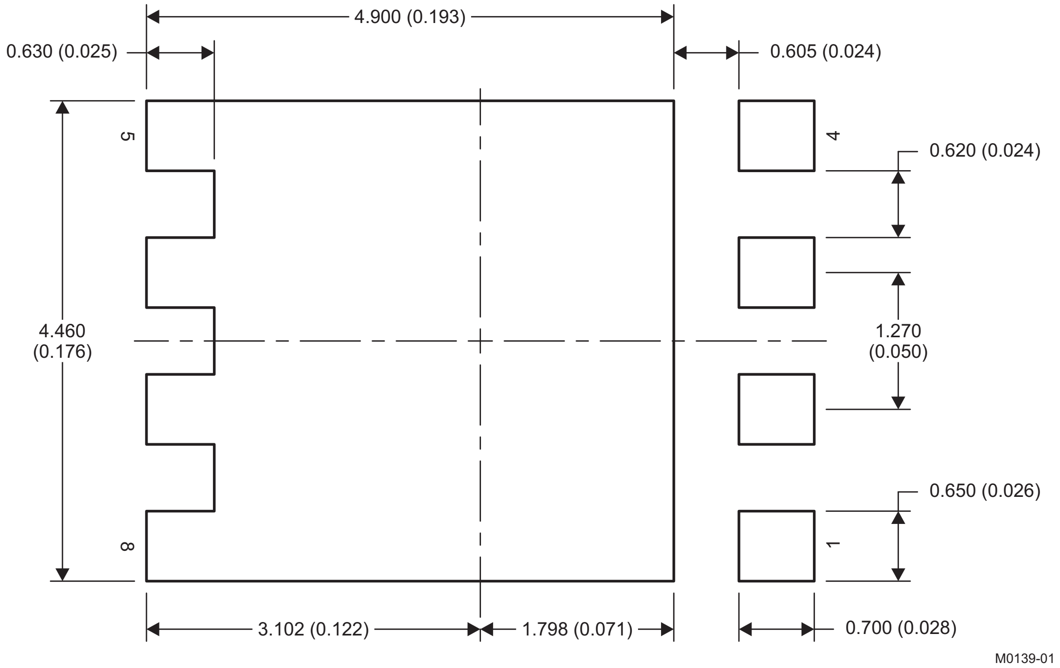


Front View

M0135-01

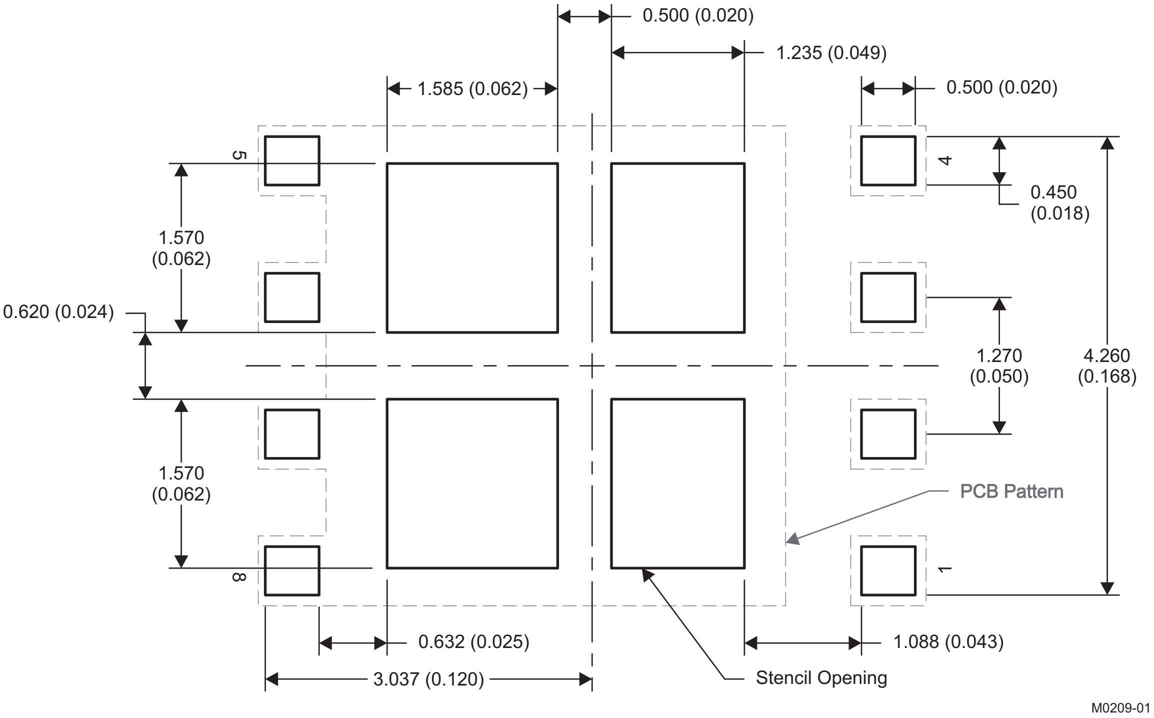
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.17	1.27	1.37
H	0.41	0.56	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°		12°

Recommended PCB Pattern



NOTE: Dimensions are in mm (inches).

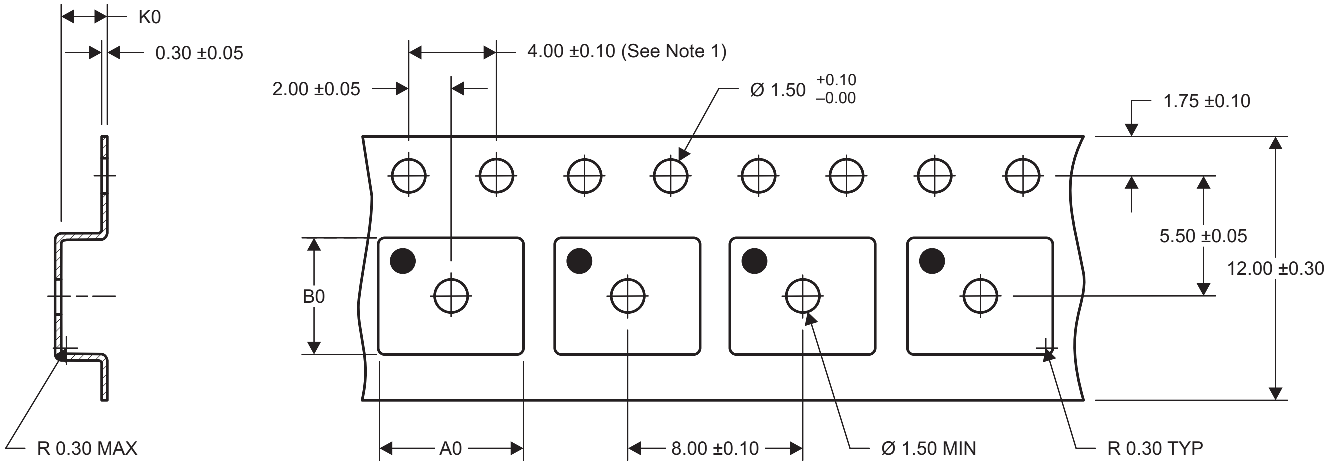
Stencil Recommendation



NOTE: Dimensions are in mm (inches).

For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Q5A Tape and Reel Information



A0 = 6.50 ±0.10
B0 = 5.30 ±0.10
K0 = 1.40 ±0.10

M0138-01

NOTES:
1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17555Q5A	Active	Production	VSONP (DQJ) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17555
CSD17555Q5A.B	Active	Production	VSONP (DQJ) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17555

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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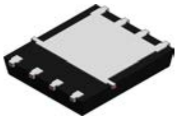
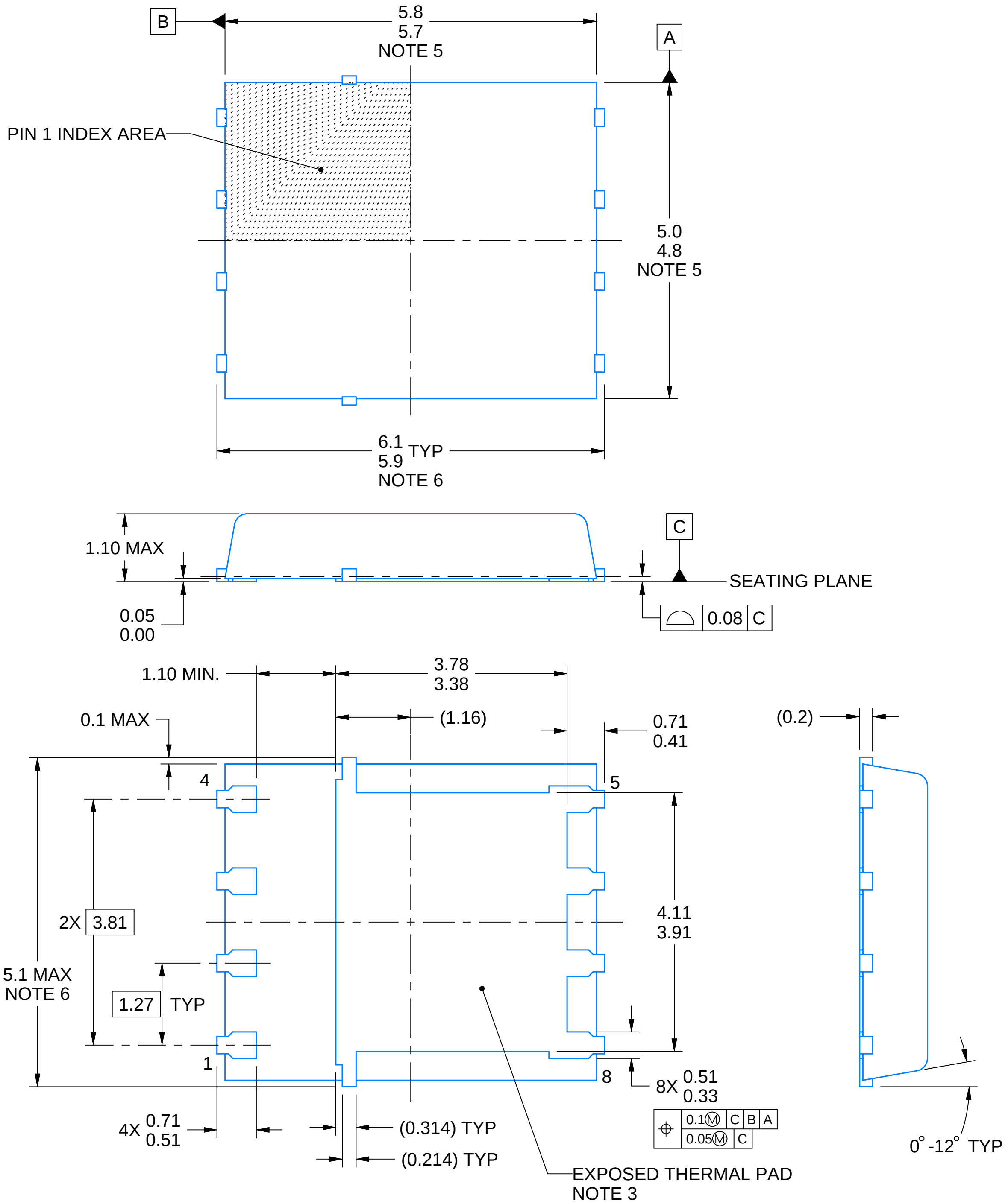


PACKAGE OUTLINE

DQJ0008A

VSONP - 1.1 mm max height

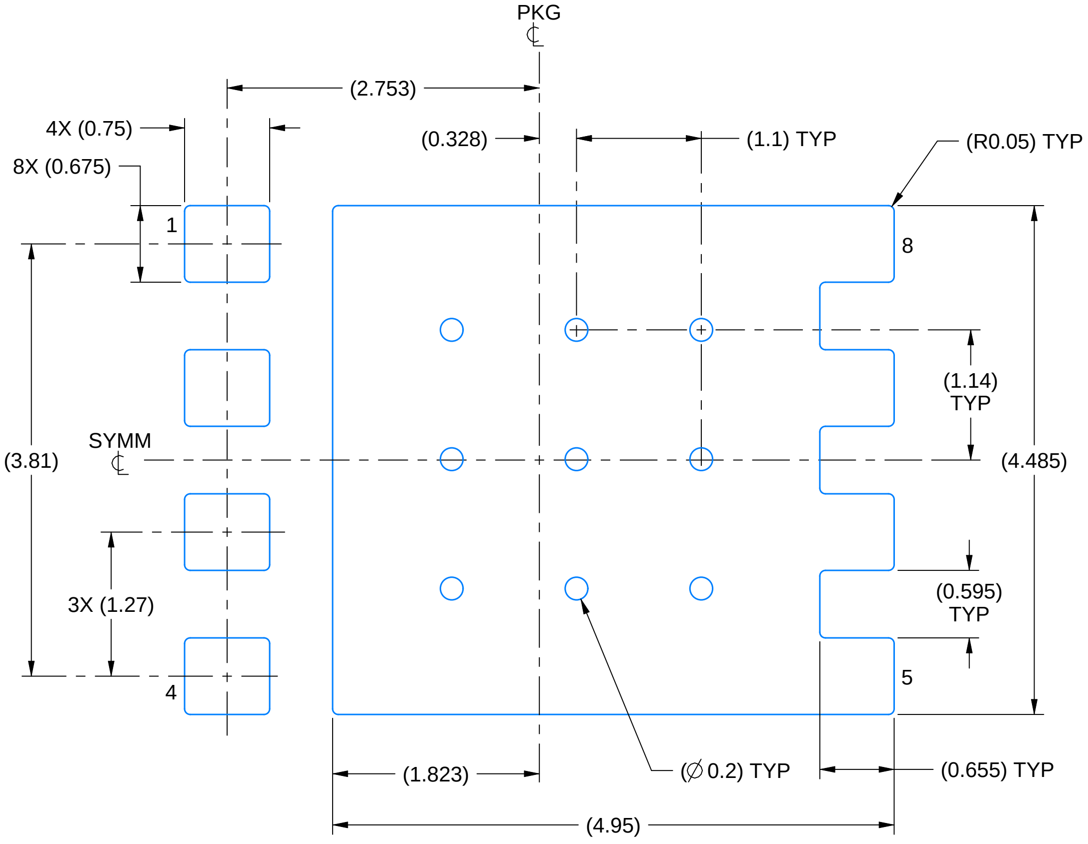
PLASTIC SMALL OUTLINE - NO LEAD



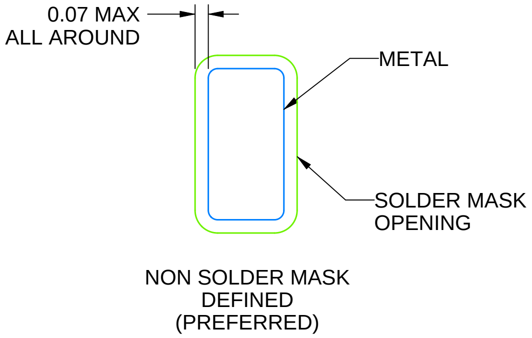
4218866/C 02/2025

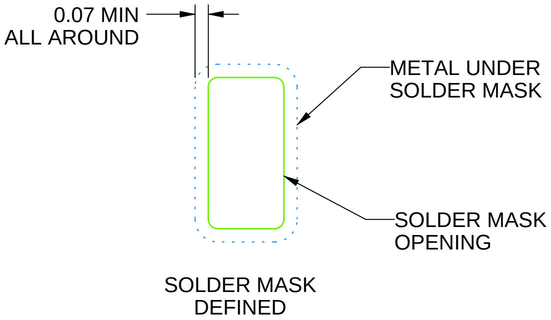
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. These dimensions do not include mold flash protrusions or gate burrs.
6. These dimensions include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 15X



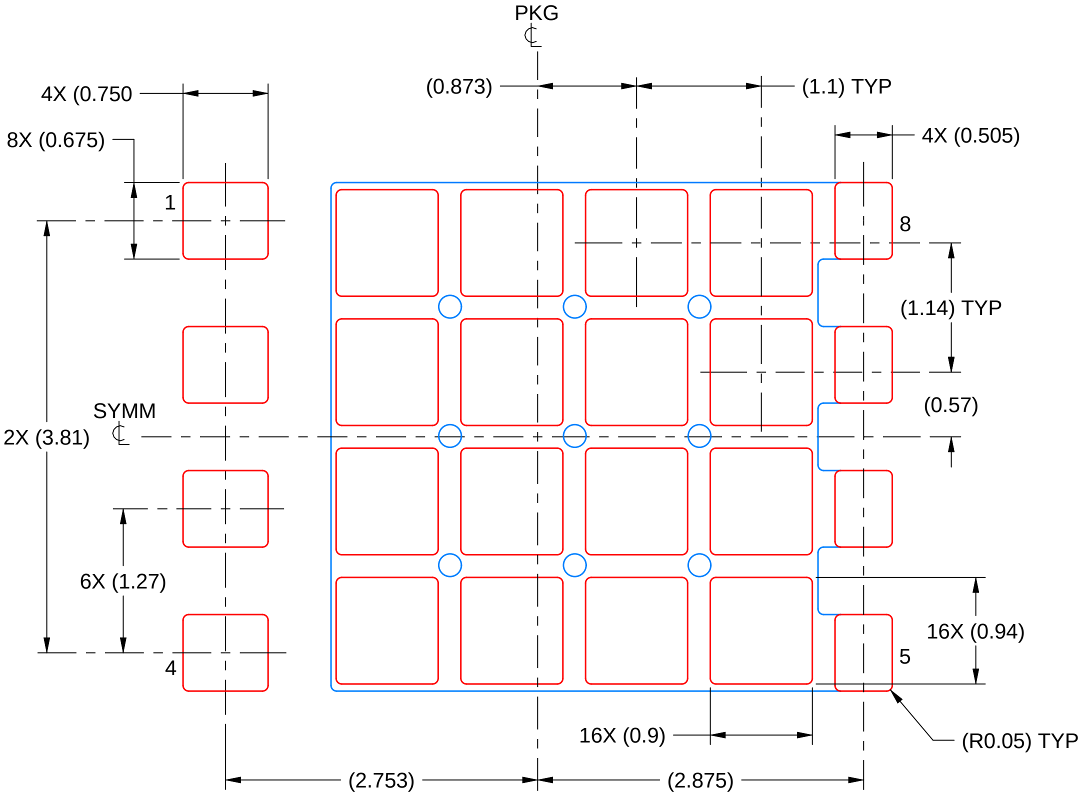


SOLDER MASK DETAILS

4218866/C 02/2025

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD:
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 15X

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

最后更新日期：2025 年 10 月