CSD17556Q5B 30V N 通道 NexFET™功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

- 极低电阻
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅引脚镀层
- 符合 RoHS 标准
- 无卤素
- SON 5mm × 6mm 塑料封装

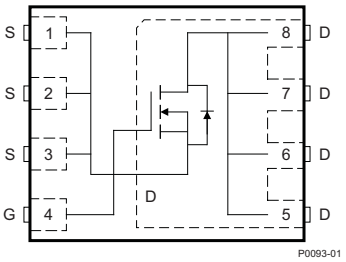
2 应用范围

- 网络互联、电信和计算系统中的负载点同步降压
- 同步整流
- 有源操作和热插拔 应用

3 说明

此 30V、1.2mΩ、5mm × 6mm NexFET™功率 MOSFET 旨在最大限度地减小同步整流和其他功率转换应用中的 损耗。

顶视图



P0093-01

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	30		V
Q_g	总栅极电荷 (4.5V)	30		nC
Q_{gd}	栅极电荷（栅极到漏极）	7.5		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 4.5 V	1.5	mΩ
		V_{GS} = 10V	1.2	
$V_{GS(th)}$	阈值电压	1.4		V

器件信息(1)

器件	数量	包装介质	封装	发货
CSD17556Q5B	2500	13 英寸卷带	SON 5.00-mm × 6.00-mm 塑料封装	卷带封装
CSD17556Q5BT	250			

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

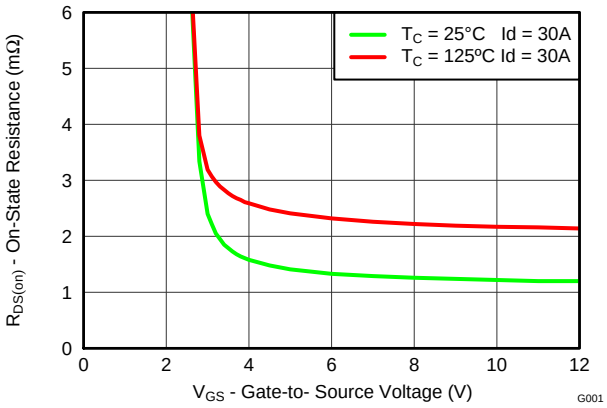
绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	30	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	100	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	215	
	持续漏极电流(1)	34	
I_{DM}	脉冲漏极电流，T_A = 25°C 时测得(1)(2)	400	A
P_D	功率耗散(1)	3.1	W
	功率耗散，T_C = 25°C 时测得	191	
T_J、T_{stg}	工作结温、储存温度	–55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D = 100A，L = 0.1mH，R_G = 25Ω	500	mJ

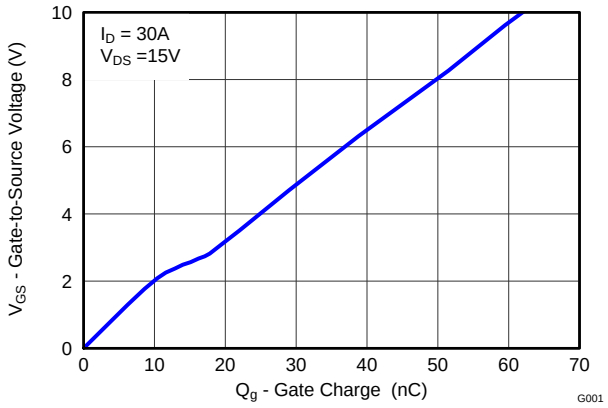
(1) 典型 $R_{\theta JA}$ = 40°C/W（当在 0.06 英寸 [1.52mm] 厚的 FR4 PCB 上将其安装在 1 平方英寸 [6.45cm^2] 2 oz [0.071mm] 厚的铜焊盘上时）。

(2) 最大 $R_{\theta JC}$ = 1.3°C/W，脉冲持续时间 ≤ 100µs，占空比 ≤ 1%。

$R_{DS(on)}$ 与 V_{GS} 对比



栅极电荷



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4 修订历史记录

Changes from Revision C (January 2017) to Revision D **Page**

- 更正了首页格式错误 2

Changes from Revision B (August 2014) to Revision C **Page**

- 已更改 *器件信息*表中的部件编号 1
- 已添加 *接收文档更新通知*部分和*社区资源*部分至*器件和文档支持*部分 8

Changes from Revision A (October 2013) to Revision B **Page**

- 将最大脉冲漏极电流增至 400A。 1
- 更新了脉冲漏极电流条件 1
- Updated Figure 1 to a normalized $R_{\theta JC}$ curve 5
- Updated the SOA in Figure 10 7
- 更新了机械制图和尺寸表以显示之前未知的尺寸 9

Changes from Original (March 2013) to Revision A **Page**

- 更新了机械数据部分中的尺寸表，新增 DIM“H”值 9

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

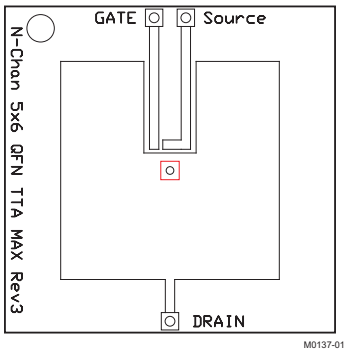
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 μA	30			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 24 V			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	1.15	1.4	1.65	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 4.5 V, I_{DS} = 40 A		1.5	1.8	mΩ
		V_{GS} = 10 V, I_{DS} = 40 A		1.2	1.4	
g_{fs}	Transconductance	V_{DS} = 15 V, I_{DS} = 40 A		197		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		5400	7020	pF
C_{oss}	Output capacitance			1770	2310	pF
C_{rss}	Reverse transfer capacitance			68	88	pF
R_G	Series gate resistance			0.7	1.4	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15 V, I_{DS} = 40 A		30	39	nC
Q_{gd}	Gate charge gate-to-drain			7.5		nC
Q_{gs}	Gate charge gate-to-source			11		nC
$Q_{g(th)}$	Gate charge at V_{th}			6.1		nC
Q_{oss}	Output charge	V_{DS} = 15 V, V_{GS} = 0 V		48		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{DS} = 40 A, R_G = 2 Ω		14		ns
t_r	Rise time			26		ns
$t_{d(off)}$	Turnoff delay time			27		ns
t_f	Fall time			12		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 40 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse recovery charge	V_{DD}= 15 V, I_F = 40 A, di/dt = 300 A/μs		68		nC
t_{rr}	Reverse recovery time			36		ns

5.2 Thermal Information

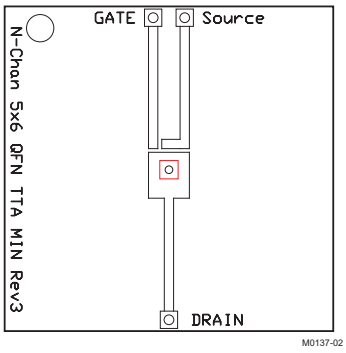
T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance(1)			1.3	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)(2)			50	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1-in^2 (6.45-cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

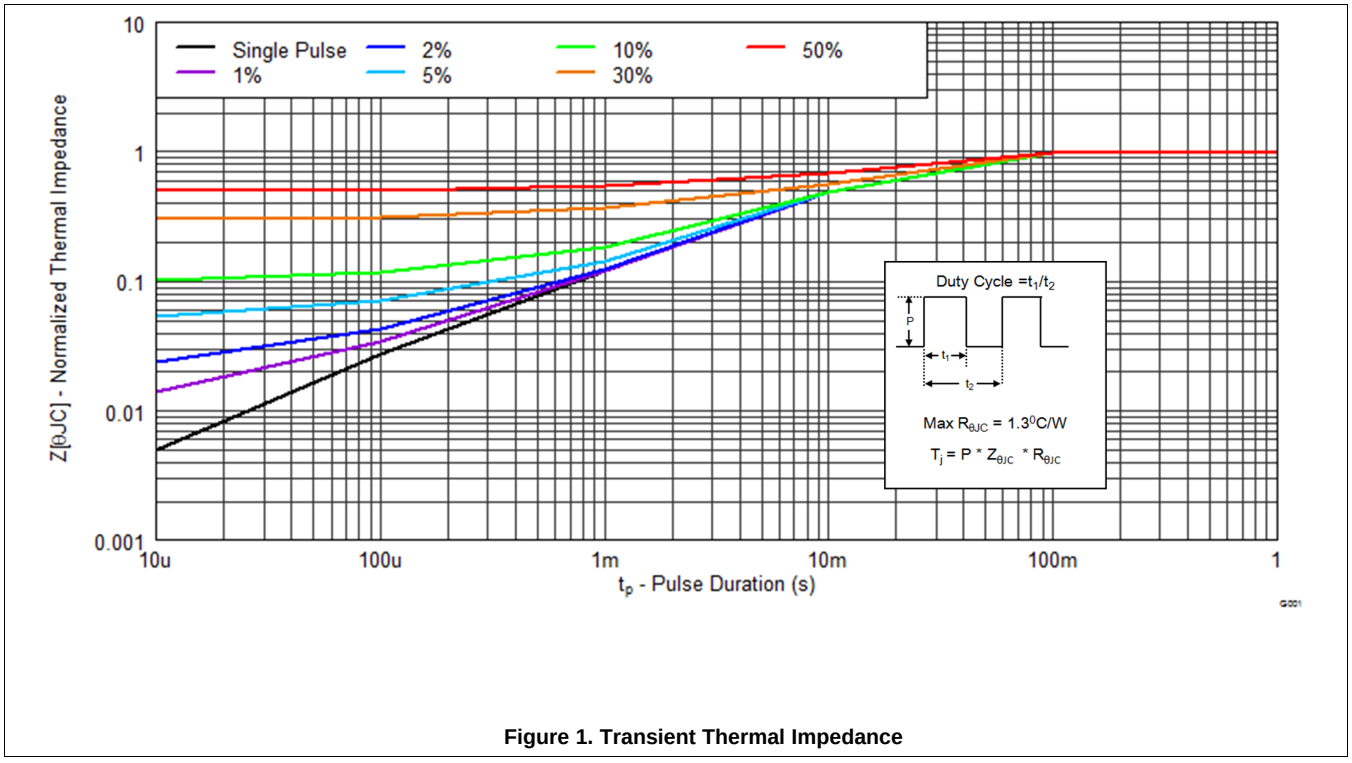


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

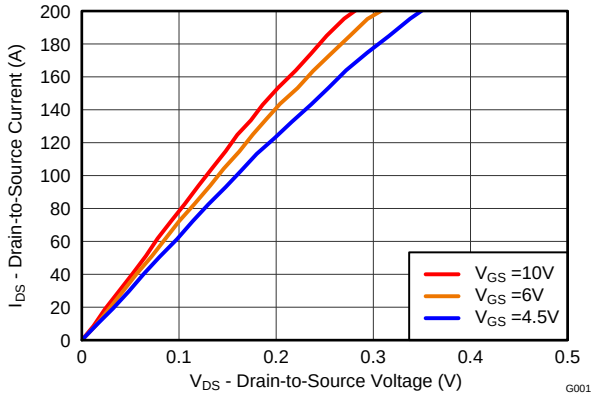


Figure 2. Saturation Characteristics

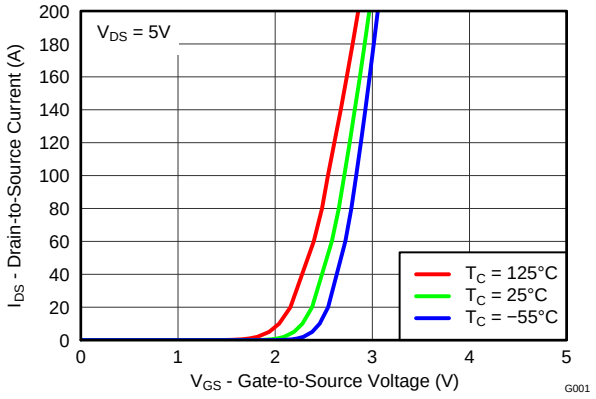


Figure 3. Transfer Characteristics

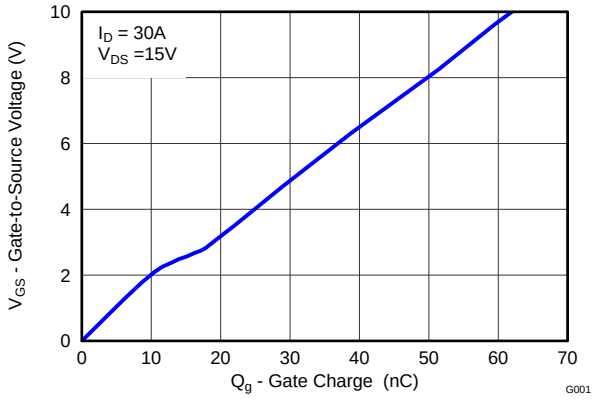


Figure 4. Gate Charge

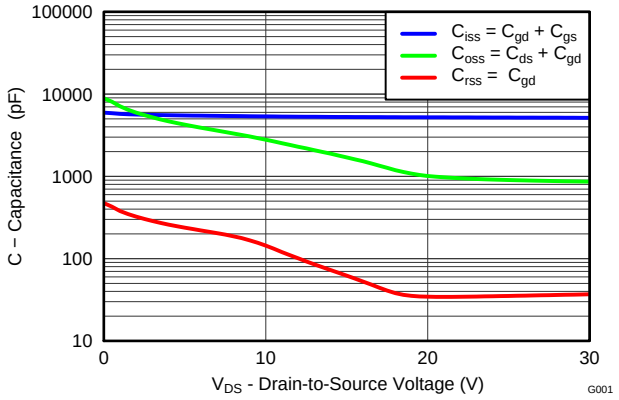


Figure 5. Capacitance

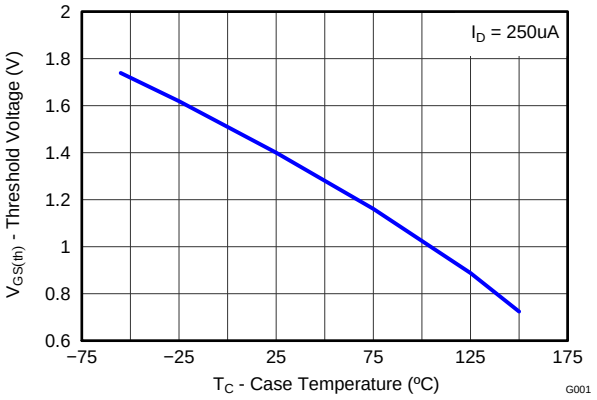


Figure 6. Threshold Voltage vs Temperature

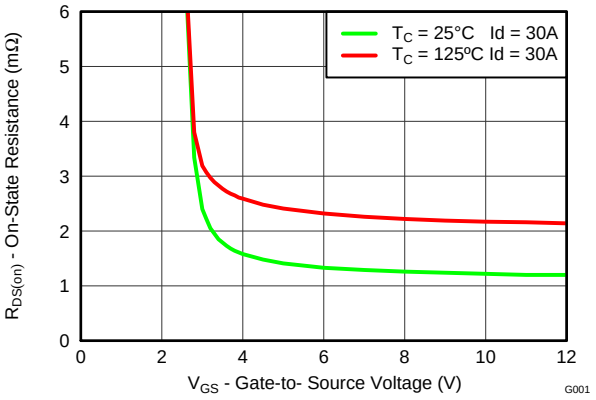


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

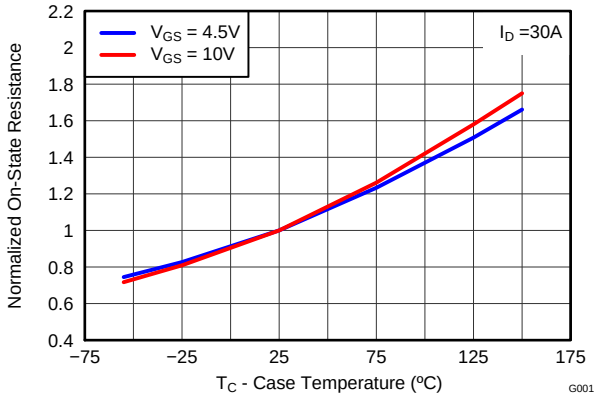


Figure 8. Normalized On-State Resistance vs Temperature

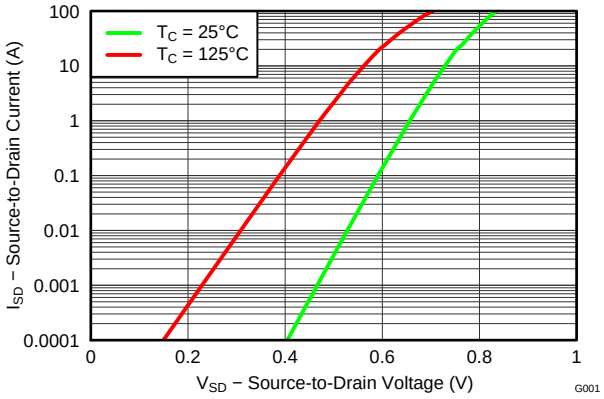


Figure 9. Typical Diode Forward Voltage

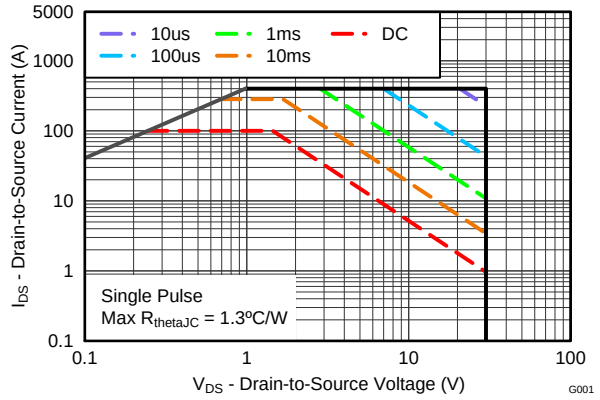


Figure 10. Maximum Safe Operating Area (SOA)

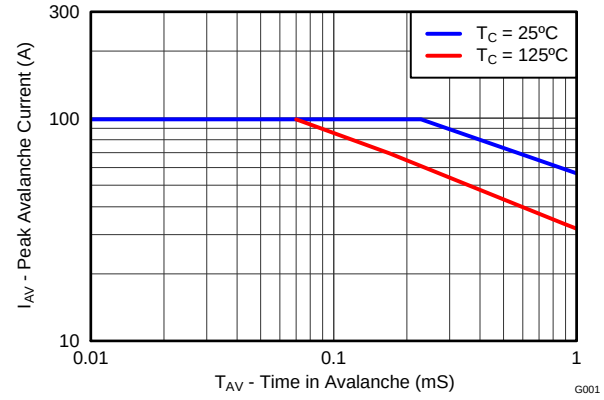


Figure 11. Single Pulse Unclamped Inductive Switching

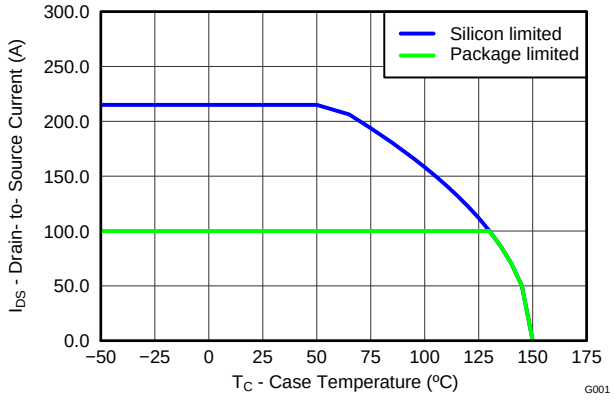


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 接收文档更新通知

如需接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

6.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

6.3 商标

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

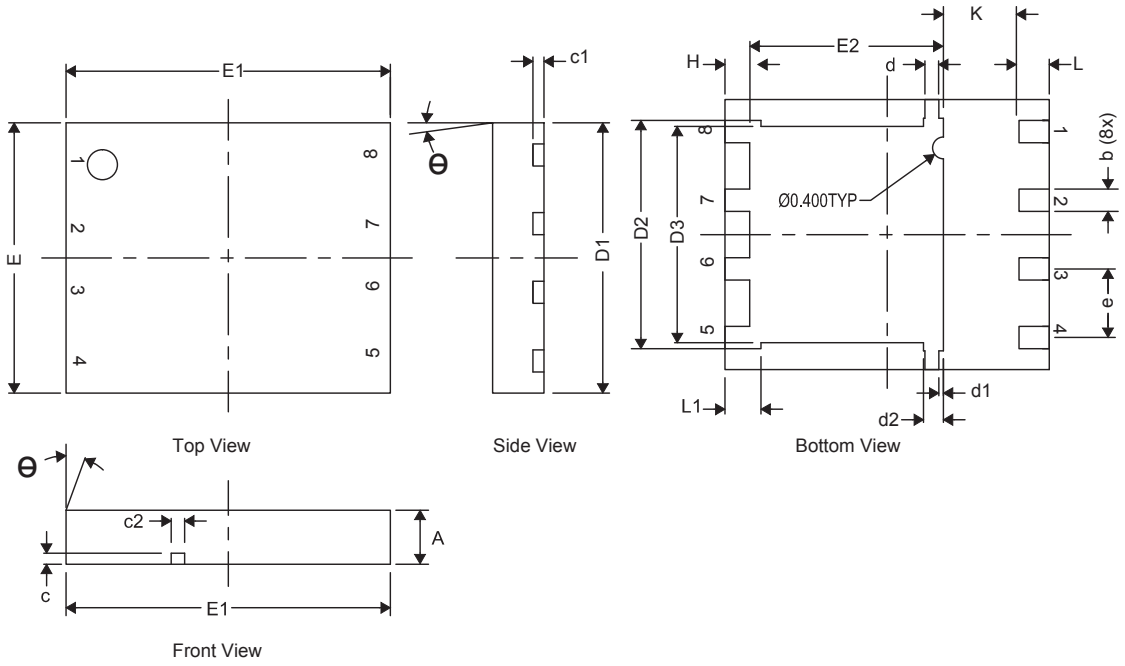
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

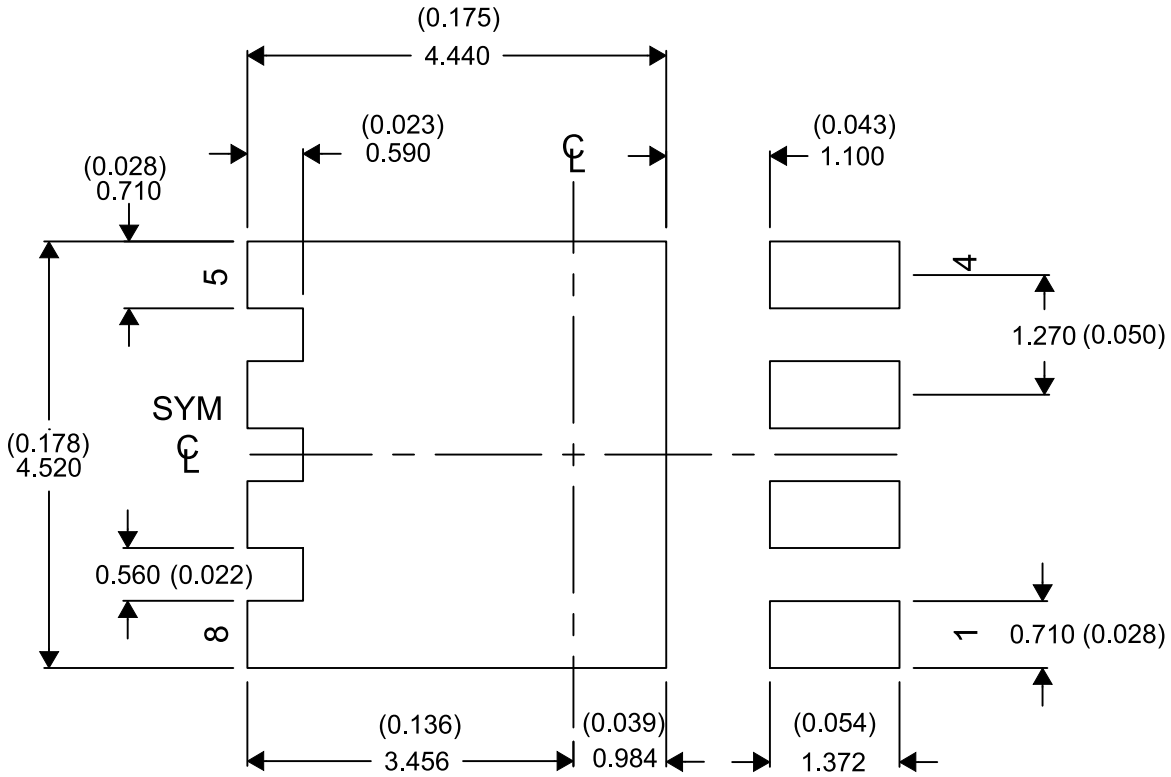
以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

7.1 Q5B 封装尺寸



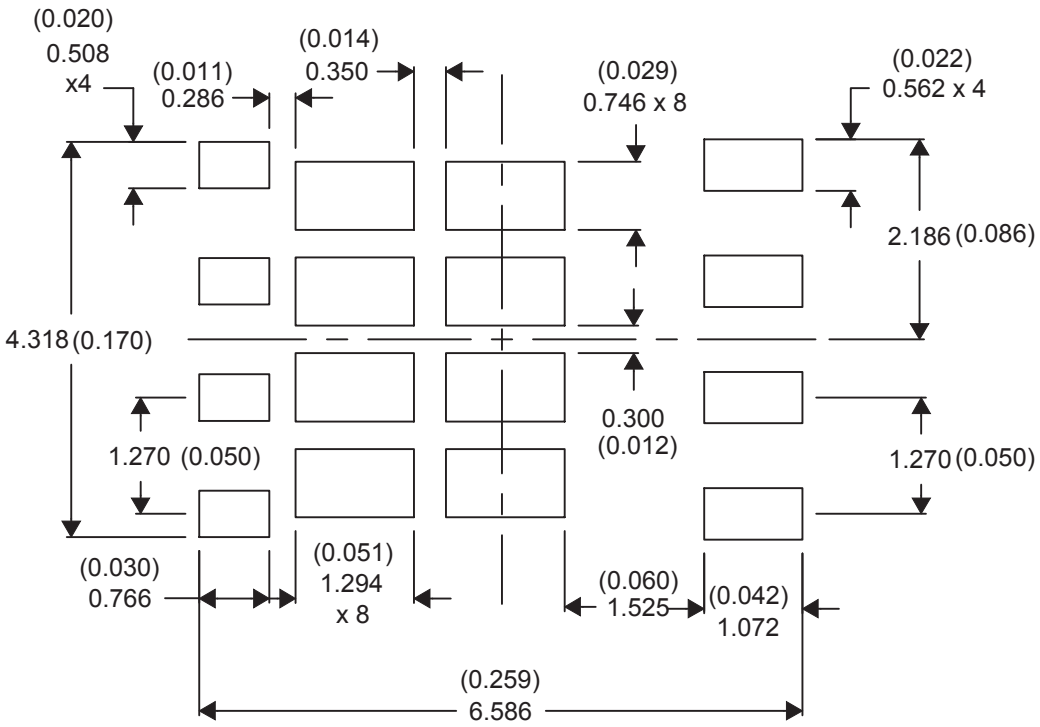
DIM	毫米		
	最小值	标称值	最大值
A	0.80	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
D3	3.90	4.00	4.10
d	0.20	0.25	0.30
d1	0.085 典型值		
d2	0.319	0.369	0.419
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e	1.27 典型值		
H	0.36	0.46	0.56
L	0.46	0.56	0.66
L1	0.57	0.67	0.77
θ	0°	—	—
K	1.40 典型值		

7.2 建议 PCB 布局

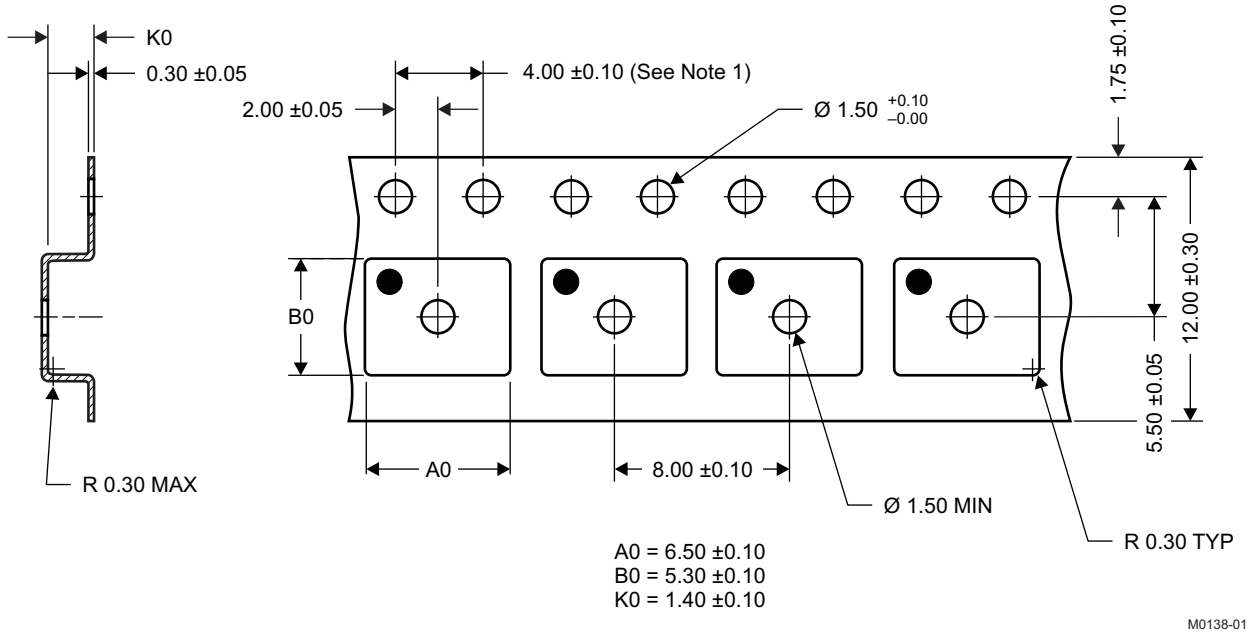


如需了解针对 PCB 设计的建议电路布局，请参阅*《通过 PCB 布局技巧来减少振铃》*(SLPA005)。

7.3 建议模板布局



7.4 Q5B 卷带信息



注释：

1. 10 个链齿孔的累积容差为 ±0.2。
2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积。
3. 材料：黑色抗静电聚苯乙烯。
4. 全部尺寸为 mm（除非另外注明）。
5. 高于孔眼底部 0.3mm 的平面上测量得到 A0 和 B0 值.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17556Q5B	Active	Production	VSON-CLIP (DNK) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17556
CSD17556Q5B.B	Active	Production	VSON-CLIP (DNK) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17556
CSD17556Q5BT	Active	Production	VSON-CLIP (DNK) | 8	250 | SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17556
CSD17556Q5BT.B	Active	Production	VSON-CLIP (DNK) | 8	250 | SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17556

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

重要通知和免责声明

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最后更新日期：2025 年 10 月