

CSD18510KTT 40V N 沟道 NexFET™ 功率 MOSFET

1 特性

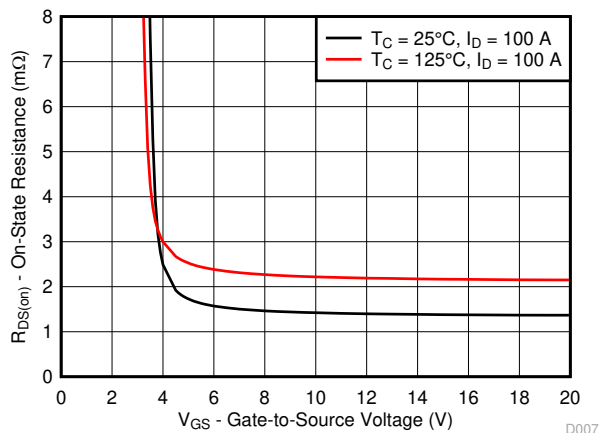
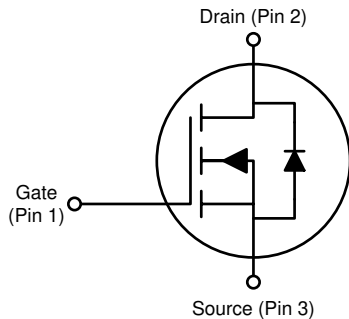
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅端子镀层
- 符合 RoHS
- 无卤素
- D²PAK 塑料封装

2 应用

- 次级侧同步整流器
- 电机控制

3 说明

这款 40V、1.4m Ω 、D²PAK (TO-263) NexFET™ 功率 MOSFET 旨在用于更大限度地降低功率转换应用中的损耗。

 $R_{DS(on)}$ 与 V_{GS} 之间的关系

D007

产品概要

$T_A = 25^\circ\text{C}$		典型值	单位
V_{DS}	漏源电压	40	V
Q_g	栅极电荷总量 (10V)	119	nC
Q_{gd}	栅极电荷 (栅极到漏极)	21	nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 4.5\text{V}$	2.0
		$V_{GS} = 10\text{V}$	1.4
$V_{GS(th)}$	阈值电压	1.7	V

器件信息 (1)

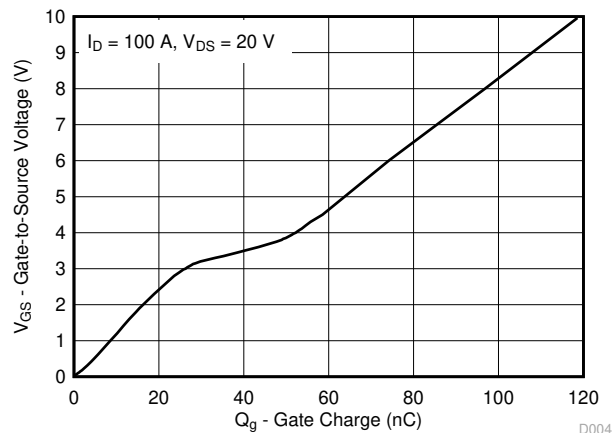
器件	数量	介质	封装	运输
CSD18510KTT	500	13 英寸卷带	D ² PAK 塑料封装	卷带包装
CSD18510KTTT	50			

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

绝对最大额定值

$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源电压	40	V
V_{GS}	栅源电压	± 20	V
I_D	持续漏极电流 (受封装限制)	200	A
	持续漏极电流 (受器件限制), $T_C = 25^\circ\text{C}$ 时测得	274	
	持续漏极电流 (受器件限制), $T_C = 100^\circ\text{C}$ 时测得	193	
I_{DM}	脉冲漏极电流 ⁽¹⁾	400	A
P_D	功率耗散	250	W
T_J , T_{stg}	工作结温, 贮存温度	-55 至 175	$^\circ\text{C}$
E_{AS}	雪崩能量, 单脉冲 $I_D = 81\text{A}$, $L = 0.1\text{mH}$, $R_G = 25\Omega$	328	mJ

(1) 最大 $R_{\theta JC} = 0.6^\circ\text{C/W}$, 脉冲持续时间 $\leq 100 \mu\text{s}$, 占空比 $\leq 1\%$ 。



栅极电荷

D004



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4 Specifications

4.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0V, I _D = 250 μ A	40			V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0V, V _{DS} = 32V			1	μ A
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0V, V _{GS} = 20V			100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 250 μ A	1.4	1.7	2.3	V
R _{DS(on)}	Drain-to-source on resistance	V _{GS} = 4.5V, I _D = 100A		2.0	2.6	mΩ
		V _{GS} = 10V, I _D = 100A		1.4	1.7	
g _{fs}	Transconductance	V _{DS} = 4V, I _D = 100A		330		S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance	V _{GS} = 0V, V _{DS} = 20V, f = 1MHz		8770	11400	pF
C _{oss}	Output capacitance			832	1080	pF
C _{rss}	Reverse transfer capacitance			424	551	pF
R _G	Series gate resistance			0.9	1.8	Ω
Q _g	Gate charge total (4.5V)	V _{DS} = 20V, I _D = 100A		58	75	nC
Q _g	Gate charge total (10V)			118	153	nC
Q _{gd}	Gate charge gate-to-drain			21		nC
Q _{gs}	Gate charge gate-to-source			28		nC
Q _{g(th)}	Gate charge at V _{th}			15		nC
Q _{oss}	Output charge		V _{DS} = 20V, V _{GS} = 0V		35	
t _{d(on)}	Turnon delay time	V _{DS} = 20V, V _{GS} = 10V, I _{DS} = 100A, R _G = 0Ω		10		ns
t _r	Rise time			8		ns
t _{d(off)}	Turnoff delay time			29		ns
t _f	Fall time			8		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 100A, V _{GS} = 0V		0.85	1.0	V
Q _{rr}	Reverse recovery charge	V _{DS} = 20V, I _F = 100A,		70		nC
t _{rr}	Reverse recovery time	di/dt = 300A/ μ s		41		ns

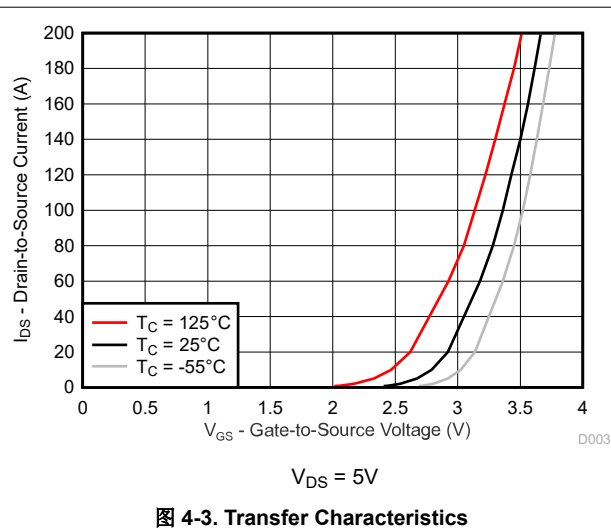
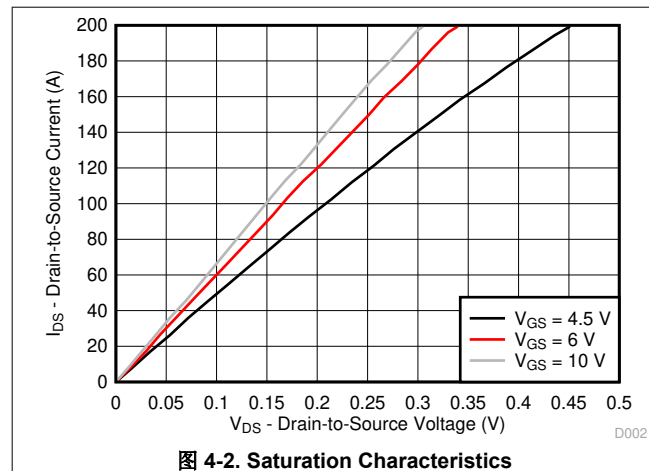
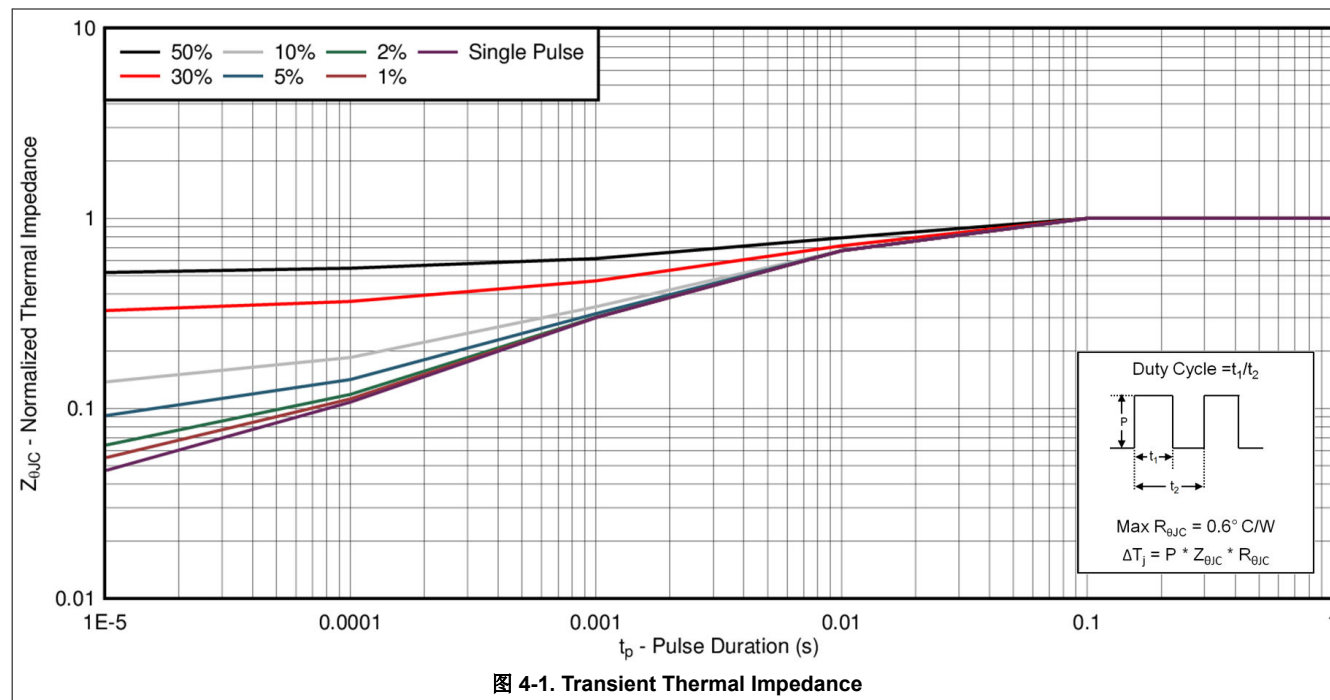
4.2 Thermal Information

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			0.6	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance			62	$^\circ\text{C/W}$

4.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)



4.3 Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

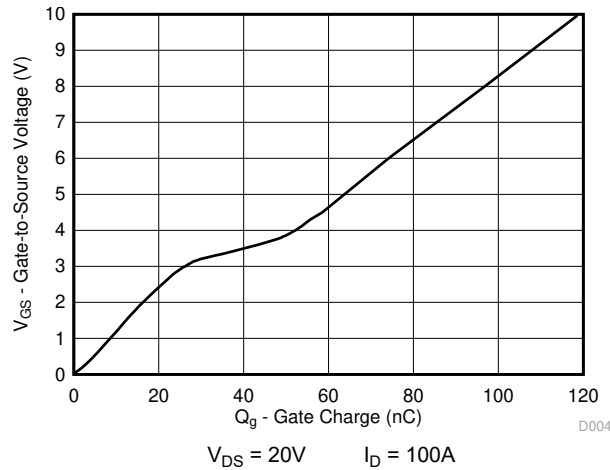


图 4-4. Gate Charge

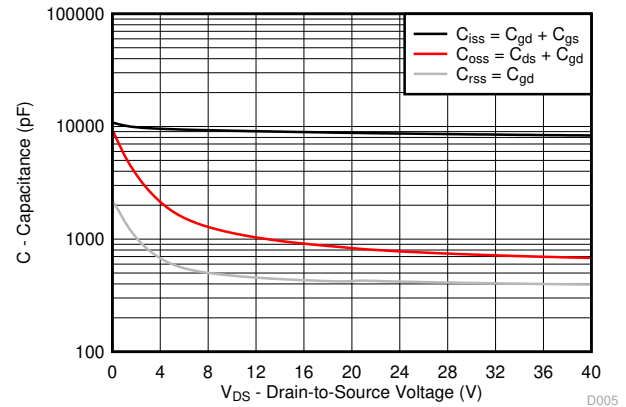


图 4-5. Capacitance

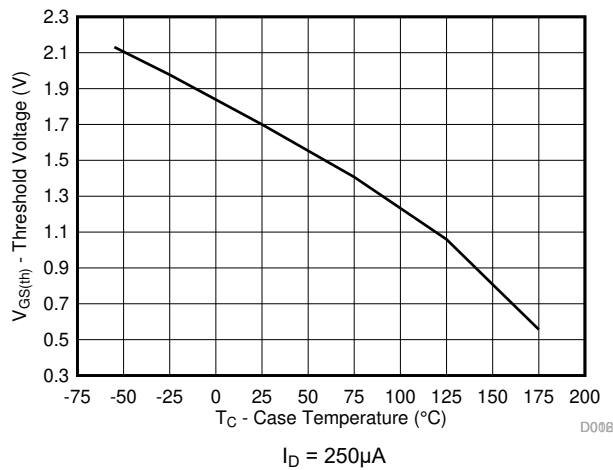


图 4-6. Threshold Voltage vs Temperature

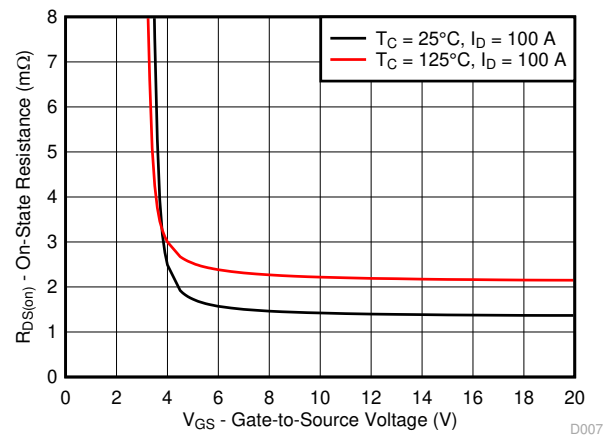


图 4-7. On-State Resistance vs Gate-to-Source Voltage

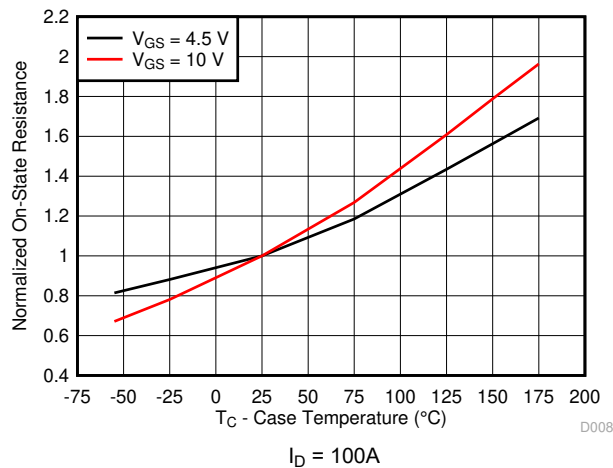


图 4-8. Normalized On-State Resistance vs Temperature

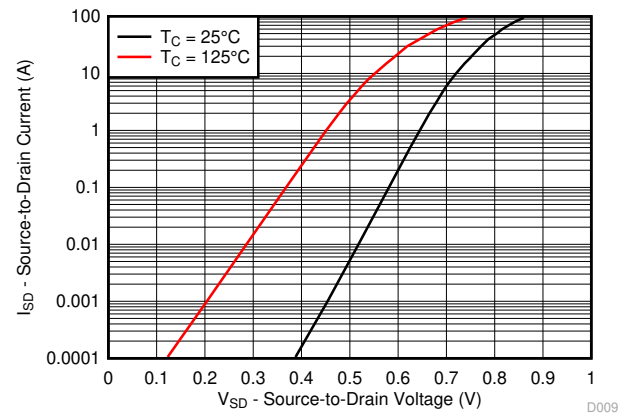


图 4-9. Typical Diode Forward Voltage

4.3 Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

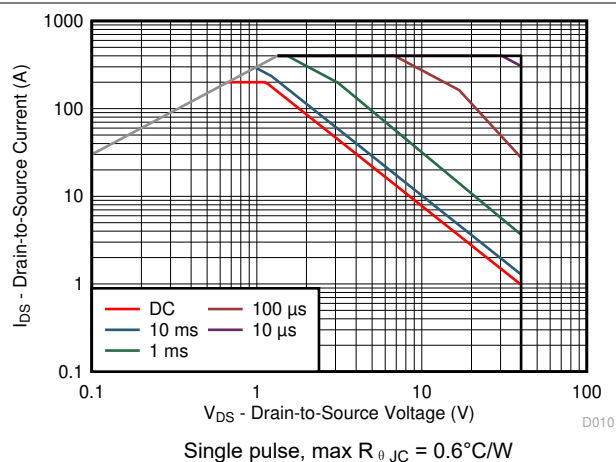


图 4-10. Maximum Safe Operating Area

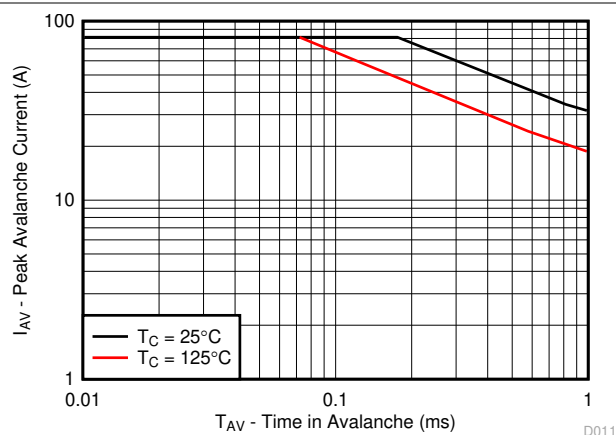


图 4-11. Single Pulse Unclamped Inductive Switching

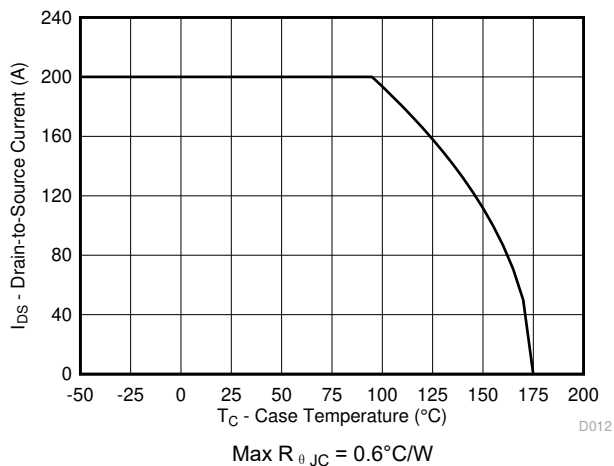


图 4-12. Maximum Drain Current vs Temperature

5 器件和文档支持

5.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.2 支持资源

TI E2E™ 中文支持论坛 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

5.3 Trademarks

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5.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

5.5 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

6 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (November 2022) to Revision C (June 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
Changes from Revision A (January 2017) to Revision B (November 2022)	Page
• Updated 图 4-3	4
Changes from Revision * (November 2016) to Revision A (January 2017)	Page
• 在 <i>绝对最大额定值</i> 表中将 $T_C = 25^\circ\text{C}$ 时的器件电流限制从 237A 更改为 274A.....	1
• 在 <i>绝对最大额定值</i> 表中将 $T_C = 100^\circ\text{C}$ 时的器件电流限制从 167A 更改为 193A.....	1
• 在 <i>绝对最大额定值</i> 表中将最大功耗从 188W 更改为 250W.....	1
• Changed the charge values in the Dynamic Characteristics section of the <i>Electrical Characteristics</i> table.....	3
• Changed max $R_{\theta JC}$ from 0.8°C/W to 0.6°C/W in the <i>Thermal Information</i> table.....	3
• Changed 图 4-4 in the <i>Typical MOSFET Characteristics</i> section to reflect updated gate charges.....	4

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD18510KTT	Active	Production	DDPAK/ TO-263 (KTT) 2	500 LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18510KTT
CSD18510KTT.B	Active	Production	DDPAK/ TO-263 (KTT) 2	500 LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18510KTT
CSD18510KTTT	Active	Production	DDPAK/ TO-263 (KTT) 2	50 SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18510KTT
CSD18510KTTT.B	Active	Production	DDPAK/ TO-263 (KTT) 2	50 SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18510KTT

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD18510KTT	DDPAK/ TO-263	KTT	2	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
CSD18510KTTT	DDPAK/ TO-263	KTT	2	50	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

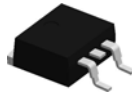
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD18510KTT	DDPAK/TO-263	KTT	2	500	340.0	340.0	38.0
CSD18510KTTT	DDPAK/TO-263	KTT	2	50	340.0	340.0	38.0

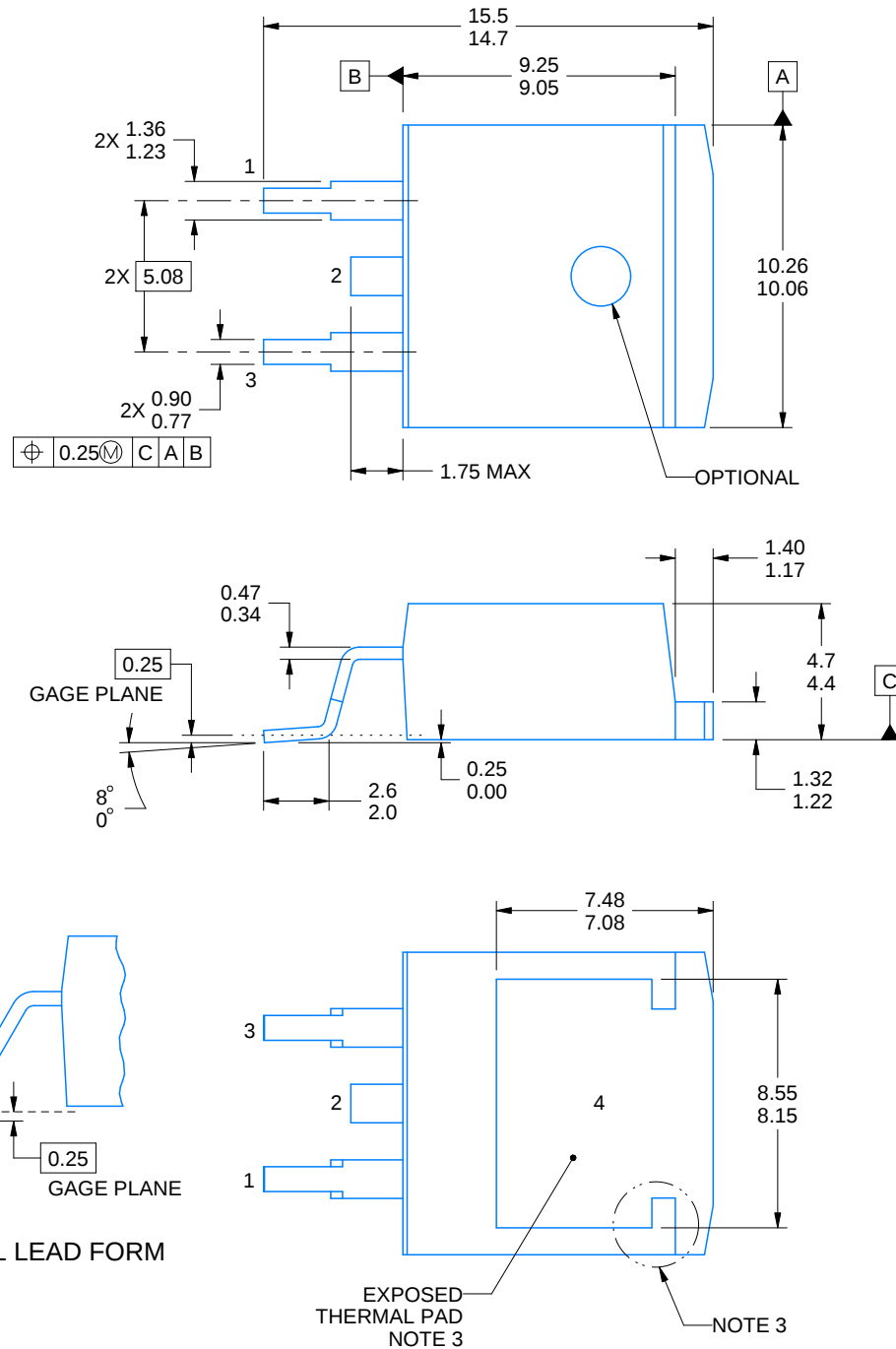
KTT0002A



PACKAGE OUTLINE

TO-263 - 4.7 mm max height

TRANSISTOR OUTLINE



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NOTES:

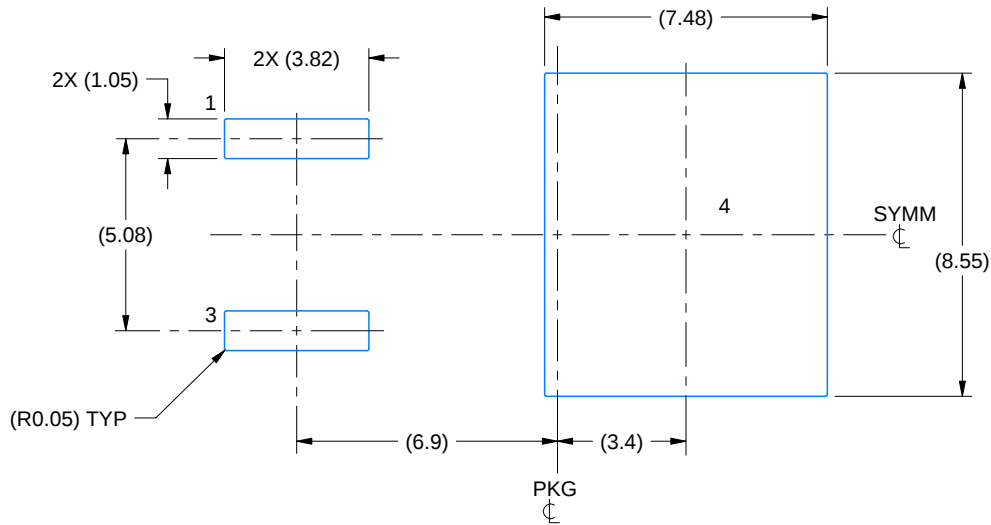
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites. Pin 2 and Pin 4 connected.
4. Reference JEDEC registration TO-263.

EXAMPLE BOARD LAYOUT

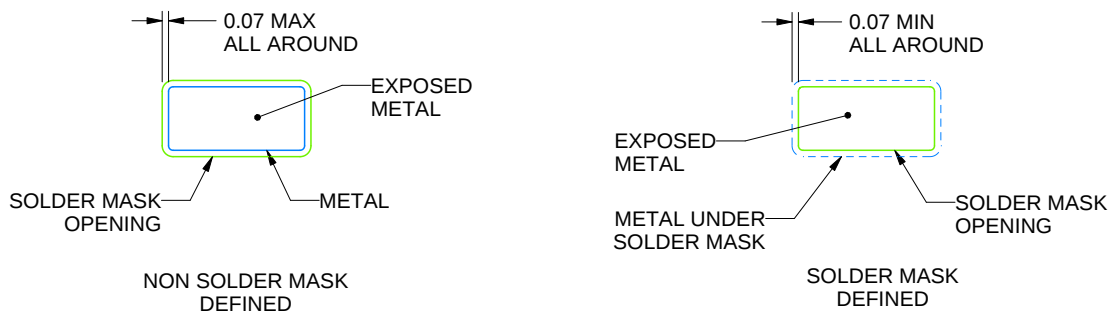
KTT0002A

TO-263 - 4.7 mm max height

TRANSISTOR OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:5X



SOLDER MASK DETAILS

4222117/D 08/2025

NOTES: (continued)

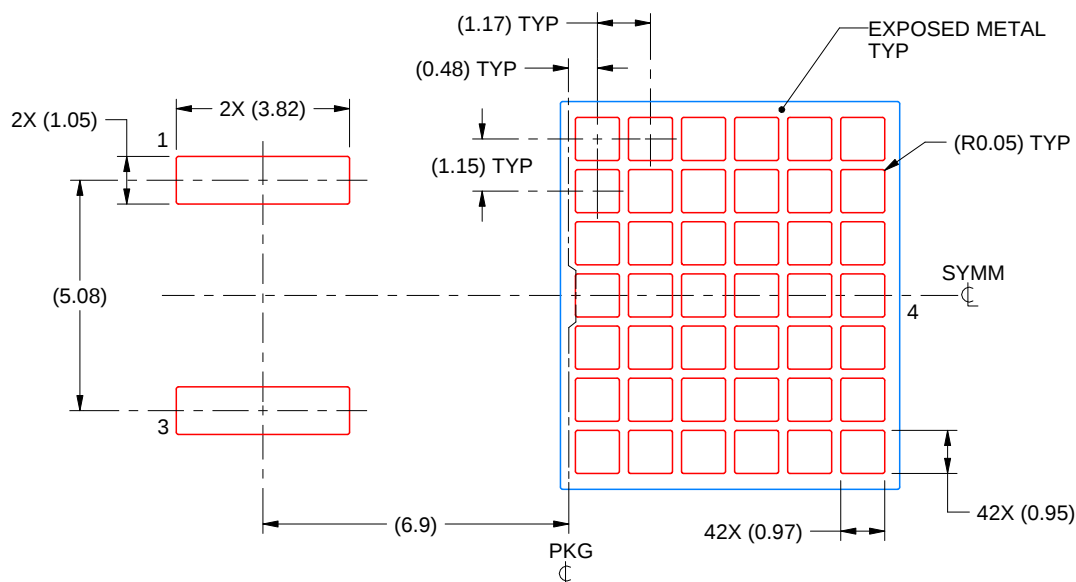
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KTT0002A

TO-263 - 4.7 mm max height

TRANSISTOR OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60.5% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

4222117/D 08/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

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