CSD23202W10 12V P 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

- 超低 Q_g 和 Q_{gd}
- 小尺寸封装 1mm x 1mm
- 薄型，0.62mm 高度
- 无铅
- 栅极静电放电 (ESD) 保护 - 3kV
- 符合 RoHS 环保标准
- 无卤素

2 应用范围

- 电池管理
- 负载开关
- 电池保护

3 说明

这款 12V，44mΩ 器件设计用于在超薄且具有出色散热特性的 1mm × 1mm 小外形
封装内提供最低的导通电阻和栅极电荷。

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	-12		V
Q_g	栅极电荷总量 (-4.5V)	2.9		nC
Q_{gd}	栅漏栅极电荷	0.28		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = –1.5V	82	mΩ
		V_{GS} = –1.8V	67	mΩ
		V_{GS} = -2.5V	54	mΩ
		V_{GS} = -4.5V	44	mΩ
$V_{GS(th)}$	阈值电压	–0.60		V

订购信息(1)

器件	数量	介质	封装	出货
CSD23202W10	3000	7 英寸卷带	1 x 1mm 晶圆级封装	卷带封装
CSD23202W10T	250	7 英寸卷带		

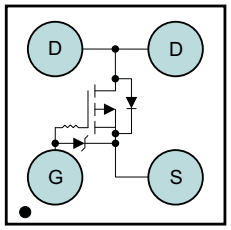
(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

最大绝对额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	-12	V
V_{GS}	栅源电压	-6	V
I_D	持续漏极电流(1)	–2.2	A
I_{DM}	脉冲漏极电流(2)	–25	A
I_G	持续栅极钳位电流	-0.5	A
	脉冲栅极钳位电流	-7	A
P_D	功率耗散(1)	1	W
T_J, T_{stg}	运行结温和储存温度范围	-55 至 150	°C

(1) 器件在 105ºC 温度下运行
(2) $R_{\theta JA}$ 典型值 = 195°C/W，脉宽 ≤ 100µs，占空比 ≤ 1%

顶视图



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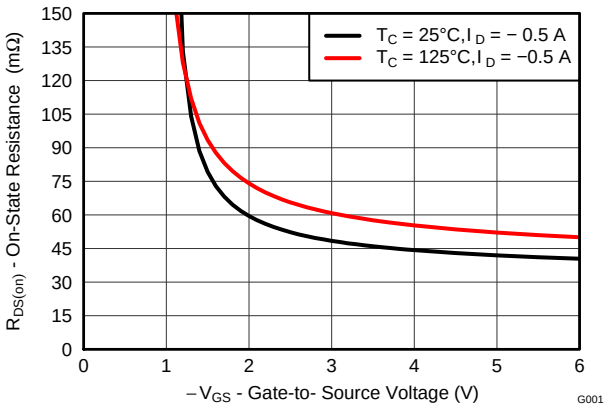
$R_{DS(on)}$ 与 V_{GS} 间的关系



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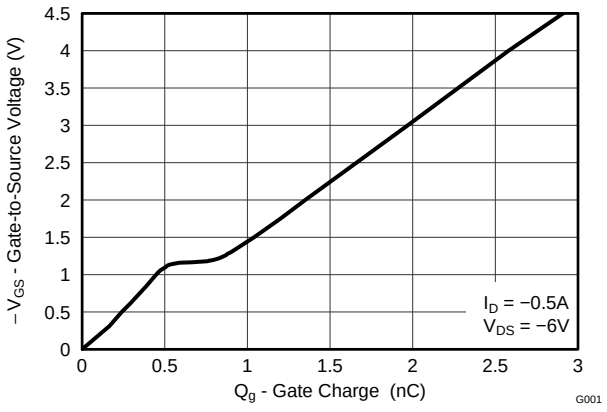
栅极电荷



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4 修订历史记录

日期	修订版本	注释
2014 年 8 月	*	最初发布。

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

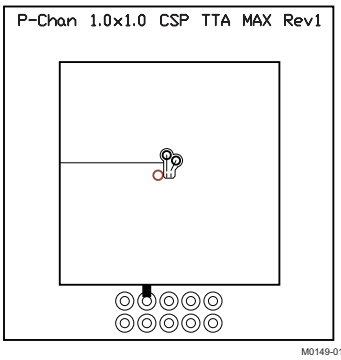
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = –250 µA	–12			V
BV_{GSS}	Gate-to-Source Voltage;	V_{DS} = 0 V, I_G = –250 µA	–6		–7.2	V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = –9.6 V			–1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = –6 V			–100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 µA	–0.4	–0.6	–0.9	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.5 V, I_D = –0.5 A		82	123	mΩ
		V_{GS} = –1.8 V, I_D = –0.5 A		67	92	mΩ
		V_{GS} = –2.5 V, I_D = –0.5 A		54	66	mΩ
		V_{GS} = –4.5 V, I_D = –0.5 A		44	53	mΩ
g_{fs}	Transconductance	V_{DS} = –1.2 V, I_D = –0.5 A		5.6		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = –6.0 V, f = 1 MHz		394	512	pF
C_{OSS}	Output Capacitance			238	310	pF
C_{RSS}	Reverse Transfer Capacitance			29	37	pF
Q_g	Gate Charge Total (–4.5 V)	V_{DS} = –6 V, I_D = –0.5 A		2.9	3.8	nC
Q_{gd}	Gate Charge Gate-to-Drain			0.28		nC
Q_{gs}	Gate Charge Gate-to-Source			0.55		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.29		nC
Q_{OSS}	Output Charge	V_{DS} = –6 V, V_{GS} = 0 V		2.0		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –6 V, V_{GS} = –4.5 V, I_D = –0.5 A R_G = 0 Ω		9		ns
t_r	Rise Time			4		ns
$t_{d(off)}$	Turn Off Delay Time			58		ns
t_f	Fall Time			21		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_S = –0.5 A, V_{GS} = 0 V		–0.66	–1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= –6 V, I_F = –0.5 A, di/dt = 100 A/µs		3.7		nC
t_{rr}	Reverse Recovery Time			12		ns

5.2 Thermal Information

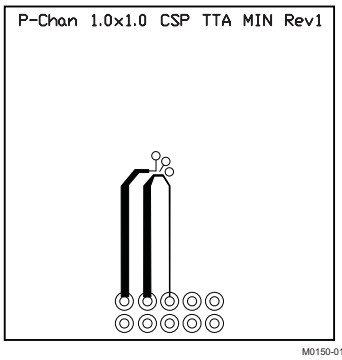
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)		195		°C/W
	Junction-to-Ambient Thermal Resistance(2)		65		

(1) Device mounted on FR4 material with minimum Cu mounting area.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Typical $R_{\theta JA}$ = 65°C/W when mounted on 1 inch^2 of 2 oz. Cu.



Typical $R_{\theta JA}$ = 195°C/W when mounted on minimum pad area of 2 oz. Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

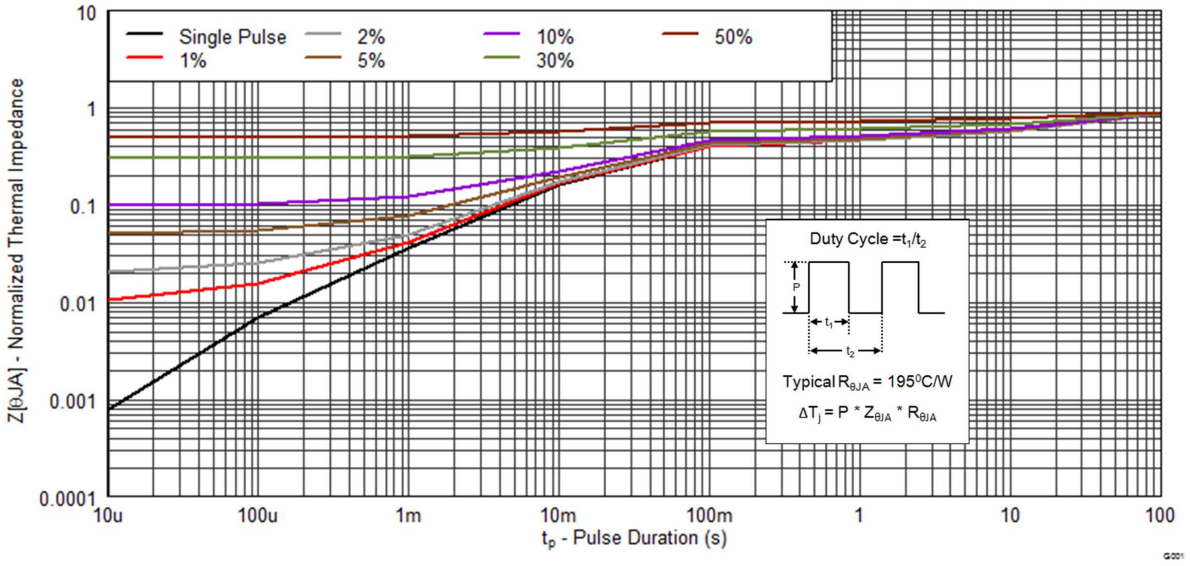


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

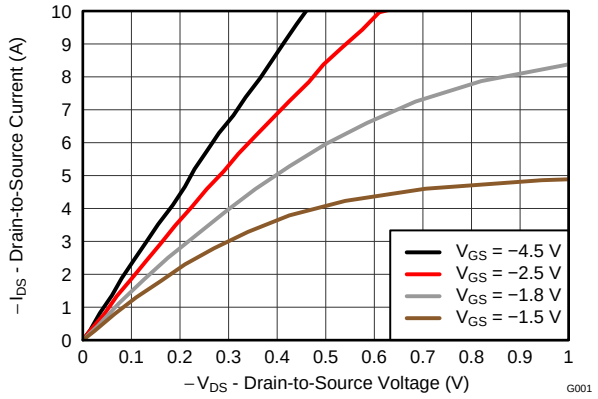


Figure 2. Saturation Characteristics

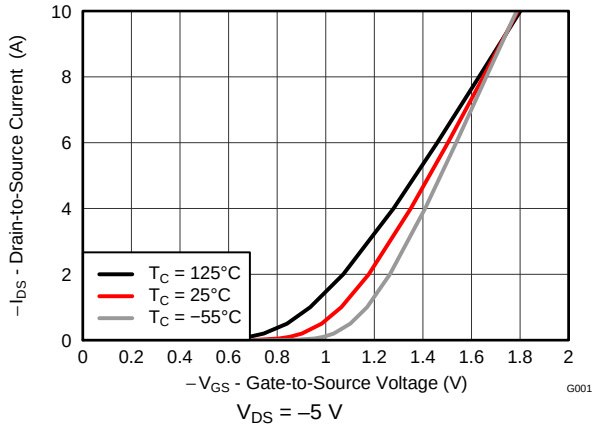


Figure 3. Transfer Characteristics

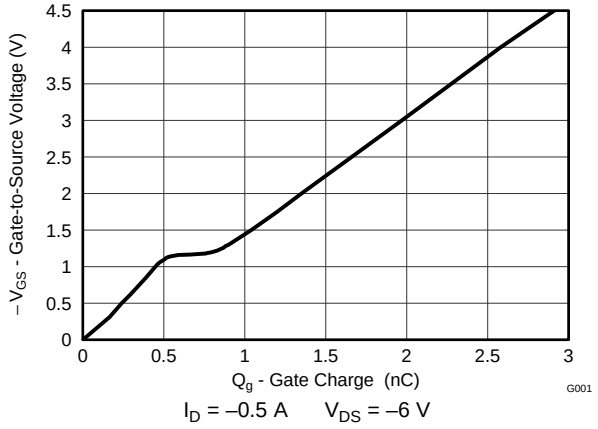


Figure 4. Gate Charge

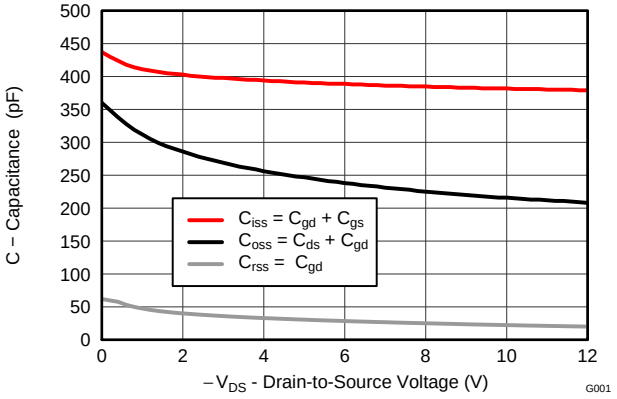


Figure 5. Capacitance

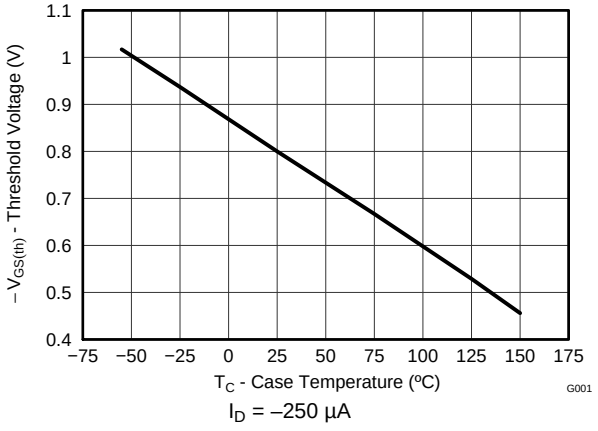


Figure 6. Threshold Voltage vs Temperature

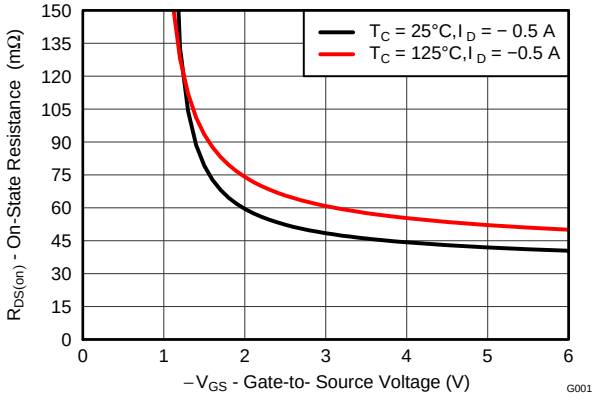


Figure 7. On-State Drain-to-Source Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

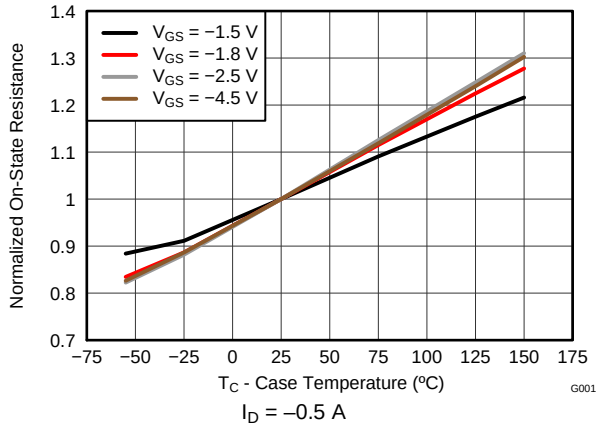


Figure 8. Normalized On-State Resistance vs Temperature

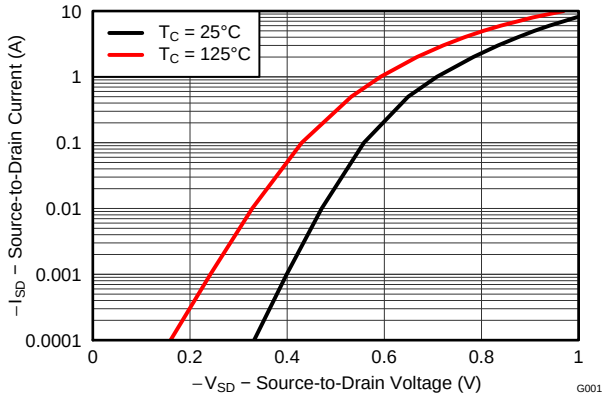


Figure 9. Typical Diode Forward Voltage

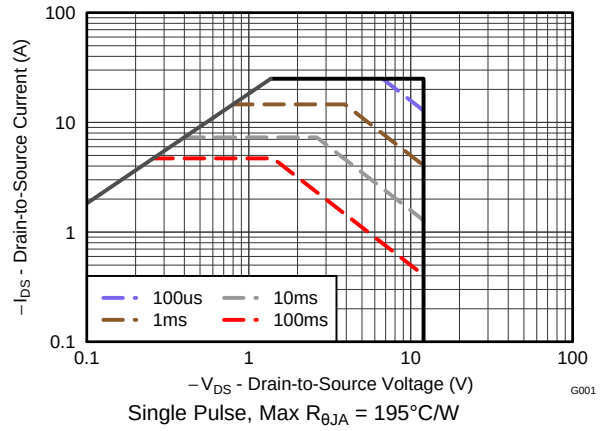


Figure 10. Maximum Safe Operating Area

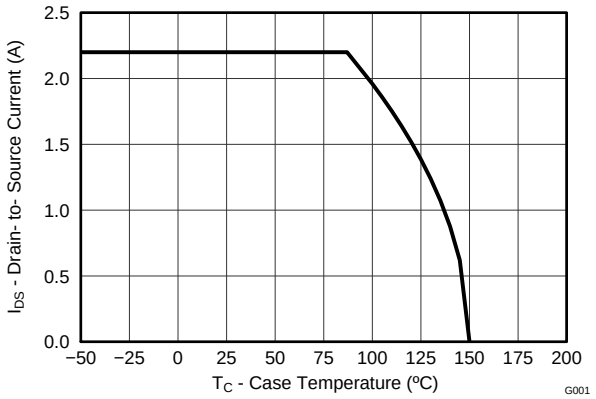


Figure 11. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 商标

NexFET is a trademark of Texas Instruments.

6.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.3 术语表

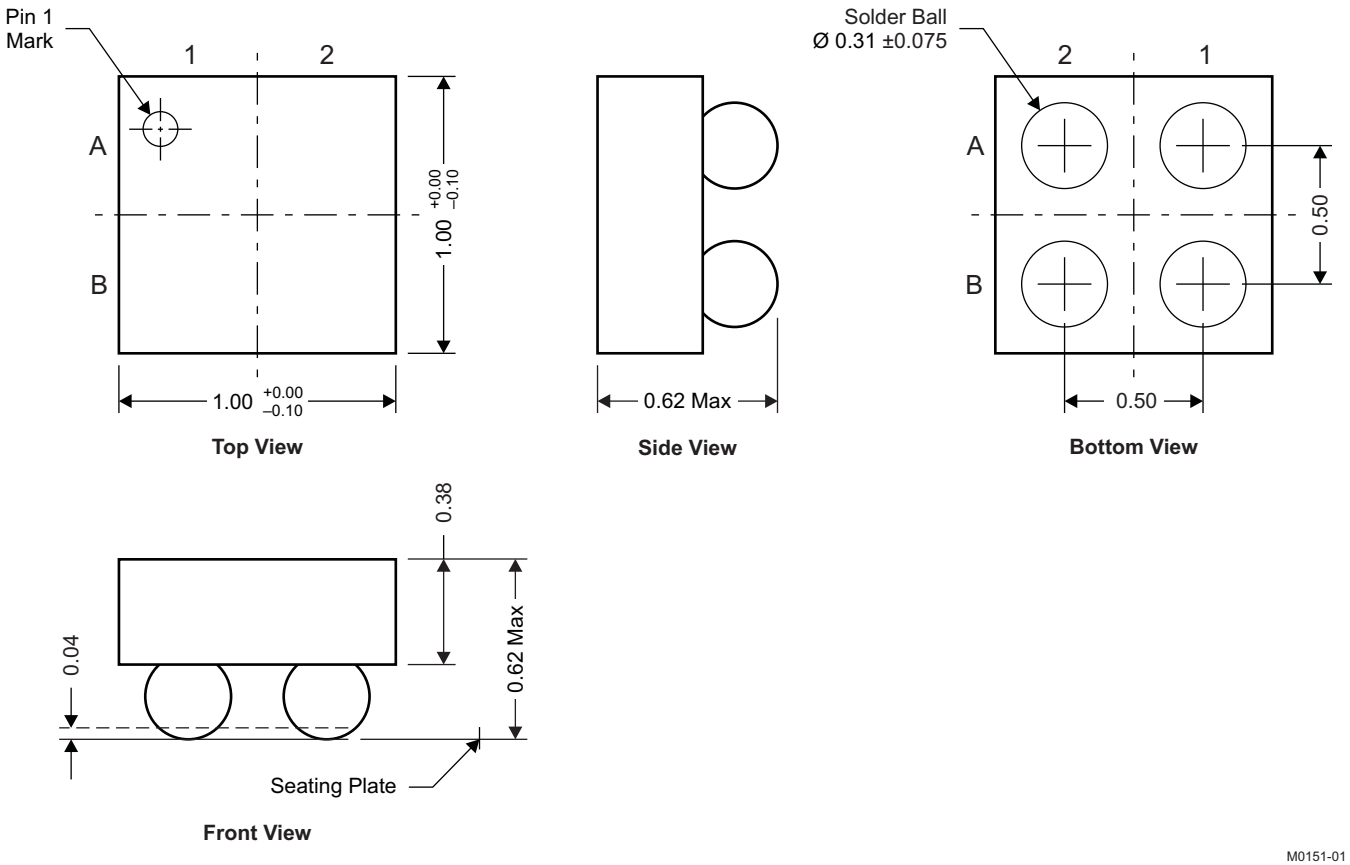
SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

7 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

7.1 CSD23202W10 封装尺寸

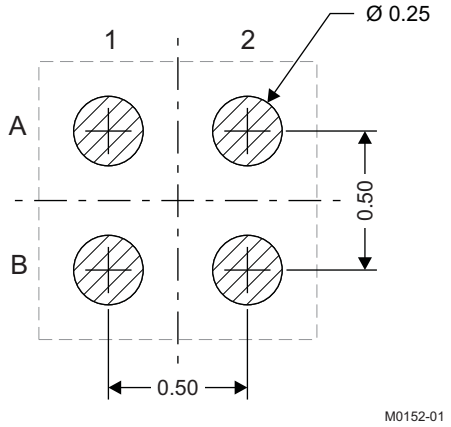


NOTE: 全部尺寸单位为 mm（除非另外注明）。

引脚配置表

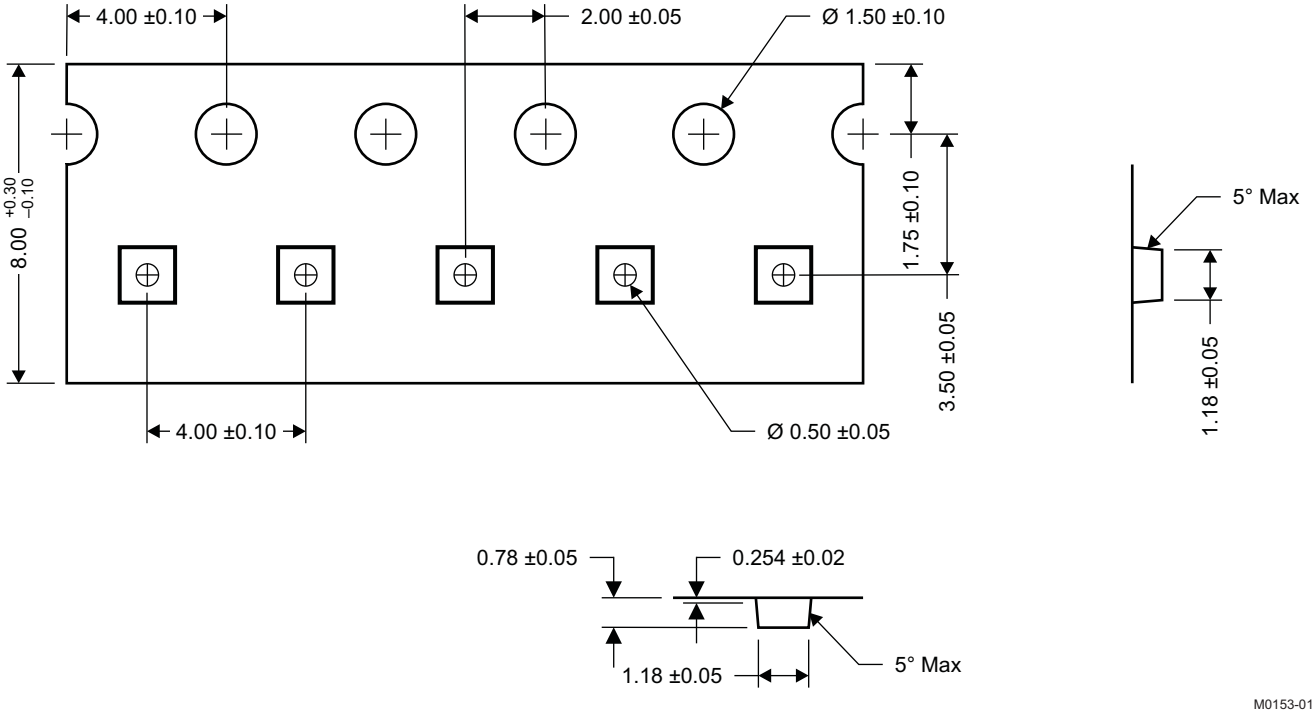
位置	名称
B1	源极
A1	栅极
A2，B2	漏极

7.2 焊盘布局建议



NOTE: 全部尺寸单位为 mm（除非另外注明）。

7.3 卷带封装信息



NOTE: 全部尺寸单位为 mm（除非另外注明）。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD23202W10	Active	Production	DSBGA (YZB) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-	202
CSD23202W10.B	Active	Production	DSBGA (YZB) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	202
CSD23202W10T	Active	Production	DSBGA (YZB) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	202
CSD23202W10T.B	Active	Production	DSBGA (YZB) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	202

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

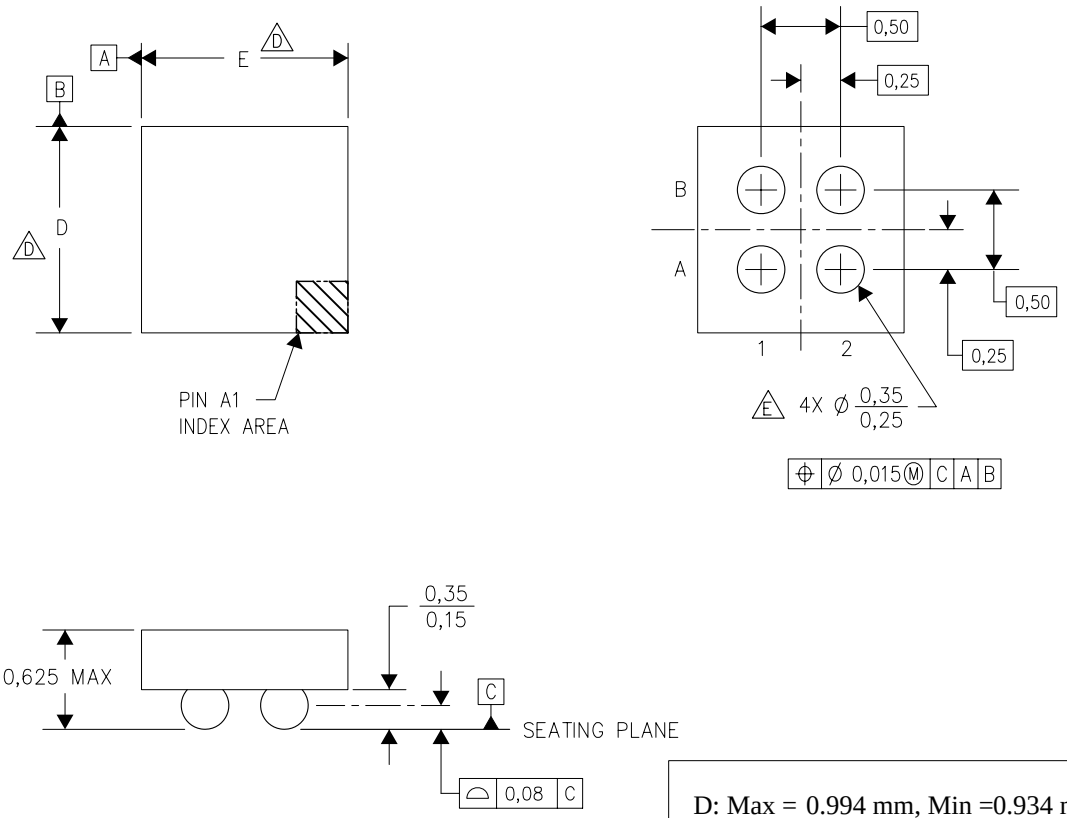
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

YZB (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY



D: Max = 0.994 mm, Min =0.934 mm

E: Max = 0.99 mm, Min = 0.93 mm

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YZB package can have dimension D ranging from 0.94 to 1.65 mm and dimension E ranging from 0.94 to 1.65 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 2 x 2 matrix pattern is shown for illustration only.
F. This package contains lead–free balls. Refer to YEB (Drawing #4204178) for tin–lead (SnPb) balls.

重要通知和免责声明

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最后更新日期：2025 年 10 月