TEXAS INSTRUMENTS
CSD23280F3
ZHCSEX4B – APRIL 2016 – REVISED FEBRUARY 2022

CSD23280F3 -12V P 沟道 FemtoFET™ MOSFET

1 特性

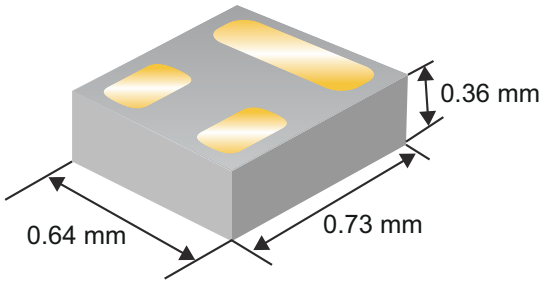
- 低导通电阻
- 超低 Q_g 和 Q_{gd}
- 高漏极工作电流
- 超小尺寸
  - 0.73mm × 0.64mm
- 超薄型封装
  - 最大厚度为 0.36mm
- 集成型 ESD 保护二极管
  - 额定值 > 4kV HBM
  - 额定值 > 2kV CDM
- 无铅且无卤素
- 符合 RoHS

2 应用

- 针对负载开关应用进行了优化
- 针对通用开关应用进行了优化
- 电池应用
- 手持式和移动类应用

3 说明

该-12V、97mΩ P 沟道 FemtoFET™ MOSFET 经过设计和优化，能够最大限度地减小在许多手持式和移动应用中占用的空间。这项技术能够在替代标准小信号 MOSFET 的同时大幅减小封装尺寸。



典型器件尺寸

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	-12		V
Q_g	栅极电荷总量 (4.5V)	0.95		nC
Q_{gd}	栅极电荷 (栅极到漏极)	0.068		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = -1.5V	230	mΩ
		V_{GS} = -1.8V	180	
		V_{GS} = -2.5V	129	
		V_{GS} = -4.5V	97	
$V_{GS(th)}$	阈值电压	-0.65		V

器件信息(1)

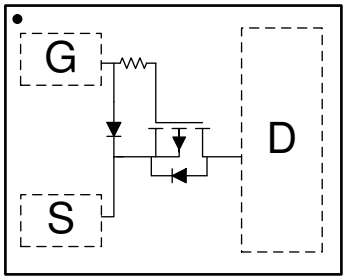
器件	数量	介质	封装	配送
CSD23280F3	3000	7 英寸卷带	Femto 0.73mm × 0.64mm 基板栅格阵列 (LGA)	卷带包装
CSD23280F3T	250			

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	-12	V
V_{GS}	栅源电压	-6	V
I_D	持续漏极电流(1)	2.9	A
	持续漏极电流(2)	1.8	
I_{DM}	脉冲漏极电流(1) (3)	11.4	A
P_D	功率耗散(1)	1.4	W
	功率耗散(2)	0.5	
$V_{(ESD)}$	人体放电模型 (HBM)	4000	V
	充电器件模型 (CDM)	2000	
T_J、T_{stg}	工作结温、贮存温度	-55 至 150	°C

(1) 典型 $R_{\theta JA}$ = 90°C/W (在 0.06 英寸 (1.52mm) 厚的 FR4 PCB 上安装 1 平方英寸 (6.45cm²)、2oz、 0.071mm 厚的铜焊盘时) 。
(2) 电路板覆铜面积最小时的典型 $R_{\theta JA}$ = 255°C/W
(3) 脉冲持续时间 ≤ 100 µs，占空比 ≤ 1%。



顶视图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

Changes from Revision A (August 2017) to Revision B (February 2022) **Page**

- 将超薄型封装要点中的厚度从 0.35mm 更改为 0.36mm 1
- 添加了覆铜面积最大时的电流和功耗限值 1
- 添加了有关覆铜面积最小电路板的脚注 1
- 将超薄型封装图片中的厚度从 0.35mm 更新为 0.36mm 1
- Changed ultra-low profile image height from 0.35 mm to 0.36 mm 8
- Added FemtoFET Surface Mount Guide note 9

Changes from Revision * (April 2016) to Revision A (August 2017) **Page**

- Added the *节 6.1* section in *节 6* 7
- Updated the *节 7.3* 9

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5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = –250 μA	–12			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = –9.6 V			–50	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –5 V			–25	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = –250 μA	–0.40	–0.65	–0.95	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = –1.5 V, I_{DS} = –0.1 A		230	399	mΩ
		V_{GS} = –1.8 V, I_{DS} = –0.4 A		180	250	
		V_{GS} = –2.5 V, I_{DS} = –0.4 A		129	165	
		V_{GS} = –4.5 V, I_{DS} = –0.4 A		97	116	
g_{fs}	Transconductance	V_{DS} = –1.2 V, I_{DS} = –0.4 A		3		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = –6 V, f = 1 MHz		180	234	pF
C_{oss}	Output capacitance			73	95	pF
C_{rss}	Reverse transfer Capacitance			8.5	11.1	pF
R_G	Series gate resistance			9		Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = –6 V, I_{DS} = –0.4 A		0.95	1.23	nC
Q_{gd}	Gate charge gate-to-drain			0.068		nC
Q_{gs}	Gate charge gate-to-source			0.30		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.15		nC
Q_{oss}	Output charge	V_{DS} = –6 V, V_{GS} = 0 V		1.07		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = –6 V, V_{GS} = –4.5 V, I_{DS} = –0.4 A, R_G = 0 Ω		8		ns
t_r	Rise time			4		ns
$t_{d(off)}$	Turnoff delay time			21		ns
t_f	Fall time			8		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = –0.4 A, V_{GS} = 0 V		–0.73	–1.0	V

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	90	°C/W
	Junction-to-ambient thermal resistance(2)	255	

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz. (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

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5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

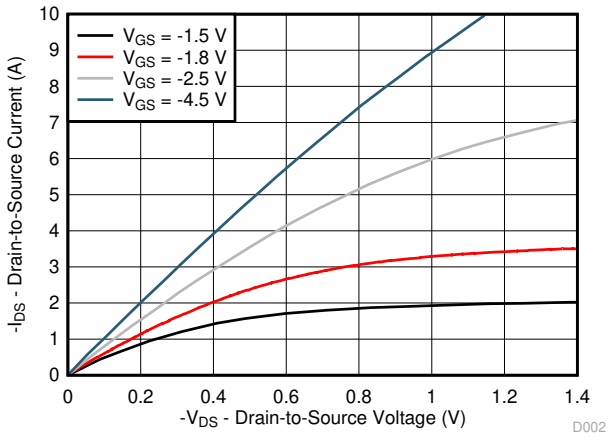
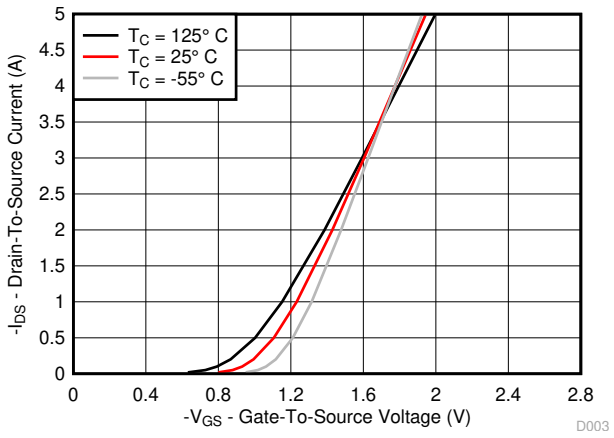


图 5-1. Saturation Characteristics



VDS = – 5 V

图 5-2. Transfer Characteristics

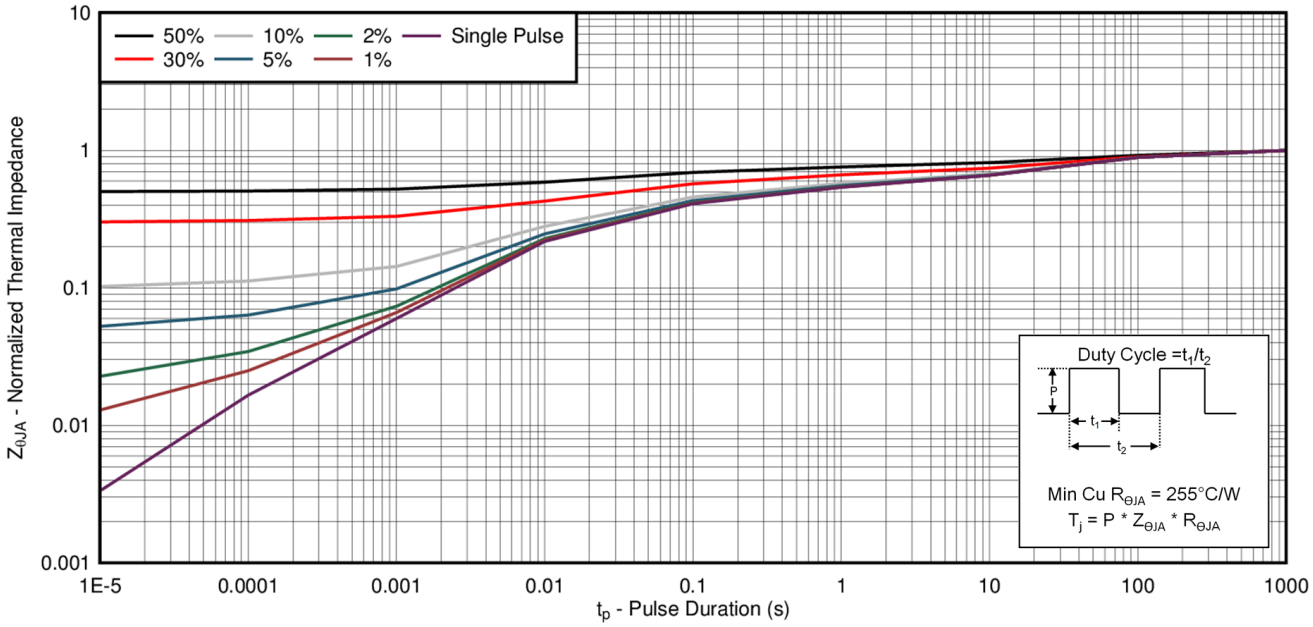


图 5-3. Transient Thermal Impedance

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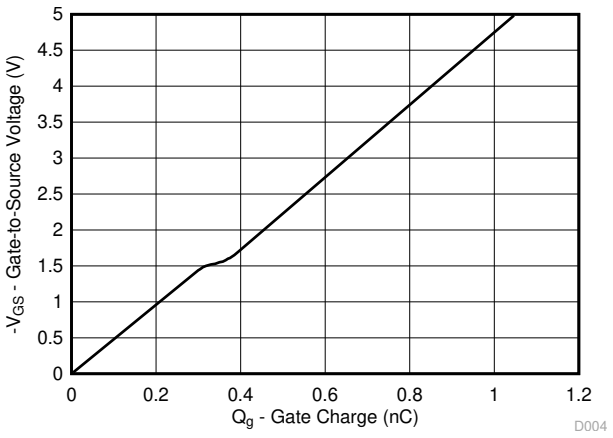


V_{DS} = – 6 V I_D = – 0.4 A

图 5-4. Gate Charge

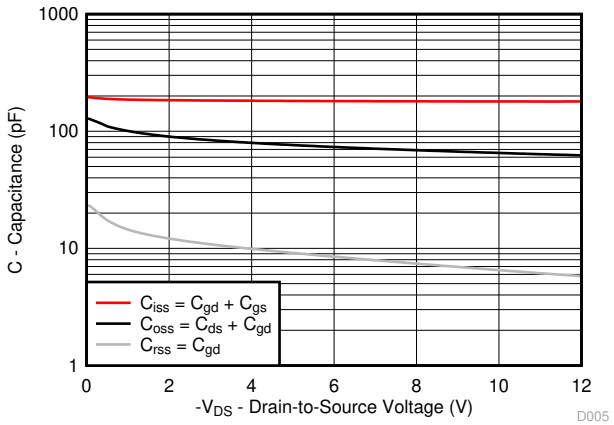
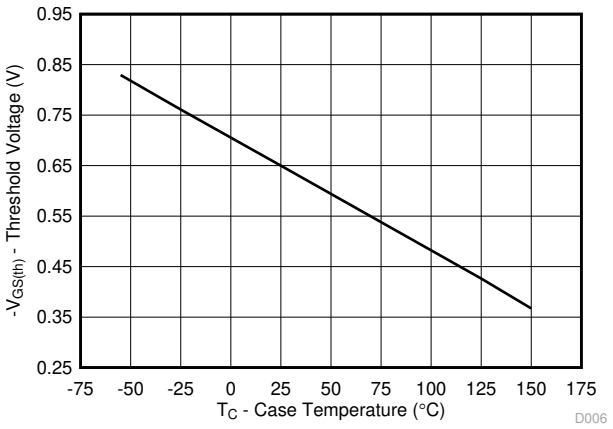


图 5-5. Capacitance



I_D = – 250 µA

图 5-6. Threshold Voltage vs Temperature

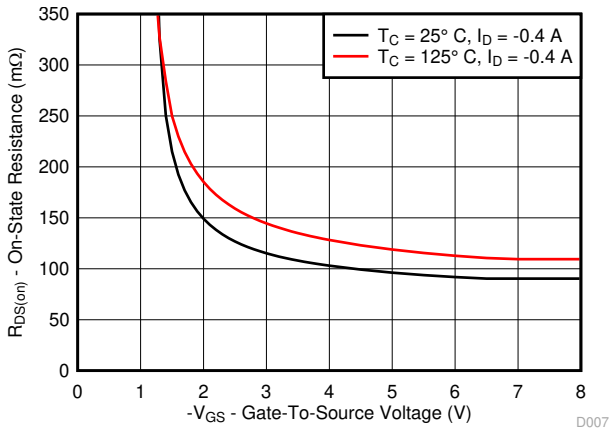
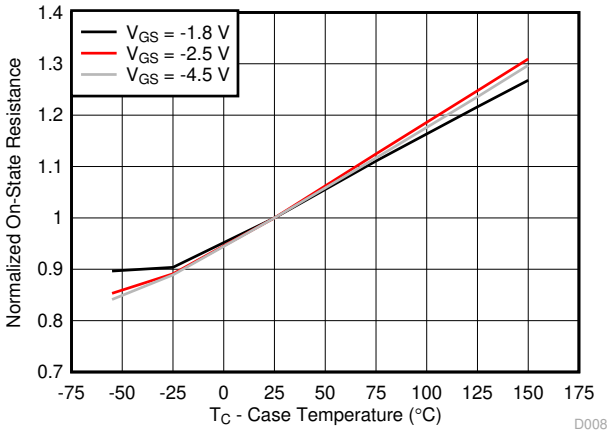


图 5-7. On-State Resistance vs Gate-to-Source Voltage



V_{GS} = – 4.5 V I_D = – 0.4 A

图 5-8. Normalized On-State Resistance vs Temperature

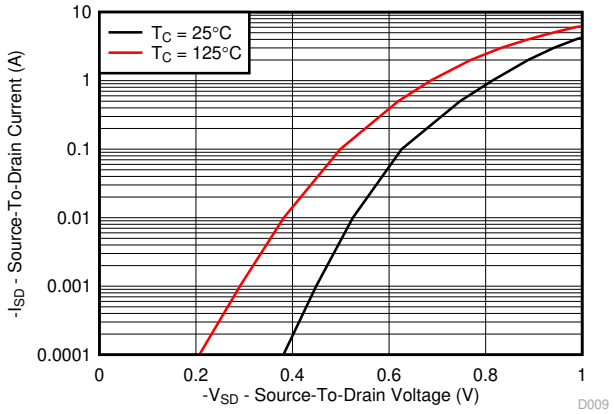


图 5-9. Typical Diode Forward Voltage

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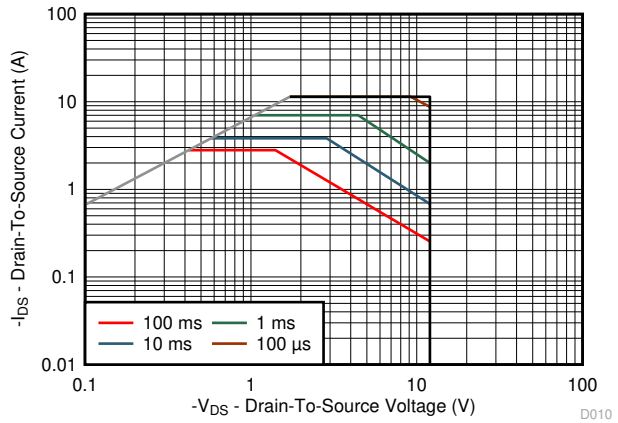

Single pulse, max $R_{\theta JA}$ = 255°C/W

图 5-10. Maximum Safe Operating Area

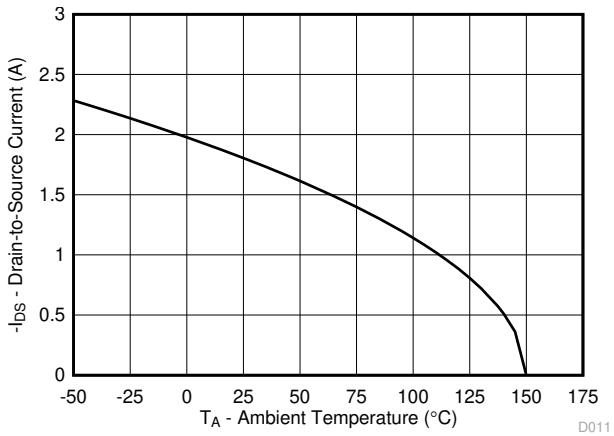

图 5-11. Maximum Drain Current vs Temperature

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6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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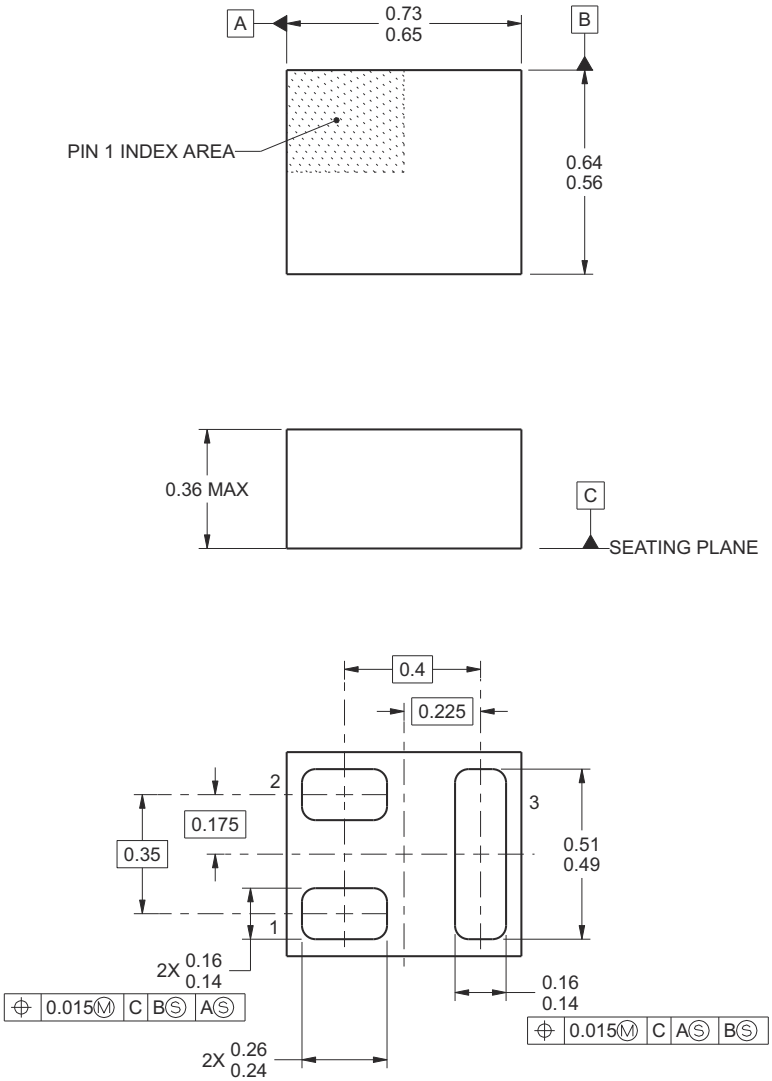
7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
B. This drawing is subject to change without notice.
C. This package is a lead-free solder land design.

表 7-1. Pin Configuration

POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

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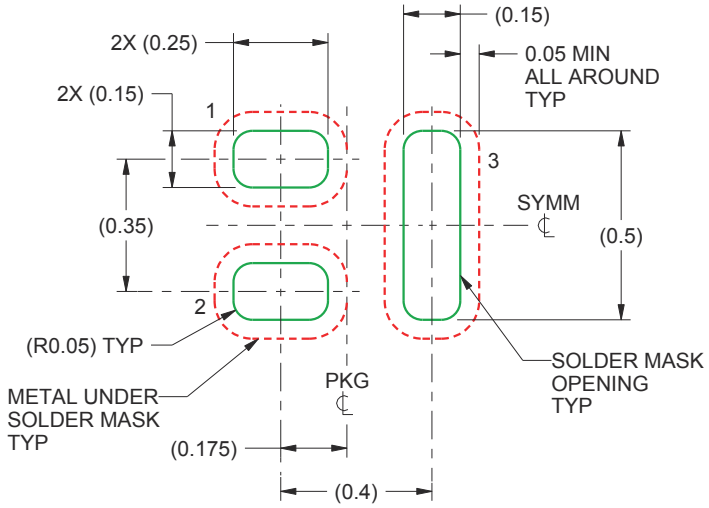
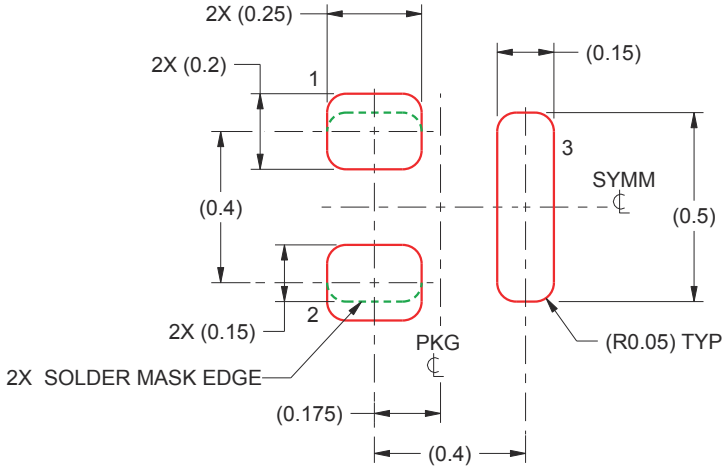
7.2 Recommended Minimum PCB Layout



A. All dimensions are in millimeters.
B. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

7.3 Recommended Stencil Pattern



A. All dimensions are in millimeters.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD23280F3	Active	Production	PICOSTAR (YJM) | 3	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	5
CSD23280F3.B	Active	Production	PICOSTAR (YJM) | 3	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	5
CSD23280F3T	Active	Production	PICOSTAR (YJM) | 3	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	5
CSD23280F3T.B	Active	Production	PICOSTAR (YJM) | 3	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	5

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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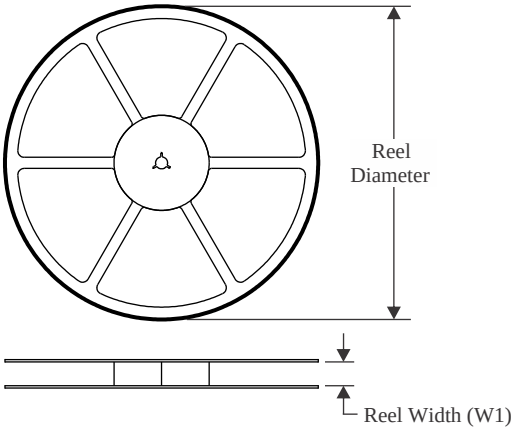
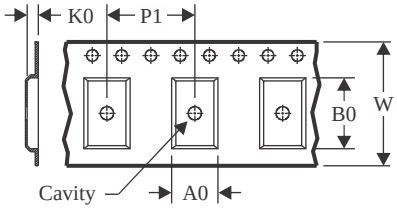
TAPE AND REEL INFORMATION

REEL DIMENSIONS

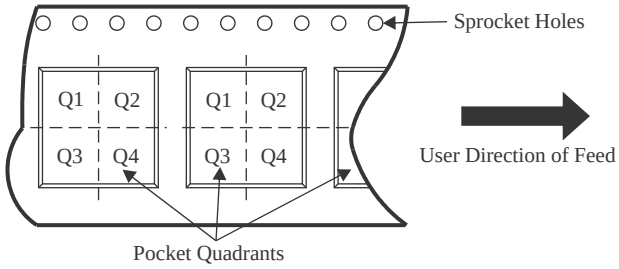


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

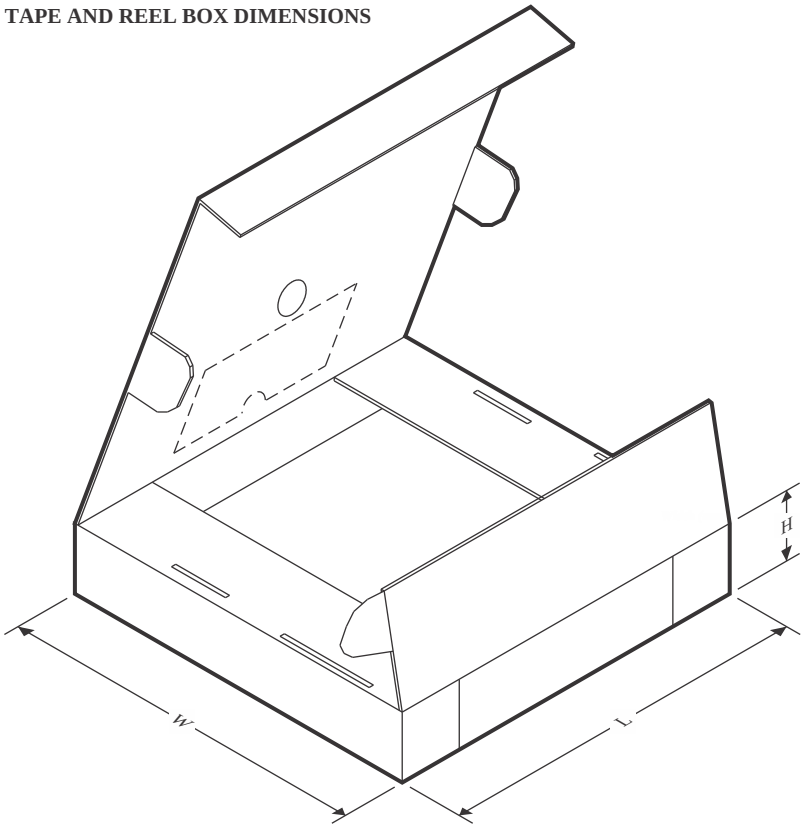
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD23280F3	PICOSTAR	YJM	3	3000	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2
CSD23280F3T	PICOSTAR	YJM	3	250	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD23280F3	PICOSTAR	YJM	3	3000	182.0	182.0	20.0
CSD23280F3T	PICOSTAR	YJM	3	250	182.0	182.0	20.0

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