CSD87503Q3E 30V N 沟道 NexFET™ 功率 MOSFET

1 特性

- 双 N 沟道共源极 MOSFET
- 针对 5V 栅极驱动器进行了优化
- 低热阻
- 低 Q_g 和 Q_{gd}
- 无铅引脚镀层
- 符合 RoHS 标准
- 无卤素
- 小外形尺寸无引线 (SON) 3.3mm × 3.3mm 塑料封装

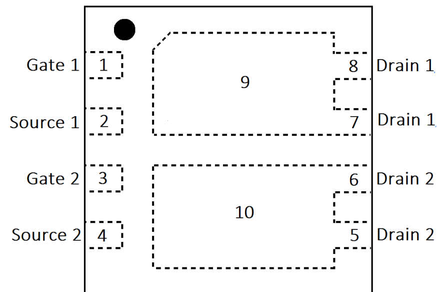
2 应用

- USB Type-C/PDVBus 保护
- 电池保护
- 负载开关

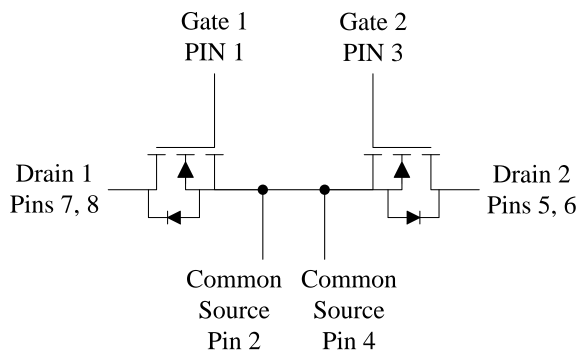
3 说明

CSD87503Q3E 是一款 30V、13.5mΩ、共源极、双路 N 沟道器件，专为 USB Type-C/PD 和电池保护而设计。此 3.3 × 3.3mm SON 器件具有低漏极至漏极导通电阻，可最大限度地较少损耗，且具有较少的组件数量，适用于空间受限的 应用。

顶视图



电路图像



产品概要

T_A = 25°C		值		单位
V_{DS}	漏源电压	30		V
Q_g	总栅极电荷 (4.5V)	13.4		nC
Q_{gd}	栅极电荷（栅极到漏极）	5.8		nC
$R_{DD(on)}$	漏极到漏极导通电阻	V_{GS} = 4.5V	17.3	mΩ
		V_{GS} = 10V	13.5	
$V_{GS(th)}$	阈值电压	1.7		V

器件信息[(1)]

器件	数量	包装介质	封装	发货
CSD87503Q3E	2500	13 英寸卷带	SON 3.30mm × 3.30mm 塑料封装	卷带封装
CSD87503Q3ET	250	7 英寸卷带		

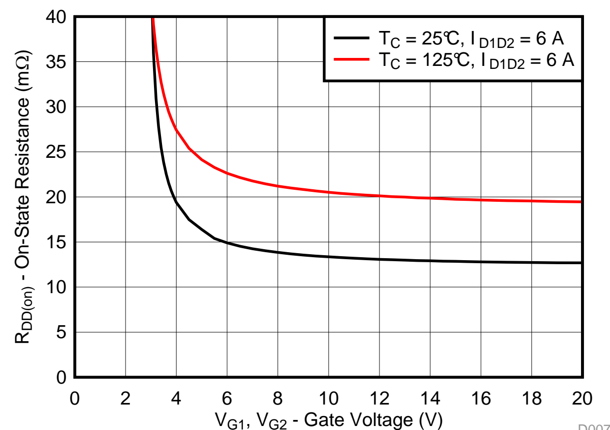
(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	30	V
V_{GS}	栅源电压	±20	V
$I_{D1,\ D2}$	持续漏极到漏极电流（受封装限制）	10	A
I_{DS}	持续漏极到源极电流（受封装限制）	1.5	A
$I_{D1,\ D2M}$	脉冲漏极到漏极电流[(1)]	89	A
P_D	功率耗散[(2)]	2.6	W
P_D	功耗，T_C = 25°C	15.6	W
T_J、T_{stg}	工作结温、储存温度	–55 至 150	°C

(1) 最大 $R_{\theta JC}$ = 8°C/W，脉冲持续时间 ≤ 100µs，占空比 ≤ 1%。
(2) 典型 $R_{\theta JA}$ = 50°C/W（当在 0.06 英寸 (1.52mm) 厚的 FR4 PCB 上将其安装在 1 平方英寸 (6.45cm^2) 2oz (0.071mm) 厚的铜焊盘上时）。

$R_{DD(on)}$ 与 V_{GS} 之间的关系



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

日期	修订版本	说明
2017 年 9 月	*	初始发行版。

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5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage(1)	V_{GS} = 0 V, I_D = 250 μA	30			V
I_{DSS}	Drain-to-source leakage current(1)	V_{GS} = 0 V, V_{DS} = 24 V			1	μA
I_{GSS}	Gate-to-source leakage current(1)	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage(1)	V_{DS} = V_{GS}, I_D = 250 μA	1.3	1.7	2.1	V
$R_{DD(on)}$	Drain-to-drain on-resistance	V_{GS} = 4.5 V, I_{D1D2} = 6 A		17.3	21.9	mΩ
		V_{GS} = 10 V, I_{D1D2} = 6 A		13.5	16.9	
g_{fs}	Transconductance	V_{DS} = 3 V, I_{D1D2} = 6 A		24		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{D1D2} = 15 V, ƒ = 1 MHz		782	1020	pF
C_{OSS}	Output capacitance			157	204	pF
C_{RSS}	Reverse transfer capacitance			149	194	pF
R_g	Series gate resistance(1)			1.5	3.0	Ω
Q_g	Gate charge total (4.5 V)	V_{D1D2} = 15 V, I_{D1D2} = 6 A		13.4	17.4	nC
	Gate charge total (10 V)			32.9	42.8	
Q_{gd}	Gate charge gate-to-drain			5.8		nC
Q_{gs}	Gate charge gate-to-source			4.8		nC
$Q_{g(th)}$	Gate charge at V_{th}			1.0		nC
Q_{OSS}	Output charge	V_{D1D2} = 15 V, V_{GS} = 0 V		4.3		nC
$t_{d(on)}$	Turnon delay time	V_{D1D2} = 15 V, V_{GS} = 10 V, I_{D1D2} = 6 A, R_G = 0 Ω		10		ns
t_r	Rise time			40		ns
$t_{d(off)}$	Turnoff delay time			25		ns
t_f	Fall time			8		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage(1)	I_D = 0.5 A, V_{GS} = 0 V		0.75	0.95	V
Q_{rr}	Reverse recovery charge(1)	V_{DS} = 15 V, I_F = 6 A, di/dt = 300 A/μs		9.2		nC
t_{rr}	Reverse recovery time(1)			14		ns

(1) Parameter measured on both MOSFETs individually. Table values are for a single FET.

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{θJC}$	Junction-to-case thermal resistance(1)			8	°C/W
$R_{θJA}$	Junction-to-ambient thermal resistance(1)(2)			60	°C/W

(1) $R_{θJC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{θJC}$ is specified by design, whereas $R_{θJA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.

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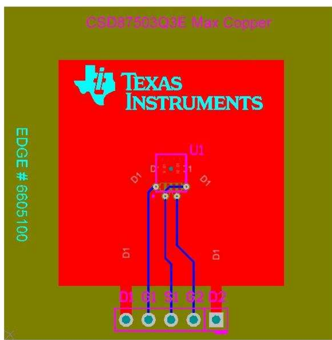
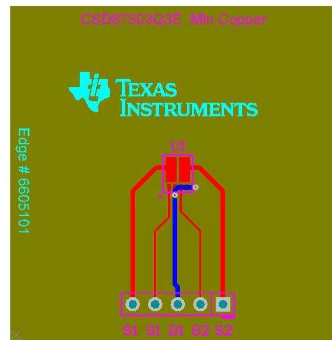


Max $R_{\theta JA}$ = 60°C/W when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 185°C/W when mounted on a minimum pad area of 2-oz (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

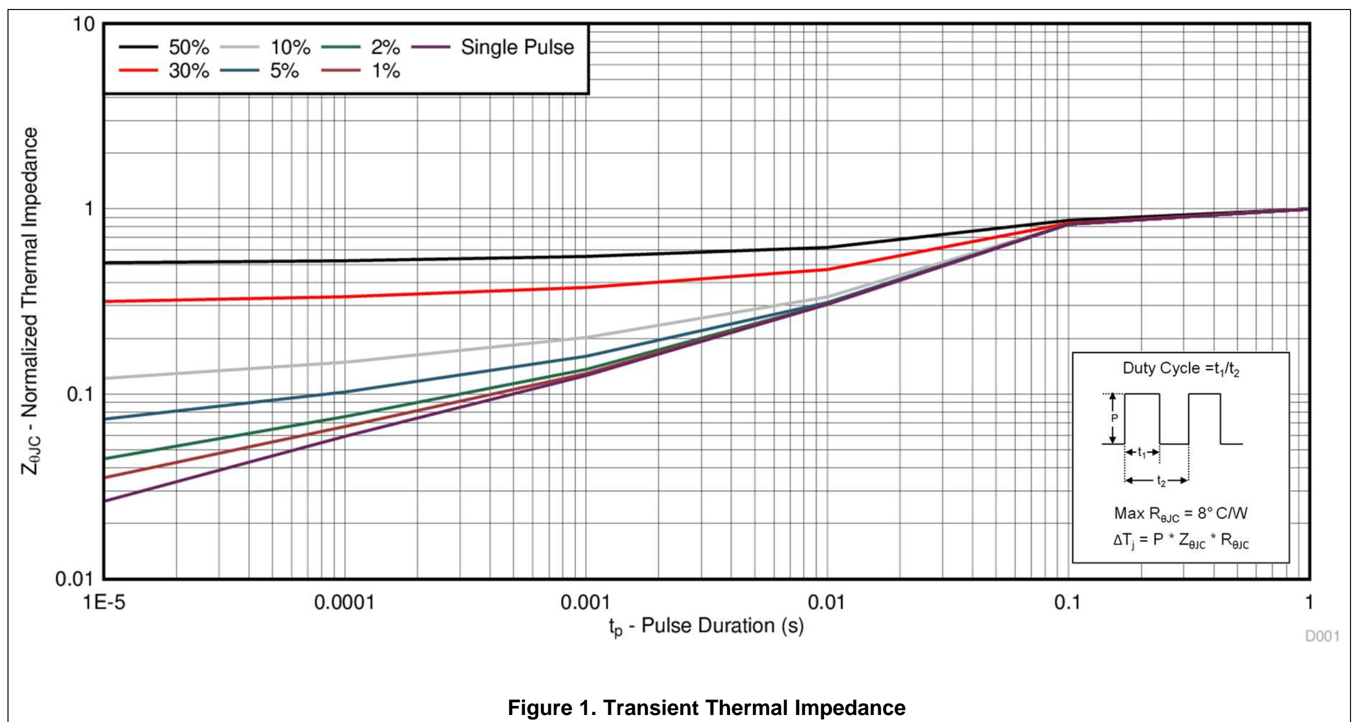


Figure 1. Transient Thermal Impedance

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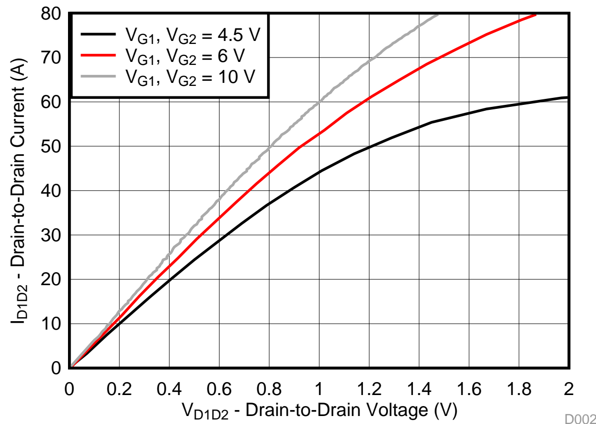
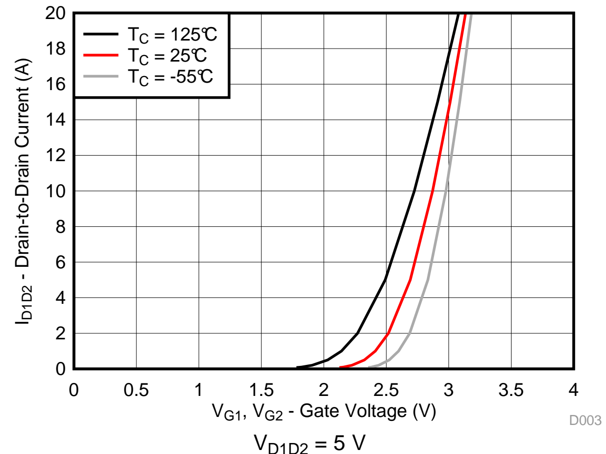
Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



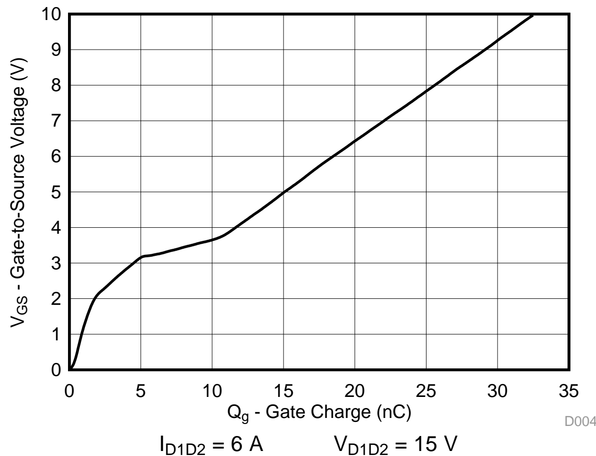
Note: Measurement taken with both gates tied together

Figure 2. Saturation Characteristics



V_{D1D2} = 5 V

Figure 3. Transfer Characteristics



I_{D1D2} = 6 A V_{D1D2} = 15 V

Figure 4. Gate Charge

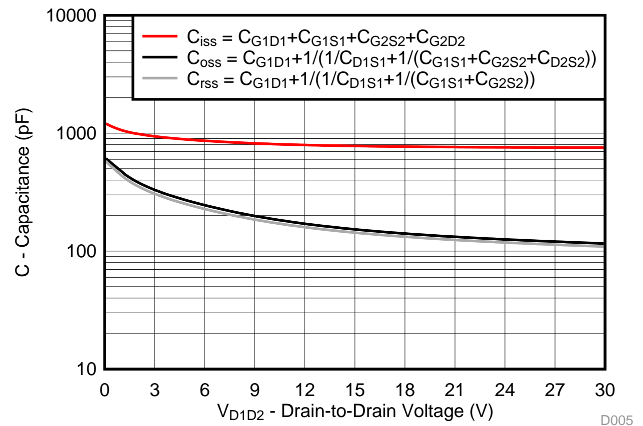
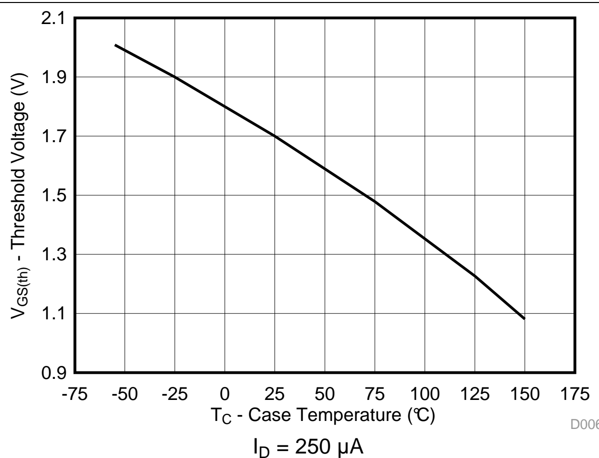


Figure 5. Capacitance



I_D = 250 μA

Figure 6. Threshold Voltage vs Temperature

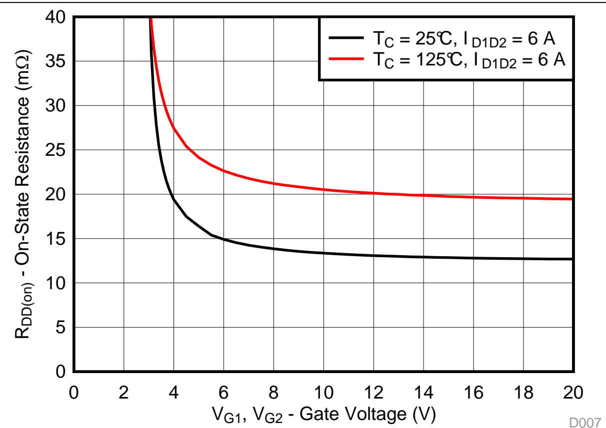


Figure 7. On-State Resistance vs Gate-to-Source Voltage

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Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

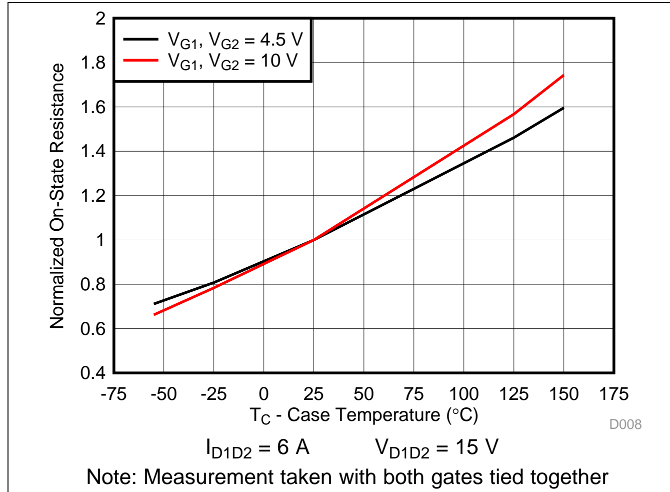

Figure 8. Normalized On-State Resistance vs Temperature

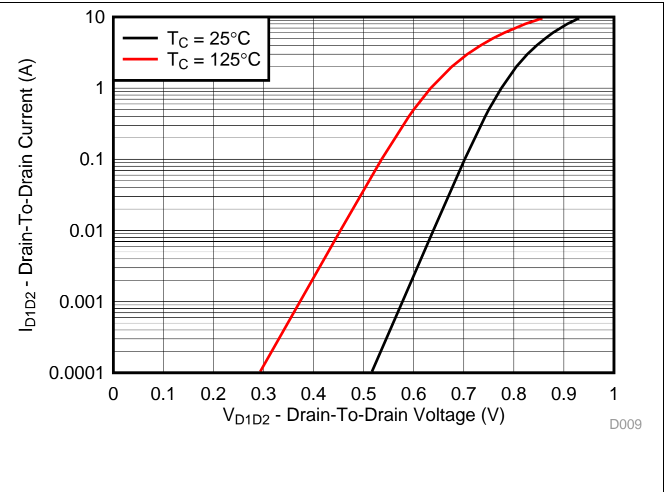

Figure 9. Typical Diode Forward Voltage

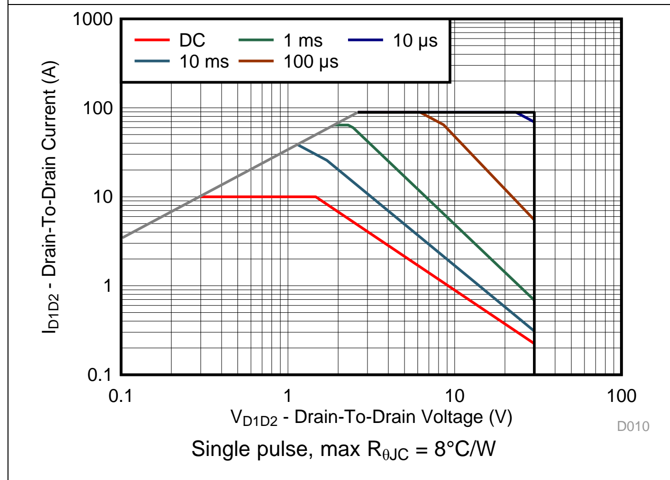

Figure 10. Maximum Safe Operating Area

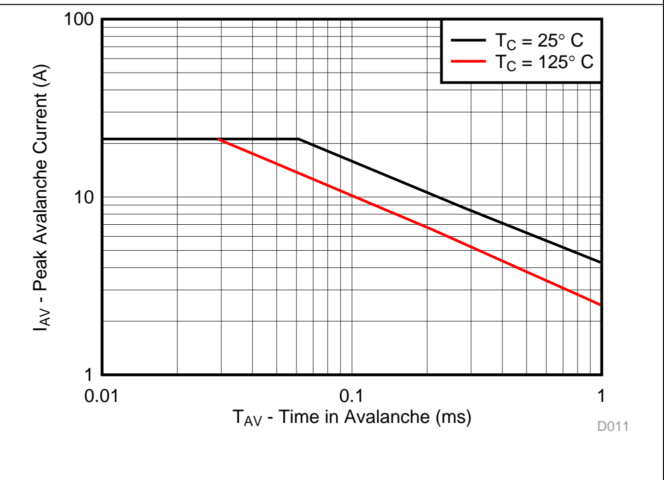

Figure 11. Single Pulse Unclamped Inductive Switching

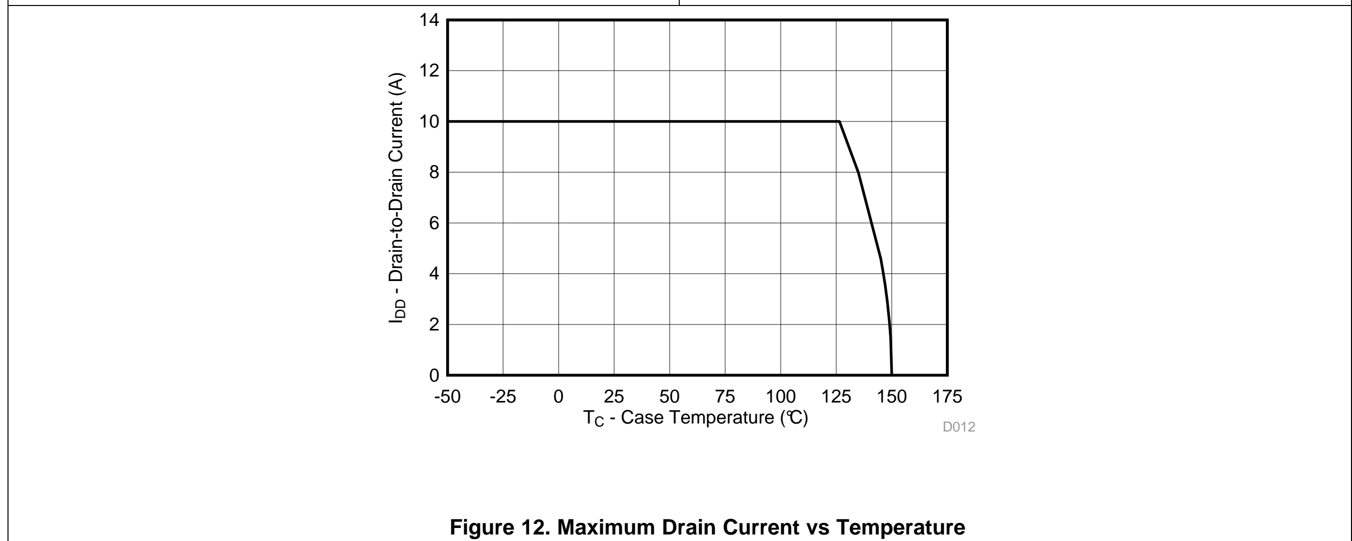

Figure 12. Maximum Drain Current vs Temperature

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6 器件和文档支持

6.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

6.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

6.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

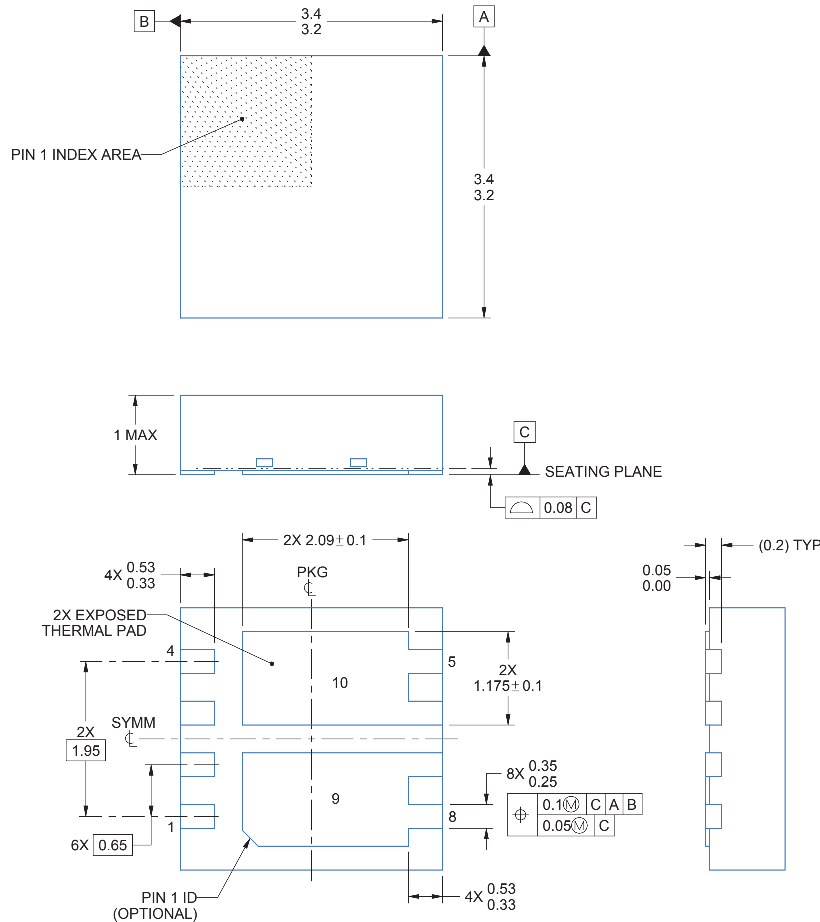
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

7.1 Q3 封装尺寸



1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和公差值符合 ASME Y14.5M 标准。
2. 本图如有变更，恕不另行通知。
3. 封装散热盘必须在印刷电路板上焊接，包装散热和机械性能。

表 **1.** 引脚配置

位置	名称
引脚 1	栅极 1
引脚 2	共源极
引脚 3	栅极 2
引脚 4	共源极
引脚 5、6	漏极 2
引脚 7、8	漏极 1

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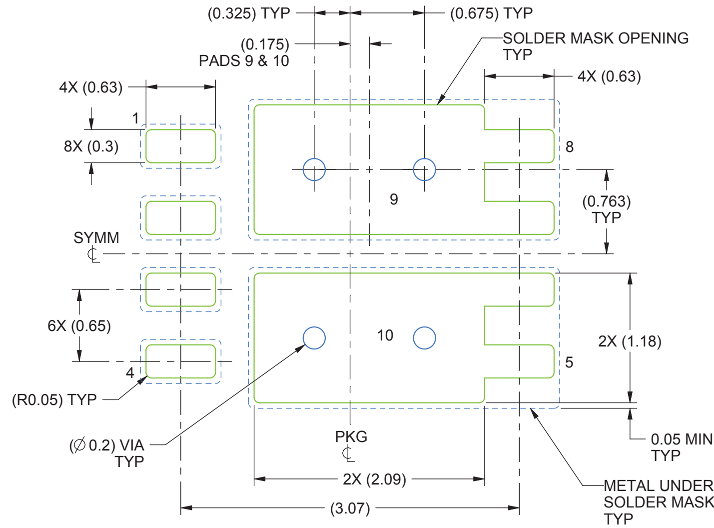
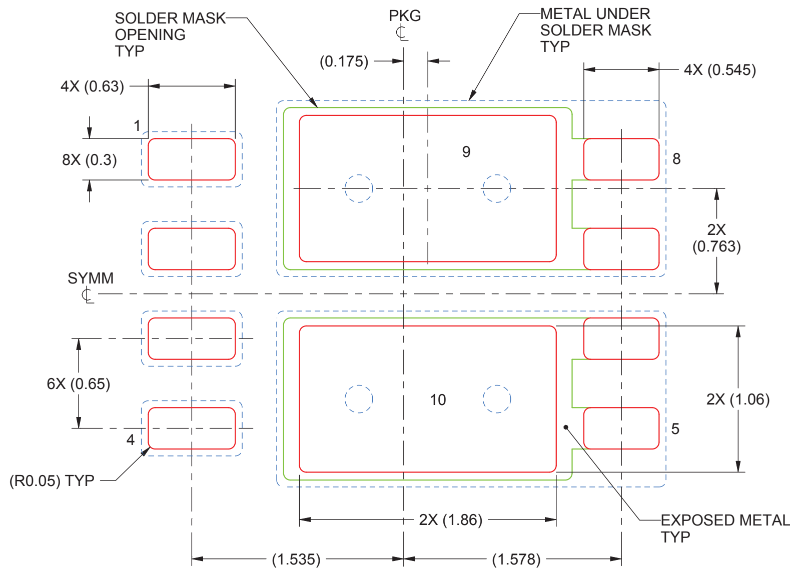
7.2 建议 PCB 布局



1. 此封装设计用于焊接到电路板的散热焊盘上。更多信息，请参见*《QFN/SON PCB 连接》*（文献编号：SLUA271）。
2. 根据具体应用决定是否选用通孔，请参见器件产品说明书。如需实施任意通孔，请参见此视图上的通孔位置。建议对焊锡膏下方的通孔进行填充、堵塞或包覆。
3. 本图如有变更，恕不另行通知。

7.3 建议模板开口



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PADS 9 & 10
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

1. 具有漏斗形壁和圆角的激光切割孔可提供更佳的锡膏脱离。IPC-7525 可能提供替代设计建议。
2. 本图如有变更，恕不另行通知。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD87503Q3E	Active	Production	VSON (DTD) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87503E
CSD87503Q3E.B	Active	Production	VSON (DTD) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87503E
CSD87503Q3EG4.B	Active	Production	VSON (DTD) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87503E
CSD87503Q3ET	Active	Production	VSON (DTD) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87503E
CSD87503Q3ET.B	Active	Production	VSON (DTD) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87503E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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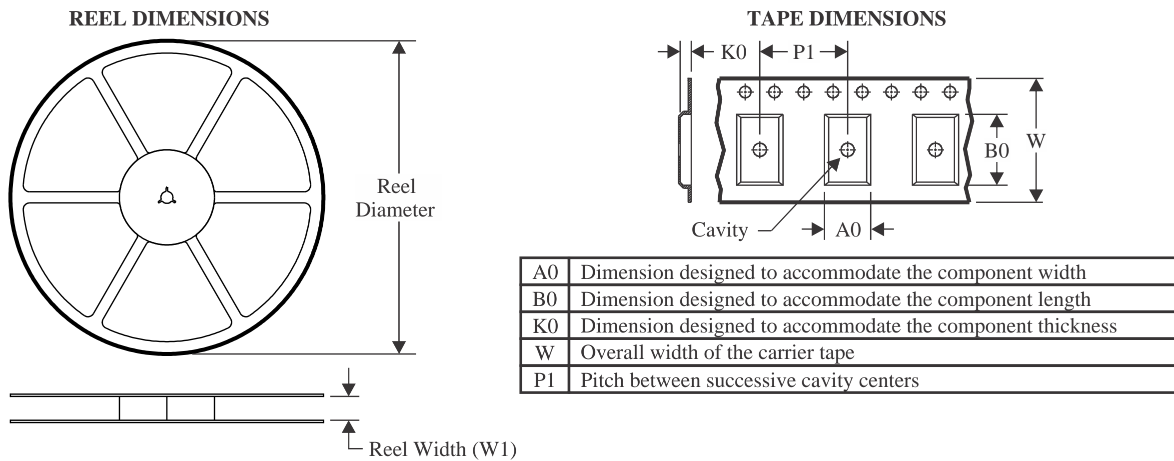
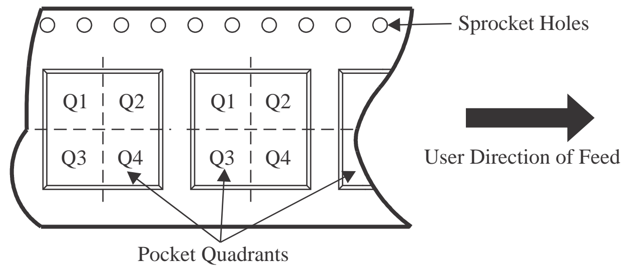
TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

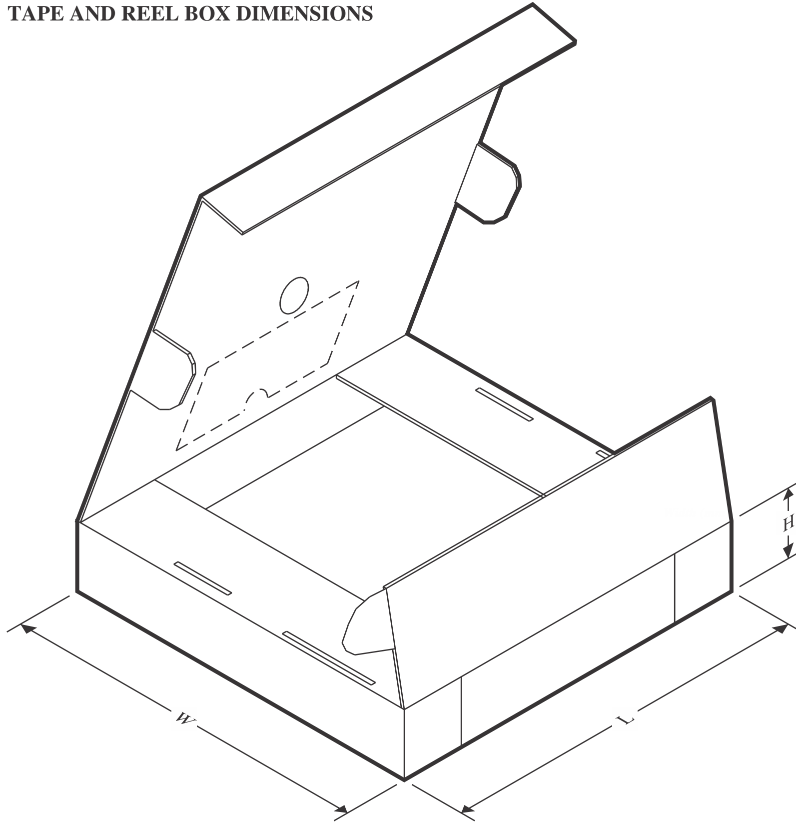
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87503Q3E	VSON	DTD	8	2500	330.0	12.4	3.6	3.6	1.2	8.0	12.0	Q1
CSD87503Q3ET	VSON	DTD	8	250	178.0	13.5	3.6	3.6	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

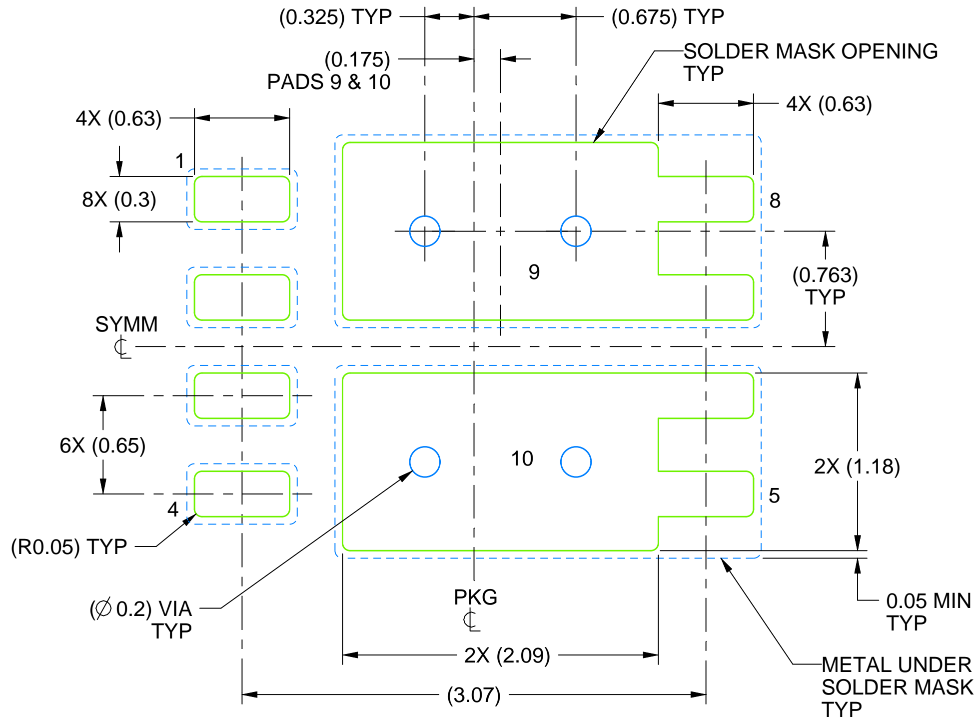


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87503Q3E	VSON	DTD	8	2500	364.0	357.0	31.0
CSD87503Q3ET	VSON	DTD	8	250	189.0	185.0	36.0

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:20X

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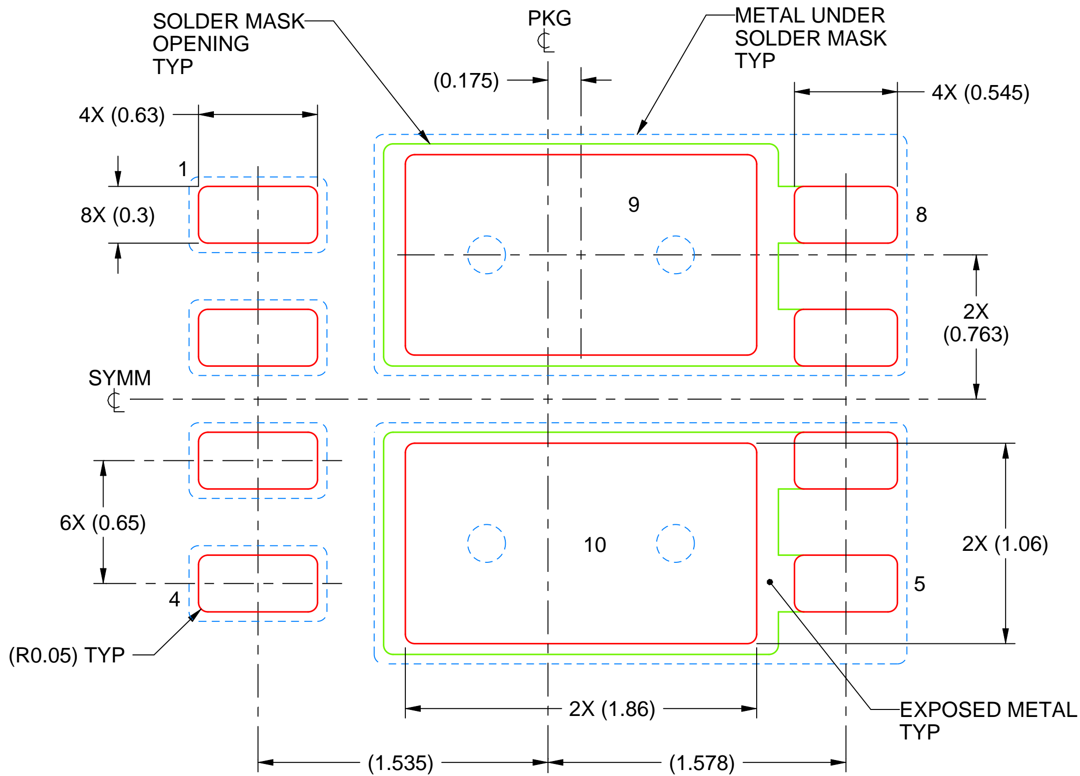
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PADS 9 & 10
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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