DAC8742H HART 和 FOUNDATION 现场总线/PROFIBUS PA 调制解调器

1 特性

- 兼容 HART 的物理层调制解调器
  - 1200/2200Hz HART FSK 正弦波
  - TX 信号振幅的寄存器编程控制（仅适用于 DAC8741H / DAC8742H）
  - 集成式 RX 解调器和带通滤波器，具有极少的外部组件
- 兼容 FOUNDATION 现场总线的 H1 控制器和介质连接单元 (MAU)
  - 基于曼彻斯特编码总线供电 (MBP) 的 31.25 kbit/s 通信
  - 集成曼彻斯特编码器和解码器
  - 与 PROFIBUS PA 兼容
- 低静态电流：最大值 180uA，典型工业工作温度范围（-40°C 至 85°C）
- 集成 1.5V 电压基准
- 灵活的时钟选项
  - 内部振荡器
  - 外部晶体振荡器
  - 外部 CMOS 时钟
- 数字接口
  - DAC8742H：UART 和 SPI
- 可靠性：CRC 位错校验、看门狗计时器
- 宽工作温度范围：-55°C 至 125°C
- 5mm x 5mm TQFP 封装

HART COMMUNICATION PROTOCOL

2 应用

- 工业过程控制和自动化
- PLC 或 DCS I/O 模块
- 现场和传感器发送器

3 说明

DAC8742H 是一款 HART®、 FOUNDATION 现场总线™和 PROFIBUS PA 兼容的低功耗调制解调器，适用于工业过程控制和工业自动化 数据隔离。

在 HART 模式下，DAC8742H 集成所有必需电路，以作为一个半双工 HART 物理层调制解调器，在从配置或主配置中使用最少的外部过滤组件运行。在 FOUNDATION 现场总线模式下，DAC8742H 集成所有必需电路，以作为兼容 FOUNDATION 现场总线的半双工 H1 控制器和 MAU 运行。

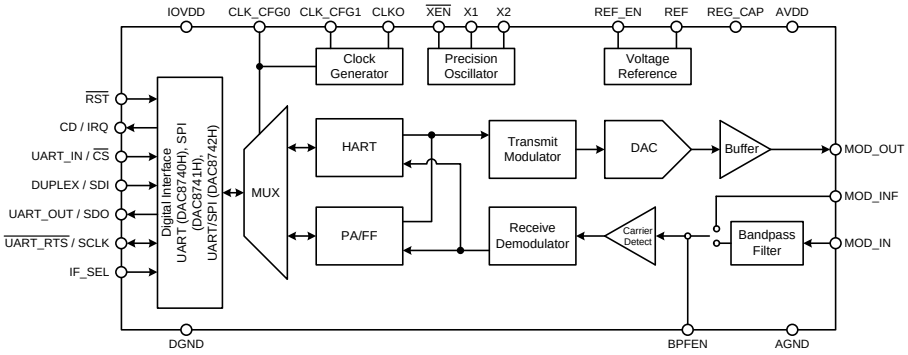
在 HART、FOUNDATION 现场总线或 PROFIBUS PA 模式下，可通过 UART 接口或 SPI 接口接入的集成式 FIFO 传输来自微控制器的数据流。SPI 接口包括一个支持菊链的 SDO 引脚、各种中断以及其他扩展 特性。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DAC8742H	TQFP (32)	5mm × 5mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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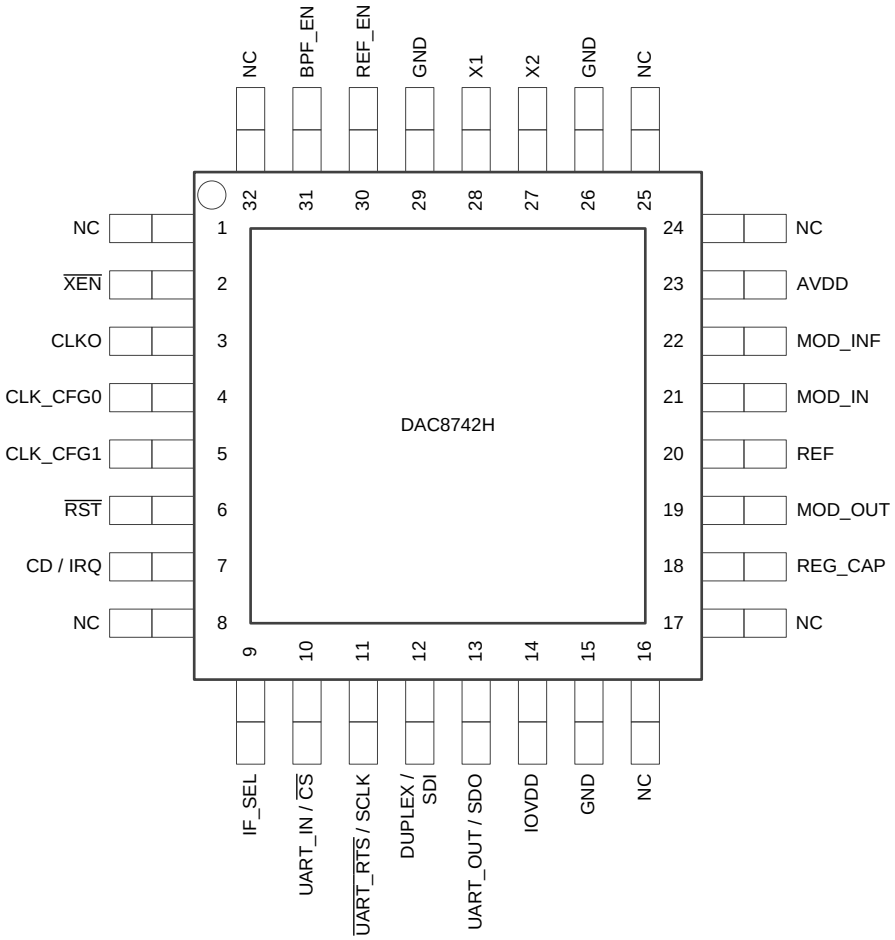
4 修订历史记录

日期	修订版本	说明
2018 年 12 月	*	DAC8742H 独立数据表的初始发行版。

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5 Pin Configuration and Functions

PBS Package
32-Pin TQFP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
XEN	2	Digital Input	Crystal Oscillator Enable. Logic low on this pin enables the crystal oscillator circuit; in this mode an external crystal is required. Logic high on this pin disables the internal crystal oscillator circuit; in this mode an external CMOS clock or the internal oscillator are required. No digital input pin should be left floating.
CLKO	3	Digital Output	Clock Output. If using the internal oscillator or an external crystal, this pin can be configured as a clock output.
CLK_CFG0	4	Digital Input	Clock Configuration Pin. This pin is used to configure the input/output clocking scheme. No digital input pin should be left floating.
CLK_CFG1	5	Digital Input	Clock Configuration Pin. This pin is used to configure the input/output clocking scheme. No digital input pin should be left floating.
RST	6	Digital Input	Reset. Logic low on this pin places the DAC8742H into power-down mode and resets the device. Logic high returns the device to normal operation. No digital input pin should be left floating.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION		
NAME	NO.				
CD / IRQ	7	Digital Output	UART Mode	HART Mode	Carrier detect. A logic high on this pin indicates a valid carrier is present.
				FF / PA Mode	While not transmitting, a logic high on this pin indicates a valid carrier is present. While transmitting, a logic high on this pin indicates that the jabber inhibitor has triggered.
			SPI Mode	Digital Interrupt. The interrupt can be configured as edge sensitive or level sensitive with positive or negative polarity, as set by the CONTROL register. Events that trigger an interrupt are controlled by the Modem IRQ Mask register.	
IF_SEL	9	Digital Input	Interface select. A logic high on this pin configures the device for SPI mode. A logic low on this pin configures the device for UART mode. An internal pull-down resistor is included. No digital input pin should be left floating.		
UART_IN / CS	10	Digital Input	UART Mode	UART data input.	
			SPI Mode	SPI chip-select. Data bits are clocked into the serial shift register when CS is low. When CS is high, SDO is in a high-impedance state and data on SDI are ignored. No digital input pin should be left floating. No digital input pin should be left floating.	
UART_RTS / SCLK	11	Digital Input, Digital Output	UART Mode	HART Mode	Request to send a logic high on this pin enables the demodulator and disables the modulator. A logic low on this pin enables the modulator and disables the demodulator. No digital input pin should be left floating.
				FF / PA Mode	This pin reports transmit FIFO threshold information as programmed by the packet initiation code.
			SPI Mode	SPI clock. Data can be transferred at rates up to 12.5MHz. Schmitt-Trigger logic input.	
DUPLEX / SDI	12	Digital Output	UART Mode	Digital input. Logic high enables full-duplex, or internal loop-back, test mode.	
			SPI Mode	SPI data input. Data is clocked into the 24-bit input shift register on the falling edge of the serial clock input. Schmitt-Trigger logic input.	
UART_OUT / SDO	13	Digital Output	UART Mode	UART data output.	
			SPI Mode	SPI data output. Data is valid on the falling edge of SCLK.	
IOVDD	14	Supply	Interface supply. Supply voltage for digital input and output circuitry. This voltage sets the logical thresholds for the digital interface.		
GND	15	Supply	Digital ground. Ground reference voltage for all digital circuitry of the device.		
REG_CAP	18	Analog Output	Capacitor for internal regulator.		
MOD_OUT	19	Analog Output	Modem output. FSK output sinusoid in HART mode or Manchester coded data stream in FOUNDATION Fieldbus and PROFIBUS PA modes. Requires parallel capacitance of 5-22 nF in HART mode or 0-100 pF in FOUNDATION Fieldbus and PROFIBUS PA mode for stability.		
REF	20	Analog Input or Output	When the internal reference is enabled this pin outputs the internal reference voltage. When the internal reference is disabled, this is the external 2.5V reference input.		
MOD_IN	21	Analog Input	HART FSK input or FOUNDATION Fieldbus and PROFIBUS PA Manchester coded data stream input. If an external filter is used, do not connect this pin.		
MOD_INF	22	Analog Input	If using the internal band-pass filter, connect 680 pF to this pin or 120 pF in FOUNDATION Fieldbus and PROFIBUS PA modes. If using an external filter, connect the output of that filter to this pin.		
AVDD	23	Supply	Power supply.		
GND	26	Supply	Analog ground. Ground reference voltage for power supply input.		
X2	27	Analog Input	Crystal stimulus.		
X1	28	Analog Input	Crystal/Clock input.		
GND	29	Supply	Digital ground. Ground reference voltage for all digital circuitry of the device.		
REF_EN	30	Digital Input	Reference enable. Logic high enables the internal 1.5V reference. No digital input pin should be left floating.		

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
BPF_EN	31	Digital Input	Filter enable. A logic high enables the internal band-pass filter. No digital input pin should be left floating.
NC	1, 8, 16, 17, 24, 25, 32	–	Do not connect these pins.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	AVDD to GND	-0.3	6	V
	IOVDD to GND	-0.3	6	
	Analog output voltage to GND	-0.3	AVDD+0.3	
	Digital output voltage to GND	-0.3	IOVDD+0.3	
Output voltage	Analog output pin to GND	-0.3	AVDD+0.3	V
	Digital output pin to GND	-0.3	IOVDD+0.3	
Input Current	Input current to any pin except supply pins	-10	10	mA
Operating junction temperature, T_J		-55	125	°C
Junction temperature range (TJ max)			150	
Storage temperature, T_{stg}		-60	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
POWER SUPPLY					
AVDD		2.7		5.5	V
IOVDD		1.71		5.5	V
ANALOG INPUTS					
External Reference Input Voltage		2.375	2.5	2.625	V
DIGITAL INPUTS					
External Clock Source Frequency (HART Mode)	3.6864 MHz Clock	3.6469	3.6864	3.7232	MHz
	1.2288 MHz Clock	1.2165	1.2288	1.2411	MHz

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Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
External Clock Source Frequency (FF / PA Modes)		3.96	4	4.04	MHz

6.4 Thermal Information

THERMAL METRIC(1)		DAC8742H PBS (TQFP) 32 PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	79.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	32.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

All specifications over -40°C to +125°C ambient operating temperature, 2.7V ≤ AVDD ≤ 5.5V, 1.71V ≤ IOVDD ≤ 5.5V, Internal Reference, Internal Filter, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER REQUIREMENTS					
IOVDD		1.71		5.5	V
AVDD		2.7		5.5	V
AVDD and IOVDD Supply Current (HART Mode)					
Demodulator active	External Clock, -40°C to 85°C		110	150	µA
	External Clock, -55°C to 125°C			220	µA
	External Clock, -40°C to 85°C, External Reference		100	140	µA
	External Clock, -55°C to 125°C, External Reference			210	µA
Modulator active	External Clock, -40°C to 85°C		160	180	µA
	External Clock, -55°C to 125°C			250	µA
	External Clock, -40°C to 85°C, External Reference		150	170	µA
	External Clock, -55°C to 125°C, External Reference			240	µA
Crystal Oscillator	External Crystal, 16pF at XTAL1 and XTAL2		40	65	µA
	External Crystal, 36pF at XTAL1 and XTAL2		40	65	µA
Internal Oscillator	External Reference		105	180	µA
SPI Interface	Additional quiescent current required when interfacing via SPI		5		µA
AVDD and IOVDD Supply Current (FF/PA Mode)					
Decoder active	External Clock, -40°C to 85°C		160	220	µA
	External Clock, -55°C to 125°C			330	µA
	External Clock, -40°C to 85°C, External Reference		175	200	µA
	External Clock, -55°C to 125°C, External Reference			320	µA
Encoder active	External Clock, -40°C to 85°C		175	250	µA
	External Clock, -55°C to 125°C			360	µA
	External Clock, -40°C to 85°C, External Reference		165	235	µA
	External Clock, -55°C to 125°C, External Reference			350	µA

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Electrical Characteristics (continued)

All specifications over -40°C to +125°C ambient operating temperature, 2.7V ≤ AVDD ≤ 5.5V, 1.71V ≤ IOVDD ≤ 5.5V, Internal Reference, Internal Filter, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crystal Oscillator	External Crystal, 16pF at XTAL1 and XTAL2		40	65	µA
	External Crystal, 36pF at XTAL1 and XTAL2		40	65	µA
SPI Interface	Additional quiescent current required when interfacing via SPI		5		µA
AVDD and IOVDD Supply Current (All Modes)					
Power-Down Mode	Internal reference disabled, -40°C to 85°C, no active clock input		30	60	µA
	Internal reference disabled, -55°C to 125°C, no active clock input			182	µA
CLOCK REQUIREMENTS					
EXTERNAL CLOCK (HART MODE)					
External Clock Source Frequency	3.6864 MHz Clock	3.6469	3.6864	3.7232	MHz
	1.2288 MHz Clock	1.2165	1.2288	1.2411	MHz
EXTERNAL CLOCK (FF/PA MODE)					
External Clock Source Frequency	4 MHz Clock	3.96	4	4.04	MHz
INTERNAL OSCILLATOR					
Frequency	-40°C to 125°C	1.2165	1.2288	1.2411	MHz
VOLTAGE REFERENCE					
INTERNAL REFERENCE VOLTAGE					
Internal Reference Voltage		1.47	1.5	1.53	V
Load Regulation			1.3		V/mA
Capacitive Load	Guaranteed by design		1		µF
OPTIONAL EXTERNAL REFERENCE VOLTAGE					
External Reference Input Voltage		2.375	2.5	2.625	V
External Reference Input Current	Demodulator		4.5		µA
	Modulator		4.5		µA
	Internal Oscillator		4.5		µA
	Power-Down		4.5		µA
HART MODEM					
MOD_IN INPUT (HART MODE)					
Input Voltage Range	External Reference Source, guaranteed by design. Signal applied at the input to the DC blocking capacitor.	0		1.5	Vp-p
	Internal Reference Source, guaranteed by design. Signal applied at the input to the DC blocking capacitor.	0		1.5	Vp-p
Receiver Sensitivity	Threshold for successful carrier detection and demodulation, assuming ideal sinusoidal input FSK signals with valid preamble using internal filter.	80	100	120	mVp-p
MOD_OUT OUTPUT (HART MODE)					
Output Voltage	AC-coupled (2.2µF), measured at MOD_OUT pin with 160Ω load	450	460	480	mVp-p
Mark Frequency	Internal Oscillator		1200		Hz
Space Frequency	Internal Oscillator		2200		Hz
Frequency Error	Internal Oscillator, -40°C to 125°C	-1		1	%
Phase Continuity Error	Guaranteed by design			0	Degrees

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Electrical Characteristics (continued)

All specifications over -40°C to +125°C ambient operating temperature, 2.7V ≤ AVDD ≤ 5.5V, 1.71V ≤ IOVDD ≤ 5.5V, Internal Reference, Internal Filter, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Minimum Resistive Load	160Ω, AC coupled with 2.2µF, guaranteed by design	160			Ω
Transmit Impedance	RTS low, measured at the MOD_OUT pin, 1mA measurement current		13		Ω
	RTS high, measured at the MOD_OUT pin, ±200nA measurement current		250		kΩ
FF / PA MODEM					
MOD_IN INPUT (FF/PA MODE)					
Input Voltage Range	External Reference Source, specified by design. Signal applied at the input to the DC blocking capacitor.	0		1	Vp-p
	Internal Reference enabled, specified by design. Signal applied at the input to the DC blocking capacitor.	0		1	Vp-p
Receiver Jitter Tolerance	Edge-to-edge measurement of Manchester Encoded waveforms	-3.2		3.2	µs
Receiver Sensitivity	Threshold for successful carrier detection and decoding, assuming ideal Manchester Encoded input trapezoidal signals with 6µs rise time, valid preamble byte(s) and start delimiter byte, using internal filter.	75			mVp-p
MOD_OUT OUTPUT (FF/PA MODE)					
Output Voltage			800		mVp-p
Maximum Amplitude Difference	Maximum difference in positive and negative amplitude signals	-50		50	mV
Transmit Bit Rate		31.1875	31.25	31.3125	kbit/s
Transmit Jitter	Measured with respect to ideal crossing of high time and low time	-0.8		0.8	µs
Output Signal Distortion	Measured peak to trough distortion for positive and negative amplitude voltage outputs	-10		10	%
Rise and Fall Time	10% to 90% of peak to peak signal			8	µs
Slew Rate	10% to 90% of peak to peak signal			0.2	V/µs
DIGITAL REQUIREMENTS					
DIGITAL INPUTS					
VIH, Input High Voltage		0.7 x IOVDD			V
VIL, Input Low Voltage				0.3 x IOVDD	V
CLK_CFG0, Input High Voltage	Guaranteed by design	0.8 x IOVDD			V
CLK_CFG0, Input Mid-Scale Voltage	Guaranteed by design	0.4 x IOVDD		0.55 x IOVDD	V
CLK_CFG0, Input Low Voltage	Guaranteed by design			0.15 x IOVDD	
Input Current		-1		1	µA
Input Capcitance			5		pF
DIGITAL OUTPUTS					
VOH, Output High Voltage	200µA source/sink	IOVDD - 0.5			V
VOL, Output Low Voltage	200µA source/sink			0.4	V

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6.6 Timing Requirements

All timing conditions guaranteed by design

PARAMETER		MIN	NOM	MAX	UNIT
t_c	SCLK Cycle Time	80			ns
t_{w1}	SCLK High Time	32			ns
t_{w2}	SCLK Low Time	32			ns
t_{su}	/CS to SCLK Falling Edge Setup Time	32			ns
t_{su1}	Data Setup Time	5			ns
t_{h1}	Data Hold Time	5			ns
t_{d1}	SCLK Falling Edge to /CS Rising Edge	32			ns
t_{w3}	Minimum /CS High Time (1)	1			us
t_v	SCLK Rising Edge to SDO Valid	32			ns
t_{rst}	Reset low time	100			ns
HART Mode Timing					
t_{cstart}	Carrier start time. Time from RTS falling edge to transmit carrier reaching its first peak.			5	Bit-Times
t_{cstop}	Carrier stop time. Time from RTS rising edge to transmit carrier amplitude falling below the receive amplitude			3	Bit-Times
t_{cdecay}	Carrier decay time. Time from RTS riding edge to carrier amplitude dropping to zero.			6	Bit-Times
t_{cdeton}	Carrier detect on. Time from valid carrier on receive path to CD rising edge.			6	Bit-Times
$t_{cdetoff1}$	Carrier detect off. Time from valid carrier removed on receive path to CD falling edge.			3	ms
$t_{cdetoff2}$	Carrier detect on when transitioning from transmit mode to receive mode in the presence of a constant valid receive carrier.	2.1			ms
t_{cos1}	Crystal oscillator power-up time from enabling the oscillator via clock configuration pins with 16pF load capacitors.	25			ms
t_{cos2}	Crystal oscillator power-up time from enabling the oscillator via clock configuration pins with 36pF load capacitors.	25			ms
t_{ref}	Reference power-up time from enabling via hardware pin.	10			ms
t_{pow}	Transition time from power-down mode to normal operating mode with external clock and external reference.	30			µs

(1) Time between two consecutive $\overline{CS}$ rising edges must be ≥3.06 µs

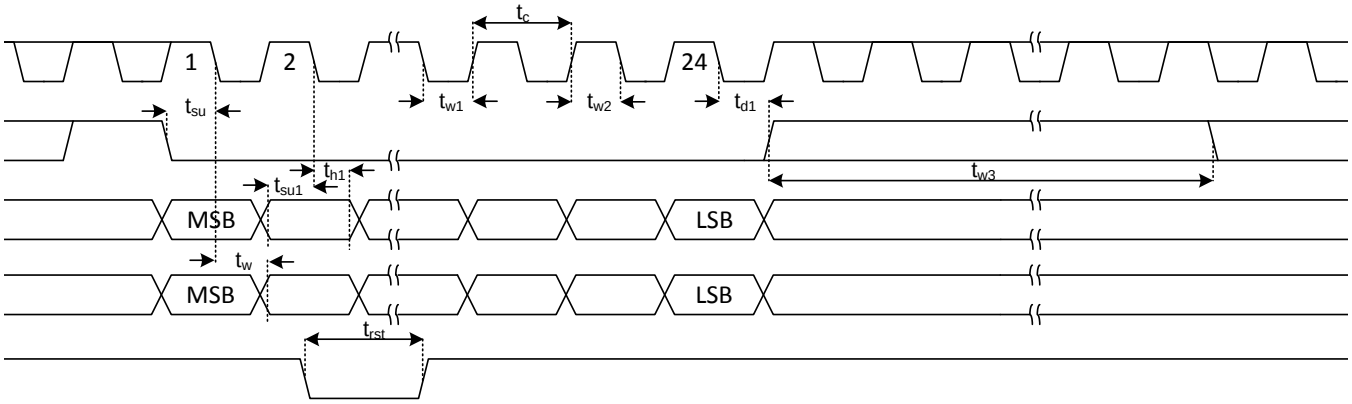


图 1. SPI Timing Diagram

6.7 Typical Characteristics

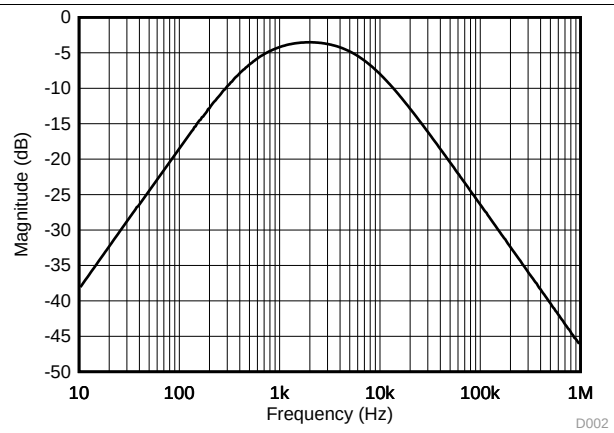


图 2. HART Mode External Band-Pass Filter Response

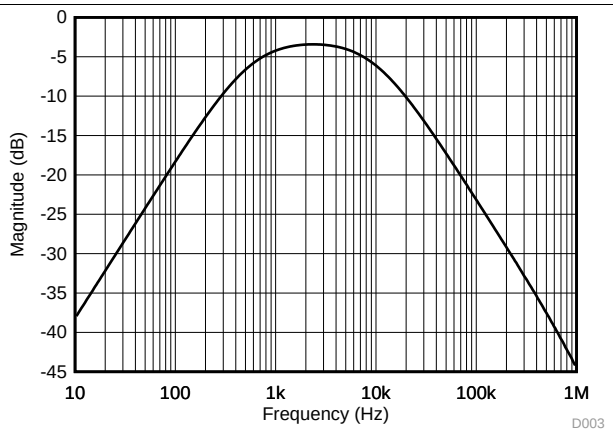


图 3. HART Mode Internal Band-Pass Filter Response

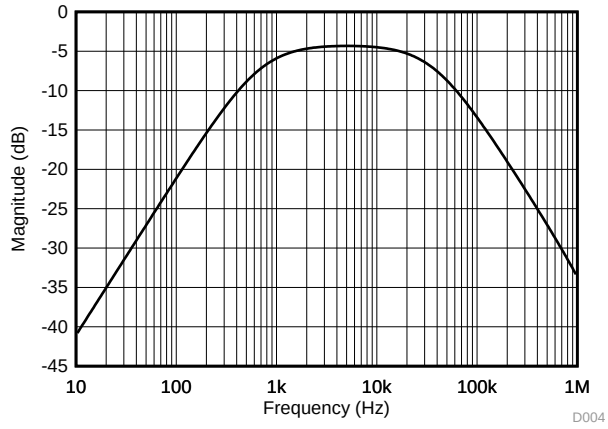


图 4. FF / PA Mode External Band-Pass Filter Response

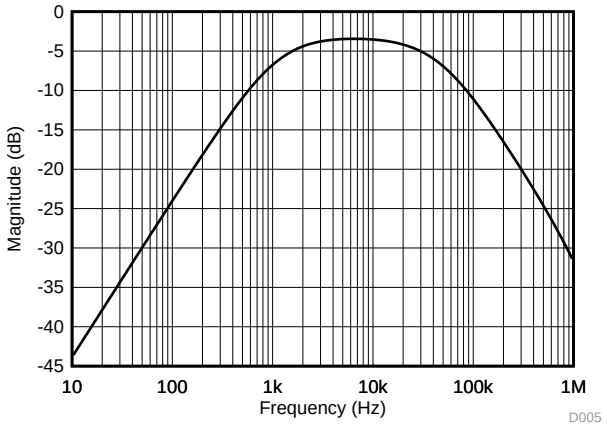


图 5. FF / PA Mode Internal Band-Pass Filter Response

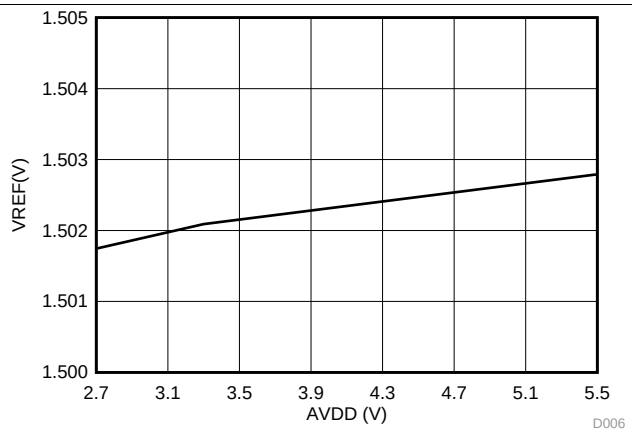


图 6. Internal Reference Voltage versus AVDD

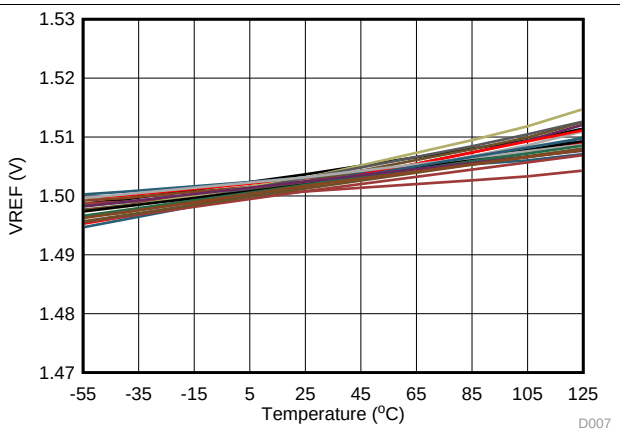


图 7. Internal Reference Voltage versus Temperature

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Typical Characteristics (接下页)

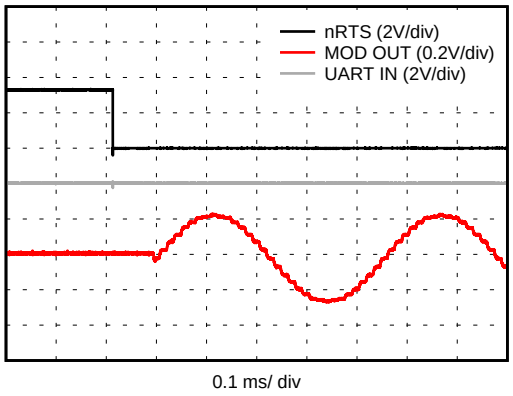


图 8. HART TX Carrier Start Time

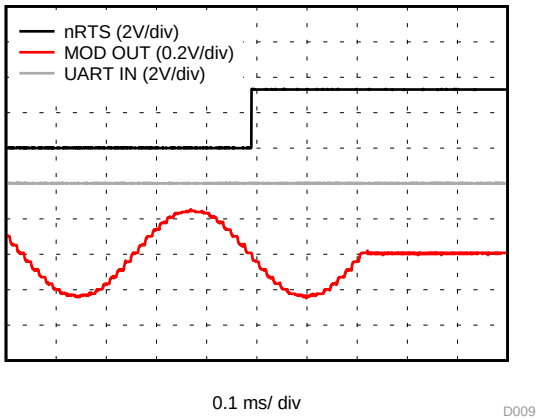


图 9. HART TX Carrier Stop / Decay Time

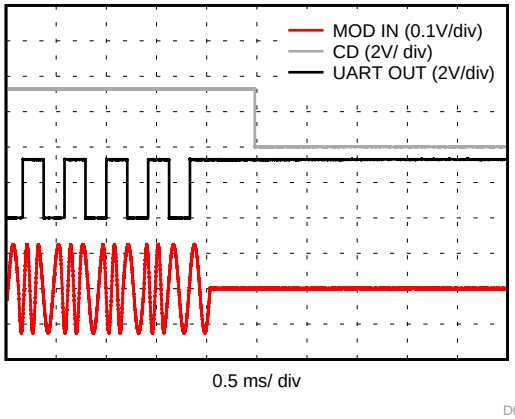


图 10. HART RX Carrier Detect Off Timing

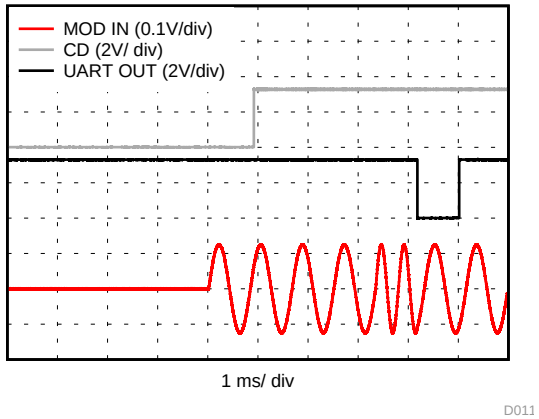


图 11. HART RX Carrier Detect On Timing

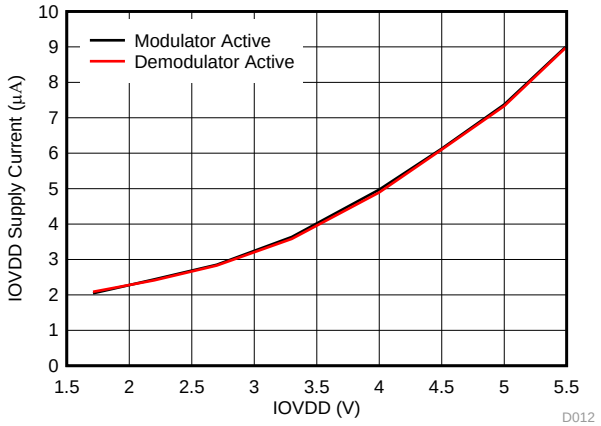


图 12. HART Mode IOVDD Supply Current versus Voltage with External Reference

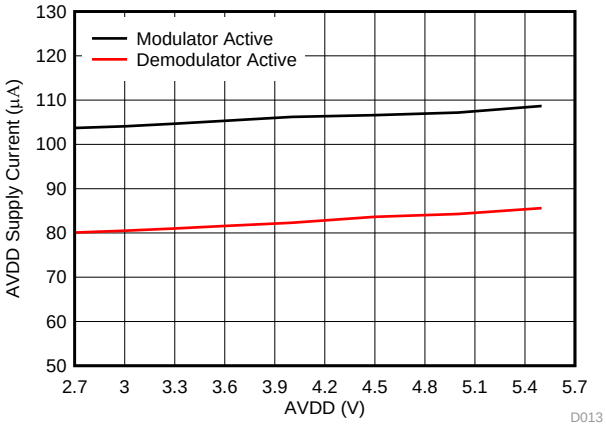


图 13. HART Mode AVDD Supply Current versus Voltage with External Reference

Typical Characteristics (接下页)

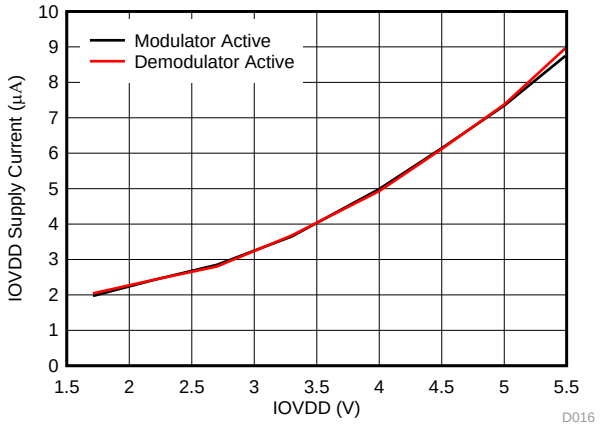


图 14. HART Mode IOVDD Supply Current versus Voltage with Internal Reference

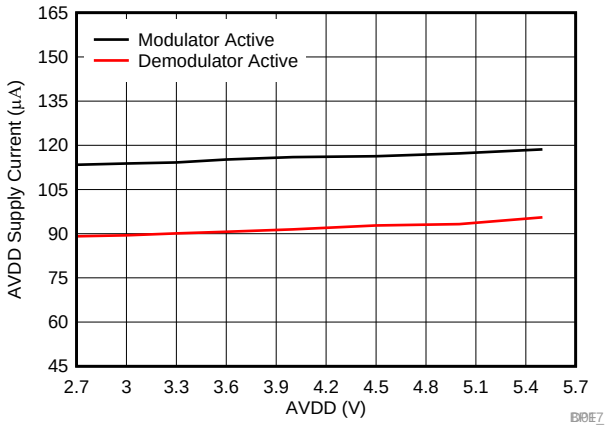


图 15. HART Mode AVDD Supply Current versus Voltage with Internal Reference

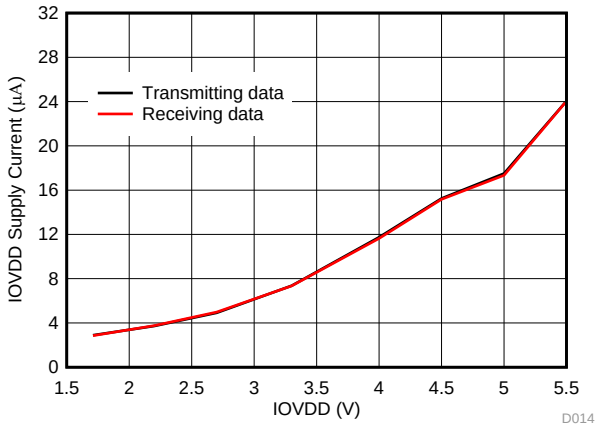


图 16. FF / PA Mode IOVDD Supply Current versus Voltage with External Reference

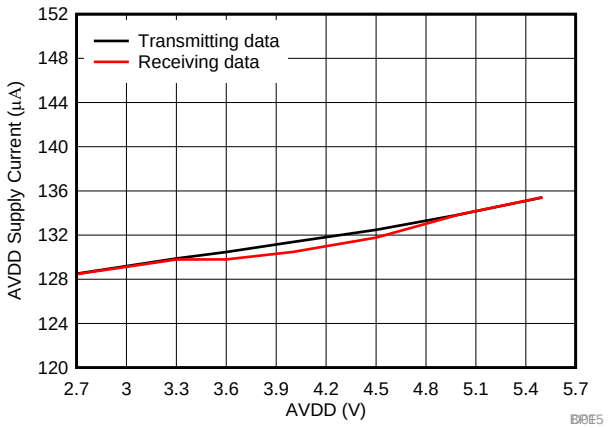


图 17. FF / PA Mode AVDD Supply Current versus Voltage with External Reference

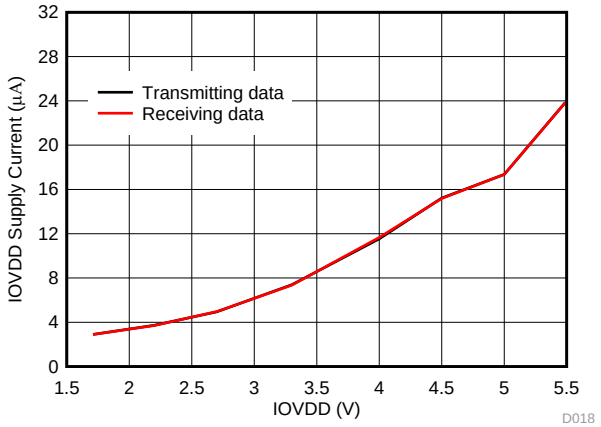


图 18. FF / PA Mode IOVDD Supply Current versus Voltage with Internal Reference

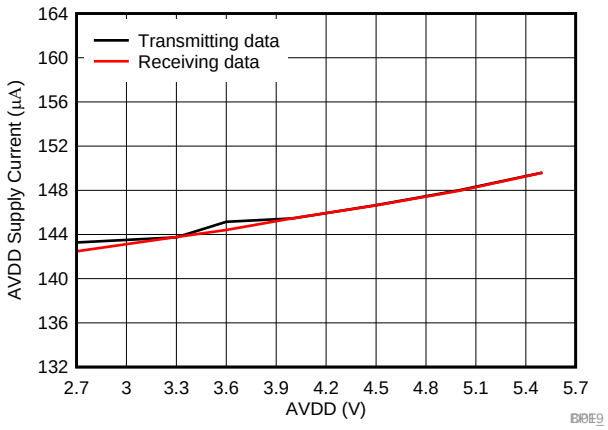


图 19. FF / PA Mode AVDD Supply Current versus Voltage with Internal Reference

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Typical Characteristics (接下页)

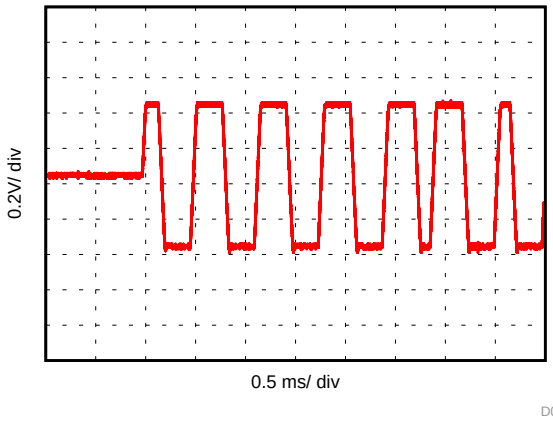


图 20. Typical Manchester Encoded Trapezoid, No Filter

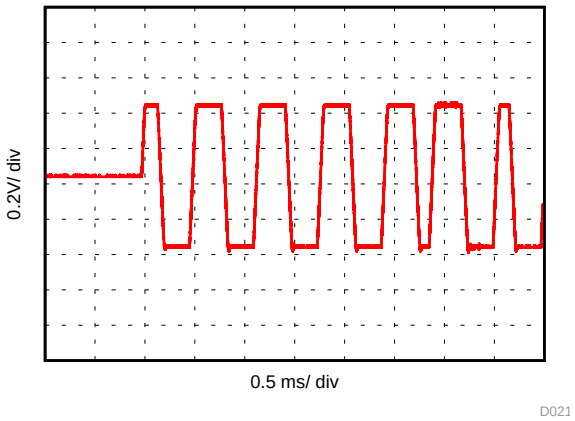


图 21. Typical Manchester Encoded Trapezoid, with Suggested Filter Response

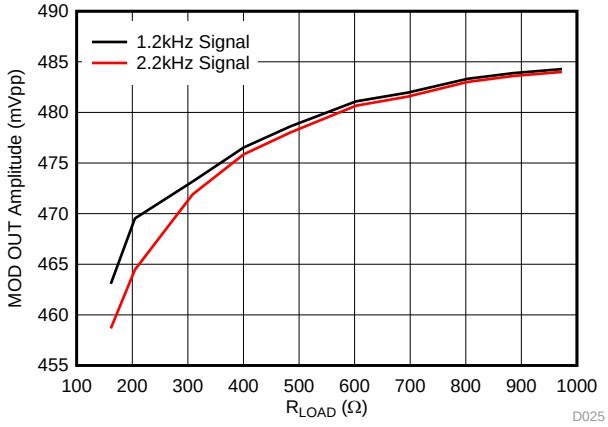


图 22. MOD_OUT Voltage versus R_{LOAD}

7 Detailed Description

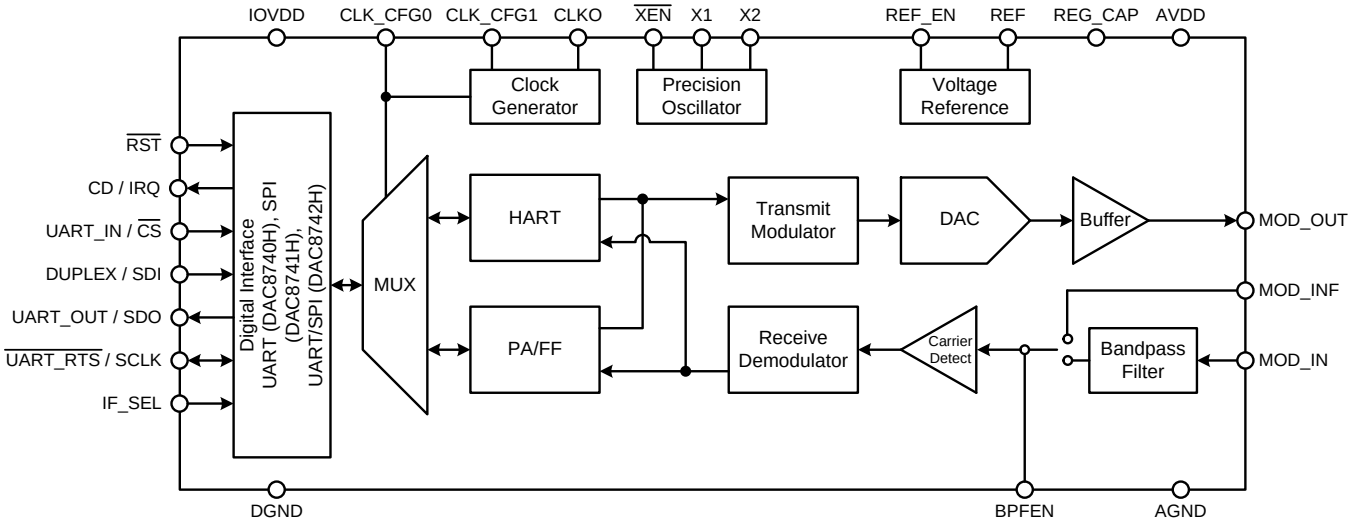
7.1 Overview

The DAC8742H is a HART© compliant and FOUNDATION Fieldbus® or PROFIBUS PA compatible low power modem designed for industrial process control and industrial automation applications.

In HART mode, the DAC8742H integrates all of the required circuitry to operate as half-duplex HART physical layer modems, in either slave or master configurations with minimal external components for filtering. In FOUNDATION Fieldbus mode, the DAC8742H integrate all of the required circuitry to operate as half-duplex FOUNDATION Fieldbus compliant H1 Controllers & MAUs.

The HART, FOUNDATION Fieldbus, or PROFIBUS PA, data stream can be transferred from the microcontroller through either a UART interface or an integrated FIFO accessed by a SPI interface. The SPI interface includes an SDO pin for daisy-chain support, various interrupts, and other extended features.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 HART Modulator

In SPI mode, HART data is loaded into a transmit FIFO via the SPI serial interface. In UART mode, the UART BAUD rate matches the HART BAUD rate and therefore the FIFO is bypassed. In both cases the input data is translated into the mark and space, 1200 Hz and 2200 Hz respectively, frequency shift keyed (FSK) analog signals used in HART communication through an internal HART modulator.

The HART modulator implements a look-up table containing 32 6-bit signed values which represent a single phase continuous sinusoidal cycle. A counter is implemented that incrementally loads the table values to a Digital-to-Analog Converter (DAC), at a clock frequency determined by the binary value of the input data, in order to create the mark and space analog output signals used to represent HART data.

The modem operates in half-duplex mode, unless placed in full-duplex mode, where the modulator and demodulator are not active simultaneously. The modem arbitrates over which component is active. To request that the modulator is activated UART devices toggle the RTS pin low, SPI devices toggle the RTS bit in the MODEM CONTROL register. These mechanics are explained in more detail in the respective sections of Device Functional Modes.

In HART mode the MOD_OUT pin requires parallel capacitance of 5-22 nF or 0-100 pF in FOUNDATION Fieldbus and PROFIBUS PA mode for stability.

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Feature Description (接下页)

7.3.2 HART Demodulator

The HART demodulator converts the HART FSK input signals applied at the MOD_IN or MOD_INF pins, depending on whether an external filter is implemented, to binary data that is loaded into a receive FIFO in SPI mode. Data in the receive FIFO can then be read by the host controller via SPI serial interface. In UART mode received data is directly fed through to the UART interface.

When a valid carrier is detected on devices using the UART interfaces, the CD pin will toggle high. For devices using the SPI interface, the IRQ pin will toggle indicating an alarm condition. The MODEM STATUS register can then be read to determine the source of the interrupt, which includes a bit for carrier detection in DB1. Hysteresis is implemented with the carrier detect feature in order to prevent erroneous carrier detection signals. More details are explained in the respective Device Functional Modes sections.

7.3.3 FOUNDATION FIELDBUS / PROFIBUS PA Manchester Encoder

FOUNDATION FIELDBUS or PROFIBUS PA data is loaded into a transmit FIFO via UART or SPI interfaces which is translated into the Manchester encoded binary analog signals used in both FOUNDATION FIELDBUS and PROFIBUS PA bus protocols through an internal Manchester encoder.

The Manchester encoder interacts with the DAC to transmit positive and negative amplitude signals, with respect to a positive common mode voltage, to create the Manchester encoded analog outputs at 31.25kHz BAUD. A binary 0 is represented by a low-to-high transition and a binary 1 is represented by a high-to-low transition.

In both UART and SPI interfaced device, the encoder is activated any time there is data available in the transmit FIFO and the decoder is not receiving data. In order to prevent FIFO buffer overflow, for UART mode the CD pin acts as an interrupt to indicate when the FIFO level has exceed a programmed threshold in the packet initiation code. In SPI mode the transmit FIFO threshold programmed in the FIFO LEVEL SET register can trigger an interrupt on the IRQ pin. Once the IRQ interrupts is triggered, the MODEM STATUS register can then be read to determine the source of the interrupt, which includes a bit for the FIFO level in DB4. More details are explained in the respective Device Functional Modes sections.

7.3.4 FOUNDATION FIELDBUS / PROFIBUS PA Manchester Decoder

The FOUNDATION FIELDBUS and PROFIBUS PA decoder converts the Manchester encoded data applied at the MOD_IN or MOD_INF pins, depending on whether an external filter is implemented, to binary data that is loaded into a receive FIFO. Data in the receive FIFO can then be read by the host controller via UART or SPI serial interfaces.

When valid data is provided to the decoder, binary data is read out serially on the UART interface. For SPI devices, the receive FIFO is loaded until the threshold programmed in FIFO LEVEL SET is met which will trigger an interrupt on the IRQ pin. The MODEM STATUS register can then be read to determine the source of the interrupt, which includes a bit for the FIFO level in DB7, indicating that data is ready to be read on the SPI bus. More details are explained in the respective Device Functional Modes sections.

7.3.5 Internal Reference

An internal reference is included in the DAC8742H. The REF_EN pin is used to enable or disable the internal reference, when the internal reference is disabled an external reference must be provided at the REF pin. In SPI mode, the $\overline{\text{PDVREF}}$ bit in the CONTROL register can be used to enable or disable the internal reference via software. If the REF_EN pin is set high, the register contents of the $\overline{\text{PDVREF}}$ bit is ignored.

INTERFACE	$\overline{\text{PDVREF}}$	REF_EN	REFERENCE MODE
UART	1 (Default)	0	External Reference
UART	1 (Default)	1	Internal Reference
SPI	1 (Default)	1	Internal Reference
SPI	0	1	Internal Reference
SPI	1 (Default)	0	External Reference
SPI	0	0	External Reference

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7.3.6 Clock Configuration

All of the devices in the DAC8742H family support a variety of clocking options in order to provide system flexibility and reduce overall current consumption in HART applications. The clocking options include: an internal oscillator (HART mode only), an external crystal oscillator, or an external CMOS clock. The selection of the clocking scheme is controlled by the XEN, CLK_CFG1, and CLK_CFG0 pins as described in the table below.

The internal oscillator takes approximately 50 ms to start oscillating from when it is enabled. During this time period the device is unable to perform modulation or demodulation activities.

表 1. Clock Configuration Table

$\overline{\text{XEN}}$	CLK_CFG1	CLK_CFG0	CLKO	DESCRIPTION	MODE
1	0	0	No Output	3.6864MHz CMOS clock connected at XTAL1	HART
1	0	1	No Output	1.2288MHz CMOS clock connected at XTAL1	
1	1	0	No Output	Internal oscillator enabled	
1	1	1	1.2288MHz Output	Internal oscillator enabled, CLKO enabled	
0	0	0	No Output	Crystal oscillator enabled	
0	0	1	3.6864MHz Output	3.6864MHz crystal oscillator, CLKO enabled	
0	1	0	1.8432MHz Output	3.6864MHz crystal oscillator, CLKO enabled	
0	1	1	1.2288MHz Output	3.6864MHz crystal oscillator, CLKO enabled	
1	0	0.5	No Output	4MHz CMOS clock connected at XTAL1	FOUNDATION FIELDBUS & PROFIBUS PA
1	1	0.5	No Output	2MHz CMOS clock connected at XTAL1	
0	0	0.5	No Output	4MHz crystal oscillator	
0	1	0.5	4MHz Output	4MHz crystal oscillator, CLKO enabled	

7.3.7 Reset and Power-Down

The $\overline{\text{RST}}$ pin functions as both a hardware reset and a power-down. When the pin is brought low a reset is issued, restoring all device components to their default state. While the pin is kept low, the device is in a power-down state where the internal reference is disabled, the modulator and demodulator or encoder and decoder are disabled, serial data output lines are high-impedance, MOD_OUT impedance is set to 70 kΩ, and the clock output is disabled. If an external crystal oscillator is used, the crystal oscillator circuit remains active to reduce start-up time when exiting the power-down state. Clock configuration pins remain active in power-down allowing the crystal oscillator to be disabled if desired.

7.3.8 Full-Duplex Mode

In full-duplex mode the modulator and demodulator (HART mode) or encoder and decoder (FOUNDATION FIELDBUS or PROFIBUS PA mode) are simultaneously enabled. This allows a self-test feature to verify functionality of the transmit and receive signal chains to improve system diagnostics.

7.3.9 I/O Selection

The DAC8742H implements both SPI and UART interfaces. Only one interface is active at a time for the DAC8742H. The interface mode is selected by the IF_SEL pin: a logic high on this pin sets the device to SPI mode and a logic low sets the device to UART mode. An internal pull-down resistor is included to ensure power-up in a known state, by default the pull-down sets the interface to UART mode. If changing I/O modes after power-up, a reset command should be issued on $\overline{\text{RST}}$.

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7.3.10 Jabber Inhibitor

The DAC8742H implements a Jabber Inhibitor feature in FOUNDATION FIELDBUS or PROFIBUS PA modes which prevents the encoder from continuously transmitting data on the bus for longer than a programmed threshold controlled by the UART or SPI interface. In SPI mode this threshold is programmed by the PAFF_JABBER register, in UART mode this threshold is programmed by the four byte initialization sequence before each transmission. This is described in further detail in the Device Functional Modes and Register Map sections.

7.4 Device Functional Modes

7.4.1 UART Interfaced HART

When interfacing the HART modem via the UART interface, the device can be thought of as a simple UART-to-HART or HART-to-UART direct feedthrough converter. The UART data is transmitted and received at 1200 BAUD, which is matched to the HART FSK input and output signals.

The HART communication protocol is a half-duplex protocol which means that either the modulator or demodulator is active, and never simultaneously enabled. The device arbitrates over which component of the modem is active at all times based on activity on the HART bus. Bus activity is interfaced to the host controller through the CD and $\overline{\text{RTS}}$ pins.

By default when $\overline{\text{RTS}}$ is high the demodulator is active and the modulator is inactive. When a valid carrier is detected and data is being received by the modem, the CD pin is toggled high and binary UART data is provided at the output. If a request to send is issued by toggling the $\overline{\text{RTS}}$ pin low while CD is high, the demodulator remains at priority and any data provided at the UART input is ignored. When CD is low no valid carrier is present and when $\overline{\text{RTS}}$ is brought low the modulator is activated and UART input data is latched into the modulator and placed onto the HART bus.

7.4.2 UART Interfaced FOUNDATION FIELDBUS / PROFIBUS PA

FOUNDATION FIELDBUS and PROFIBUS PA are half-duplex communication protocols where only the encoder or decoder are active at any time and the DAC8742H arbitrates over which path is active. When interfacing the FOUNDATION FIELDBUS or PROFIBUS PA modem via the UART interface, data placed in the transmit FIFO is automatically placed on the FF/PA bus until the FIFO is empty any time the device is not receiving data, assuming correct data format.

When receiving data the decoder will expect a preamble byte(s) and a start delimiter byte. These bytes, as well as the stop byte, will be stripped from the UART communication and only the first data byte will be transmitted to start the data packet. The host controller must use a timer to detect the end of the packet. Each byte transmitted on the UART will be at 57.6 kHz BAUD and byte spacing of 256 us. If a new byte has not been started within 512 us it can be assumed that the incoming packet has ended.

The device expects to see a four byte sequence to initiate transmission: 0xEA followed by 0x80-0x9F, where bits 4:3 of the second byte configure an interrupt threshold for the transmit FIFO level and bits 2:0 set the number of preamble bytes to be transmitted. The third byte contains the information to configure the Jabber Inhibitor followed by the final byte of 0xAE. To send inverted Manchester encoded data the first byte, 0xEA, is inverted to 0x15 and the first three bits of the second byte are inverted such that the range of values for the second byte are from 0x60-0x7F. The functionality of bits 4:3 and 2:0 and the Jabber Inhibitor byte remain the same and the final byte is inverted to 0x51. The details concerning this four byte sequence are explained in the tables below.

	B3								B2							
Mode	D7:D0								D7	D6	D5	D4	D3	D2	D1	D0
Non-inverted	1	1	1	0	1	0	1	0	1	0	0	D2M_LEVEL		PRE_BYTES		
Inverted	0	0	0	1	0	1	0	1	0	1	1	D2M_LEVEL		PRE_BYTES		

	B1	B0							
Mode	D7:D0	D7	D6	D5	D4	D3	D2	D1	D0
Non-inverted	JABBER_TIMEOUT	1	0	1	0	1	1	1	0
Inverted	JABBER_TIMEOUT	0	1	0	1	0	0	0	1

CONTROL BITS	DESCRIPTION		
D2M_LEVEL	0	0	Alarm on UART_RTS when transmit FIFO has less than 2 bytes loaded
	0	1	Alarm on UART_RTS when transmit FIFO has less than 4 bytes loaded
	1	0	Alarm on UART_RTS when transmit FIFO has less than 6 bytes loaded
	1	1	Alarm on UART_RTS when transmit FIFO has less than 8 bytes loaded
PRE_BYTES	Number of preamble bytes is equivalent to the straight binary decimal value in this register plus one		

The JABBER_TIMEOUT bits control the timeout period for the Jabber Inhibitor. If a value of 0x0 is programmed the Jabber Inhibitor is disabled. Otherwise the timer will be programmed in 2.048ms increments such that the timeout can be calculated as shown below. If the Jabber Inhibitor triggers the CD pin will be taken high. The CD pin will be returned to logic low when the silence period of 3 seconds has ended.

$$\text{TimeOut} = \text{JABBER_TIMEOUT} \times 2.048\text{ms} \quad (1)$$

The encoder will begin transmitting data once the following conditions are met: a valid four-byte transmission initiation sequence has been sent to the device, the FIFO is not empty, and the device is not receiving data. Transmission will begin by sending the preamble byte(s) followed by a start delimiter. Then, the encoder will begin to remove data from the FIFO – this creates at least a five-byte lag of the encoder with respect to the UART.

During transmission of a packet the UART must take care to ensure that the FIFO does not become empty before the packet is complete. The encoder transmits at a BAUD rate of 31.25 kHz or 256 µs per byte in the FIFO so the UART must keep up with this rate. The four-byte sequence that initiates a transmission includes setting a transmit FIFO threshold in bits 4:3. When the FIFO level is less than or equal to this threshold the UART_RTS pin will be taken high, this can be leveraged to ensure the FIFO is not prematurely empty. Once the FIFO is empty a stop delimiter is placed on the bus. Once the FIFO is empty a new packet can be initiated with a new four-byte transmission initiation sequence.

The device expects UART BAUD rate of 57.6 kHz. This BAUD rate is faster than the 31.25 kHz BAUD rate specified by FOUNDATION FIELDBUS and PROFIBUS PA, therefore FIFO overflow is possible. In order to prevent FIFO overflow, the UART_RTS pin FIFO threshold alarm can be leveraged by never adding more data to the FIFO than it can contain based on the programmed alarm threshold.

7.4.3 SPI Interfaced HART

When interfacing the HART modem via the SPI interface, the device utilizes transmit and receive FIFOs that are 9-bits wide and 16 locations deep to buffer all HART data.

The HART communication protocol is half-duplex protocol which means that either the modulator or demodulator is active, and never simultaneously enabled. The device arbitrates over which component of the modem is active at all times based on activity on the HART bus. Bus activity is interfaced to the host controller through the IRQ pin and MODEM STATUS register.

By default the demodulator is active and the modulator is inactive. When a valid carrier is detected and data is being received by the modem, the CD bit (bit 1) in the MODEM STATUS register is set high. If the CD bit (bit 1) in the MODEM IRQ MASK register is set to 0, this will also cause the IRQ pin to toggle as programmed in the status CONTROL register. The IRQ pin may be programmed to be edge sensitive or level sensitive, the polarity of the signal is also programmable. When the IRQ pin toggles, the MODEM STATUS register should be read to determine the source of the interrupt. Receive data can be read from the RECEIVE FIFO by issuing an SPI read command.

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Alternatively, the CD pin can be ignored by setting the CD bit (bit 1) in the MODEM IRQ MASK register to a 1. In this mode the IRQ pin will not toggle when the CD bit in the MODEM STATUS register is a 1. Instead, a RECEIVE FIFO read event can be triggered by the RECEIVE FIFO level threshold. This is achieved by programming the FIFO LEVEL SET register (bits 7:4) to the desired threshold value from 1-15, if a full FIFO (level 16 threshold) is desired the M2D FIFO FULL alarm can be used instead. If the M2D FIFO LEVEL bit (bit 7) in the MODEM IRQ MASK register is set to 0, the IRQ pin will toggle and the MODEM STATUS register should be read to determine the source of the interrupt. Receive data can then be read from the RECEIVE FIFO by issuing an SPI read command.

If data is placed in the transmit FIFO while the demodulator is active and the CD bit is high, the data remains in the FIFO until the modulator is activated. To request that the modulator is activated and the demodulator is deactivated the $\overline{\text{RTS}}$ bit (bit 0) in the MODEM CONTROL register should be set high. When the modulator is activated and the demodulator is deactivated the clear to send, or CTS, bit (bit 0) in the MODEM STATUS register is set high. If the CTS bit (bit 0) in the MODEM IRQ MASK register is set to a 0 this will cause the IRQ pin to toggle, indicating that transmit FIFO data will begin to be placed on the bus.

The level of the transmit FIFO may be monitored in order to avoid buffer overflow. This can be done either by watching for a buffer full or buffer threshold event. To monitor by a FIFO level threshold the FIFO LEVEL SET register (bits 3:0) can be programmed to the desired threshold value from 1-15. If the D2M FIFO LEVEL bit (bit 4) in the MODEM IRQ MASK register is set to a 0, this will cause the IRQ pin to toggle. Similarly an alarm can be triggered based on the D2M FIFO FULL bit in the MODEM STATUS register.

7.4.4 SPI Interfaced FOUNDATION FIELDBUS / PROFIBUS PA

FOUNDATION FIELDBUS and PROFIBUS PA are half-duplex communication protocols where only the encoder or decoder are active at any time and the DAC8742H arbitrates over which path is active. When interfacing the FOUNDATION FIELDBUS or PROFIBUS PA encoder via SPI interface, data is placed in transmit and receive FIFOs that are each 16-bytes deep to buffer all data.

When receiving data the decoder will expect a preamble byte(s) and a start delimiter byte, followed by the data bytes for the packet, and concluded with a stop delimiter byte. All of these bytes are placed into the RECEIVE FIFO where bits 7:0 represent the data and bit 8 is used as a special bit to indicate the start of a packet, with data 0x014D, the end of a packet, with data 0x0126, or a half-bit slip, with data 0x0100. If a half-bit slip occurs it is recommended to discard the packet. A timer is not necessary to detect the end of receiving a packet in SPI mode because the stop delimiter is included in the RECEIVE FIFO data.

In order to prevent RECEIVE FIFO overflow, alarms are available to watch a threshold of the FIFO or when the FIFO is full. If the FIFO is full it is possible for data to be lost. This is achieved by programming the FIFO LEVEL SET register (bits 7:4) to the desired threshold value from 1-15, if a full FIFO (level 16 threshold) is desired the M2D FIFO FULL alarm can be used instead. If the M2D FIFO LEVEL bit (bit 7) in the MODEM IRQ MASK register is set to 0, the IRQ pin will toggle and the MODEM STATUS register should be read to determine the source of the interrupt. Receive data can then be read from the RECEIVE FIFO by issuing an SPI read command.

The encoder will begin to send data by sending the preamble byte(s) followed by a start delimiter when the TRANSMIT FIFO is not empty and the device is not receiving data. The number of preamble bytes used in the packet is controlled by the PAFF PREAMBLE bits (bits14:12) in the MODEM CONTROL REGISTER. The polarity of the Manchester encoded data can also be programmed by the PAFF POLARITY bit (bit 15) in the MODEM CONTROL REGISTER. After transmitting the preamble byte(s) and start delimiter the encoder will begin taking data from the TRANSMIT FIFO.

During transmission the SPI controller must take care to ensure that the TRANSMIT FIFO does not become empty before the packet is complete. When the TRANSMIT FIFO is empty a stop delimiter is placed on the bus.

The level of the transmit FIFO may be monitored in order to avoid buffer overflow. This can be done either by watching for a buffer full or buffer threshold event. To monitor by a FIFO level threshold the FIFO LEVEL SET register (bits 3:0) can be programmed to the desired threshold value from 1-15. If the D2M FIFO LEVEL bit (bit 4) in the MODEM IRQ MASK register is set to a 0, this will cause the IRQ pin to toggle. Similarly an alarm can be triggered based on the D2M FIFO FULL bit in the MODEM STATUS register.

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The Jabber Inhibitor threshold can be programmed by the PAFF_JABBER register (address 0x27). The 8-bit value programmed in this register can be used to calculate the threshold using the equation below. When the timeout triggers the JAB_ON bit in the STATUS register will be taken high and transmission will be blocked for the 3 second timeout period. The JAB_OFF bit will go high when the timeout period has expired. Both JAB_ON and JAB_OFF bits trigger and IRQ event, meaning the IRQ pin will be triggered for both events.

$$\text{TimeOut} = \text{JABBER_TIMEOUT} \times 2.048\text{ms} \quad (2)$$

7.4.5 Interface

7.4.5.1 UART

The behavior of the UART interface changes based on whether the device is operating in HART mode or in FOUNDATION FIELDBUS and PROFIBUS PA mode.

In HART mode, the device expects 1 start bit, 8 data bits, 1 odd parity bit, and 1 stop bit or an 8O1 UART character format. The transmit path of the device acts as a direct feedthrough of the UART input to the HART FSK output, therefore the UART BAUD rate from the host controller must be 1200Hz ±1% as required by the HART standard. The receive path of the device will also operate at 1200Hz ±1%.

In FOUNDATION FIELDBUS and PROFIBUS PA mode the UART interface expects 1 start bit, 8 data bits, no parity bit, and 1 stop bit or an 8N1 UART character format. In this mode the UART interfaces transmit and receive FIFOs so the BAUD rate is not required to match the 31.25 kHz BAUD used by FOUNDATION FIELDBUS and PROFIBUS PA. In this mode the expected transmit and receive UART BAUD is 57.6 Hz ±2.5%.

7.4.5.1.1 UART Carrier Detect

The behavior of the carrier detect or CD pin changes depending on whether the device is in HART mode or FOUNDATION FIELDBUS and PROFIBUS PA mode.

In HART mode the pin operates as a carrier detect pin. When a valid carrier is detected and the modem is receiving data the CD pin is taken high. When the CD pin is high, UART data sent to the device and the request to send, or $\overline{\text{RTS}}$, pin will be ignored until the carrier is no longer present.

In FOUNDATION FIELDBUS and PROFIBUS PA the CD pin operates as a carrier detect pin when not in transmit mode. When the CD pin is high, UART data sent to the device will be ignored until the carrier is no longer present. When in transmit mode the CD pin functions as an alarm indicator that the jabber inhibitor has triggered and further UART transmission data will be ignored. In general if the CD pin is high the host controller should not be sending transmit data to the device.

7.4.5.2 SPI

The SPI interface can operate on SCLK speeds up to 12.5 MHz, but the frame-rate must be greater than 2442 ns in HART mode and 3000 ns in FOUNDATION FIELDBUS and PROFIBUS PA mode. Frames must contain at least 24-bits without CRC enabled and 32-bits with CRC enabled. The data within the frame is right justified, meaning that upon the rising edge of CS the right-most, or last, 24-bits or 32-bits will be evaluated as the input data word. Two modes of SPI are supported by the interface: clock polarity 0 and clock phase 1 or clock polarity 1 and clock phase 0.

The SDO pin will output data on the rising edge of SCLK or the falling edge of CS. SDO will always provide information from the previous frame, if the previous frame was a read then the output data will be the requested data. If the previous write was a command or register write, that data will be repeated. This allows a method for the user to verify what was written to the device. If CRC is enabled and write data is being repeated on SDO, the CRC provided during the previous frame will be output – not a newly calculated CRC.

The SPI frame structure is shown in the figure below. The frame includes a read/write bit, followed by a 7-bit address, then 16-bit write data for a write frame or don't care bits for a read frame. If CRC is enabled, an additional 8-bits are placed at the end of the frame containing the CRC word.

R/W FRAME	D23	D22:16	D15:0
Write Frame	0	7-Bit Address	Write Data
Read Frame	1	7-Bit Address	X

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7.4.5.2.1 SPI Cyclic Redundancy Check

The SPI interface includes an optional CRC mode to enhance the reliability of the interface by blocking erroneous commands sent to the device due to noise or other errors sources. When writing to or reading from the device the last 8-bits in the frame contain the CRC word which is calculated based on the polynomial x^8+x^2+x+1. If a bad CRC word is included in a write-frame to the device, the frame will be ignored. When reading from the device, the host controller should check the CRC word to validate the frame.

Read commands with a bad CRC value will output 0x80000000 and, in the case of a receive FIFO read, prevent data from leaving the FIFO and subsequently being lost.

7.4.5.2.2 SPI Interrupt Request

SPI interfaced devices include an interrupt request, or IRQ, pin to communicate the occurrence of a variety of events to the host controller. The behavior of the IRQ pin is controlled by the CONTROL register and MODEM IRQ MASK register.

The CONTROL register allows the host controller to configure the IRQ pin as level sensitive or edge sensitive via the IRQ LEVEL bit (bit 2). For both level sensitive and edge sensitive modes, the polarity of the IRQ pin can be set via the IRQ POLARITY bit (bit 3) in the CONTROL register.

The MODEM IRQ MASK register allows the controller to decide which events are able to trigger the IRQ pin to toggle. If a logic 0 is written to the respective bit, that event is allowed to toggle the IRQ pin. If a logic 1 is written to the respective bit, the event is masked from the IRQ pin.

When an event occurs the IRQ pin signal, in the case of level-sensitive configurations, is latched and the IRQ pin voltage stays at logic high until the status has been reset, or cleared, by reading the contents of the MODEM_STATUS register. In the case of edge-sensitive configurations a pulse is generated any time a new event is detected.

7.5 Register Maps

Table 2 lists the memory-mapped registers for the DAC8742H. All register offset addresses not listed in Table 2 should be considered as reserved locations and the register contents should not be modified.

Table 2. DAC8742H Registers

Offset	Acronym	Register Name	Section
2h	CONTROL	CONTROL Register	Go
7h	RESET	RESET Register	Go
20h	MODEM_STATUS	MODEM STATUS Register	Go
21h	MODEM_IRQ_MASK	MODEM IRQ MASK Register	Go
22h	MODEM_CONTROL	MODEM CONTROL Register	Go
23h	FIFO_D2M	FIFO D2M Register	Go
24h	FIFO_M2D	FIFO M2D Register	Go
25h	FIFO_LEVEL_SET	FIFO LEVEL SET Register	Go
27h	PAFF_JABBER	PAFF JABBER Register	Go

Complex bit access types are encoded to fit into small table cells. Table 3 shows the codes that are used for access types in this section.

Table 3. DAC8742H Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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7.5.1 CONTROL Register (Offset = 2h) [reset = 0x8042]

This register controls the SPI watch-dog timer, internal reference, CRC mode, IRQ pin behavior, and SDO pin behavior.

CONTROL is shown in Figure 23 and described in Table 4.

Return to Summary Table.

Figure 23. CONTROL Register

15	14	13	12	11	10	9	8
WDTO			WDT	RESERVED			
R/W			R/W	R			
7	6	5	4	3	2	1	0
RESERVED	PDVREF	RESERVED	CRC_EN	IRQ_POL	IRQ_LEVEL	SDO_Z	SDO_B
R	R/W	R	R/W	R/W	R/W	R/W	R/W

Table 4. CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	WDTO	R/W	100	SPI Watch-dog Timer (based on 3.6864MHz Clock) D15 D14 D13 Timeout Period 0 0 0 50 ms 0 0 1 100 ms 0 1 0 500 ms 0 1 1 1 second 1 0 0 2 seconds (default) 1 0 1 3 seconds 1 1 0 4 seconds 1 1 1 5 seconds
12	WDT	R/W	0	0 = SPI Watch-dog Timer Disabled (default) 1 = SPI Watch-dog Timer Enabled
11-7	RESERVED	R	00000	Reserved
6	PDVREF	R/W	1	This bit is only functional if the hardware reference enabled is enabled. 0 = Internal reference is powered down 1 = Internal reference is powered up (default)
5	RESERVED	R	0	Reserved
4	CRC_EN	R/W	0	0 = No CRC (default) 1 = CRC is enabled
3	IRQ_POL	R/W	0	0 = IRQ is active low (default) 1 = IRQ is active high
2	IRQ_LEVEL	R/W	0	0 = IRQ creates a pulse for edge sensitivity (default) 1 = IRQ asserts to a level until MODEM STATUS is read
1	SDO_Z	R/W	1	0 = SDO will be driven during writes and read requests 1 = SDO will be HiZ during writes requests (default)
0	SDO_B	R/W	0	0 = SDO will remain filled from last frame (default) 1 = SDO will clear with the beginning of each frame

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7.5.2 RESET Register (Offset = 7h) [reset = 0x0000]

Writing 0x0001 to this register will reset all registers to their default values and the FIFOs will be emptied.

RESET is shown in Figure 24 and described in Table 5.

Return to Summary Table.

Figure 24. RESET Register

15	14	13	12	11	10	9	8
RESERVED							
R							
7	6	5	4	3	2	1	0
RESERVED							RST
R							R/W

Table 5. RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R/W	000000000000000	Reserved
0	RST	W	0	Writing a 1 to this bit triggers a software reset.

7.5.3 MODEM_STATUS Register (Offset = 20h) [reset = 0x0000]

The modem status register is a read/write register. When an event occurs, the corresponding bit to indicate that event is set to a logic 1 in this register. The status bits are sticky, meaning they are not cleared unless a 1 is written to the corresponding bit position, except for carrier detect, or CD, which responds based on the presences of a carrier, the FIFO level registers, which respond based on the conditions of the FIFOs, and JAB_OFF and JAB_ON which represent the current status of the jabber inibhior. CTS will assert after RTS is set and no carrier is present if not operating in full-duplex mode.

MODEM_STATUS is shown in Figure 25 and described in Table 6.

Return to Summary Table.

Figure 25. MODEM_STATUS Register

15	14	13	12	11	10	9	8
RST	JAB_OFF	JAB_ON	GAP	FRAME	PARITY	WDT	CRC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
FIFO_M2D LEVEL	FIFO_M2D FULL	FIFO_M2D EMPTY	FIFO_D2M LEVEL	FIFO_D2M FULL	FIFO_D2M EMPTY	CD	CTS
R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 6. MODEM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RST	R/W	0	A reset has occurred
14	JAB_OFF	R/W	0	This bit goes high when the jabber inhibitor timeout period has expired
13	JAB_ON	R/W	0	This bit goes high when the jabber inhibitor has been triggered
12	GAP	R/W	0	A gap error in HART mode
11	FRAME	R/W	0	A frame error in HART mode or a 1/2 bit slip in FF/PA mode
10	PARITY	R/W	0	A Parity error in HART mode
9	WDT	R/W	0	The watch-dog timer has expired
8	CRC	R/W	0	An incorrect CRC word was provided in a read or write command
7	FIFO_M2D_LEVEL	R/W	0	The receive FIFO is at the programmed level
6	FIFO_M2D_FULL	R/W	0	The receive FIFO is full
5	FIFO_M2D_EMPTY	R/W	0	The receive FIFO is empty

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Table 6. MODEM_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	FIFO_D2M_LEVEL	R/W	0	The transmit FIFO is at the programmed level
3	FIFO_D2M_FULL	R/W	0	The transmit FIFO is full
2	FIFO_D2M_EMPTY	R/W	0	The transmit FIFO is empty
1	CD	R	0	In HART mode, a valid carrier has been detected
0	CTS	R	0	In HART mode, the modem is cleared to send data and the modulator is active

7.5.4 MODEM_IRQ_MASK Register (Offset = 21h) [reset = 0x0024]

This register controls which MODEM STATUS events are allowed to trigger an interrupt on the IRQ pin. A 0 in the respective bit position allows the interrupt event to toggle the IRQ pin. A 1 in the respective bit position blocks the interrupt event from toggling the IRQ pin, but the event can still be detected by reading the MODEM STATUS register.

MODEM_IRQ_MASK is shown in Figure 26 and described in Table 7.

Return to Summary Table.

Figure 26. MODEM_IRQ_MASK Register

15	14	13	12	11	10	9	8
RESERVED	JAB_OFF	JAB_ON	GAP	FRAME	PARITY	WDT	CRC
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
FIFO_M2D LEVEL	FIFO_M2D FULL	FIFO_M2D EMPTY	FIFO_D2M LEVEL	FIFO_D2M FULL	FIFO_D2M EMPTY	CD	CTS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 7. MODEM_IRQ_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0	Reserved
14	JAB_OFF	R/W	0	Writing a 1 to this bit blocks the JAB_OFF event from triggering the IRQ pin
13	JAB_ON	R/W	0	Writing a 1 to this bit blocks the JAB_ON event from triggering the IRQ pin
12	GAP	R/W	0	Writing a 1 to this bit blocks the GAP event from triggering the IRQ pin
11	FRAME	R/W	0	Writing a 1 to this bit blocks the FRAME event from triggering the IRQ pin
10	PARITY	R/W	0	Writing a 1 to this bit blocks the PARITY event from triggering the IRQ pin
9	WDT	R/W	0	Writing a 1 to this bit blocks the WDT event from triggering the IRQ pin
8	CRC	R/W	0	Writing a 1 to this bit blocks the CRC event from triggering the IRQ pin
7	FIFO_M2D_LEVEL	R/W	0	Writing a 1 to this bit blocks the FIFO_M2D_LEVEL event from triggering the IRQ pin
6	FIFO_M2D_FULL	R/W	0	Writing a 1 to this bit blocks the FIFO_M2D_FULL event from triggering the IRQ pin
5	FIFO_M2D_EMPTY	R/W	1	Writing a 1 to this bit blocks the FIFO_M2D_EMPTY event from triggering the IRQ pin
4	FIFO_D2M_LEVEL	R/W	0	Writing a 1 to this bit blocks the FIFO_D2M_LEVEL event from triggering the IRQ pin
3	FIFO_D2M_FULL	R/W	0	Writing a 1 to this bit blocks the FIFO_D2M_FULL event from triggering the IRQ pin
2	FIFO_D2M_EMPTY	R/W	1	Writing a 1 to this bit blocks the FIFO_D2M_EMPTY event from triggering the IRQ pin

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Table 7. MODEM_IRQ_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CD	R/W	0	Writing a 1 to this bit blocks the CD event from triggering the IRQ pin
0	CTS	R/W	0	Writing a 1 to this bit blocks the CTS event from triggering the IRQ pin

7.5.5 MODEM_CONTROL Register (Offset = 22h) [reset = 0x0048]

This register controls various modem features including: FF/PA Manchester data polarity, number of FF/PA preamble bits, analog output amplitude, modem enable, duplex mode, and request to send.

MODEM_CONTROL is shown in Figure 27 and described in Table 8.

Return to Summary Table.

Figure 27. MODEM_CONTROL Register

15	14	13	12	11	10	9	8
FFPA_POL	FFPA_PREAMBLE			RESERVED			TX_AMP
R/W	R/W			R			R/W
7	6	5	4	3	2	1	0
TX_AMP				MOD_EN	DUP_EN	RESERVED	RTS
R/W				R/W	R/W	R	R/W

Table 8. MODEM_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FFPA_POL	R/W	0	Sets the transmitted polarity of the Manchester encoded data 0 = Logical 1 is transmitted as a transition from high-to-low (default) 1 = Logical 1 is transmitted as a transition from low-to-high
14-12	FFPA_PREAMBLE	R/W	0	Number of preamble bytes sent is the value programmed in this register plus 1
11-9	RESERVED	R	0	Reserved
8-4	TX_AMP	R/W	00100	Unsigned binary value that controls the amplitude (HART mode only) of the transmitted waveform in 25mVpp steps. Default value 00100 for 500mVpp output amplitude. Amplitude may vary from 400mVpp to 800mVpp.
3	MOD_EN	R/W	1	0 = Disables TX/RX of the modem 1 = Enables TX/RX of the modem (default)
2	DUP_EN	R/W	0	0 – TX FIFO is not connected to RX FIFO (default) 1 = Connects TX FIFO to RX FIFO
1	RESERVED	R	0	Reserved
0	RTS	R/W	0	0 = No active request to send in HART mode (default) 1 = Active request to send in HART mode

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7.5.6 FIFO_D2M Register (Offset = 23h) [reset = 0x0200]

This register interfaces the FIFO that transmits data from the digital interface to the modem.

FIFO_D2M is shown in Figure 28 and described in Table 9.

Return to Summary Table.

Figure 28. FIFO_D2M Register

15	14	13	12	11	10	9	8
FIFO_LEVEL				LEVEL_FLAG	FULL_FLAG	EMPTY_FLAG	PARITY_BIT
R				R	R	R	W
7	6	5	4	3	2	1	0
DATA							
W							

Table 9. FIFO_D2M Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	FIFO_LEVEL	R	0	Reads back the current level of the FIFO, read only
11	LEVEL_FLAG	R	0	Indicates the programmed level has been reached, read only
10	FULL_FLAG	R	0	Indicates the FIFO is full, read only
9	EMPTY_FLAG	R	1	Indicates the FIFO is empty, read only
8	PARITY_BIT	W	0	Odd parity for 8-bit data read on bus, write only
7-0	DATA	W	0	Data transmitted from the digital interface to the modem, write only

7.5.7 FIFO_M2D Register (Offset = 24h) [reset = 0x0200]

This register interfaces the FIFO that receives data from the modem to the digital interface. This register is read only

FIFO_M2D is shown in Figure 29 and described in Table 10.

Return to Summary Table.

Figure 29. FIFO_M2D Register

15	14	13	12	11	10	9	8
FIFO_LEVEL				LEVEL_FLAG	FULL_FLAG	EMPTY_FLAG	PARITY_BIT
R				R	R	R	R
7	6	5	4	3	2	1	0
DATA							
R							

Table 10. FIFO_M2D Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	FIFO_LEVEL	R	0	Reads back the current level of the FIFO, read only
11	LEVEL_FLAG	R	0	Indicates the programmed level has been reached, read only
10	FULL_FLAG	R	0	Indicates the FIFO is full, read only
9	EMPTY_FLAG	R	1	Indicates the FIFO is empty, read only
8	PARITY_BIT	R	0	Odd parity for 8-bit data read on bus, read only
7-0	DATA	R	0	Data transmitted from the modem to the digital interface, read only

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7.5.8 FIFO_LEVEL_SET Register (Offset = 25h) [reset = 0x0000]

This register programs the alarm threshold for both transmit and receive FIFOs. Each bit field allows for the FIFO alarm threshold to be programmed to integer values from 1-15.

FIFO_LEVEL_SET is shown in Figure 30 and described in Table 11.

Return to Summary Table.

Figure 30. FIFO_LEVEL_SET Register

15	14	13	12	11	10	9	8
RESERVED							
R							
7	6	5	4	3	2	1	0
M2D_LEVEL				D2M_LEVEL			
R/W				R/W			

Table 11. FIFO_LEVEL_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	00000000	Reserved
7-4	M2D_LEVEL	R/W	0000	The binary value in this register sets the modulator FIFO alarm threshold
3-0	D2M_LEVEL	R/W	0000	The binary value in this register sets the demodulator FIFO alarm threshold

7.5.9 PAFF_JABBER Register (Offset = 27h) [reset = 0x0000]

This register controls the jabber inhibitor time-out behavior. The time-out can be calculated using the equation below with PAFF_JABBER in decimal format.

PAFF_JABBER is shown in Figure 31 and described in Table 12.

Return to Summary Table.

Figure 31. PAFF_JABBER Register

15	14	13	12	11	10	9	8
RESERVED							
R							
7	6	5	4	3	2	1	0
PAFF_JABBER							
R/W							

Table 12. PAFF_JABBER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	00000000	Reserved
7-0	PAFF_JABBER	R/W	00000000	TimeOut = JABBER_TIMEOUT * 2.048ms

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8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DAC8742H family of devices integrates modem functionality for several largely used Industrial protocols: Highway Addressable Remote Transducer (HART), FOUNDATION Fieldbus (FF), and PROFIBUS (PA). The different modes are set via the CLK_CFGx pins of the device that allow the device to either enter HART or PAFF mode. In HART mode, a 1200-/2200-Hz HART FSK Signal is modulated and demodulated, while the PAFF mode communicates via a 31.25 Kbit/s Manchester coded/encoded signal. The small package sizes, wide temperature range and low quiescent current make this device an ideal candidate for applications in Industrial Process Control and Automation.

8.1.1 Design Recommendations

Local power supply decoupling is recommended by placing 10-µF capacitors on the IOVDD and AVDD supply lines, and 0.1-µF capacitors close to the DAC8742H supply pins. Ceramic capacitor types such as C0G or X7R are recommended for its optimal performance across temperature, and very low dissipation factor. DC bias characteristics of the capacitors should also be considered when selecting passive components, such as the voltage rating and equivalent series resistance (ESR).

8.1.2 Selecting the Crystal/Resonator

Both communication modes, HART and PAFF, require different clocking frequencies for correct operation: HART – 1.2288 MHz or 3.686 MHz, PAFF – 4 MHz. In addition to selecting the communication mode, the CLK_CFGx and XEN pins also select whether an internal oscillator or external clock source is configured for device operation. The configuration table is explained in 表 1. Accuracy over the applications temperature range should be considered when selecting the external crystal or resonator. Furthermore, crystals with a low drift specification over the desired application temperature range should also be selected when using the DAC8742H devices in HART, FOUNDATION Fieldbus, and PROFIBUS PA applications as communication timing is critical. In order to reduce quiescent current consumption, the XTAL nets should be optimized during layout to reduce any length that may increase net capacitance. This increase in capacitance is directly proportion to current consumption.

8.1.3 Included Functions and Filter Selection

As a highly integrated device, the DAC8742H not only includes the modulation and demodulation capabilities for the previously described industrial protocols, but also includes an internal reference, and integrated receive bandpass filter, with other aforementioned functions. In HART mode, an internal amplifier provides high output drive capability, and can drive a wide range of purely capacitive loads, ranging from 5 nF to 22 nF. The lower value specified in the load range is to ensure output stability. Two different filter configurations, external and internal, are achievable through the BPF_EN digital input -- logic high on this pin enables the internal bandpass filter. The external filter configuration is shown in 图 32. The example provided displays the DAC8742H device configured with an external reference and external bandpass filter.

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Application Information (接下页)

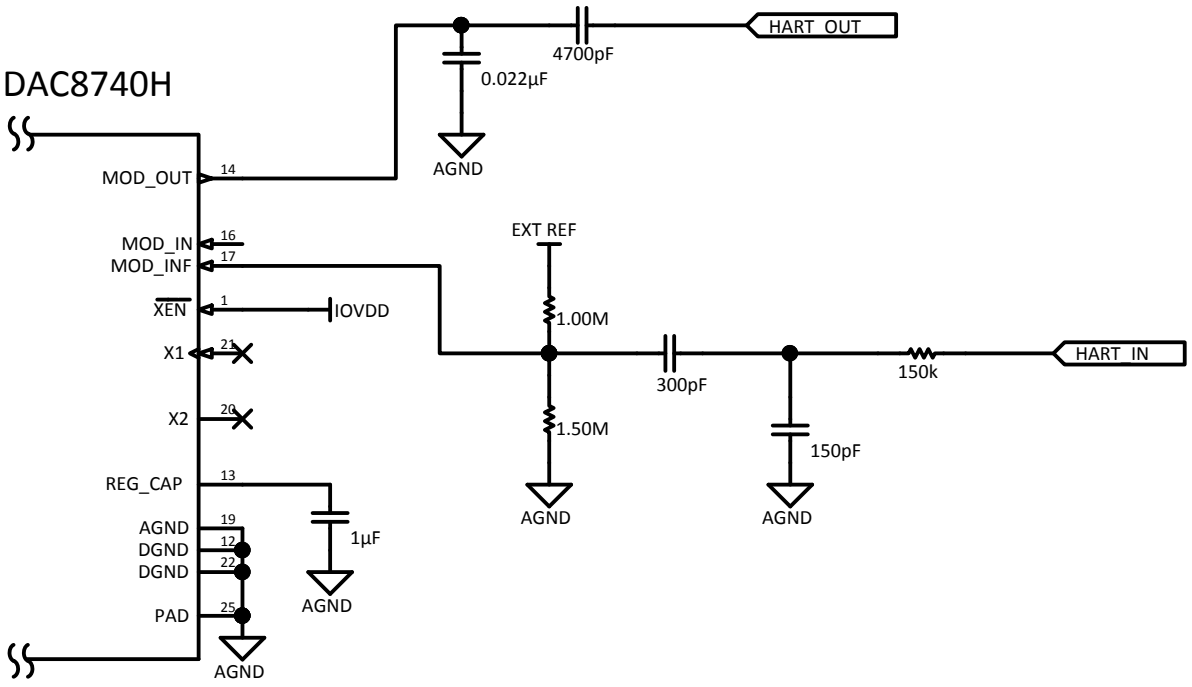


图 32. HART Mode: DAC8742H Passive Selection For External Bandpass Filter and External Reference

The second configuration, which can reduce costs associated with PCB development and BOM component counts, additionally aids in the optimization of board space. This optimization gives the user flexibility into achieving industrial applications with smaller form factor sizes. The internal filter configuration, with correct MOD_IN, MOD_INF, and MOD_OUT connections, is shown in 图 33.

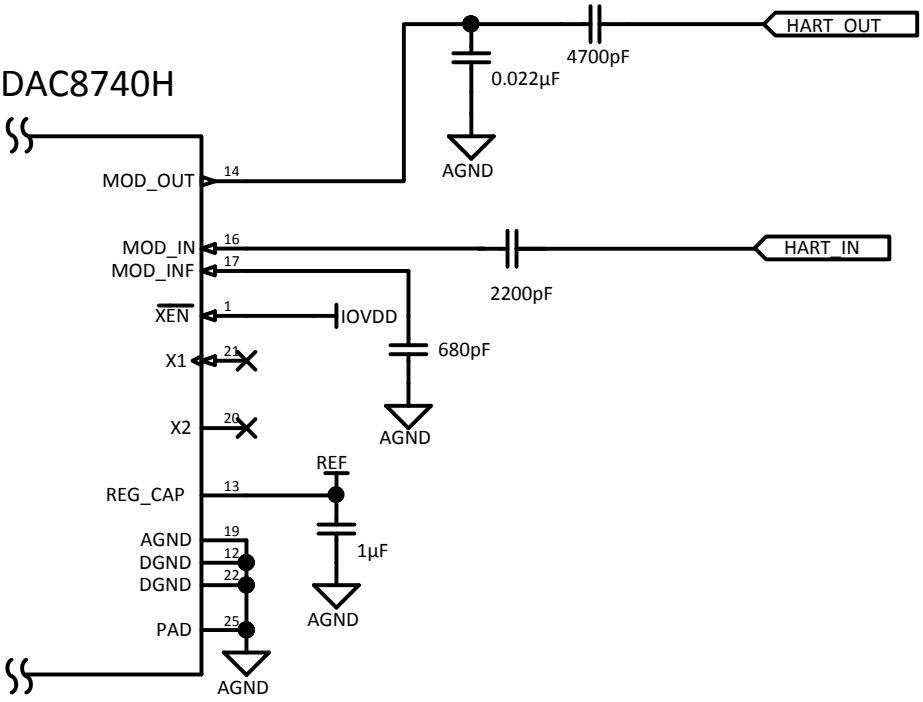


图 33. HART Mode: DAC8742H Passive Selection For Internal Filter

8.2 Typical Application

The application schematic shown in 图 34 is described in the following sections.

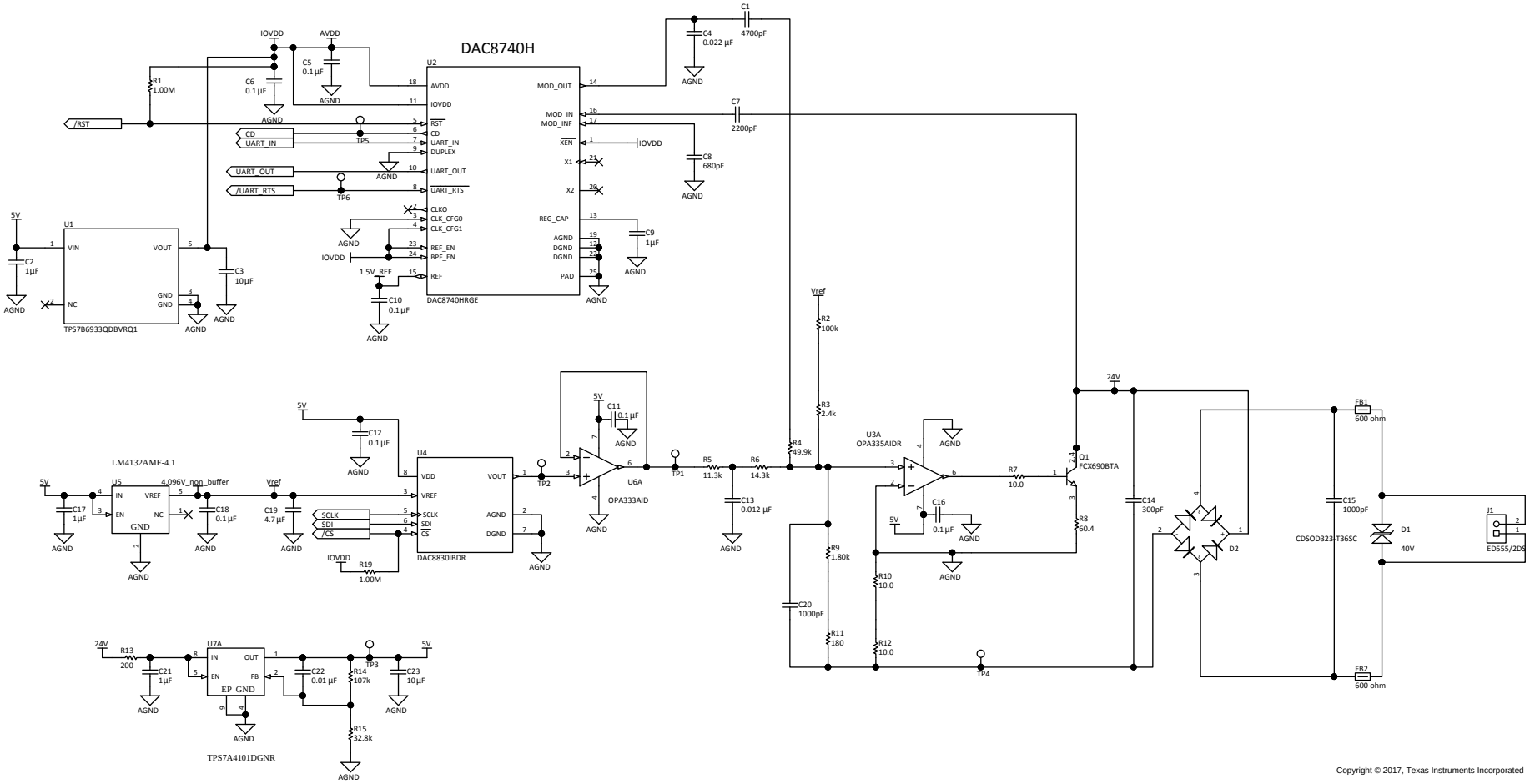


图 34. 2-Wire Transmitter with DAC8742H HART Modem Design Schematic

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8.2.1 Design Requirements

The application presented in 图 34 represents a loop-powered, 2-wire, smart 4-mA to 20-mA transmitter that commonly resides in factory control and industrial automation sectors. In this application, the DAC8742H enables a smart interface by providing HART communication, which is responsible for modulating two-way digital information that encapsulate a wide variety of data, including device/sensor information, calibration data, and system diagnostic information. This circuit has been successfully HART certification and registered with the FieldComm Group.

8.2.2 Detailed Design Procedure

8.2.2.1 DAC8742H HART Modem

In this design the DAC8742H internal reference and bandpass filter was chosen to optimize board area, consequently reducing form factor and cost. X7R, 10% accurate, bypass capacitances of 1-µF and 0.1-µF values were chosen for the reference and supplies, respectively.

The DAC8742H device interfaces with the MSP430FR5969, or other similar host controller, through a standard UART interface. The DAC8742H digital pins connected through this interface include UART_RTS, UART_OUT (TX), UART_IN (RX), and CD.

The remaining portion of the schematic includes other TI devices that aid in the realization of a highly accurate 4-mA to 20-mA, 2-wire transmitter. This combination of circuitry is ideally suited for remote signal conditioning of a wide variety of sensors and transducers, including thermocouples, RTDs, thermistors, and strain gauge bridges.

The two-wire transmitter is powered from an external DC power supply that is connected via the two BUS supply lines. The transmitter communicates by sourcing a 4-mA to 20-mA current through the connected bus, and back to the central host, which is typically a PLC analog input module. This expressed range of 4 mA to 20 mA is typically employed to adhere to industry standard, and ensures that the transmitter receives a minimum of 4 mA for correct powered operation.

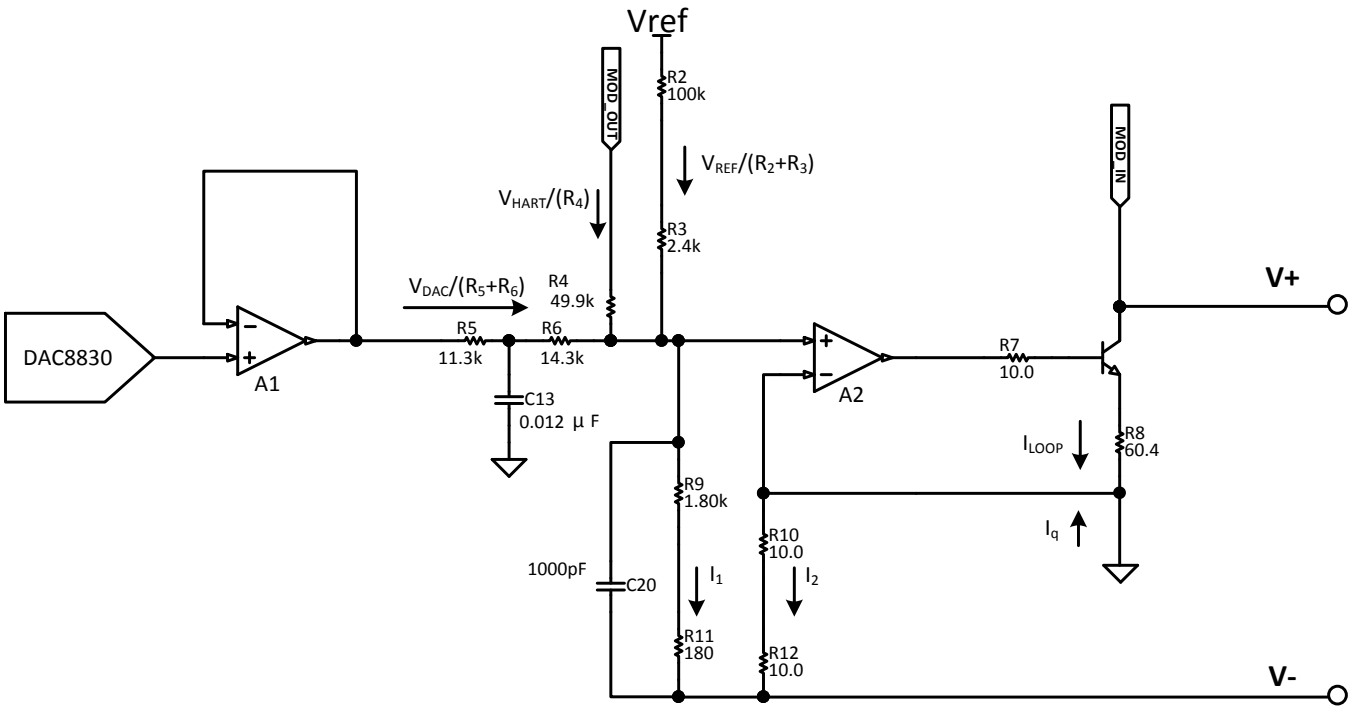


图 35. Simplified Schematic of the 2-Wire Current Loop

8.2.2.2 2-Wire Current Loop

The A2 operational amplifier employs negative feedback to ensure potentials at both input nodes, V+ and V-, are equivalent. This establishes the set of KCL equations (1) – assuming no HART communication, V_{HART} = 0 V.

I1 = VDAC/(25.6k) + VREF/(102.4k) (3)

A2 also drives the base of the NPN BJT, Q1, which enables current to flow from its collector through emitter pins and through the R8 resistor, while maintaining an equivalent potential drop from its input nodes to the net represented by TP4. This ensures that the combined voltage drop across R9 and R11 is equivalent to the combined drop of R10 and R12.

Using this relationship, along with current 公式 3 and 公式 4, I_{OUT} is calculated as follows:

$$I2 = I1 *(1.80k + 180)/(10 + 10) = I1*(1.980k/20) = I1*99 \quad (4)$$

$$I_{OUT} = I1 + I2 = [VDAC/(25.6k) + VREF/(102.4k)] + I1*99 = [VDAC/(25.6k) + VREF/(102.4k)]*(100) \quad (5)$$

For a VREF value of 4.096 V, the zero-scale portion of the transfer function, [VREF/(102.4k)]*(100), translates to 4 mA, while the span, [VDAC/(25.6k)]*100, encompasses 16 mA. This final product is a system capable of sourcing 4 mA to 20 mA, which is dependent on DAC output voltage. The value of R4 is responsible for converting the 500-mV p-p HART signal into a 1-mA p-p frequency shift keyed (FSK) signal that resides on top of the 4-mA to 20-mA analog current signal.

8.2.2.3 Regulator

The primary supply for the transmitter is the TPS7A4101 device, which is a 50-V input, 50-mA Single output low-dropout linear regulator with very low quiescent current, 25 µA. The device supplies a well-regulated voltage rail (1% accuracy), operating within an extended temperature range of –40°C to 125°C, and also withstands and maintains regulation during very high and fast voltage transients. In this design the LDO converts the external supply to a 5-V rail that is used by the DAC8830, LM4132 and OPA333/OPA335. The 200-Ω resistor that separates the loop supply from the LDO acts as a current limiting resistor at startup and additionally improves the overall receiver impedance of the design.

Generally, series references are preferred over shunt references because of their lower power consumption; in this case the LM4132 exhibits a maximum of 60-µA quiescent current. Moreover, the device has an initial accuracy of 0.05% with a specified temperature coefficient of 10 ppm/°C or less, and is capable of operating with these metrics at an extended temperature range of –40°C to 125°C.

In order to generate a 3.3-V supply for the DAC8742H, the TPS7B6933-Q1, a low-dropout linear regulator with low quiescent current, is incorporated into the design. This LDO is capable of operating over a wide temperature range of –40°C to 125°C, while exhibiting a maximum quiescent value of 25 µA over this temperature range.

8.2.2.4 DAC

After sufficient bypass, this precision reference voltage is applied to the VREF pin of the DAC8830 device. An accurate reference along with an accurate DAC are largely responsible for the overall accuracy of the current loop, as any accuracy errors associated with the DAC will propagate through the rest of the signal chain and decrease the accuracy of the solution. In this case, the DAC8830, a 16-bit voltage-output DAC with excellent linearity (1 LSB INL), low glitch, low noise, and fast settling was chosen to set the base line performance of the design.

8.2.2.5 Amplifiers

Next, the voltage output is buffered with the OPA333 CMOS operation amplifier, which features near-zero drift over time and temperature, low quiescent current (17 µA), and single supply operation with rail-to-rail output that swings within 50 mV of the supply rail.

As with the OPA333, the OPA335 was chosen due to its excellent DC accuracy specifications. These parameters include low input bias current, low offset voltage, and high CMRR/PSRR. In addition to these DC specifications, the OPA335 features an operating bandwidth of up to 2 MHz, which provides ample margin for HART communication.

8.2.2.6 Diodes

For transient voltage protection, a 40-V bidirectional transient voltage suppressor (TVS) diode is placed across the BUS lines of the design. Certain criteria should be considered when making this diode selection, such as the diode's working voltage, breakdown voltage, leakage current and power rating. In addition to these parameters, leakage current should also be factored into the design as it will impact the accuracy of the analog current loop.

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2-wire polarity protection is also employed by using the DSRHD10 as a diode bridge rectifier. The placement of this component ensures that the current loop will always correctly operate regardless of the arrangement of input connections. As with other elements, leakage and biasing voltage should be considered as it will affect system accuracy and compliance voltage.

8.2.2.7 Passives

Among the passives included in the design, the gain setting resistors should be chosen to exhibit tight tolerances in order to achieve high accuracy. These resistors -- R4, R5, R6, R9, R11, R10, and R12 -- are primarily responsible for setting the gain of the current loop, along with primary path of the output current flow. Since the biased transistor, Q1, is responsible for sourcing most of the output current, components in the path of this current flow should be chosen with appropriate power ratings. In this case R8 is a 0.25-W resistor.

8.2.3 Application Curves

Five hundred datapoints were taken on five different boards, producing the 4 to 20-mA transfer function below in 图 36. The total unadjusted error (TUE) of the transmitters is displayed in 图 37.

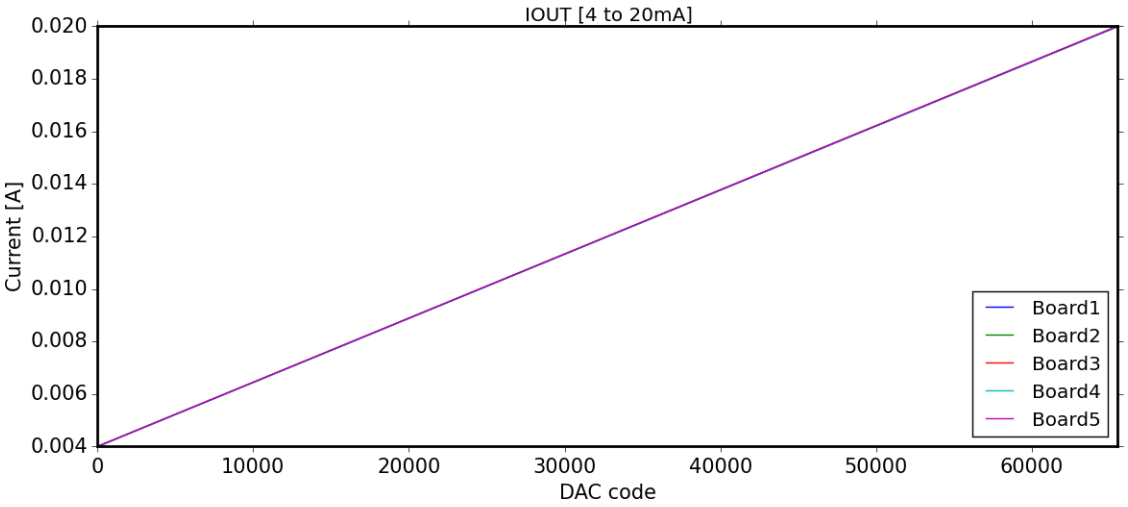


图 36. 4-20mA Transfer Function

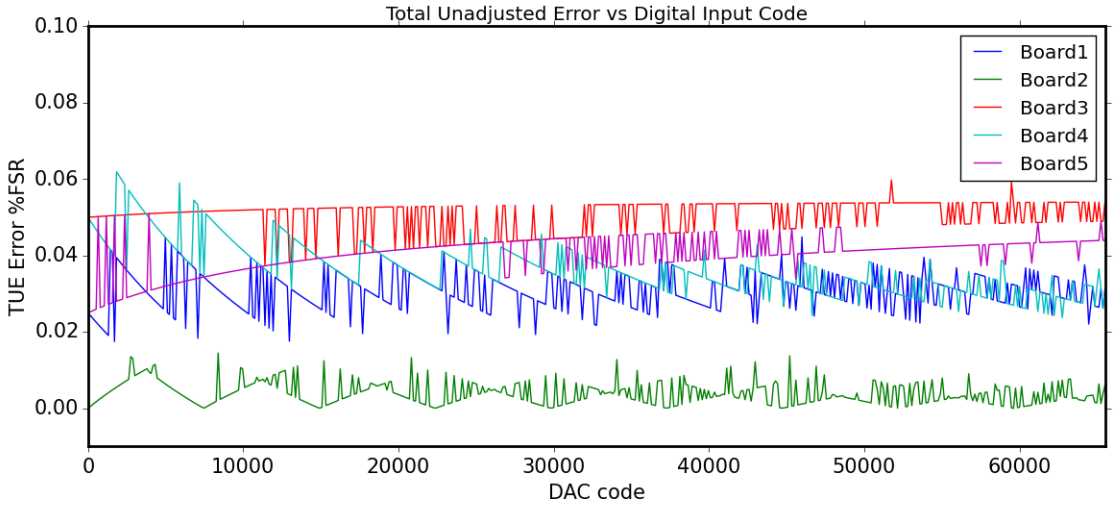


图 37. Total Unadjusted Error Graph of Application Circuit

9 Power Supply Recommendations

The DAC8742H can operate with analog supplies from 2.7 V to 5.5 V and digital supplies from 1.71 V to 5.5 V, enabling interfacing host controller platforms with low voltage digital logic. For applications that are particularly focused on reducing power dissipation in the modem, it is suggested to use the lowest supply voltage available for both analog and digital supplies.

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10 Layout

10.1 Layout Guidelines

Precision designs require careful layout, the list below provides some insight into good layout practices.

• All Power Supply pins should be bypassed to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 0.1 to 1 µF ceramic with a X7R or NP0 dielectric.

• Power supply and Reference bypass capacitors should be placed close to terminals to minimize inductance and optimize performance.

• A high-quality ceramic type NP0 or X7R is recommended for its optimal performance across temperature, and very low dissipation factor.

• The digital and analog sections should have proper placement with respect to the digital and analog components. The separation of analog and digital circuitry will allow for better design and practice as it will ensure less coupling into neighboring blocks, and will minimize the interaction between analog and digital return currents.

10.2 Layout Example

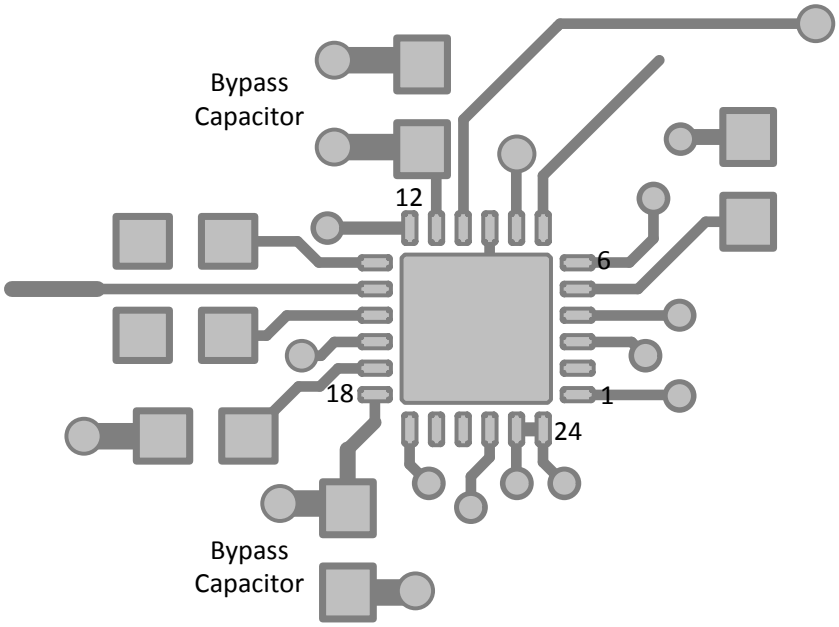


图 38. DAC8742H Basic Layout Example

Layout Example (接下页)

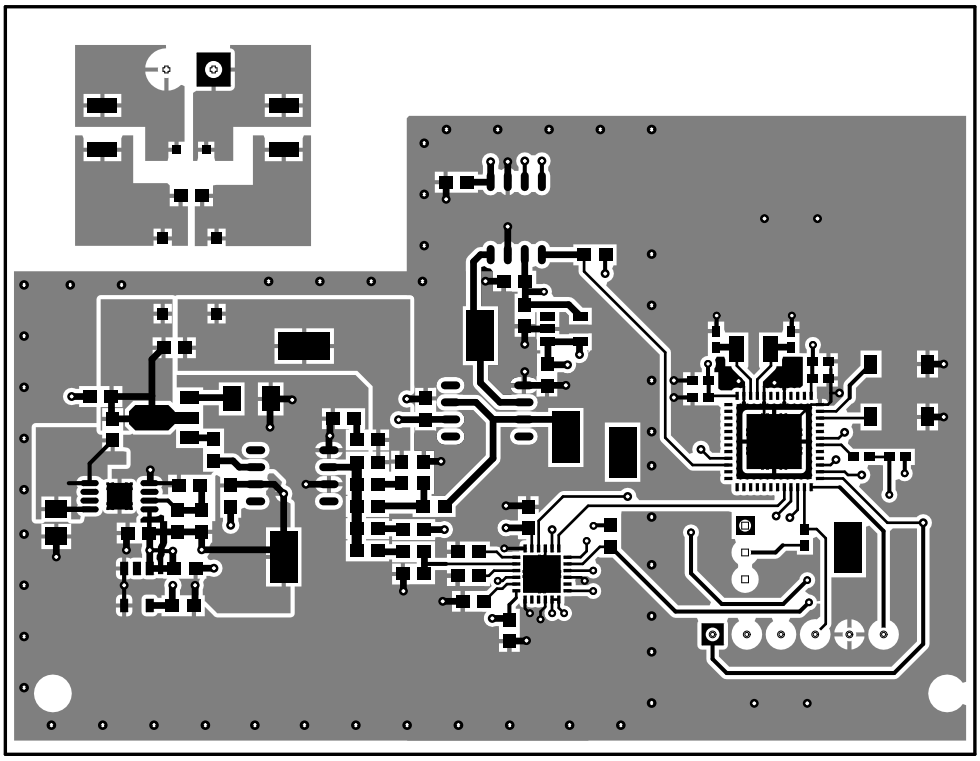


图 39. 2-Wire Transmitter with DAC8742H HART Modem Layout - Top Layer

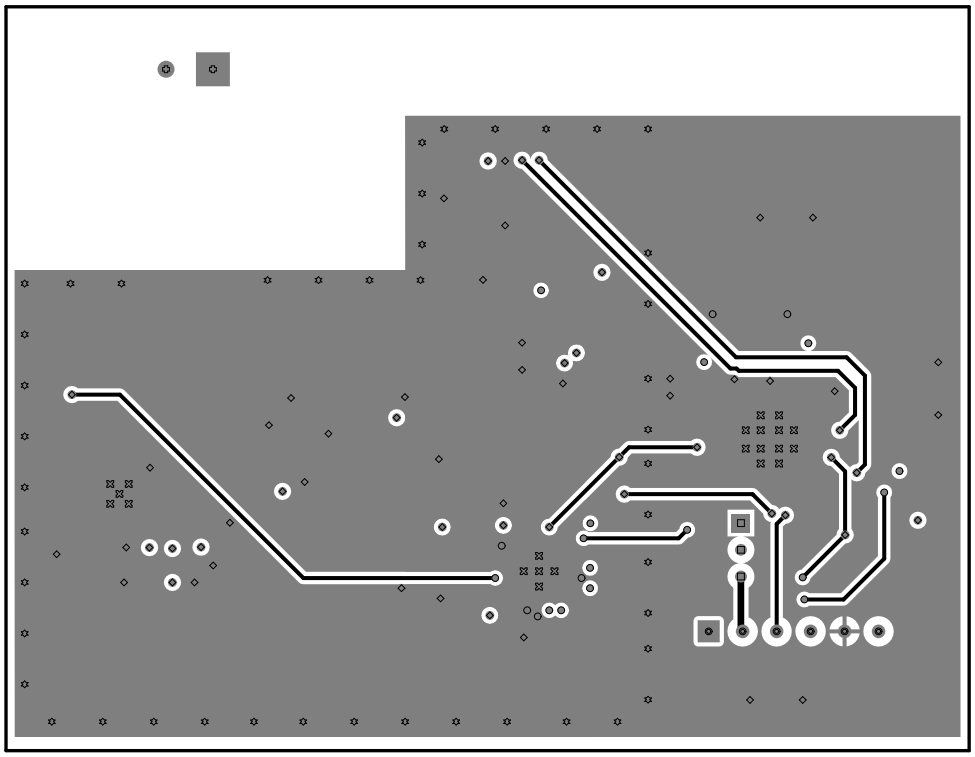


图 40. 2-Wire Transmitter with DAC8742H HART Modem Layout - Bottom Layer

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11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：《DAC8742H 评估模块用户指南》（SLAU700）

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC8742HPBS	Active	Production	TQFP (PBS) | 32	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	8742H
DAC8742HPBS.A	Active	Production	TQFP (PBS) | 32	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	8742H
DAC8742HPBSR	Active	Production	TQFP (PBS) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	8742H
DAC8742HPBSR.A	Active	Production	TQFP (PBS) | 32	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	8742H

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

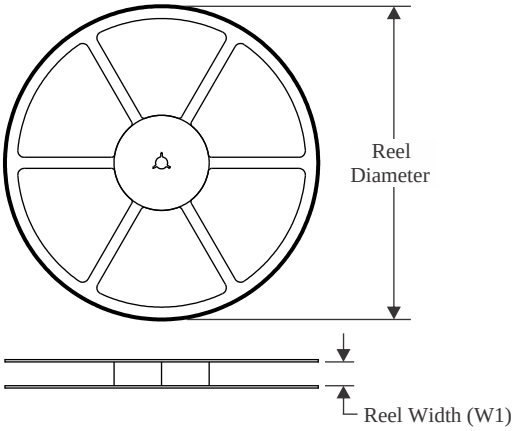
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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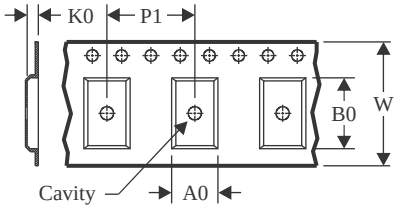
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

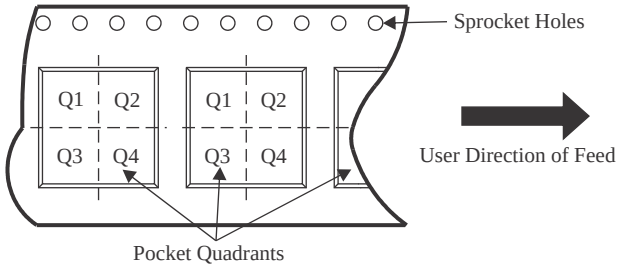


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

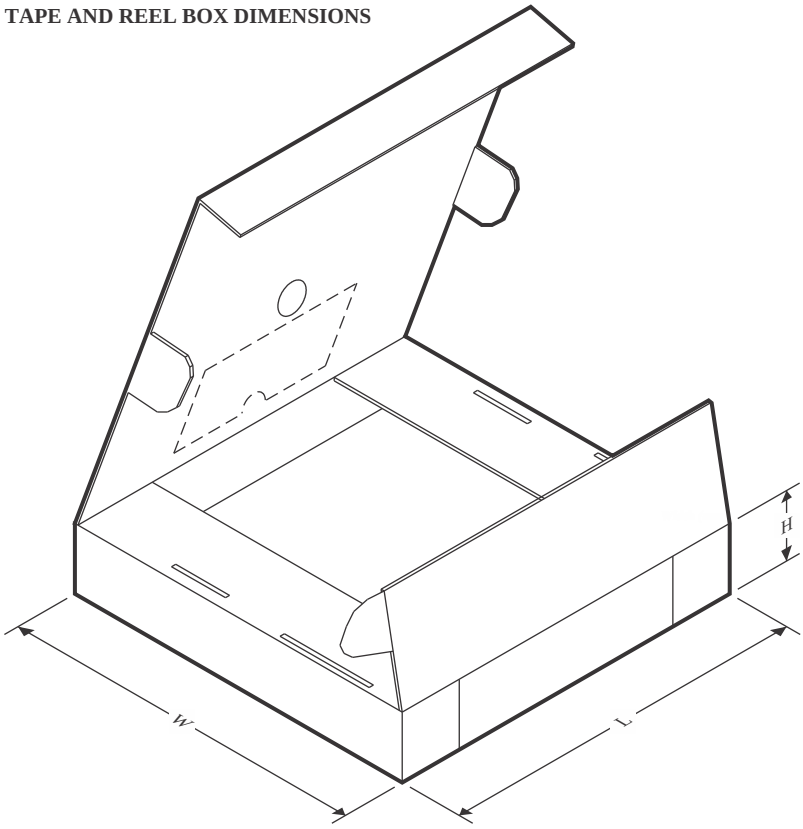
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8742HPBSR	TQFP	PBS	32	1000	330.0	16.4	7.2	7.2	1.5	12.0	16.0	Q2

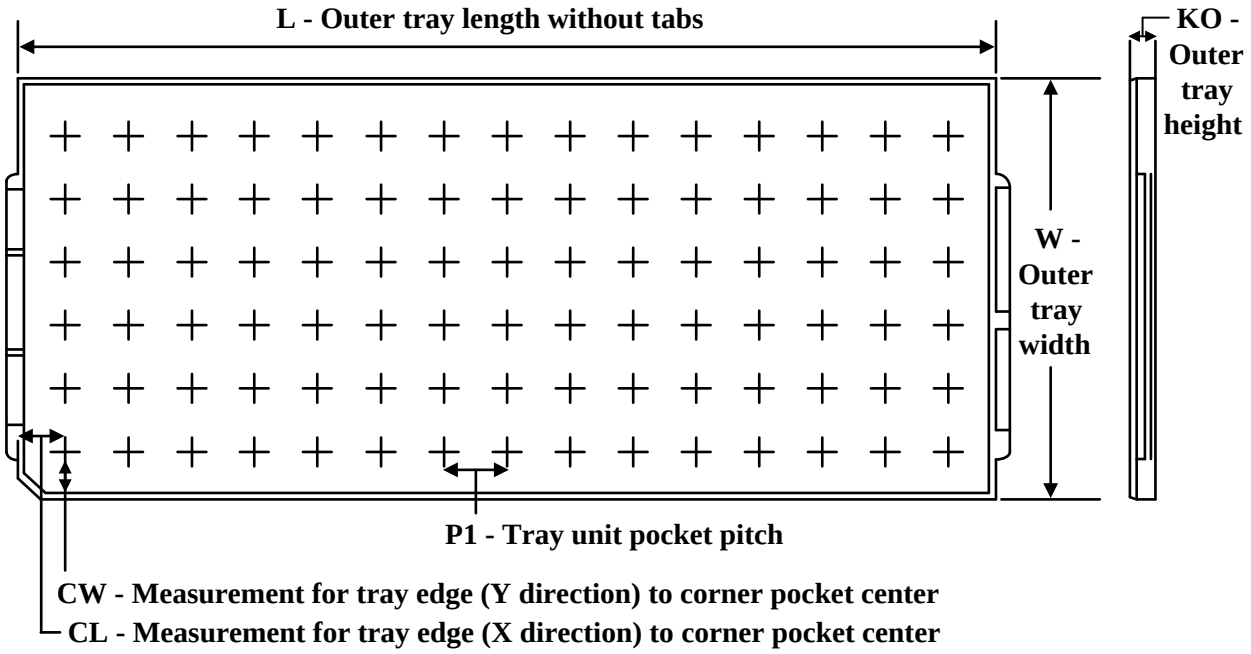
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8742HPBSR	TQFP	PBS	32	1000	350.0	350.0	43.0

TRAY

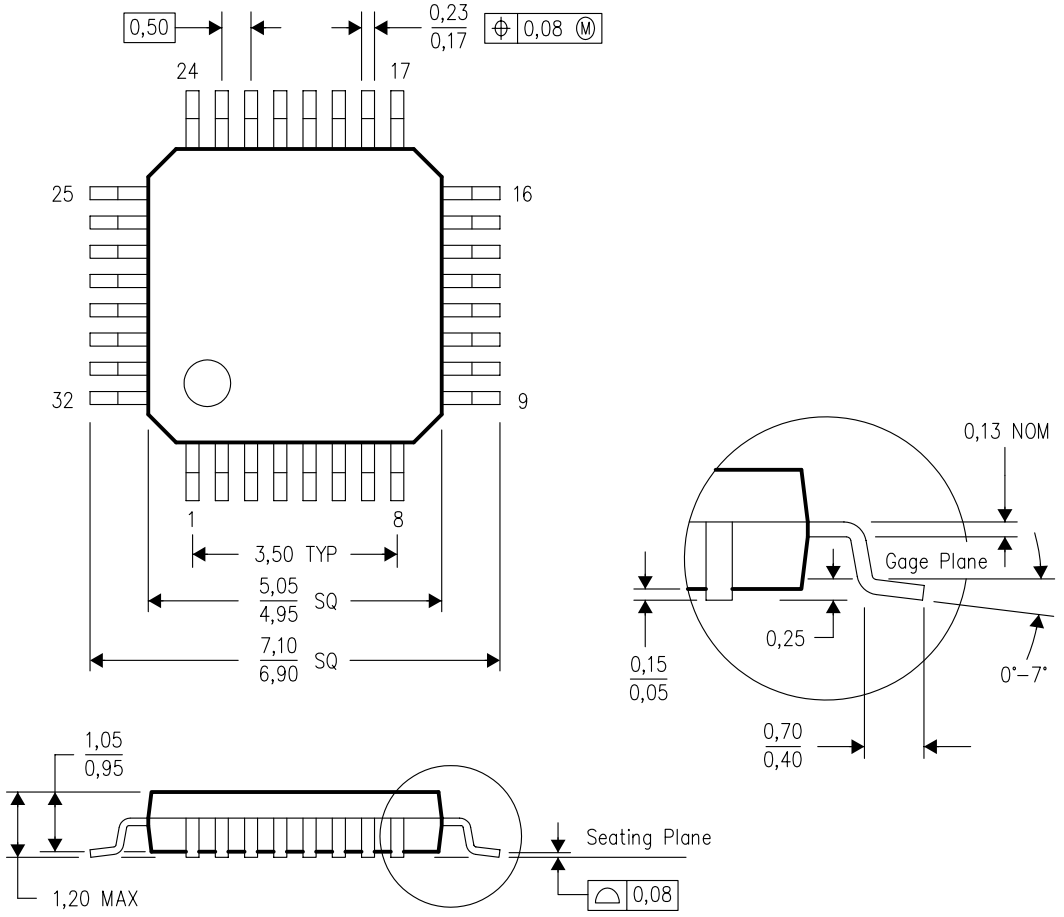


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DAC8742HPBS	PBS	TQFP	32	250	10 X 25	150	315	135.9	7620	12.2	11.1	11.25
DAC8742HPBS.A	PBS	TQFP	32	250	10 X 25	150	315	135.9	7620	12.2	11.1	11.25

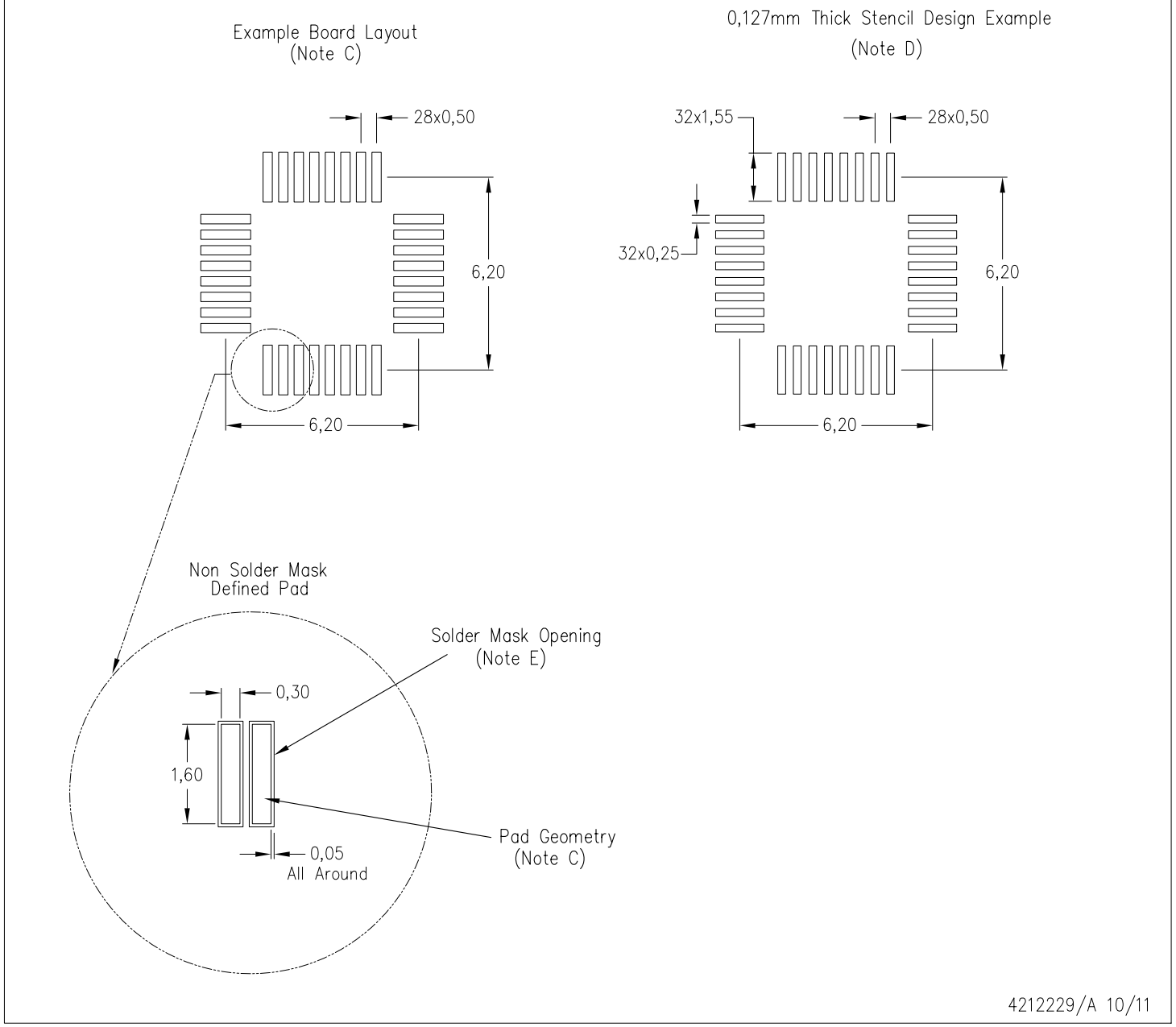
PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK



4087735/B 07/05

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances between and around signal pads.

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