

DCH01 Series, 1W, 3000V_{DC} Isolated, Unregulated DC/DC Converter Modules

1 Features

- 3kVDC Isolation (operational): 1-second test
- Continuous voltage applied across isolation barrier: **60VDC / 42.5VAC**
- UL60950 certified product
- Industry standard footprint
- JEDEC 7-pin SIP package
- Input voltage: 5V ±10%
- Output voltage: ±5V, ±12V, or ±15V
- Supports series operation for higher output voltage
- Supports parallel operation for higher output power
- Up to 78% efficiency

2 Applications

- [Point-of-use power conversion](#)
- [Ground loop elimination](#)
- [Data acquisition](#)
- [Industrial control and instrumentation](#)
- [Test equipment](#)

3 Description

The DCH010505, DCH010512, and DCH010515 devices are a family of miniature, 1W, 3kV isolated DC/DC converters. Featured in an industry standard 7-pin SIP package, the DCH01 series requires minimal external components, reducing board space. The DCH01 series provides both single and dual split-supply outputs.

The use of a highly integrated package design results in highly reliable products with high power densities. High performance and small size makes the DCH01 suitable for a wide range of applications including signal chain applications and ground loop elimination.

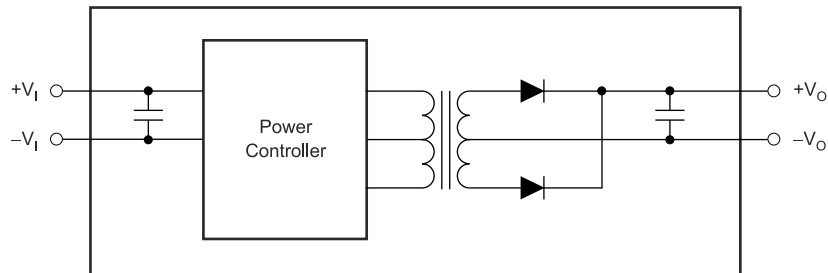
WARNING

This product has operational isolation and is intended for signal isolation only. It must not be used as a part of a safety isolation circuit requiring reinforced isolation. See definitions in [Section 7.3](#).

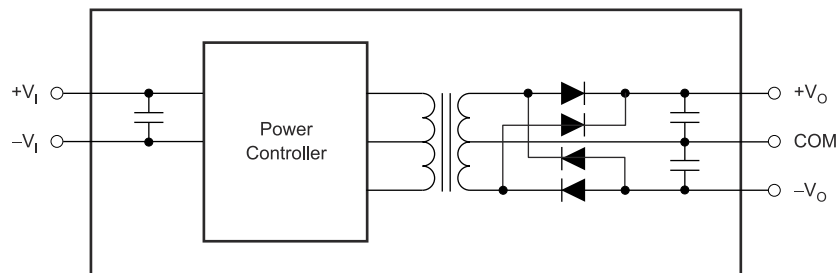
Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
DCH0105xx	EDJ-Single (7)	19.50mm × 10.00mm
	EDJ-Dual (7)	19.50mm × 10.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Single-Output Block Diagram



Dual-Output Block Diagram



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4 Device Comparison Tables

Table 4-1. DCH01 Products

MODEL	INPUT VOLTAGE (V)	OUTPUT VOLTAGE (V)	OUTPUT CURRENT (mA)	OUTPUT POWER (W)	ISOLATION VOLTAGE (kVDC)	PACKAGE-LEAD
DCH010505S	5 ± 10%	5	200	1	3	SIP-7
DCH010512S	5 ± 10%	12	83	1	3	SIP-7
DCH010515S	5 ± 10%	15	67	1	3	SIP-7
DCH010505D	5 ± 10%	±5	±100	1	3	SIP-7
DCH010512D	5 ± 10%	±12	±42	1	3	SIP-7
DCH010515D	5 ± 10%	±15	±33	1	3	SIP-7

Table 4-2. Part Numbering Scheme

PRODUCT LINE	POWER	INPUT VOLTAGE	OUTPUT VOLTAGE	SINGLE/DUAL	PACKAGE	PIN CONFIG	TRANSPORT MEDIA
DCH	01	05	05	S	N	7	
H = 3 kV, unregulated output	01 = 1 W	05 = 5 V	05 = 5 V 12 = 12 V 15 = 15 V	S = Single D = Dual	N = SIP Thru-hole	7 = SIP-7	Blank = Tray

5 Pin Functions and Configuration

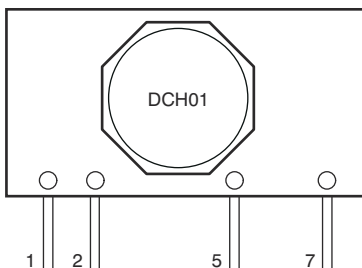


Figure 5-1. EDJ Package 7-Pin SIP (Single) Top View

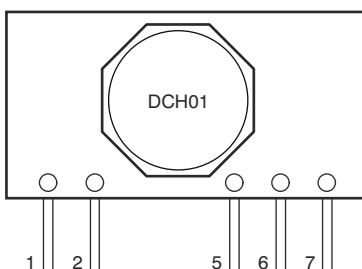


Figure 5-2. EDJ Package 7-Pin SIP (Dual) Top View

Table 5-1. Pin Functions

NAME	PIN		I/O	DESCRIPTION
	EDJ (SINGLE)	EDJ (DUAL)		
$-V_I$	2	2	I	Input side common
$+V_I$	1	1	I	Voltage input
$-V_O$	5	5	O	-Voltage out
$+V_O$	7	7	O	+Voltage out
COM	—	6	—	Output side common

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Input voltage (5-V input models)		7	V
Storage temperature, T _{stg}	-55	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
+V _I Input voltage	4.5	5.5	V
T _A Operating ambient temperature	-40	85	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	DCH01 SERIES		UNIT
	EDJ (SIP-SINGLE)	EDJ (SIP-DUAL)	
	7 PINS	7 PINS	
R _{θJA} Junction-to-ambient thermal resistance	66	66	°C/W
ψ _{JT} Junction-to-top characterization parameter	3	3	°C/W
ψ _{JB} Junction-to-board characterization parameter	66	66	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

At $T_A = 25^\circ\text{C}$ and $V_I = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Input voltage	All devices nominal			5		V
V_{NOM}	Output voltage	100% load ⁽¹⁾	DCH010505S		5.1		V
			DCH010505D		±5.2		
			DCH010512S		12.4		
			DCH010512D		±12.5		
			DCH010515S		15.2		
			DCH010515D		±15.3		
	Load regulation	10% to 100% load ⁽²⁾	DCH010505S		10%		
			DCH010505D		9%		
			DCH010512S		6%		
			DCH010512D		5%		
			DCH010515S		6%		
			DCH010515D		5%		
	Output ripple	100% LOAD ⁽¹⁾	DCH010505S		35		mV _{PP}
			DCH010505D		20		
			DCH010512S		18		
			DCH010512D		19		
			DCH010515S		31		
			DCH010515D		22		
I_Q	Input current	No load; 0% load	DCH010505x		60		mA
			DCH010512x		65		
			DCH010515x		65		
	Efficiency	100% load ⁽¹⁾	DCH010505x		72%		
			DCH010512S		74%		
			DCH010512D		75%		
			DCH010515S		75%		
			DCH010515D		76%		
C_{ISO}	Barrier capacitance	DCH010505x & DCH010515x			3		pF
		DCH010512x			4		
	Output power	100% full load				1 ⁽³⁾	W
		Over current duration ⁽³⁾				1	sec
	Input voltage on V_I			-10%		10%	
	Isolation voltage	100% tested for 1 second			3.5		kVDC
	Line regulation	1% change in V_I			1%		
	Switching frequency (f_{SW})				70		kHz
	Calculated reliability	Per Telcordia SR-332, 50% stress, $T_A = 40^\circ\text{C}$	Single output		18		FITS
			Dual output		22		

(1) 100% load current = $1\text{ W} / V_{\text{NOM}}$ typical.

(2) Load regulation = $(V_O \text{ at } 10\% \text{ load} - V_O \text{ at } 100\% \text{ load}) / V_O \text{ at } 100\% \text{ load}$.

(3) This converter does not have continuous over-current protection.

6.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$ and $V_{IN} = 5\text{ V}$ (unless otherwise noted)

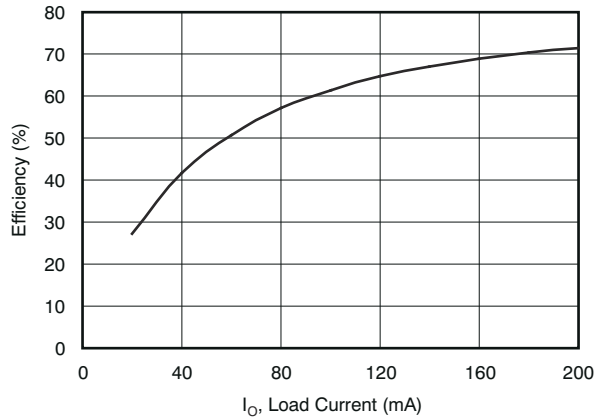


Figure 6-1. DCH010505S Efficiency

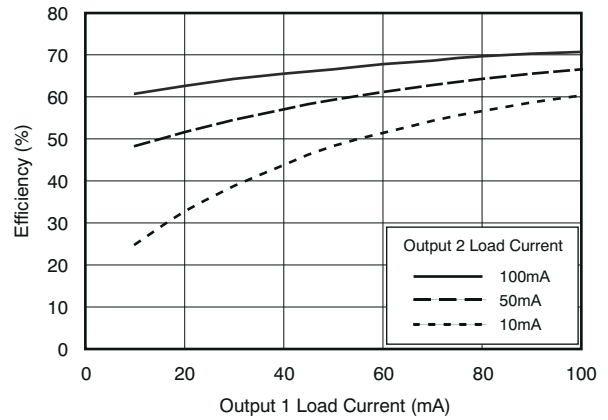


Figure 6-2. DCH010505D Efficiency

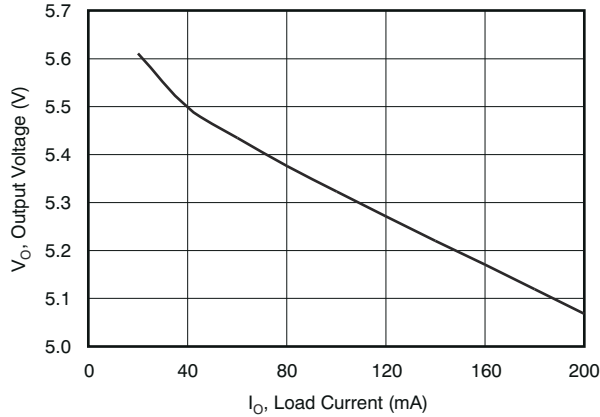


Figure 6-3. DCH010505S Load Regulation

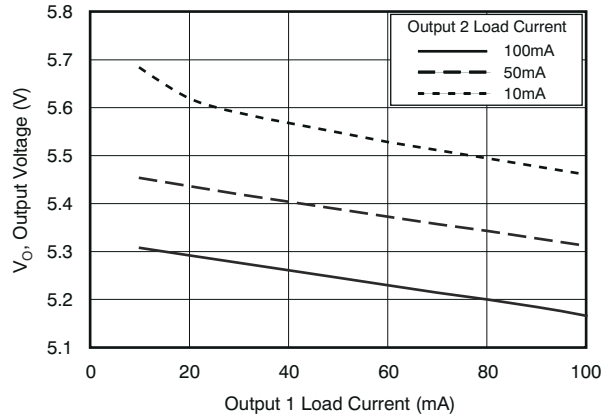


Figure 6-4. DCH010505D Load Regulation

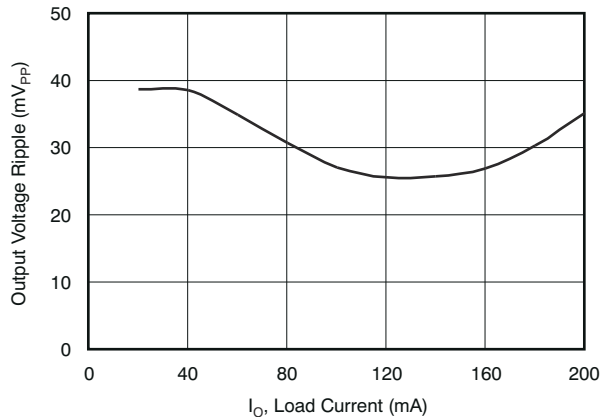


Figure 6-5. DCH010505S Ripple Voltage

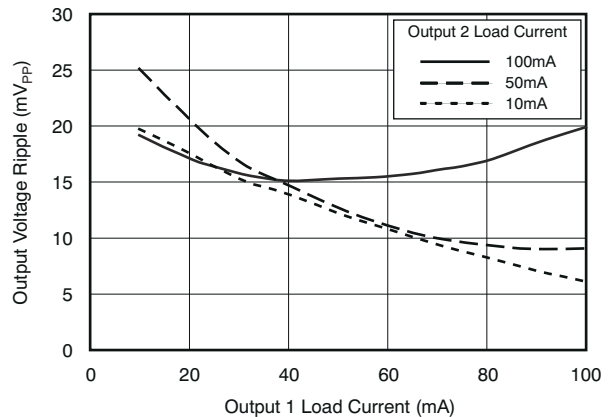


Figure 6-6. DCH010505D Ripple Voltage

6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$ and $V_{IN} = 5\text{ V}$ (unless otherwise noted)

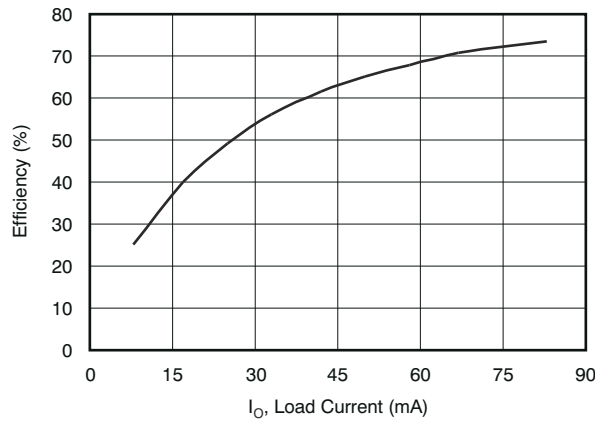


Figure 6-7. DCH010512S Efficiency

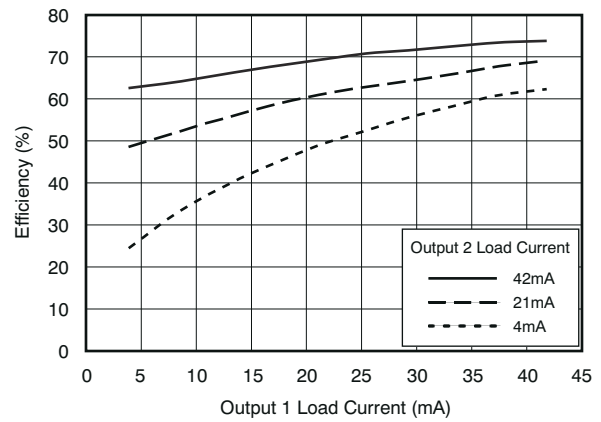


Figure 6-8. DCH010512D Efficiency

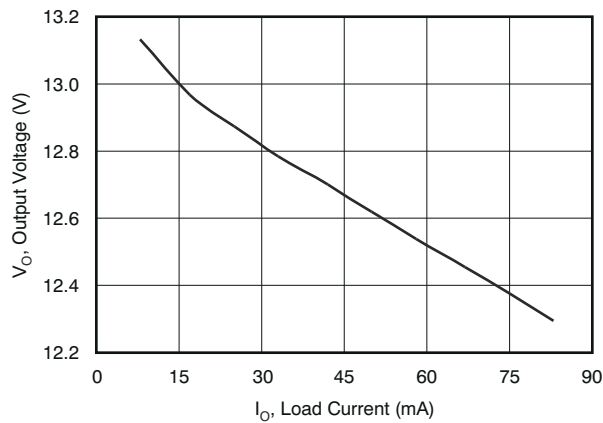


Figure 6-9. DCH010512S Load Regulation

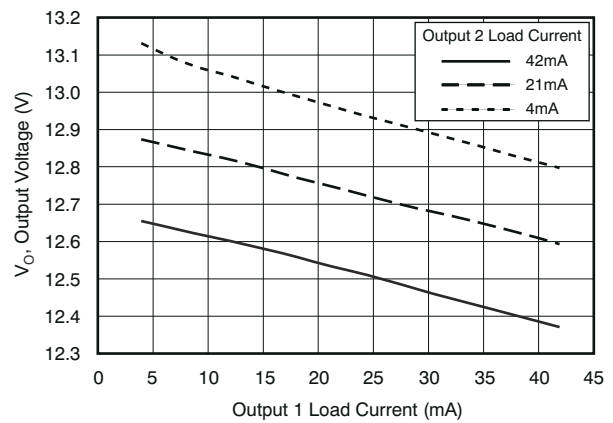


Figure 6-10. DCH010512D Load Regulation

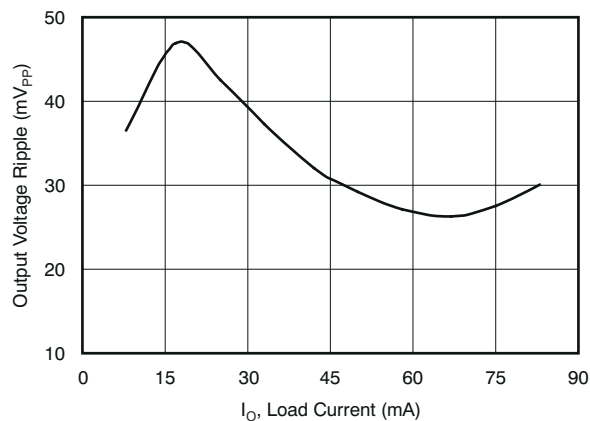


Figure 6-11. DCH010512S Ripple Voltage

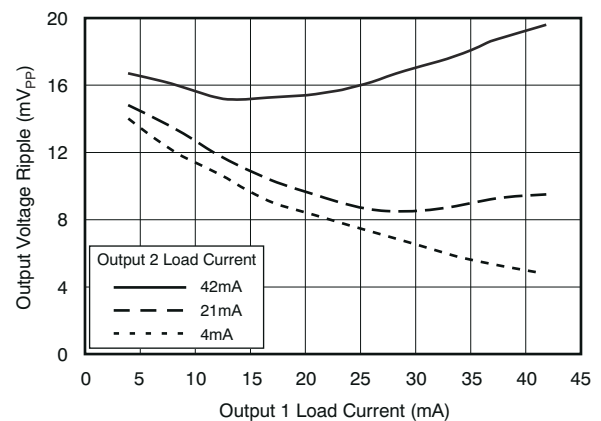


Figure 6-12. DCH010512D Ripple Voltage

6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$ and $V_{IN} = 5\text{ V}$ (unless otherwise noted)

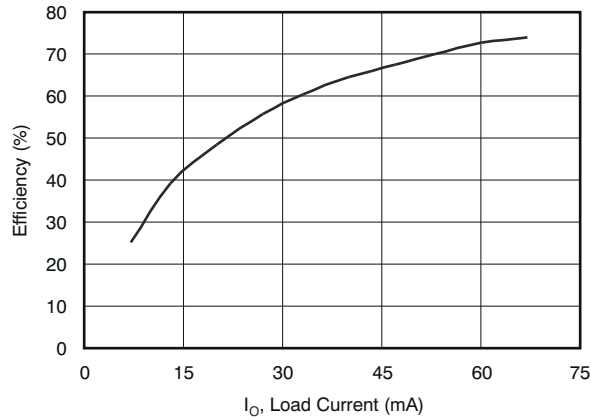


Figure 6-13. DCH010515S Efficiency

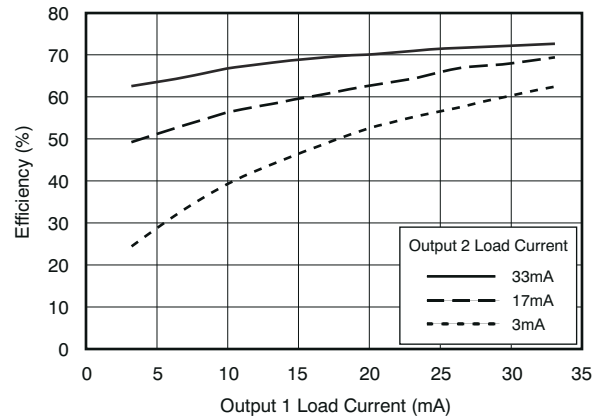


Figure 6-14. DCH010515D Efficiency

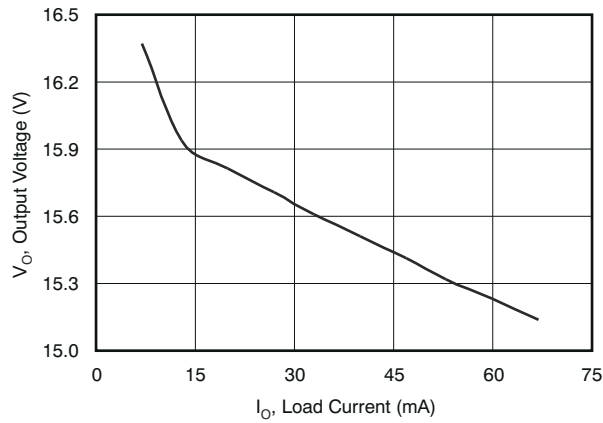


Figure 6-15. DCH010515S Load Regulation

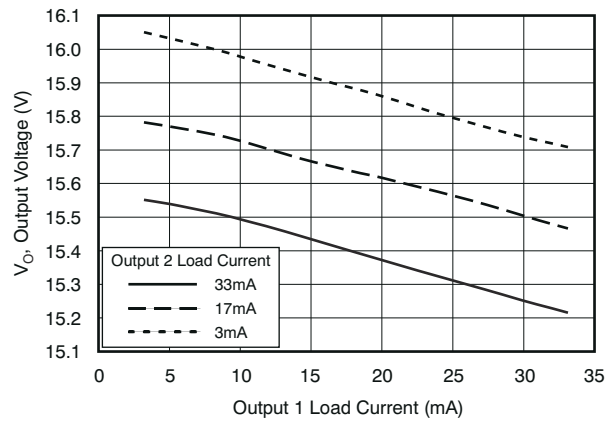


Figure 6-16. DCH010515D Load Regulation

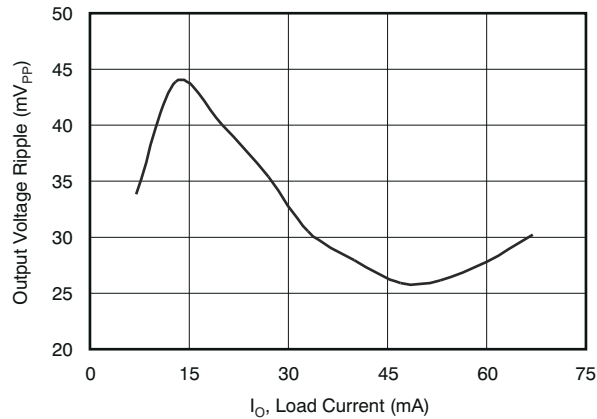


Figure 6-17. DCH010515S Ripple Voltage

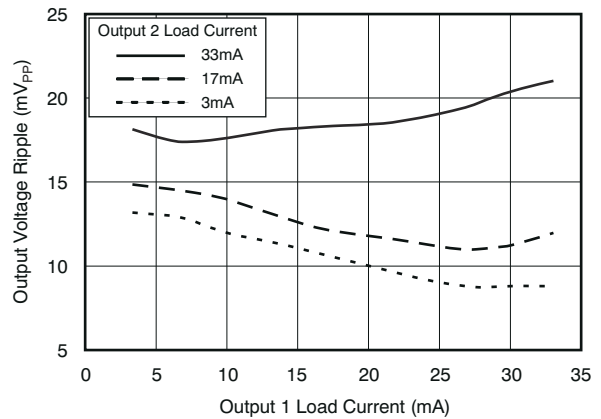


Figure 6-18. DCH010515D Ripple Voltage

6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$ and $V_{IN} = 5\text{ V}$ (unless otherwise noted)

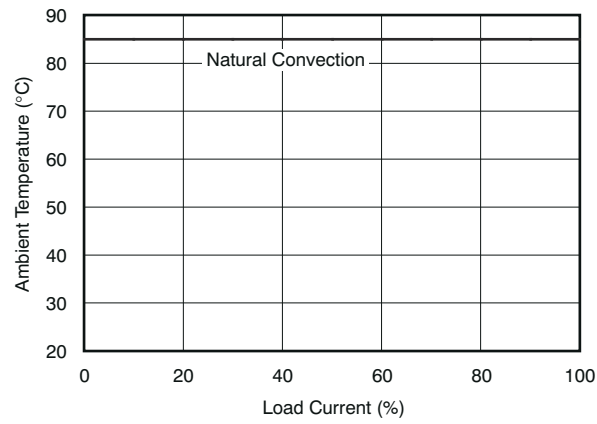


Figure 6-19. Safe Operating Area (All DCH0105 Products)

7 Detailed Description

7.1 Overview

The DCH01 series of DC/DC converters are 100% production tested at 3.5 kVDC for 1 second. The isolation test voltage represents an operational isolation to transient voltages and must not be relied upon for safety isolation.

The continuous voltage that can be applied across the DCH01 during normal operation must be < 60 VDC (within SELV limits).

7.1.1 Repeated High-Voltage Isolation Testing

Repeated high-voltage isolation testing can degrade the isolation capability of the DCH01.

7.2 Functional Block Diagrams

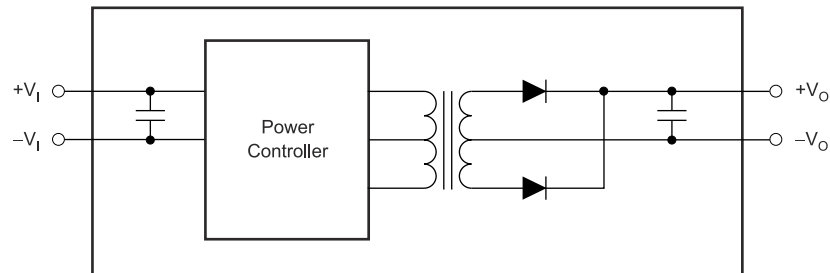


Figure 7-1. Single-Output Block Diagram

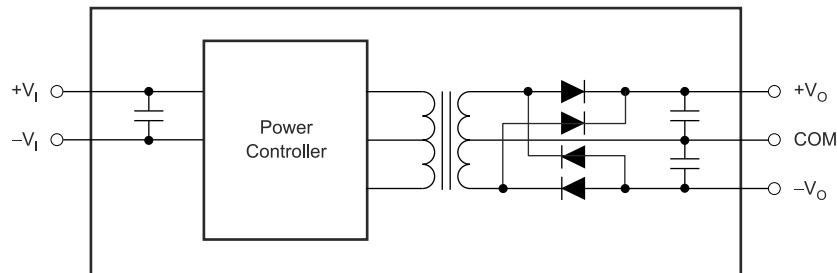


Figure 7-2. Dual-Output Block Diagram

7.3 Feature Description

7.3.1 Isolation

Underwriters Laboratories (UL)[™] defines several classes of isolation that are used in modern power supplies.

Safety extra low voltage (SELV) is defined by UL (UL1950 E199929) as a secondary circuit which is so designated and protected that under normal and single fault conditions the voltage between any two accessible parts, or between an accessible part and the equipment earthing terminal for operational isolation does not exceed steady state 42-V peak or 60 V_{DC} for more than 1 second.

7.3.1.1 Operation or Functional Isolation

Operational or functional isolation is defined by the use of a high-potential (hipot) test only. Typically, this isolation is defined as the use of insulated wire in the construction of the transformer as the primary isolation barrier. The hipot one-second duration test (dielectric voltage, withstand test) is a production test used to verify that the isolation barrier is functioning. Products with operational isolation must never be used as an element in a safety-isolation system.

7.3.1.2 Basic or Enhanced Isolation

Basic or enhanced isolation is defined by specified creepage and clearance limits between the primary and secondary circuits of the power supply. Basic isolation is the use of an isolation barrier in addition to the insulated wire in the construction of the transformer. Input and output circuits must also be physically separated by specified distances.

7.3.1.3 Continuous Voltage

For a device that has no specific safety agency approvals (operational isolation), the continuous voltage that can be applied across the part in normal operation is less than $42.4 V_{RMS}$ or $60 V_{DC}$. Ensure that both input and output voltages maintain normal SELV limits. The isolation test voltage represents a measure of immunity to transient voltages.

WARNING

Do not use the device as an element of a safety isolation system when SELV is exceeded.

If the device is expected to function correctly with more than $42.4 V_{RMS}$ or $60 V_{DC}$ applied continuously across the isolation barrier, then the circuitry on both sides of the barrier must be regarded as operating at an unsafe voltage. Further isolation or insulation systems must form a barrier between these circuits and any user-accessible circuitry according to safety standard requirements.

7.3.1.4 Isolation Voltage

Hipot test, flash-tested, withstand voltage, proof voltage, dielectric withstand voltage, and isolation test voltage are all terms that relate to the same thing: a test voltage applied for a specified time across a component designed to provide electrical isolation to verify the integrity of that isolation. TI's DCH01 series of dc-dc converters are all 100% production tested at $3.5 kV_{DC}$ for 1 second.

7.3.1.5 Repeated High-Voltage Isolation Testing

Repeated high-voltage isolation testing of a barrier component can degrade the isolation capability, depending on materials, construction, and environment. The DCH01 series of dc-dc converters have toroidal, enameled, wire isolation transformers with no additional insulation between the primary and secondary windings. While a device can be expected to withstand several times the stated test voltage, the isolation capability depends on the wire insulation. Any material, including this enamel (typically polyurethane), is susceptible to eventual chemical degradation when subject to very-high applied voltages. Therefore, strictly limit the number of high-voltage tests and repeated high-voltage isolation testing. However, if it is absolutely required, reduce the voltage by 20% from specified test voltage with a duration limit of 1 second per test.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Optional Input and Output Filters

DCH01 power modules include internal input and output ceramic capacitors in all their designs. However, some applications require much lower levels of either input reflected or output ripple or noise. This application note describes various filters and design techniques found to be successful in reducing both input and output ripple or noise.

8.1.1.1 Input and Output Capacitors

The easiest way to reduce output ripple and noise is to add one or more ceramic capacitors each with a value of 4.7- μ F or greater. Ceramic capacitors must be placed close to the output power terminals. A single 4.7- μ F ceramic capacitor reduces the output ripple or noise by 10% to 30%.

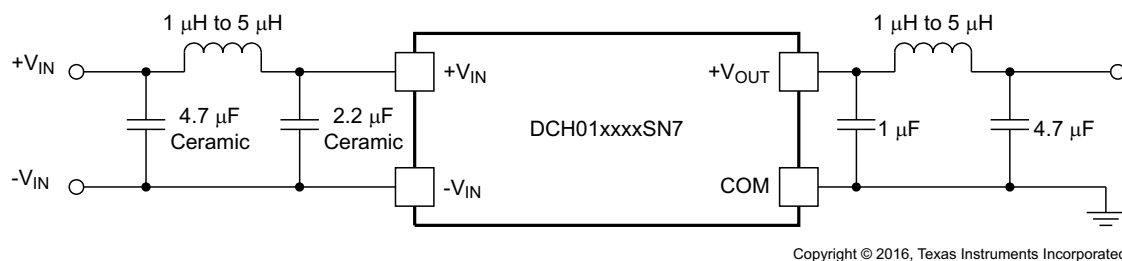
Switching regulators draw current from the input line in pulses at their operating frequency. The amount of reflected (input) ripple or noise generated is directly proportional to the equivalent source impedance of the power source including the impedance of any input lines. The addition of a 4.7- μ F ceramic capacitor, near the input power pins, reduces reflected conducted ripple or noise by 30% to 50%.

The recommended maximum capacitive load on the output of the DCH01 is 100 μ F (non-ceramic).

8.1.1.2 π Filters

If a further reduction in ripple or noise level is required for an application, higher order filters must be used. A π (pi) filter, employing a ferrite bead inductor in series with the input or output terminals of the regulator reduces the ripple or noise by at least 15-20 db (see [Figure 8-1](#) and [Figure 8-2](#)). Ceramic capacitors are required for the inductor to be effective in reduction of ripple and noise.

These inductors plus ceramic capacitors form an excellent filter because of the rejection at the switching frequency. The placement of this filter is critical. It must be located as close as possible to the input or output pins to be effective. The ferrite bead is small (5.1 mm x 3 mm), easy to use, low cost, and has low dc resistance. Fair-Rite manufactures a surface-mount bead (part number 2773019447) or through hole (part number 2673000701) rated to 5 A. Inductors with a value from 1 μ H to 5 μ H can be used in place of the ferrite bead inductor.



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Figure 8-1. DCH01 Series π Filter

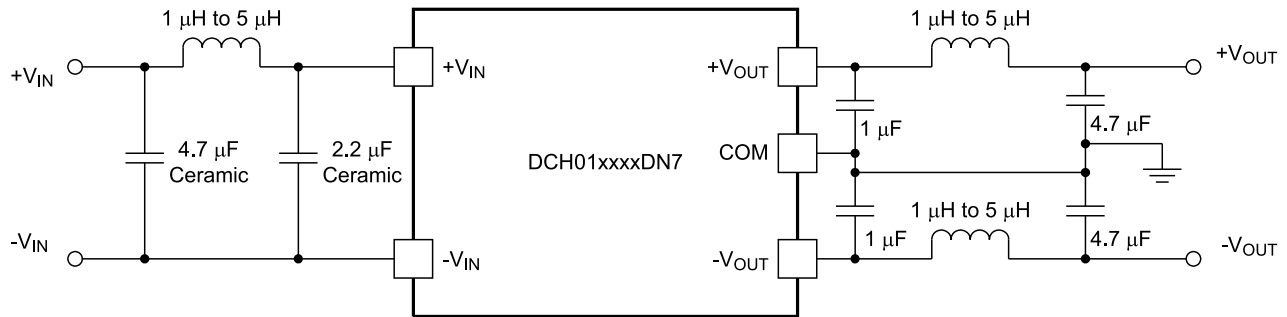


Figure 8-2. DCH01 Series π Filter (5 V at 1 W)

8.1.2 Start-Up

See [Figure 8-3](#) for start-up waveforms.

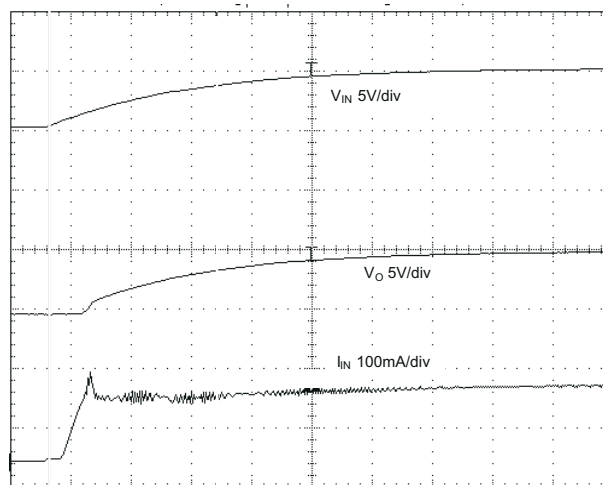
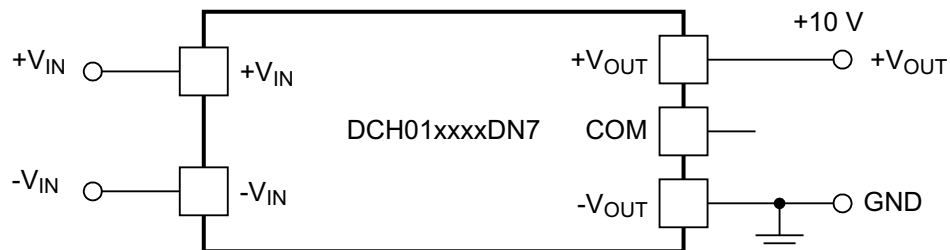


Figure 8-3. StartUp Waveforms

8.1.3 Connecting the DCH01 in Series

It is possible to connect the outputs of multiple DCH01s in series to provide non-standard voltage rails. The outputs of dual output DCH01 versions can also be connected in series to provide $2 \times$ the magnitude of V_O (as shown in [Figure 8-4](#)). For example, a dual 5-V DCH01 could be connected to provide a 10-V rail.



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Figure 8-4. Connecting Dual Outputs in Series

8.1.4 Connecting the DCH01 in Parallel

If the output power from 1 DCH01 is not sufficient, it is possible to parallel the outputs of multiple DCH01s (as shown in Figure 8-5).

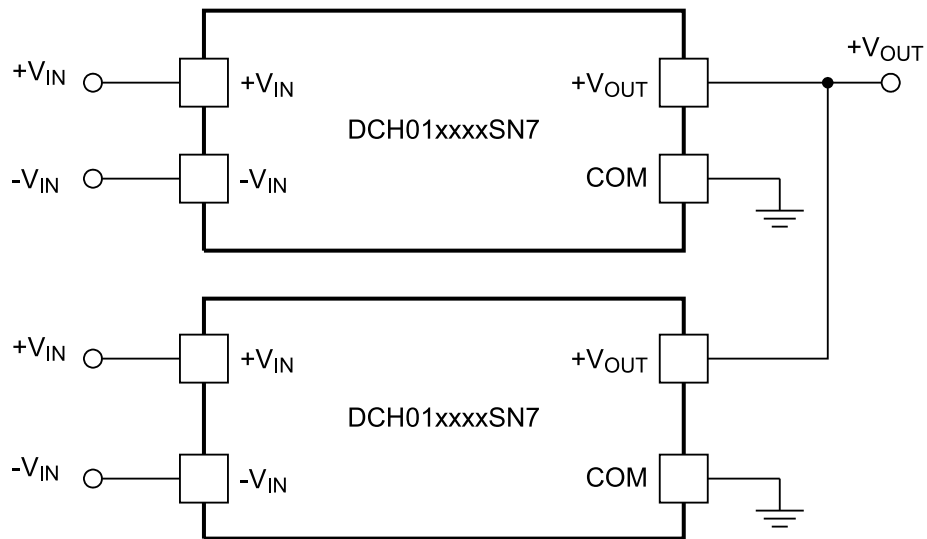


Figure 8-5. Connecting Multiple DCH01s in Parallel

8.2 Typical Application

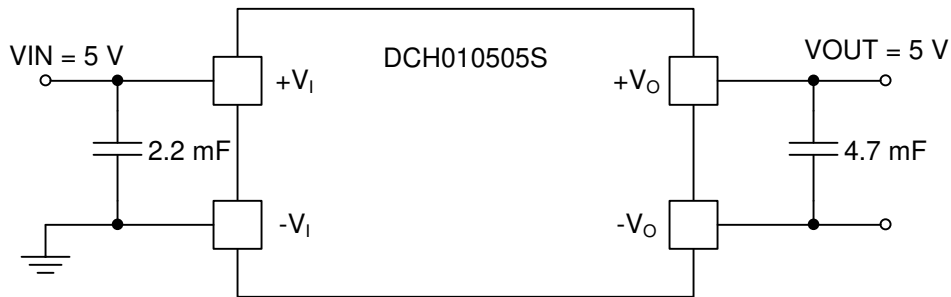


Figure 8-6. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 8-1](#) and follow the procedures in the [Section 8.2.2](#).

Table 8-1. Design Example Parameters

PARAMETER	VALUE
+V _I Input voltage	5 V
+V _O Output voltage	5 V
I _{OUT} Output current rating	200 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Input Capacitor

For any DCH01 design, select a 2.2- μ F, low-ESR, ceramic input capacitor to ensure a good startup performance.

8.2.2.2 Output Capacitor

For any DCH01 design, select a 4.7- μ F, low-ESR, ceramic output capacitor to reduce output ripple.

8.2.3 Application Curves

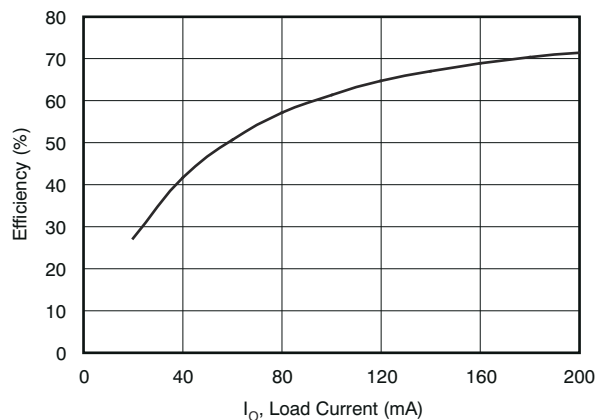


Figure 8-7. DCH010505S Efficiency

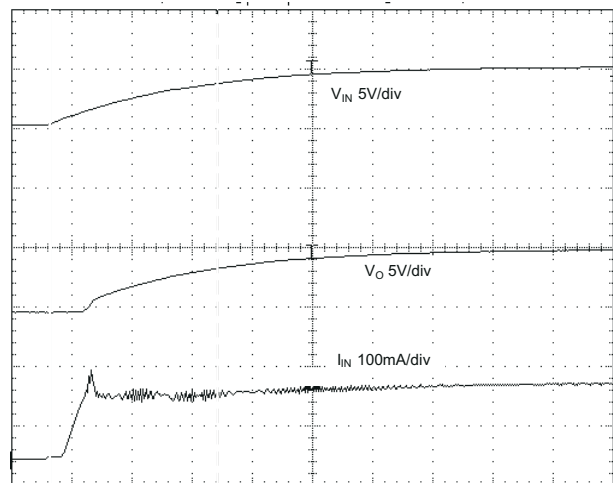


Figure 8-8. DCH010505 Start-up Waveforms

9 Power Supply Recommendations

The DCH01 is a switching power supply, and as such can place high peak current demands on the input supply. To avoid the supply falling momentarily during the fast switching pulses, ground and power planes must be used to connect the power to the input of DCH01. If this connection is not possible, then the supplies must be connected in a star formation with the traces made as wide as possible.

10 Layout

10.1 Layout Guidelines

Carefully consider the layout of the PCB in order for the best results to be obtained.

Input and output power and ground planes provide a low-impedance path for the input and output power. For the output, the positive and negative voltage outputs conduct through wide traces to minimize losses.

A good-quality, low-ESR, ceramic capacitor placed as close as practical across the input reduces reflected ripple and ensure a smooth start-up.

The location of the decoupling capacitors in close proximity to their respective pins ensures low losses due to the effects of stray inductance, thus improving the ripple performance. This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.

10.2 Layout Example

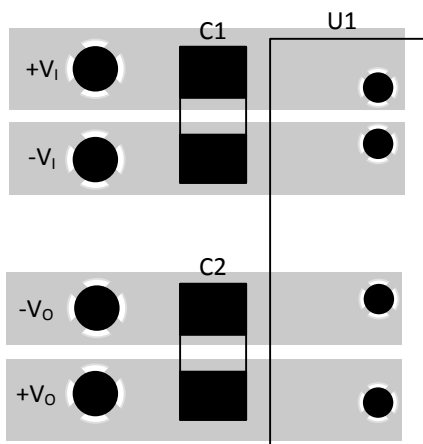


Figure 10-1. DCH01 Single Output Layout (Component-Side View)

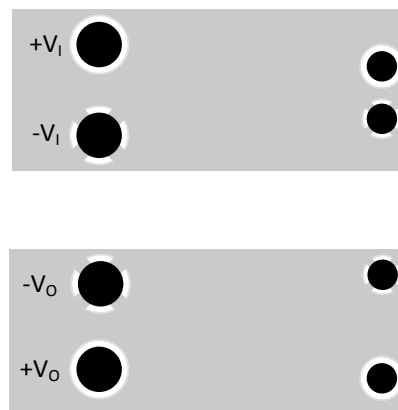


Figure 10-2. DCH01 Single Output Layout (Non-Component-Side View)

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.3 Trademarks

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11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (April 2020) to Revision K (May 2026) Page

- Updated format to match new TI layout and flow. Tables, figures and cross-references use a new numbering sequence throughout the document..... 1

Changes from Revision I (November 2016) to Revision J (April 2020) Page

- Added links to [Section 2](#) 1

Changes from Revision H (January 2009) to Revision I (November 2016) Page

- Added *ESD Ratings* table, *Feature Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section..... 1
- Changed *Ordering Information* to *Device Comparison Tables* 3
- Deleted Wave soldering temperature (260°C maximum) from *Absolute Maximum Ratings* table..... 5
- Added *Thermal Information* table..... 5
- Added *Isolation* subsection to the *Feature Description* 11

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DCH010505DN7	Active	Production	SIP MODULE (EDJ) 5	70 TIW TRAY	Exempt	Call TI	N/A for Pkg Type	-40 to 85	
DCH010505DN7.B	Active	Production	SIP MODULE (EDJ) 5	70 TIW TRAY	-	Call TI	N/A for Pkg Type	-40 to 85	
DCH010505SN7	Active	Production	SIP MODULE (EDJ) 4	70 TIW TRAY	Exempt	Call TI	N/A for Pkg Type	-40 to 85	
DCH010505SN7.B	Active	Production	SIP MODULE (EDJ) 4	70 TIW TRAY	-	Call TI	N/A for Pkg Type	-40 to 85	
DCH010512DN7	Active	Production	SIP MODULE (EDJ) 5	70 TIW TRAY	Exempt	Call TI	N/A for Pkg Type	-40 to 85	
DCH010512DN7.B	Active	Production	SIP MODULE (EDJ) 5	70 TIW TRAY	-	Call TI	N/A for Pkg Type	-40 to 85	
DCH010512SN7	Active	Production	SIP MODULE (EDJ) 4	70 TIW TRAY	Exempt	Call TI	N/A for Pkg Type	-40 to 85	
DCH010512SN7.B	Active	Production	SIP MODULE (EDJ) 4	70 TIW TRAY	-	Call TI	N/A for Pkg Type	-40 to 85	
DCH010515DN7	Active	Production	SIP MODULE (EDJ) 5	70 TIW TRAY	In-Work	Call TI	N/A for Pkg Type	-40 to 85	
DCH010515DN7.B	Active	Production	SIP MODULE (EDJ) 5	70 TIW TRAY	-	Call TI	N/A for Pkg Type	-40 to 85	
DCH010515SN7	Active	Production	SIP MODULE (EDJ) 4	70 TIW TRAY	Exempt	Call TI	N/A for Pkg Type	-40 to 85	
DCH010515SN7.B	Active	Production	SIP MODULE (EDJ) 4	70 TIW TRAY	-	Call TI	N/A for Pkg Type	-40 to 85	

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

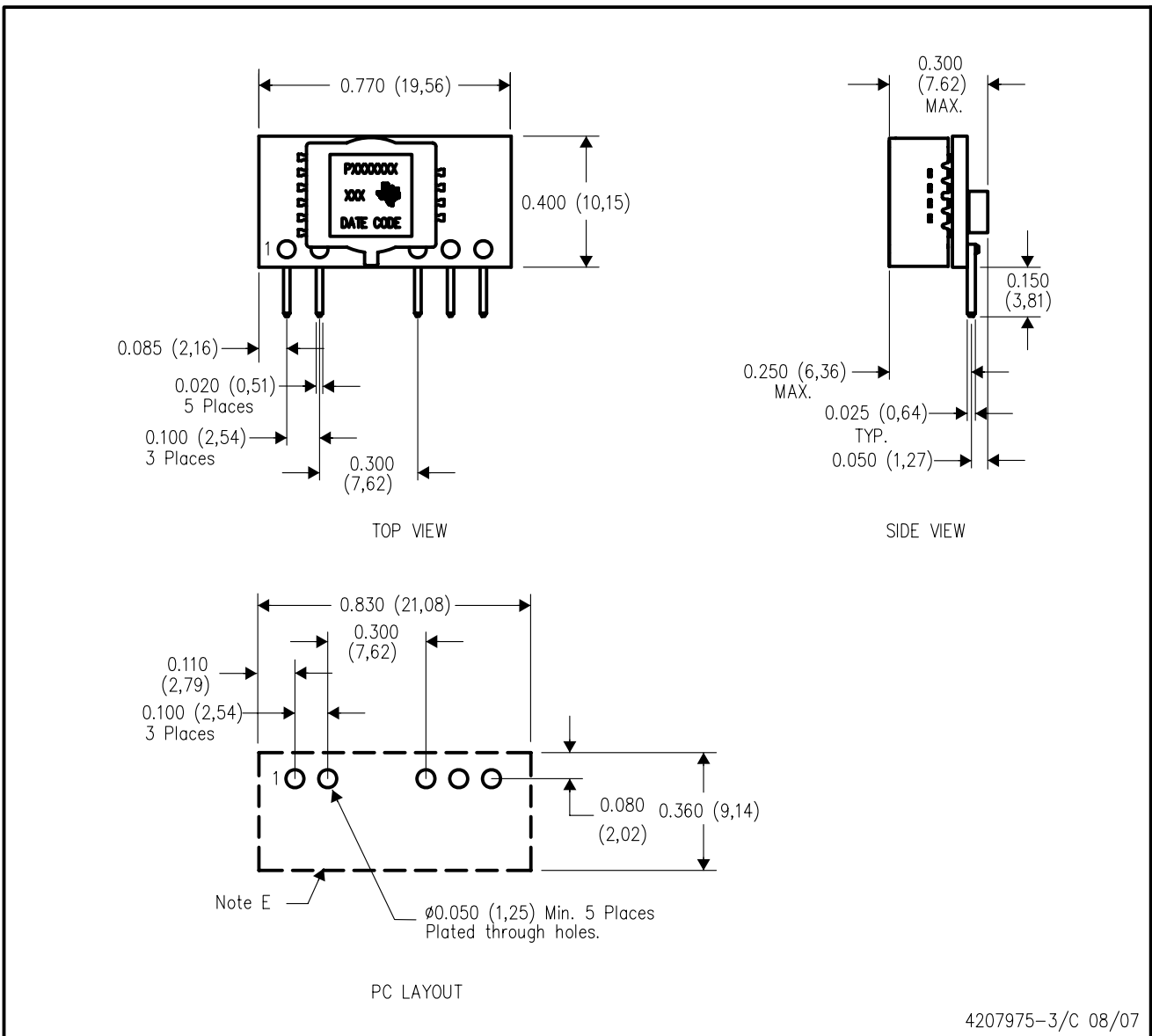
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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EDJ (R-PDSS-T5)

DOUBLE SIDED MODULE

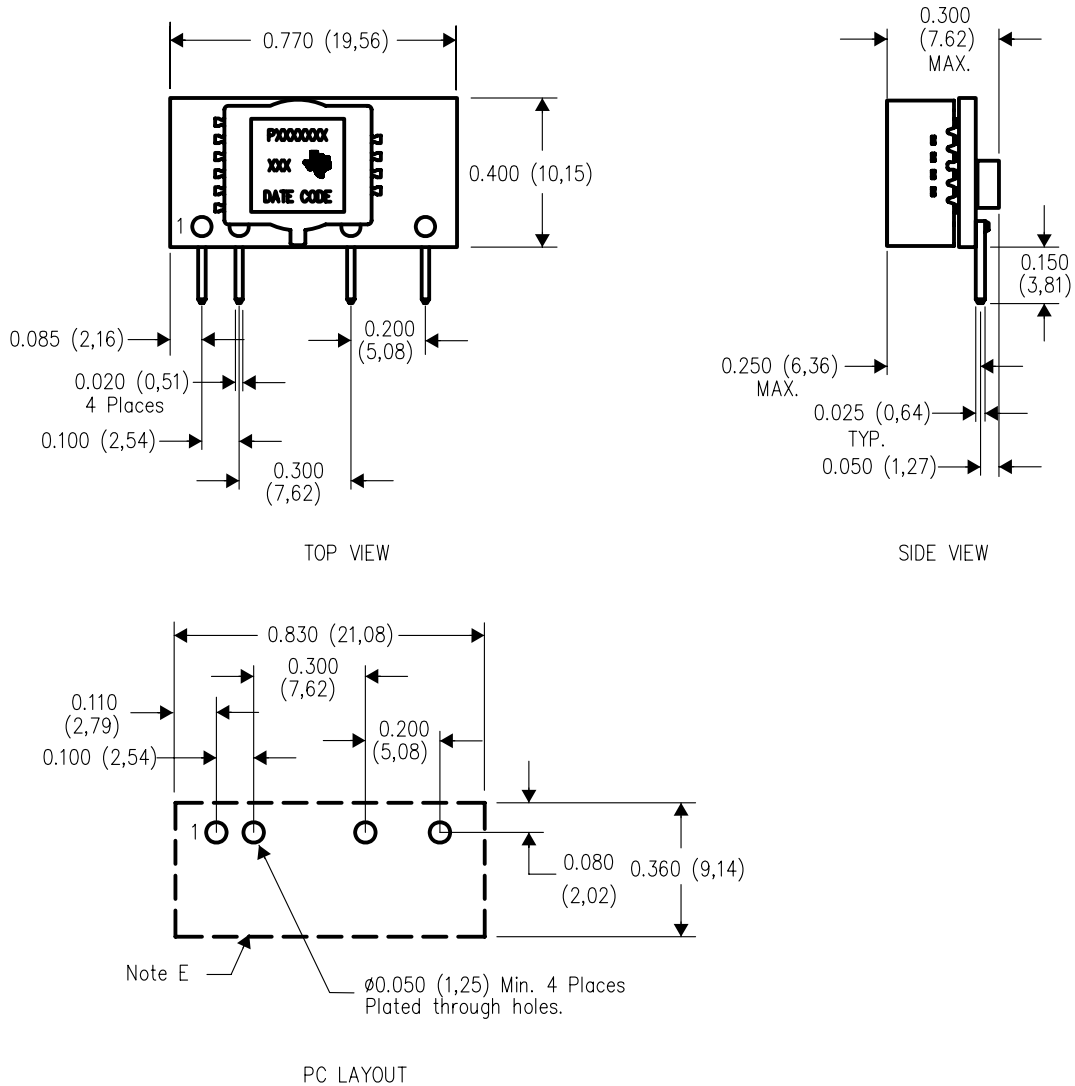


4207975-3/C 08/07

- NOTES:
- A. All linear dimensions are in inches (mm).
 - B. This drawing is subject to change without notice.
 - C. 2 place decimals are ± 0.030 ($\pm 0,76$ mm).
 - D. 3 place decimals are ± 0.010 ($\pm 0,25$ mm).
 - E. Recommended keep out area for user components.
 - F. Pins are 0.020" (0,51) x 0.025" (0,64).
 - G. All pins: Material - Copper Alloy
Finish - Tin (100%) over Nickel plate

EDJ (R-PDSS-T4)

DOUBLE SIDED MODULE



4207975-2/C 08/07

- NOTES:
- A. All linear dimensions are in inches (mm).
 - B. This drawing is subject to change without notice.
 - C. 2 place decimals are ± 0.030 ($\pm 0,76$ mm).
 - D. 3 place decimals are ± 0.010 ($\pm 0,25$ mm).
 - E. Recommended keep out area for user components.
 - F. Pins are 0.020" (0,51) x 0.025" (0,64).
 - G. All pins: Material - Copper Alloy
Finish - Tin (100%) over Nickel plate

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