# DRV2605L-Q1 用于 LRA 和 ERM 的 汽车触觉驱动器，具有效果库和智能环路架构

## 1 特性

- 符合汽车类应用的 标准
- 具有符合 AEC-Q100 的下列结果：
  - 器件温度等级 2：-40°C 至 105°C
  - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 1B
  - 器件充电器件模型 (CDM) ESD 分类等级 C6
- 灵活的触觉和振动驱动器
  - LRA（线性谐振致动器）
  - ERM（偏轴转动惯量)
- $I^2C$ 控制的数字回放引擎
  - 波形序列器和触发器
  - 通过 $I^2C$ 实现的实时回放模式
  - $I^2C$ 双模式驱动（开环和闭环）
- 智能环路架构（正在申请专利的控制算法）
  - 自动过驱动和制动
  - 自动谐振跟踪和报告（仅限 LRA）
  - 自动致动器诊断
  - 自动级别校准
  - 支持宽泛的致动器型号
- 许可版与 Immersion TouchSense® 2200 特性：
  - 集成 Immersion 效果库
  - Audio-to-Vibe
- 可在电池放电过程进行驱动补偿
- 宽工作电压范围（2V 至 5.2V）
- 高效的差分开关输出驱动
- 脉宽调制 (PWM) 输入，占空比可控范围为 0% 至 100%
- 硬件触发输入
- 快速启动时间
- 1.8V 兼容、$V_{DD}$ 耐压数字接口

## 2 应用

- 支持触控的信息娱乐
- 替代机械按钮
- 汽车车身控制
- 驾驶员警报

## 3 说明

DRV2605L-Q1 器件是一款一款汽车触觉驱动器，其包含触觉效果库和闭环致动器控制系统，可为 ERM 和 LRA 提供高质量的触觉反馈。此方案有助于提升致动器在加速度稳定性、启动时间和制动时间方面的性能，通过共用的 $I^2C$ 兼容总线或 PWM 输入信号即可触发该方案。

DRV2605L-Q1 器件提供了 Immersion 公司的许可版 TouchSense 2200 软件，其中包含 100 多种许可版效果（6 个 ERM 库和 1 个 LRA 库）和 audio-to-vibe 功能，因此无需设计触觉波形。 特性。

此外，主机处理器可利用实时回放模式绕过库回放引擎并通过 $I^2C$ 从主机直接播放波形。

DRV2605L-Q1 器件内部采用智能环路架构，可轻松实现自动谐振 LRA 驱动，以及优化反馈的 ERM 驱动，从而提供自动过驱动和制动。这种智能环路架构可构建简化的输入波形接口，并且能够提供可靠的电机控制和稳定的电机性能。 DRV2605L-Q1 还可以利用内部生成的 PWM 信号实现开环驱动。 此外，“audio-to-vibe”模式可自动将音频输入信号转换为实际的触控效果。

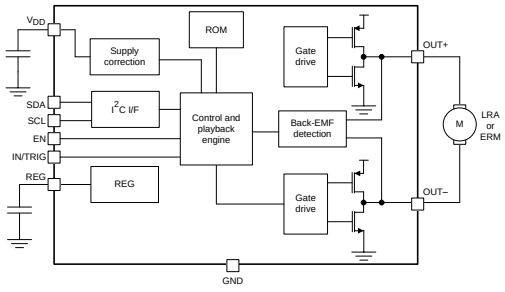
有关 Immersion 软件的重要说明，请参阅 *法律声明* 部分。

**器件信息(1)**

| 器件型号 | 封装 | 封装尺寸（最大值） |
|---|---|---|
| DRV2605L-Q1 | VSSOP (10) | 3.00mm × 3.00mm |

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化原理图




本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from Revision A (October 2015) to Revision B** — **Page**

- Added: 7: TS2200 Library F to Table 7 ... 35

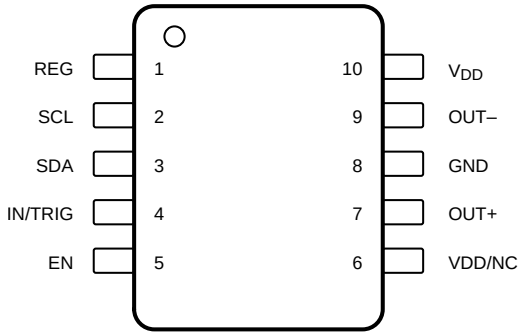
**Changes from Original (October 2015) to Revision A** — **Page**

- 已更改 数据表状态，从“产品预览”更改为“量产数据” ... 1
- Changed minimum supported resonant frequency from 50 Hz to 125 Hz ... 4
- Added digital pulldown resistance parameter to *Electrical Characteristics* ... 5
- Changed calibration diagram to include DRIVE_TIME into ERM requirements ... 25
- Changed bitfield name from "LRA_DRIVE_MODE" to "OTP_STATUS" ... 49


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# 5 Pin Configuration and Functions

**DGS Package**
**10-Pin VSSOP**
**(Top View)**




Not to scale

**Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | REG | O | The REG pin is the 1.8-V regulator output. A 1-µF capacitor required |
| 2 | SCL | I | $I^2C$ clock |
| 3 | SDA | I/O | $I^2C$ data |
| 4 | IN/TRIG | I | Multi-mode Input. $I^2C$ is selectable as PWM, analog, or trigger. If not used, this pin should be connected to GND |
| 5 | EN | I | Device enable |
| 6 | $V_{DD}$/NC | P | Optional supply input. This pin should be tied to $V_{DD}$ or left floating. |
| 7 | OUT+ | O | Positive haptic driver differential output |
| 8 | GND | P | Supply ground |
| 9 | OUT– | O | Negative haptic driver differential output |
| 10 | $V_{DD}$ | P | Supply Input (2 V to 5.2 V). A 1-µF capacitor is required. |

(1) I = input, O = output, I/O = input and output, P = power

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range, $T_A$ = 25°C (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | $V_{DD}$ | –0.3 | 5.5 | V |
| | EN | –0.3 | $V_{DD}$ + 0.3 | V |
| | SDA | –0.3 | $V_{DD}$ + 0.3 | V |
| | SCL | –0.3 | $V_{DD}$ + 0.3 | V |
| | IN/TRIG | –0.3 | $V_{DD}$ + 0.3 | V |
| Operating free-air temperature, $T_A$ | | –40 | 105 | °C |
| Operating junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1) | ±500 | V |
| | | Charged device model (CDM), per AEC Q100-011 | ±1000 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | $V_{DD}$ | 2 | 5.2 | V |
| $f_{(PWM)}$ | PWM input frequency(1) | IN/TRIG Pin | 10 | 250 | kHz |
| $Z_L$ | Load impedance(1) | $V_{DD}$ = 5.2 V | 8 | | Ω |
| $V_{IL}$ | Digital low-level input voltage | EN, IN/TRIG, SDA, SCL | | 0.5 | V |
| $V_{IH}$ | Digital high-level input voltage | EN, IN/TRIG, SDA, SCL | 1.3 | | V |
| $V_{I(ANA)}$ | Input voltage (analog mode) | IN/TRIG | 0 | 1.8 | V |
| $f_{(LRA)}$ | LRA Frequency Range(1) | | 125 | 300 | Hz |

(1) Ensured by design. Not production tested.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | DRV2605L-Q1 DGS (VSSOP) (10-PINS) | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 161.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 38.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 82 | °C/W |
| $\varphi_{JT}$ | Junction-to-top characterization parameter | 1.3 | °C/W |
| $\varphi_{JB}$ | Junction-to-board characterization parameter | 80.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.


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## 6.5 Electrical Characteristics

$V_{DD}$ = 3.6 V over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(REG)}$ | Voltage at the REG pin | | | 1.83 | | V |
| $I_{IL}$ | Digital low-level input current | EN, IN/TRIG, SDA, SCL<br>$V_{DD}$ = 5.2 V , $V_I$ = 0 V | | | 1 | µA |
| $I_{IH}$ | Digital high-level input current | IN/TRIG, SDA, SCL<br>$V_{DD}$ = 5.2 V, $V_I$ = $V_{DD}$ | | | 1 | µA |
| | | EN<br>$V_{DD}$ = 5.2 V, $V_I$ = $V_{DD}$ | | | 3.5 | |
| $V_{OL}$ | Digital low-level output voltage | $SDAI_{OL}$= 4 mA | | | 0.4 | V |
| $I_{(SD)}$ | Shutdown current, $T_A$ = 25°C | $V_{(EN)}$ = 0 V | | 4 | 7 | µA |
| $I_{I(standby)}$ | Standby current, $T_A$ = 25°C | $V_{(EN)}$ = 1.8 V, STANDBY = 1 | | 4.1 | 7 | µA |
| $I_Q$ | Quiescent current | $V_{(EN)}$ = 1.8 V, STANDBY = 0, no signal | | 0.5 | 0.65 | mA |
| $Z_I$ | Input impedance | IN/TRIG to $V_{(CM_ANA)}$ | | 100 | | kΩ |
| $V_{(CM_ANA)}$ | IN/TRIG common-mode voltage (AC-coupled) | AC_COUPLE = 1 | | 0.9 | | V |
| $Z_{O(SD)}$ | Output impedance in shutdown | OUT+ to GND, OUT– to GND | | 15 | | kΩ |
| $Z_{L(th)}$ | Load impedance threshold for over-current detection | OUT+ to GND, OUT– to GND | | 4 | | Ω |
| $I_{(BAT_AV)}$ | Average battery current during operation | Duty cycle = 90%, LRA mode, no load | | 2.4 | 3.5 | mA |
| | | Duty cycle = 90%, ERM mode, no load | | 2.3 | 3.5 | |

## 6.6 Timing Requirements

$T_A$ = 25°C, $V_{DD}$ = 3.6 V (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{(SCL)}$ | Frequency at the SCL pin with no wait states | | | | 400 | kHz |
| $t_{w(H)}$ | Pulse duration, SCL high | See Figure 1. | 0.6 | | | µs |
| $t_{w(L)}$ | Pulse duration, SCL low | | 1.3 | | | µs |
| $t_{su(1)}$ | Setup time, SDA to SCL | | 100 | | | ns |
| $t_{h(1)}$ | Hold time, SCL to SDA | | 10 | | | ns |
| $t_{(BUF)}$ | Bus free time between stop and start condition | See Figure 2. | 1.3 | | | µs |
| $t_{su(2)}$ | Setup time, SCL to start condition | | 0.6 | | | µs |
| $t_{h(2)}$ | Hold time, start condition to SCL | | 0.6 | | | µs |
| $t_{su(3)}$ | Setup time, SCL to stop condition | | 0.6 | | | µs |

## 6.7 Switching Characteristics

$V_{DD}$ = 3.6 V over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(start)}$ | Start-up time | Time from the GO bit or external trigger command to output signal | | 0.7 | | ms |
| | | Time from EN high to output signal (PWM/Analog Modes) | | 1.17 | | |
| $f_{O(PWM)}$ | PWM Output Frequency | | 19.5 | 20.5 | 21.5 | kHz |

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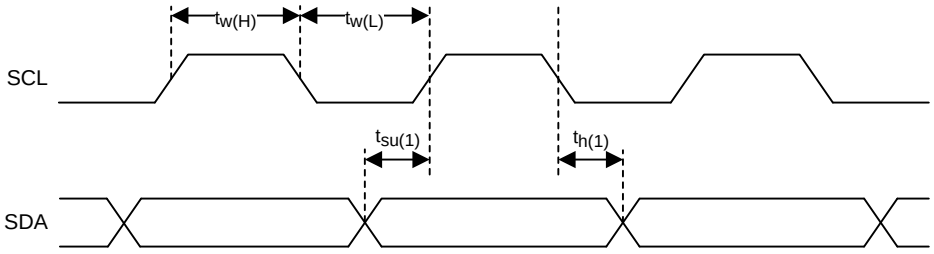



**Figure 1. SCL and SDA Timing**

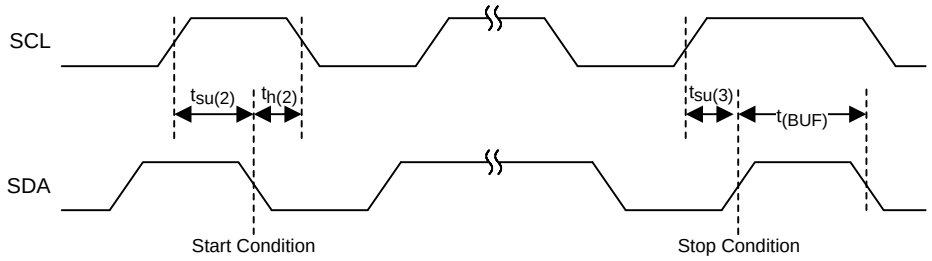
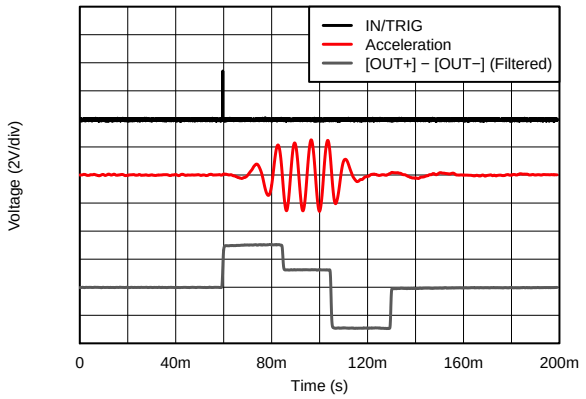



**Figure 2. Timing for Start and Stop Conditions**

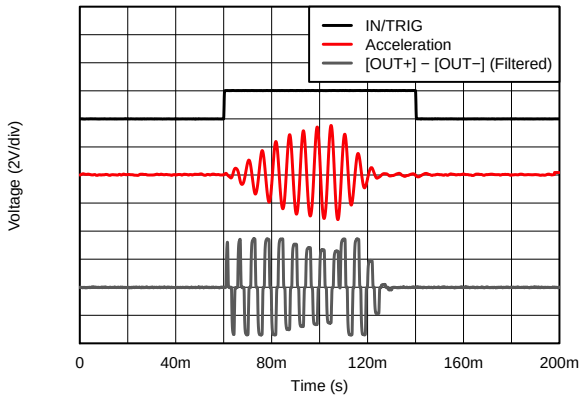

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## 6.8 Typical Characteristics



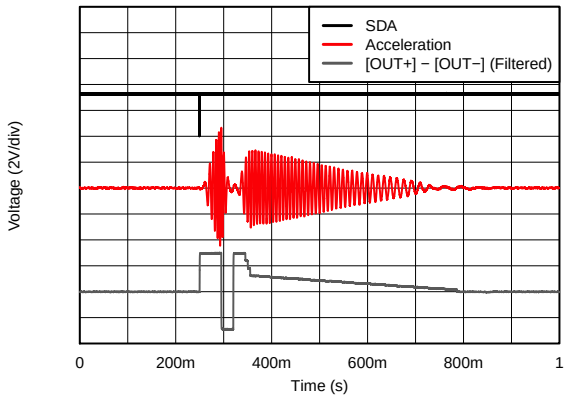

$V_{DD}$ = 3.6 V ERM open loop
Strong click - 60% External edge trigger

**Figure 3. ERM Click with Braking (ROM)**



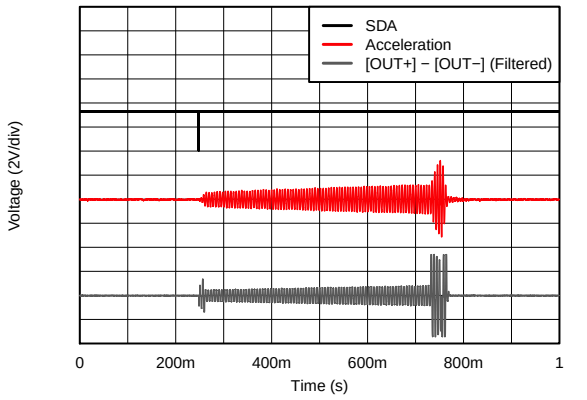

$V_{DD}$ = 3.6 V LRA closed loop
Strong click - 100% External level trigger

**Figure 4. LRA Click with Braking (ROM)**



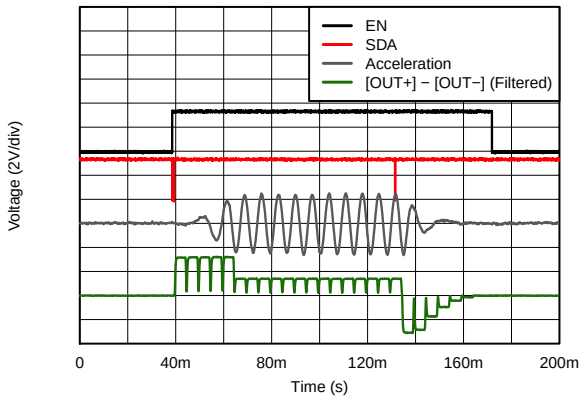

$V_{DD}$ = 3.6 V ERM open loop
Sequence = 0x01, 0x48 Internal trigger

**Figure 5. ERM Click-Bounce (ROM)**



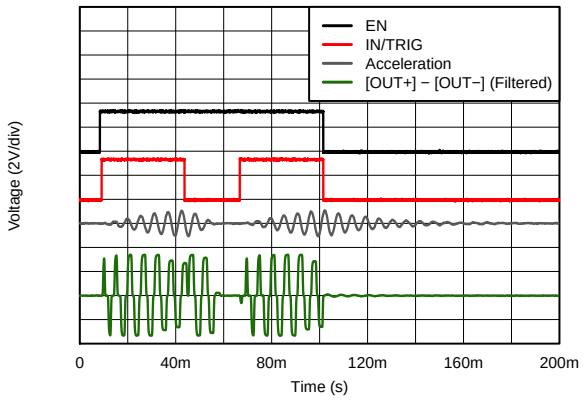

$V_{DD}$ = 3.6 V LRA closed loop
Transition click 1 - 100% Internal trigger

**Figure 6. LRA Transition-Click (ROM)**




$V_{DD}$ = 3.6 V ERM closed loop RTP Mode

**Figure 7. ERM Buzz (RTP)**




$V_{DD}$ = 3.6 V LRA closed loop PWM Mode

**Figure 8. LRA Click With and Without Braking (PWM)**

## Typical Characteristics (continued)

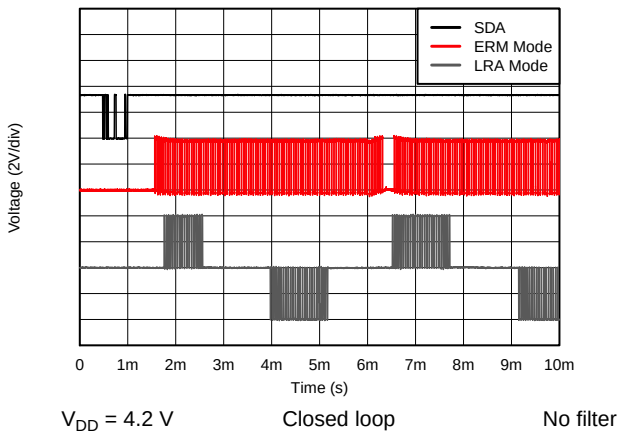



**Figure 9. Startup Latency for ERM and LRA**

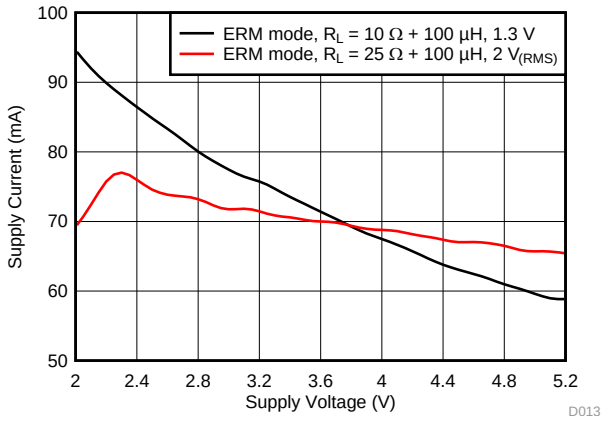



**Figure 10. Supply Current vs Supply Voltage (Full Vibration)**


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# 7 Detailed Description

## 7.1 Overview

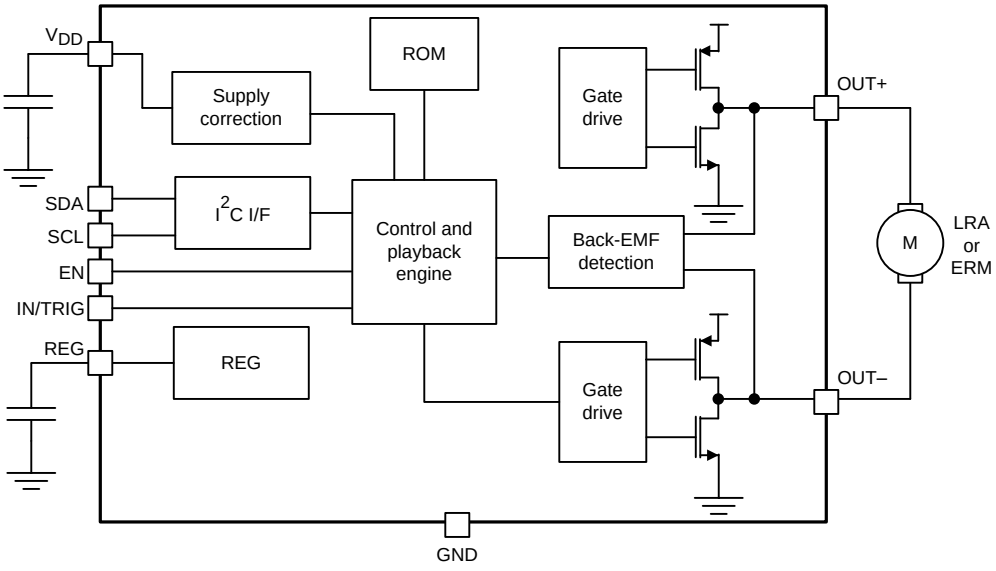
The DRV2605L-Q1 device is a low-voltage haptic driver that relies on the back-EMF produced by an actuator to provide a closed-loop system that offers extremely flexible control of LRA and ERM actuators over a shared $I^2C$-compatible bus or PWM input signal. This schema helps improve actuator performance in terms of acceleration consistency, start time, and brake time.

The improved smart-loop architecture inside the DRV2605L-Q1 device provides effortless auto-resonant drive for LRA, as well as feedback-optimized ERM drive allowing for automatic overdrive and braking. These features create a simplified input waveform paradigm as well as reliable motor control and consistent motor performance. The DRV2605L-Q1 device also features an automatic transition to open-loop operation in the event that an LRA actuator is not generating a valid back-EMF voltage and automatic synchronization with the LRA when the LRA is generating a valid back-EMF voltage. The DRV2605L-Q1 device also allows for open-loop driving by using internally-generated PWM. Additionally, the audio-to-vibe mode automatically converts an audio input signal to meaningful haptic effects.

The DRV2605L-Q1 device offers a licensed version of TouchSense 2200 software from Immersion which eliminates the requirement to design haptic waveforms because the software includes over 100 licensed effects (6 ERM libraries and 1 LRA library) and audio-to-vibe features. The waveforms can be instantly played back through an $I^2C$ or can be triggered through a hardware trigger pin. Additionally, the real-time playback mode allows the host processor to bypass the library playback engine and play waveforms directly from the host through the $I^2C$.

The DRV2605L-Q1 device features a trinary-modulated output stage that provides more efficiency than linear-based output drivers.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Support for ERM and LRA Actuators

The DRV2605L-Q1 device supports both ERM and LRA actuators. The ERM_LRA bit in register 0x1A must be configured to select the type of actuator that the device uses.

### 7.3.2 Smart-Loop Architecture

The smart-loop architecture is an advanced closed-loop system that optimizes the performance of the actuator and allows for failure detection. The architecture consists of automatic resonance tracking and reporting (for an LRA), automatic level calibration, accelerated startup and braking, diagnostics routines, and other proprietary algorithms.

#### *7.3.2.1 Auto-Resonance Engine for LRA*

The DRV2605L-Q1 auto-resonance engine tracks the resonant frequency of an LRA in real time, effectively locking onto the resonance frequency after half of a cycle. If the resonant frequency shifts in the middle of a waveform for any reason, the engine tracks the frequency from cycle to cycle. The auto-resonance engine accomplishes the tracking by constantly monitoring the back-EMF of the actuator. The auto-resonance engine is not affected by the auto calibration process, which is only used for level calibration. No calibration is required for the auto resonance engine. See the *Auto-Resonance Engine Programming for the LRA* section for auto-resonance engine programming information.

#### *7.3.2.2 Real-Time Resonance-Frequency Reporting for LRA*

The smart-loop architecture makes the resonant frequency of the LRA available through $I^2C$ (see the *LRA Resonance Period (Address: 0x22)* section). Because frequency reporting occurs in real time, the frequency must be polled while the DRV2605L-Q1 device synchronizes with the LRA. The data should not be polled when the actuator is idle or braking.

#### *7.3.2.3 Automatic Switch to Open-Loop for LRA*

In the event that an LRA produces a non-valid back-EMF signal, the DRV2605L-Q1 device automatically switches to open-loop operation and continues to deliver energy to the actuator in overdrive mode at a default and configurable frequency. Use Equation 1 to calculate the default frequency. If the LRA begins to produce a valid back-EMF signal, the auto-resonance engine automatically takes control and continues to track the resonant frequency in real time. When synchronized, the mode enjoys all of the benefits that the smart-loop architecture has to offer.

$$f_{(LRA_NO\text{-}BEMF)} \approx \frac{1}{2 \times \left(t_{(DRIVE_TIME[4:0])} - t_{(ZC_DET_TIME[1:0])}\right)} \quad (1)$$

The DRV2605L-Q1 device offers an automatic transition to open-loop mode without the re-synchronization option. The feature is enabled by setting the LRA_AUTO_OPEN_LOOP bit in register 0x1F. The transition to open-loop mode only occurs when the driver fails to synchronize with the LRA. The AUTO_OL_CNT[1:0] bit in register 0x1F can be adjusted to set the amount of non-synchronized cycles allowed before the transition to the open-loop mode. Use Equation 2 to calculate the open-loop frequency. The open-loop mode does not receive benefits from the smart-loop architecture, such as automatic overdrive and braking.

$$f_{(LRA_OL)} = \frac{1}{OL_LRA_PERIOD[6:0] \times 98.49 \times 10^{-6}} \quad (2)$$

#### *7.3.2.4 Automatic Overdrive and Braking*

A key feature of the DRV2605L-Q1 is the smart-loop architecture which employs actuator feedback control for both ERMs and LRAs. The feedback control desensitizes the input waveform from the motor-response behavior by providing automatic overdrive and automatic braking.


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## Feature Description (continued)

An open-loop haptic system typically drives an overdrive voltage at startup that is higher than the steady-state rated voltage of the actuator to decrease the startup latency of the actuator. Likewise, a braking algorithm must be employed for effective braking. When using an open-loop driver, these behaviors must be contained in the input waveform data. Figure 11 shows how two different ERMs with different startup behaviors (Motor A and Motor B) can both be driven optimally by the smart-loop architecture with a simple input for both motors. The smart-loop architecture works equally well for LRAs with a combination of feedback control and an auto-resonance engine.

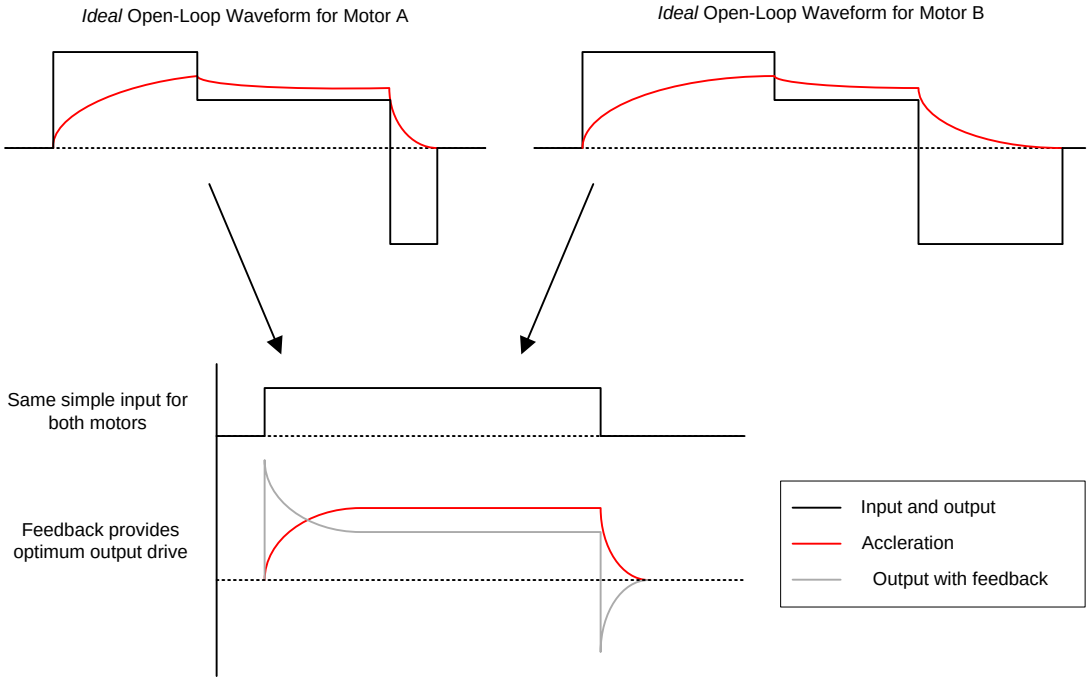



**Figure 11. Waveform Simplification With Smart Loop**

#### 7.3.2.4.1 Startup Boost

To reduce the actuator start-time performance, the DRV2605L-Q1 device has an overdrive boost feature that applies higher loop gain to transient response of the actuator. The STARTUP_BOOST bit enables the feature.

#### 7.3.2.4.2 Brake Factor

To reduce the actuator brake-time performance, the DRV2605L-Q1 device provides a means to increase the gain ratio between braking and driving gain. Higher feedback-gain ratios reduce the brake time, however, the gain ratios also reduce the stability of the closed-loop system. The FB_BRAKE_FACTOR[2:0] bits can be adjusted to set the brake factor.

#### 7.3.2.4.3 Brake Stabilizer

To improve brake stability at high brake-factor gain ratios, the DRV2605L-Q1 device has a brake-stabilizer mechanism that automatically reduces the loop gain when the braking is near completion. The BRAKE_STABILIZER bit enables the feature.

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## Feature Description (continued)

### 7.3.2.5 Automatic Level Calibration

The smart-loop architecture uses actuator feedback by monitoring the back-EMF behavior of the actuator. The level of back-EMF voltage can vary across actuator manufacturers because of the specific actuator construction. Auto calibration compensates for the variation and also performs scaling for the desired actuator according to the specified rated voltage and overdrive clamp-register settings. When auto calibration is performed, a 100% signal level at any of the DRV2605L-Q1 input interfaces supplies the rated voltage to the actuator at steady-state. The feedback allows the output level to increase above the rated voltage level for automatic overdrive and braking, but without allowing the output level to exceed the programmable overdrive clamp voltage.

In the event where the automatic level-calibration routine fails, the DIAG_RESULT bit in register 0x00 is asserted to flag the problem. Calibration failures are typically fixed by adjusting the registers associated with the automatic level-calibration routine or, for LRA actuators, the registers associated with the automatic-resonance detection engine. See the *器件和文档支持* section for automatic-level calibration programming.

#### 7.3.2.5.1 Automatic Compensation for Resistive Losses

The DRV2605L-Q1 device automatically compensates for resistive losses in the driver. During the automatic level-calibration routine, the impedance of the actuator is checked and the compensation factor is determined and stored in the A_CAL_COMP[7:0] bit.

#### 7.3.2.5.2 Automatic Back-EMF Normalization

The DRV2605L-Q1 device automatically compensates for differences in back-EMF magnitude between actuators. The compensation factor is determined during the automatic level-calibration routine and the factor is stored in the A_CAL_BEMF[7:0] bit.

#### 7.3.2.5.3 Calibration Time Adjustment

The duration of the automatic level-calibration routine has an impact on accuracy. The impact is highly dependent on the start-time characteristic of the actuator. The auto-calibration routine expects the actuator to have reached a steady acceleration before the calibration factors are calculated. Because the start-time characteristic can be different for each actuator, the AUTO_CAL_TIME[1:0] bit can change the duration of the automatic level-calibration routine to optimize calibration performance.

#### 7.3.2.5.4 Loop-Gain Control

The DRV2605L-Q1 device allows the user to control how fast the driver attempts to match the back-EMF (and thus motor velocity) and the input signal level. Higher loop-gain (or faster settling) options result in less-stable operation than lower loop gain (or slower settling). The LOOP_GAIN[1:0] bit controls the loop gain.

#### 7.3.2.5.5 Back-EMF Gain Control

The BEMF_GAIN[1:0] bit sets the analog gain for the back-EMF amplifier. The auto-calibration routine automatically populates the bit with the most appropriate value for the actuator.

Modifying the SAMPLE_TIME[1:0] bit also adjusts the back-EMF gain. The higher the sample time, the higher the gain.

By default, the back-EMF is sampled once during a period. In the event that a twice per-period sampling is desired, assert the LRA_DRIVE_MODE bit.

### 7.3.2.6 Actuator Diagnostics

The DRV2605L-Q1 device is capable of determining whether the actuator is not present (open) or shorted. If a fault is detected during the diagnostic process, the DIAG_RESULT bit is asserted.

### 7.3.2.7 Automatic Re-Synchronization

For the LRA, the DRV2605L-Q1 device features an automatic re-synchronization mode which automatically pushes the actuator in the correct direction when a waveform begins playing while the actuator is moving. If the actuator is at rest when the waveform begins, the DRV2605L-Q1 device drives in the default direction.


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## Feature Description (continued)

### 7.3.3 Open-Loop Operation for LRA

In the event that open-loop operation is desired (such as for off-resonance driving) the DRV2605L-Q1 device includes an open-loop LRA drive mode that is available through the PWM input or through the digital interface.

When using the PWM input in open-loop mode, the DRV2605L-Q1 device employs a fixed divider that observes the PWM signal and commutates the output drive signal at the PWM frequency divided by 128. To accomplish LRA drive, the host should drive the PWM frequency at 128 times the desired operating frequency.

When activated, the digital open-loop mode is available for pre-stored waveforms as well as for RTP mode. The OL_LRA_PERIOD bit in register 0x20 programs the operating frequency, which is derived from the PWM output frequency, $f_{O(PWM)}$. Use Equation 1 to calculate the driving frequency. The open-loop mode does not receive the benefits of the smart-loop architecture.

### 7.3.4 Open-Loop Operation for ERM

The DRV2605L-Q1 device offers ERM open-loop operation through the PWM input. The output voltage is based on the duty cycle of the provided PWM signal, where the OD_CLAMP[7:0] bit in register 0x17 sets the full-scale amplitude. For details see the *Rated Voltage Programming* section.

### 7.3.5 Flexible Front-End Interface

The DRV2605L-Q1 device offers multiple ways to launch and control haptic effects. The MODE[2:0] bit in register 0x01 is used to select the interface mode.

#### *7.3.5.1 PWM Interface*

When the DRV2605L-Q1 device is in PWM interface mode, the device accepts PWM data at the IN/TRIG pin. The DRV2605L-Q1 device drives the actuator continuously in PWM interface mode until the user sets the device to standby mode or to enter another interface mode. In standby mode, the strength of vibration is determined by the duty cycle.

For the LRA, the DRV2605L-Q1 device automatically tracks the resonance frequency unless the LRA_OPEN_LOOP bit in register 0x1D is set. If the LRA_OPEN_LOOP bit is set, the LRA is driven according to the frequency of the PWM input signal. Specifically, the driving frequency is the PWM frequency divided by 128.

#### *7.3.5.2 Internal Memory Interface*

The DRV2605L-Q1 device has seven internal-ROM libraries designed by Immersion called TS2200. The first five libraries and the last library are specifically tuned for six categories of ERMs operated in open-loop mode (see Table 1). Library 6 is a closed-loop library tuned for LRAs. The library selection occurs through register 0x03 (see the *(Address: 0x03)* section).

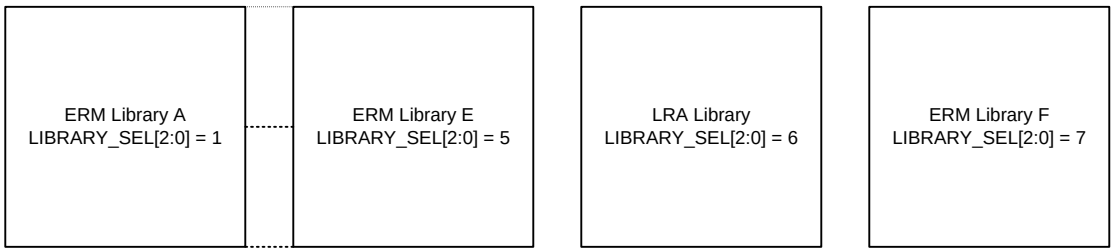



**Figure 12. Library Selection**

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## Feature Description (continued)

**Table 1. ERM Library Table**

| LIBRARY | RATED VOLTAGE | OVERDRIVE VOLTAGE | RISE TIME | BRAKE TIME |
|---|---|---|---|---|
| A | 1.3 V | 3 V | 40 ms to 60 ms | 20 ms to 40 ms |
| B | 3 V | 3 V | 40 ms to 60 ms | 5 ms to 15 ms |
| C | 3 V | 3 V | 60 ms to 80 ms | 10 ms to 20 ms |
| D | 3 V | 3 V | 100 ms to 140 ms | 15 ms to 25 ms |
| E | 3 V | 3 V | > 140 ms | > 30 ms |
| F | 4.5 V | 5 V | 35 ms to 45 ms | 10 ms to 20 ms |

#### 7.3.5.2.1 Waveform Sequencer

The waveform sequencer queues waveform identifiers for playback. Eight sequence registers queue up to eight waveforms for sequential playback. A waveform identifier is an integer value referring to the index position of a waveform in the ROM library. Playback begins at register address 0x04 when the user asserts the GO bit (register 0x0C). When playback of that waveform ends, the waveform sequencer plays the waveform identifier held in register 0x05 if the next waveform is non-zero. The waveform sequencer continues in this way until it reaches an identifier value of zero or until all eight identifiers are played (register addresses 0x04 through 0x0B), whichever scenario is reached first.

The waveform identifier range is 1 to 127. The MSB of each sequence register can implement a delay between sequence waveforms. When the MSB is high, bits [6:0] indicate the length of the wait time. The wait time for that step then becomes WAV_FRM_SEQ[6:0] × 10 ms.

#### 7.3.5.2.2 Library Parameterization

The ROM waveforms are augmented by the time offset registers (registers 0x0D to 0x10). The augmentation occurs only for the ROM waveforms and not for the other interfaces (such as PWM and RTP). The purpose of the functionality is to add *time stretching* (or time shrinking) to the waveform. This functionality is useful for customizing the entire library of waveforms for a specific actuator rise time and fall time.

The time parameters that can be stretched or shrunk include:

**ODT** Overdrive time

**SPT** Sustain positive time

**SNT** Sustain Negative Time

**BRT** Brake Time

The time values are additive offsets and are 8-bit signed values. The default offset of the time values is 0. Positive values add and negative values subtract from the time value of the effect that is currently played. The most positive value in the waveform is automatically interpreted as the overdrive time, and the most negative value in the waveform is automatically interpreted as the brake time. The time-offset parameters are applied to both voltage-time pairs and linear ramps. For linear ramps, linear interpolation is stretched (or shrunk) over the two operative points for the period (see Equation 3).

$$t + t_{(ofs)} \quad (3)$$

where

- $t_{(ofs)}$ is the time offset

Changing the playback interval can also manipulate the waveforms stored in memory. Each waveform in memory has a granularity of 5 ms. If the user desires greater granularity, a 1-ms playback interval can be obtained by asserting the PLAYBACK_INTERVAL bit in register 0x1F.


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#### 7.3.5.3 Real-Time Playback (RTP) Interface

The real-time playback mode is a simple, single 8-bit register interface that holds an amplitude value. When real-time playback is enabled, the real-time playback register is sent directly to the playback engine. The amplitude value is played until the user sends the device to standby mode or removes the device from RTP mode. The RTP mode operates exactly like the PWM mode except that the user enters a register value over the $I^2C$ rather than a duty cycle through the input pin. Therefore, any API (application-programming interface) designed for use with a PWM generator in the host processor can write the data values over the $I^2C$ rather than writing the data values to the host timer. This ability frees a timer in the host while retaining compatibility with the original software.

For the LRA, the DRV2605L-Q1 device automatically tracks the resonance frequency unless the LRA_OPEN_LOOP bit is set (in register 0x1D). If the LRA_OPEN_LOOP bit is set, the LRA is driven according to the open-loop frequency set in the OL_LRA_PERIOD[6:0] bit in register 0x20.

#### 7.3.5.4 Analog Input Interface

When the DRV2605L-Q1 device is in analog-input interface mode, the device accepts an analog voltage at the IN/TRIG pin. The DRV2605L-Q1 device drives the actuator continuously in analog-input interface mode until the user sets the device to standby mode or to enter another interface mode. The reference voltage in standby mode is 1.8 V. Therefore, the 1.8-V reference voltage is interpreted as a 100% input value. A reference voltage of 0.9 V is interpreted as a 50% input value and a reference voltage of 0 V is interpreted as a 0% input value. The input value in standby mode is analogous to the duty-cycle percentage in PWM mode.

For the LRA, the DRV2605L-Q1 automatically tracks the resonance frequency unless the LRA_OPEN_LOOP bit is set (in register 0x1D). If the LRA_OPEN_LOOP bit is set, the LRA is driven according to the open-loop frequency set in OL_LRA_PERIOD[6:0] bit in register 0x20.

#### 7.3.5.5 Audio-to-Vibe Interface

The DRV2605L-Q1 device features an audio-to-vibe mode that converts an audio input signal into meaningful haptic effects using the Immersion audio-to-vibe technology. Audio-to-Vibe mode adds a vibratory *bass extension* to portable devices which allows users to feel the audio and visual content. Audio-to-Vibe mode is a key feature because it allows for existing applications to include haptic sensations without requiring additional software drivers. Additionally, event-driven audio effects generated within an operating system can be used to automatically provide a product with haptic sensations. See the *Waveform Playback Using Audio-to-Vibe Mode* section for details.

#### 7.3.5.6 Input Trigger Option

The DRV2605L-Q1 device includes continuous haptic modes (such as PWM and RTP mode) as well as triggered modes (such as the internal memory interface). The haptic effects in the continuous haptic modes begin as soon as the device enters the mode and stop when the device goes into standby mode or exits the continuous haptic mode. For the triggered mode, the DRV2605L-Q1 device has a variety of trigger options that are explained in this section.

In the continuous haptic modes, the IN/TRIG pin provides external trigger control of the GO bit, which allows GPIO control to fire ROM waveforms. The external trigger control can provide improved latencies in systems where a significant delay exists between the desired effect time and the time a GO command can be sent over the $I^2C$ interface.

**NOTE**

The triggered effect must already be selected to take advantage of the lower latency. This option works best for accelerating a pre-queued high-priority effect (such as a button press) or for the repeated firing of the same effect (such as scrolling).

##### 7.3.5.6.1 $I^2C$ Trigger

Setting the GO bit (in register 0x0C) launches the waveform. The user can cancel the launching of the waveform by clearing the GO bit.

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#### 7.3.5.6.2 Edge Trigger

A low-to-high transition on the IN/TRIG pin sets the GO bit. The playback sequence indicated in the waveform sequencer plays as normal. The user can cancel the transaction by clearing the GO bit. An additional low-to-high transition while the GO bit is high also cancels the transaction which clears and resets the GO bit. Clearing the trigger pin (high-to-low transition) does nothing, therefore the user can send a short pulse without knowing how long the waveform is. The pulse width should be at least 1 µs to ensure detection.

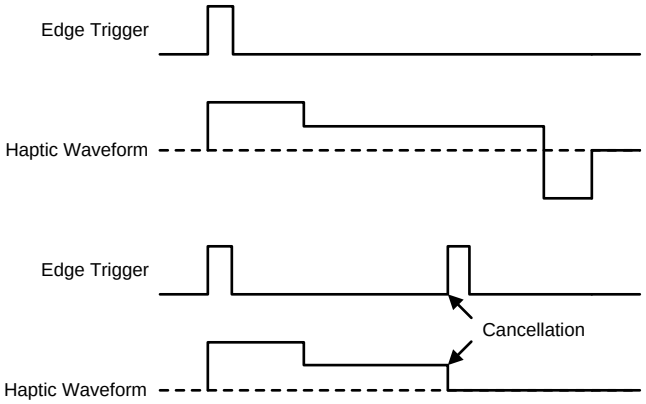



**Figure 13. Edge Trigger Mode**

#### 7.3.5.6.3 Level Trigger

The actions of the GO bit directly follow the IN/TRIG pin. When the IN/TRIG pin is high, the GO bit is high. When the IN/TRIG pin goes low, the GO bit clears. Therefore, a falling edge cancels the transaction. The level trigger can implement a GPIO-controlled buzz on-off controller if an appropriately long waveform is selected. The user must hold the IN/TRIG high for the entire duration of the waveform to complete the effect.

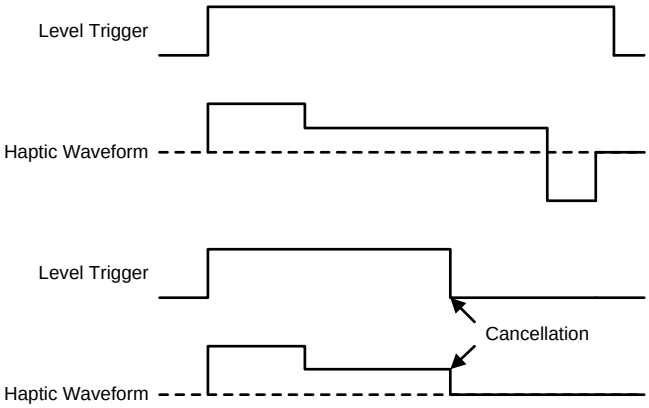



**Figure 14. Level Trigger Mode**

### *7.3.5.7 Noise Gate Control*

When an actuator is driven with an analog or PWM signal, noise in the line can cause the actuator to vibrate unintentionally. For that reason, the DRV2605L-Q1 device features a noise gate that filters out any voltage smaller than a particular threshold. The NG_THRESH[1:0] bit in register 0x1D controls the threshold.

## 7.3.6 Edge Rate Control

The DRV2605L-Q1 output driver implements edge rate control (ERC). The ERC ensures that the rise and fall characteristics of the output drivers do not emit levels of radiation that could interfere with other circuitry common in mobile and portable platforms. Because of ERC most system do not require external output filters, capacitors, or ferrite beads.


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### 7.3.7 Constant Vibration Strength

The DRV2605L-Q1 PWM input uses a digital level-shifter. Therefore, as long as the input voltage meets the $V_{IH}$ and $V_{IL}$ levels, the vibration strength remains the same even if the digital levels vary. The DRV2605L-Q1 device also features power-supply feedback. If the supply voltage drifts over time (because of battery discharge, for example), the vibration strength remains the same as long as enough supply voltage is available to sustain the required output voltage.

### 7.3.8 Battery Voltage Reporting

During playback, the DRV2605L-Q1 device provides real-time voltage measurement of the $V_{DD}$ pin. The VBAT[7:0] bit located in register 0x21 provides this information.

### 7.3.9 Low-Power Standby

Setting the device to standby reduces the idle power consumption without resetting the registers. In Low-Power Standby mode, the DRV2605L-Q1 device features a fast turnon time when it is requested to play a waveform.

### 7.3.10 $I^2C$ Watchdog Timer

If an $I^2C$ stops unexpectedly, the possibility exists for the $I^2C$ protocol to remain in a *hanged* state. To allow for the recovery of the communication without having to power cycle the device, the DRV2605L-Q1 device includes an automatic watchdog timer that resets the $I^2C$ protocol without user intervention after 4.33 ms. This behavior happens in all conditions except in standby mode. If the $I^2C$ stops unexpectedly during standby mode, the only way to recover communication is by power-cycling the device.

### 7.3.11 Device Protection

#### *7.3.11.1 Thermal Protection*

The DRV2605L-Q1 device has thermal protection that causes the device to shut down if it becomes too hot. In the event where the thermal protection kicks in, the DRV2605L-Q1 device asserts a flag (bit OVER_TEMP in register 0x00) to notify the host processor.

#### *7.3.11.2 Overcurrent Protection of the Actuator*

If the impedance at the output pin of the DRV2605L-Q1 device is too low, the device latches the over-current flag (OC_DETECT bit in register 0x00) and shuts down. The device periodically monitors the status of the short and remains in this condition until the short is removed. When the short is removed, the DRV2605L-Q1 device restarts in the default state.

#### *7.3.11.3 Overcurrent Protection of the Regulator*

The DRV2605L-Q1 device has an internal regulator that powers a portion of the system. If a short occurs at the output of the REG pin, an internal overcurrent protection circuit is enabled and limits the current.

During a REG short, the device is not functional. When the short is removed, the DRV2605L-Q1 device automatically resets to default conditions.

#### *7.3.11.4 Brownout Protection*

The DRV2605L-Q1 device has on-chip brownout protection. When activated, a reset signal is issued that returns the DRV2605L-Q1 device to the initial default state. If the regulator voltage $V_{(REG)}$ goes below the brownout protection threshold ($V_{(BOT)}$) the DRV2605L-Q1 device automatically shuts down. When $V_{(REG)}$ returns to the typical output voltage (1.8 V) the DRV2605L-Q1 device returns to the initial device state. The brownout protection threshold ($V_{(BOT)}$) is typically at 0.84 V.

The previously described behavior has one exception. The brownout circuit is designed to tolerate fast brownout conditions as shown by Case 1 in Figure 15. If the $V_{DD}$ ramp-up rate is slower than 3.6 kV/s, then the device can fall into an unknown state. In such a situation, to return to the initial default state the device must be power-cycled with a $V_{DD}$ ramp-up rate that is faster than 3.6 kV/s.

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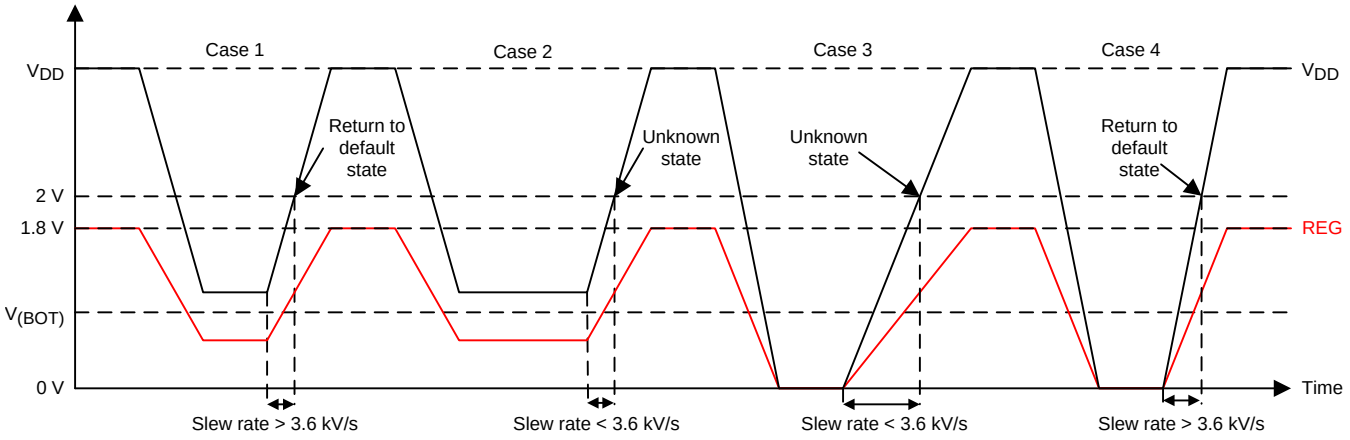



**Figure 15. Brownout Behavior**

## 7.4 Device Functional Modes

### 7.4.1 Power States

The DRV2605L-Q1 device has three different power states which allow for different power-consumption levels and functions. Figure 16 shows the transition in to and out of each state.

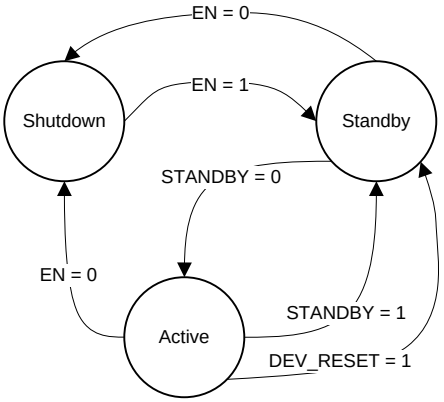



**Figure 16. Power-State Transition Diagram**

#### *7.4.1.1 Operation With $V_{DD}$ < 2 V (Minimum $V_{DD}$)*

Operating the device with a $V_{DD}$ value below 2 V is not recommended.

#### *7.4.1.2 Operation With $V_{DD}$ > 5.5 V (Absolute Maximum $V_{DD}$)*

The DRV2605L-Q1 device is designed to operate at up to 5.2 V, with an absolute maximum voltage of 5.5 V. If exposed to voltages above 5.5 V, the device can suffer permanent damage.

#### *7.4.1.3 Operation With EN Control*

The EN pin of the DRV2605L-Q1 device gates the active operation. When the EN pin is logic high, the DRV2605L-Q1 device is active. When the EN pin is logic low, the device enters the shutdown state, which is the lowest power state of the device. The device registers are not reset. The EN pin operation is particularly useful for constant-source PWM and analog input modes to maintain compatibility with non-$I^2C$ device signaling. The EN pin must be high to write $I^2C$ device registers. However, if the EN pin is low the DRV2605L-Q1 device can still acknowledge (ACK) during an $I^2C$ transaction, however, no read or write is possible. To completely reset the device to the powerup state, set the DEV_RESET bit in register 0x01.


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## Device Functional Modes (continued)

### 7.4.1.4 Operation With STANDBY Control

The STANDBY bit in register 0x01 forces the device in an out of the standby state. The STANDBY bit is asserted by default. When the STANDBY bit is asserted, the DRV2605L-Q1 device goes into a low-power state. In the standby state the device retains register values and the ability to have $I^2C$ communication. The properties of the standby state also feature a fast turn, wake up, and play, on-time. Asserting the STANDBY bit has an immediate effect. For example, if a waveform is played, it immediately stops when the STANDBY bit is asserted.

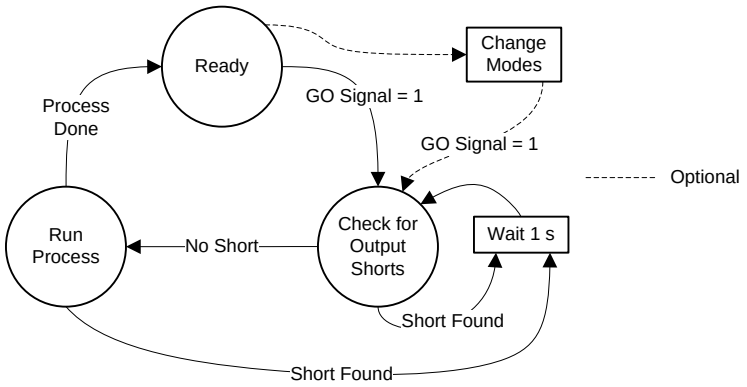
Clear the STANDBY bit to exit the standby state (and go to the ready state).

### 7.4.1.5 Operation With DEV_RESET Control

The DEV_RESET bit in register 0x01 performs the equivalent of power cycling the device. Any playback operations are immediately interrupted, and all registers are reset to the default values. The Dev_Reset bit automatically-clears after the reset operation is complete.

### 7.4.1.6 Operation in the Active State

In the active state, the DRV2605L-Q1 device has $I^2C$ communication and is capable of playing waveforms, running calibration, and running diagnostics. These operations are referred to as *processes*. Figure 17 shows the flow of starting, or *firing*, a process. Notice that the GO signal fires the processes. Note that the GO signal is not the same as the GO bit. Figure 18 shows a diagram of the GO-signal behavior.




Note: If an output short is present before a waveform is played, changing modes (with the MODE[2:0] bit in register 0x01) is required to resume normal playback.

**Figure 17. Diagram of Active States**

### 7.4.2 Changing Modes of Operation

The DRV2605L-Q1 has multiple modes for playing waveforms, as well as a calibration mode and a diagnostic mode. Table 2 lists the available modes.

**Table 2. Mode Selection Table**

| MODE | MODE[2:0] | N_PWM_ANALOG |
|---|---|---|
| Internal trigger mode | 0 | X |
| External Trigger mode (edge) | 1 | X |
| External trigger mode (level) | 2 | X |
| Analog input mode | 3 | 0 |
| PWM mode | 3 | 1 |
| Audio-to-vibe mode | 4 | X |
| RTP mode | 5 | X |
| Diagnostics mode | 6 | X |
| Calibration mode | 7 | X |

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### 7.4.3 Operation of the GO Bit

The GO bit is the primary way to assert the GO signal, which fires processes in the DRV2605L-Q1 device. The primary purpose of the GO bit is to fire the playback of the waveform identifiers in the waveform sequencer (registers 0x04 to 0x0B). However, The GO bit can also fire the calibration or diagnostics processes.

When using the GO bit to play waveforms in internal trigger mode, the GO bit is asserted by writing 0x01 to register 0x0C. In this case, the GO bit can be thought of as a *software trigger* for haptic waveforms. The GO bit remains high until the playback of the haptic waveform sequence is complete. Clearing the GO bit during waveform playback cancels the waveform sequence. The GO bit can also be asserted by the external trigger when in external trigger mode. The GO bit in register 0x0C mirrors the state of the external trigger.

Setting RTP mode , PWM mode, or audio-to-vibe mode also sets the GO bit. However, setting the GO bit in this way has no impact on the GO bit located in register 0x0C.

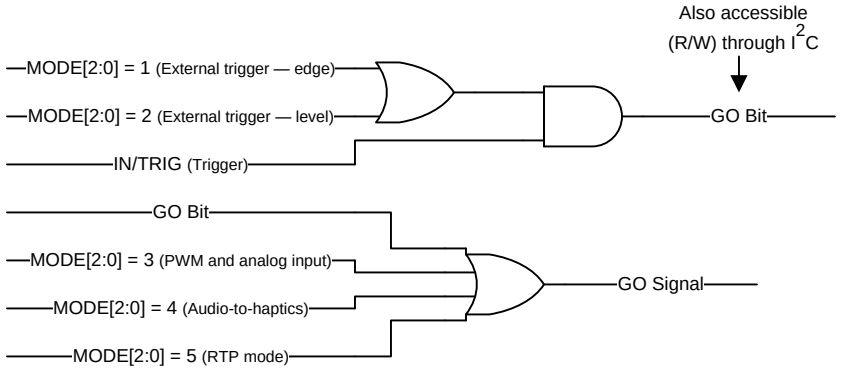



**Figure 18. GO-Signal Logic**

### 7.4.4 Operation During Exceptional Conditions

This section lists different exceptional conditions and the ways that the DRV2605L-Q1 device operates during these conditions. This section also describes how the device goes into and out of these states.

#### *7.4.4.1 Operation With No Actuator Attached*

In LRA closed-loop mode, if a waveform is played without an actuator connected to the OUT+ and OUT– pins, the output pins toggle. However, the toggling frequency is not predictable. In LRA open-loop mode, the output pins toggle at the specified open-loop frequency.

#### *7.4.4.2 Operation With a Non-Moving Actuator Attached*

The model of a non-moving actuator can be simplified as a resistor. If a resistor (with similar loading as an LRA, such as 25 O) is connected across the OUT+ and OUT– pins, and the DRV2605L-Q1 device is in LRA closed-loop mode, the output pins toggle at a default frequency calculated with Equation 1. In LRA open-loop mode the output pins toggle at the specified open-loop frequency.

#### *7.4.4.3 Operation With a Short at REG Pin*

If the REG pin is shorted to GND, the device automatically shuts down and an overcurrent-protection circuit is enabled and clamps the maximum current supplied by the regulator. When the short is removed, the device starts in the default condition.

#### *7.4.4.4 Operation With a Short at OUT+, OUT–, or Both*

If any of the output pins (OUT+ or OUT–) is shorted to $V_{DD}$, GND, or to each other while the device is playing a waveform, the OC_DETECT bit is asserted and remains asserted until the short is removed. A current-protection circuit automatically enables to shutdown the current through the short.

If the driver is playing a waveform the DRV2605L-Q1 device checks for shorts in the output through either a haptic-playback, auto-calibration, or diagnostics process. If the short occurs when the device is idle, the short is not detected until the device attempts to run a waveform.


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## 7.5 Programming

### 7.5.1 Auto-Resonance Engine Programming for the LRA

#### *7.5.1.1 Drive-Time Programming*

The resonance frequency of each LRA actuator varies based on many factors and is generally dominated by mechanical properties. The auto-resonance engine-tracking system is optimized by providing information about the resonance frequency of the actuator. The DRIVE_TIME[4:0] bit is used as an initial guess for the half-period of the LRA. The drive time is automatically and quickly adjusted for optimum drive. For example, if the LRA has a resonance frequency of 200 Hz, then the drive time should be set to 2.5 ms.

For ERM actuators, the DRIVE_TIME[4:0] bit controls the rate for back-EMF sampling. Lower drive times imply higher back-EMF sampling frequencies which cause higher peak-to-average ratios in the output signal, and requires more supply headroom. Higher drive times imply lower back-EMF sampling frequencies which cause the feedback to react at a slower rate.

#### *7.5.1.2 Current-Dissipation Time Programming*

To sense the back-EMF of the actuator, the DRV2605L-Q1 device goes into high impedance mode. However, before the device enters high impedance mode, the device must dissipate the current in the actuator. The DRV2605L-Q1 device controls the time allocated for dissipation-current through the IDISS_TIME[3:0] bit.

#### *7.5.1.3 Blanking Time Programming*

After the current in the actuator dissipates, the DRV2605L-Q1 device waits for a blanking time of the signal to settle before the back-EMF analog-to-digital (AD) conversion converts. The BLANKING_TIME[3:0] bit controls this time.

#### *7.5.1.4 Zero-Crossing Detect-Time Programming*

When the blanking time expires, the back-EMF AD monitors for zero crossings. The ZC_DET_TIME[1:0] bit controls the minimum time allowed for detecting zero crossings.

### 7.5.2 Automatic-Level Calibration Programming

#### *7.5.2.1 Rated Voltage Programming*

The rated voltage is the driving voltage that the driver will output during steady state. However, in closed-loop drive mode, temporarily having an output voltage that is higher than the rated voltage is possible. See the *Overdrive Voltage-Clamp Programming* section for details.

The RATED_VOLTAGE[7:0] bit in register 0x16 sets the rated voltage for the closed-loop drive modes. For the ERM, Equation 4 calculates the average steady-state voltage when a full-scale input signal is provided. For the LRA, Equation 5 calculates the root-mean-square (RMS) voltage when driven to steady state with a full-scale input signal.

$$V_{(ERM\text{-}CL_AV)} = 21.18 \times 10^{-3}\,\text{RATED_VOLTAGE[7:0]} \tag{4}$$

$$V_{(LRA\text{-}CL_RMS)} = \frac{20.58 \times 10^{-3} \times \text{RATED_VOLTAGE[7:0]}}{\sqrt{1 - (4 \times t_{(SAMPLE_TIME)} + 300 \times 10^{-6}) \times f_{(LRA)}}} \tag{5}$$

In open-loop mode, the RATED_VOLTAGE[7:0] bit is ignored. Instead, the OD_CLAMP[7:0] bit (in register 0x17) is used to set the rated voltage for the open-loop drive modes. For the ERM, Equation 6 calculates the rated voltage with a full-scale input signal. For the LRA, Equation 7 calculates the RMS voltage with a full-scale input signal.

$$V_{(ERM\text{-}OL_AV)} = 21.59 \times 10^{-3}\,\text{OD_CLAMP[7:0]} \tag{6}$$

$$V_{(LRA\text{-}OL_RMS)} = 21.32 \times 10^{-3} \times \text{OD_CLAMP[7:0]} \times \sqrt{1 - f_{(LRA)} \times 800 \times 10^{-6}} \tag{7}$$

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## Programming (continued)

The auto-calibration routine uses the RATED_VOLTAGE[7:0] and OD_CLAMP[7:0] bits as inputs and therefore these registers must be written before calibration is performed. Any modification of this register value should be followed by calibration to appropriately set A_CAL_BEMF[7:0].

#### *7.5.2.2 Overdrive Voltage-Clamp Programming*

During closed-loop operation, the actuator feedback allows the output voltage go above the rated voltage during the automatic overdrive and automatic braking periods. The OD_CLAMP[7:0] bit (in Register 0x17) sets a clamp so that the automatic overdrive is bounded. The OD_CLAMP[7:0] bit also serves as the full-scale reference voltage for open-loop operation. The OD_CLAMP[7:0] bit always represents the maximum *peak voltage* that is allowed, regardless of the mode.

**NOTE**

If the supply voltage ($V_{DD}$) is less than the overdrive clamp voltage, the output driver is unable to reach the clamp voltage value because the output voltage cannot exceed the supply voltage. If the rated voltage exceeds the overdrive clamp voltage, the overdrive clamp voltage has priority over the rated voltage.

In ERM mode, use Equation 8 to calculate the allowed maximum voltage. In LRA mode, use Equation 9 to calculate the maximum peak voltage.

$$V_{(ERM_clamp)} = \frac{21.64 \times 10^{-3} \times OD_CLAMP[7:0] \times (t_{(DRIVE_TIME)} - 300 \times 10^{-6})}{t_{(DRIVE_TIME)} + t_{(IDISS_TIME)} + t_{(BLANKING_TIME)}} \quad (8)$$

$$V_{(LRA_clamp)} = 21.22 \times 10^{-3} \times OD_CLAMP[7:0] \quad (9)$$

### 7.5.3 I²C Interface

#### *7.5.3.1 General I²C Operation*

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The bus transfers data serially, one bit at a time. The 8-bit address and data bytes are transferred with the most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on the SDA signal indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. Figure 19 shows a typical sequence. The master device generates the 7-bit slave address and the read-write (R/W) bit to start communication with a slave device. The master device then waits for an acknowledge condition. The slave device holds the SDA signal low during the acknowledge clock period to indicate acknowledgment. When this acknowledgment occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus a R/W bit (1 byte). All compatible devices share the same signals through a bidirectional bus using a wired-AND connection.

The number of bytes that can be transmitted between start and stop conditions is not limited. When the last word transfers, the master generates a stop condition to release the bus. Figure 19 shows a generic data-transfer sequence.

Use external pullup resistors for the SDA and SCL signals to set the logic-high level for the bus. Pullup resistors with values between 660 Ω and 4.7 kΩ are recommended. Do not allow the SDA and SCL voltages to exceed the DRV2605L-Q1 supply voltage, $V_{DD}$.

**NOTE**

The DRV2605L-Q1 slave address is 0x5A (7-bit), or 1011010 in binary.


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## Programming (continued)

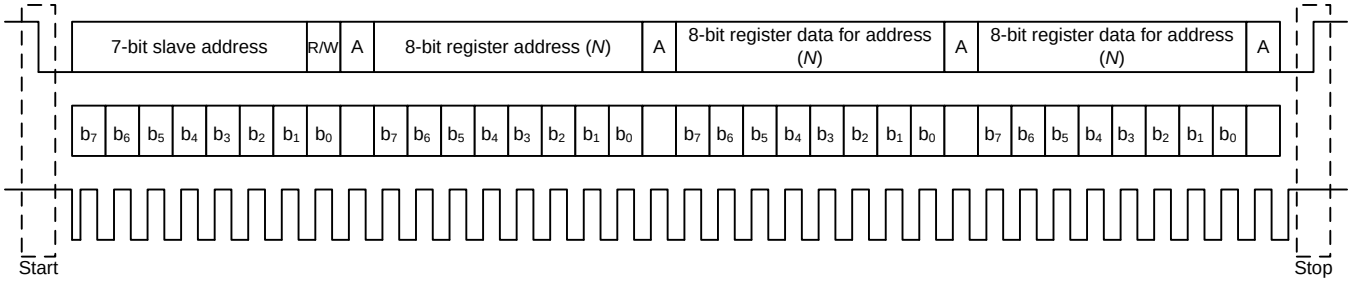



**Figure 19. Typical I²C Sequence**

The DRV2605L-Q1 device operates as an I²C-slave 1.8-V logic thresholds, but can operate up to the $V_{DD}$ voltage. The device address is 0x5A (7-bit), or 1011010 in binary which is equivalent to 0xB4 (8-bit) for writing and 0xB5 (8-bit) for reading.

### *7.5.3.2 Single-Byte and Multiple-Byte Transfers*

The serial control interface supports both single-byte and multiple-byte R/W operations for all registers.

During multiple-byte read operations, the DRV2605L-Q1 device responds with data one byte at a time and beginning at the signed register. The device responds as long as the master device continues to respond with acknowledges.

The DRV2605L-Q1 supports sequential I²C addressing. For write transactions, a sequential I²C write transaction has taken place if a register is issued followed by data for that register as well as the remaining registers that follow. For I²C sequential-write transactions, the register issued then serves as the starting point and the amount of data transmitted subsequently before a stop or start is transmitted determines how many registers are written.

### *7.5.3.3 Single-Byte Write*

As shown in Figure 20, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read-write bit. The read-write bit determines the direction of the data transfer. For a write-data transfer, the read-write bit must be set to 0. After receiving the correct I²C device address and the read-write bit, the DRV2605L-Q1 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the DRV2605L-Q1 internal-memory address that is accessed. After receiving the register byte, the device responds again with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

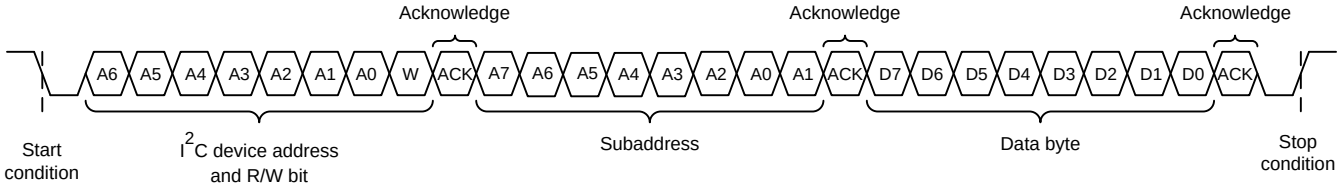



**Figure 20. Single-Byte Write Transfer**

## Programming (continued)

### 7.5.3.4 Multiple-Byte Write and Incremental Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the DRV2605L-Q1 device as shown in Figure 21. After receiving each data byte, the DRV2605L-Q1 device responds with an acknowledge bit.

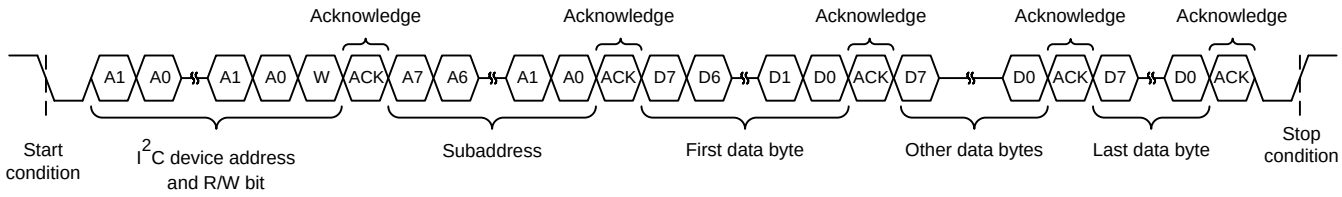



**Figure 21. Multiple-Byte Write Transfer**

### 7.5.3.5 Single-Byte Read

Figure 22 shows that a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read-write bit. For the data-read transfer, both a write followed by a read actually occur. Initially, a write occurs to transfer the address byte of the internal memory address to be read. As a result, the read-write bit is set to 0.

After receiving the DRV2605L-Q1 address and the read-write bit, the DRV2605L-Q1 device responds with an acknowledge bit. The master then sends the internal memory address byte, after which the device issues an acknowledge bit. The master device transmits another start condition followed by the DRV2605L-Q1 address and the read-write bit again. This time, the read-write bit is set to 1, indicating a read transfer. Next, the DRV2605L-Q1 device transmits the data byte from the memory address that is read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer. See the note in the *General I²C Operation* section.

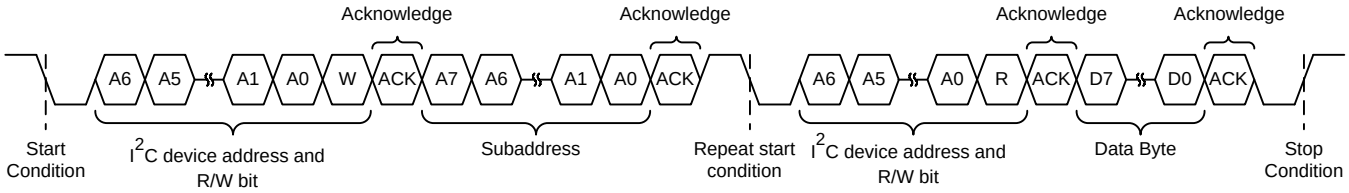



**Figure 22. Single-Byte Read Transfer**

### 7.5.3.6 Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the DRV2605L-Q1 device to the master device as shown in Figure 23. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

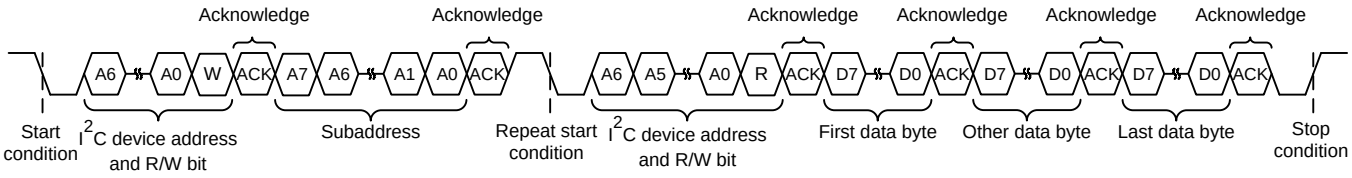



**Figure 23. Multiple-Byte Read Transfer**


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## Programming (continued)

### 7.5.4 Programming for Open-Loop Operation

The DRV2605L-Q1 device can be used in open-loop mode and closed-loop mode. If open-loop operation is desired, the first step is to determine which actuator type is to use, either ERM or LRA.

#### *7.5.4.1 Programming for ERM Open-Loop Operation*

To configure the DRV2605L-Q1 device in ERM open-loop operation, the ERM must be selected by writing the N_ERM_LRA bit to 0 (in register 0x1A), and the ERM_OPEN_LOOP bit to 1 in register 0x1D.

#### *7.5.4.2 Programming for LRA Open-Loop Operation*

To configure the DRV2605L-Q1 device in LRA open-loop operation, the LRA must be selected by writing the N_ERM_LRA bit to 1 in register 0x1A, and the LRA_OPEN_LOOP bit to 1 in register 0x1D. If PWM interface is used, the open-loop frequency is given by the PWM frequency divided by 128. If PWM interface is not used, the open-loop frequency is given by the OL_LRA_PERIOD[6:0] bit in register 0x20.

### 7.5.5 Programming for Closed-Loop Operation

For closed-loop operation, the device must be calibrated according to the actuator selection. When calibrated accordingly, the user is only required to provide the desired waveform. The DRV2605L-Q1 device automatically adjusts the level and, for the LRA, automatically adjusts the driving frequency.

### 7.5.6 Auto Calibration Procedure

The calibration engine requires a number of bits as inputs before the engine can be executed (see Figure 24). When the inputs are configured, the calibration routine can be executed. After calibration execution occurs, the output parameters are written over the specified register locations. Figure 24 shows all of the required inputs and generated outputs. To ensure proper auto-resonance operation, the LRA actuator type requires more input parameters than the ERM. The LRA parameters are ignored when the device is in ERM mode.

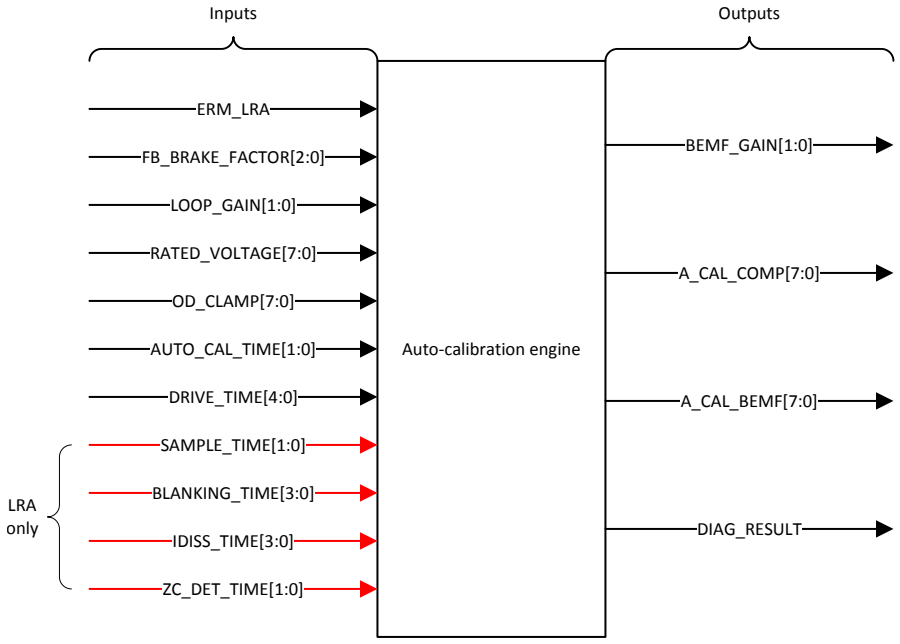



**Figure 24. Calibration-Engine Functional Diagram**

Variation occurs between different actuators even if the actuators are of the same model. To ensure optimal results, TI recommends that the calibration routine be run at least once for each actuator. Having a single set of calibration register values that can be loaded during the system initialization is possible.

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## Programming (continued)

The following instructions list the step-by-step register configuration for auto-calibration. For additional details see the *Register Map* section.

1. Apply the supply voltage to the DRV2605L-Q1 device, and pull the EN pin high. The supply voltage should allow for adequate drive voltage of the selected actuator.
2. Write a value of 0x07 to register 0x01. This value moves the DRV2605L-Q1 device out of STANDBY and places the MODE[2:0] bits in auto-calibration mode.
3. Populate the input parameters required by the auto-calibration engine:
   a. ERM_LRA — selection will depend on desired actuator.
   b. FB_BRAKE_FACTOR[2:0] — A value of 2 is valid for most actuators.
   c. LOOP_GAIN[1:0] — A value of 2 is valid for most actuators.
   d. RATED_VOLTAGE[7:0] — See the *Rated Voltage Programming* section for calculating the correct register value.
   e. OD_CLAMP[7:0] — See the *Overdrive Voltage-Clamp Programming* section for calculating the correct register value.
   f. AUTO_CAL_TIME[1:0] — A value of 3 is valid for most actuators.
   g. DRIVE_TIME[3:0] — See the *Drive-Time Programming* for calculating the correct register value.
   h. SAMPLE_TIME[1:0] — A value of 3 is valid for most actuators.
   i. BLANKING_TIME[3:0] — A value of 1 is valid for most actuators.
   j. IDISS_TIME[3:0] — A value of 1 is valid for most actuators.
   k. ZC_DET_TIME[1:0] — A value of 0 is valid for most actuators.
4. Set the GO bit (write 0x01 to register 0x0C) to start the auto-calibration process. When auto calibration is complete, the GO bit automatically clears. The auto-calibration results are written in the respective registers as shown in Figure 24.
5. Check the status of the DIAG_RESULT bit (in register 0x00) to ensure that the auto-calibration routine is complete without faults.
6. Evaluate system performance with the auto-calibrated settings. Note that the evaluation should occur during the final assembly of the device because the auto-calibration process can affect actuator performance and behavior. If any adjustment is required, the inputs can be modified and this sequence can be repeated. If the performance is satisfactory, the user can do any of the following:
   a. Repeat the calibration process upon subsequent power ups.
   b. Store the auto-calibration results in host processor memory and rewrite them to the DRV2605L-Q1 device upon subsequent power ups. The device retains these settings when in STANDBY mode or when the EN pin is low.


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## Programming (continued)

### 7.5.7 Waveform Playback Programming

#### *7.5.7.1 Data Formats for Waveform Playback*

The DRV2605L-Q1 smart-loop architecture has three modes of operation. Each of the modes can drive either ERM or LRA devices.

1. Open-loop mode
2. Closed-loop mode (unidirectional)
3. Closed-loop mode (bidirectional)

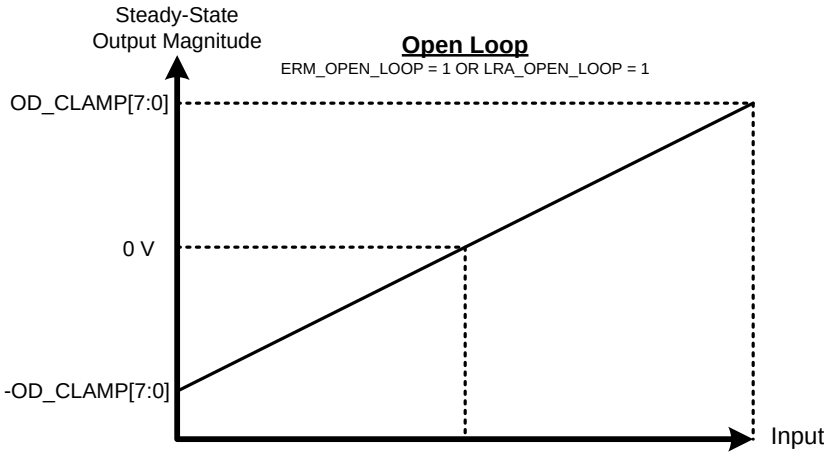
Each mode has different advantages and disadvantages. The DRV2605L-Q1 device brings new cutting-edge actuator control with closed-loop operation around the back-EMF for automatic overdrive and braking. However, some existing haptic implementations already include overdrive and braking that are embedded in the waveform data. Open-loop mode is used to preserve compatibility with such systems.

The following sections show how the input data for each DRV2605L-Q1 interface is translated to the output drive signal.

##### 7.5.7.1.1 Open-Loop Mode

In open-loop mode, the reference level for full-scale drive is set by the OD_CLAMP[7:0] bit in Register 0x17. A mid-scale input value gives no drive signal, and a less-than mid-scale gives a negative drive value. For an ERM, a negative drive value results in counter-rotation, or braking. For an LRA, a negative drive value results in a 180-degree phase shift in commutation.

The RTP mode has 8 bits of resolution over the $I^2C$ bus. The RTP data can either be in a signed (2s complement) or unsigned format as defined by the DATA_FORMAT_RTP bit.




| Input Interface | | | |
|---|---|---|---|
| PWM | 0% | 50% | 100% |
| RTP (8-bit) DATA_FORMAT_RTP = 0 | 0x81 | 0x00 | 0x7F |
| RTP (8-bit) DATA_FORMAT_RTP = 1 | 0x00 | 0x7F | 0xFF |

**Figure 25.**

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## Programming (continued)

#### 7.5.7.1.2 Closed-Loop Mode, Unidirectional

In closed-loop unidirectional mode, the DRV2605L-Q1 device provides automatic overdrive and braking for both ERM and LRA actuators. Closed-loop unidirectional mode is the easiest mode to use and understand. Closed-loop unidirectional mode uses the full 8-bit resolution of the driver. Closed-loop unidirectional mode offers the best performance; however, the data format is not physically compatible with the open-loop mode data that can be used in some existing systems

The reference level for steady-state full-scale drive is set by the RATED_VOLTAGE[7:0] bit (when auto-calibration is performed). The output voltage can momentarily exceed the rated voltage for automatic overdrive and braking, but does not exceed the OD_CLAMP[7:0] voltage. Braking occurs automatically based on the input signal when the back-EMF feedback determines that braking is necessary.

Because the system is unidirectional in closed-loop unidirectional mode, only unsigned data should be used. The RTP mode has 8 bits of resolution over the $I^2C$ bus. Setting the DATA_FORMAT_RTP bit to 0 (signed) is not recommended for closed-loop unidirectional mode.

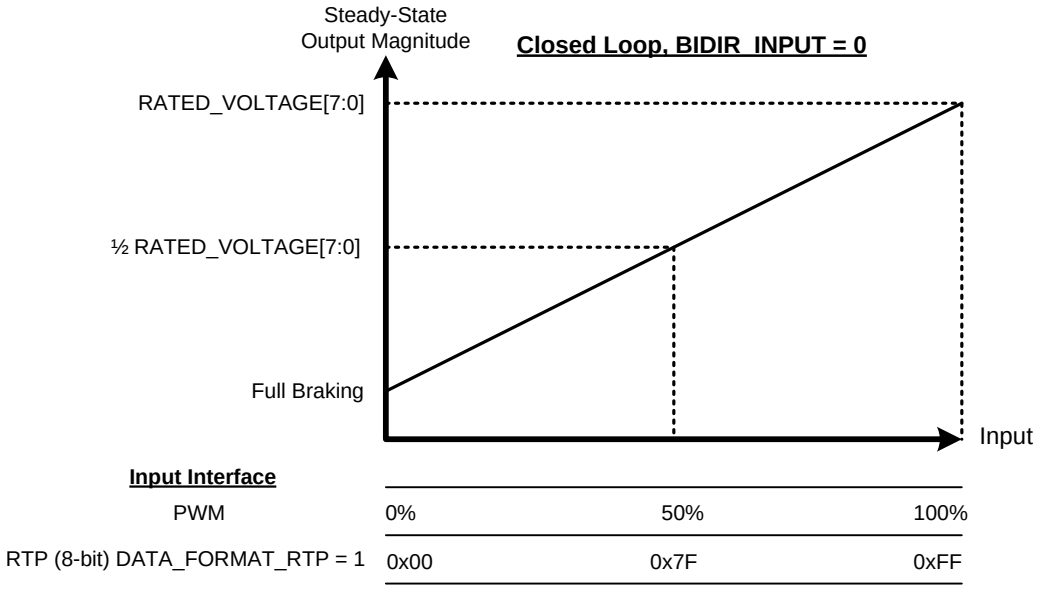



**Figure 26.**

**NOTE**

The TS2200 library data is stored in bidirectional format and cannot be used in unidirectional mode.

For the RTP interface, set the DATA_FORMAT_RTP bit to 1 (unsigned).


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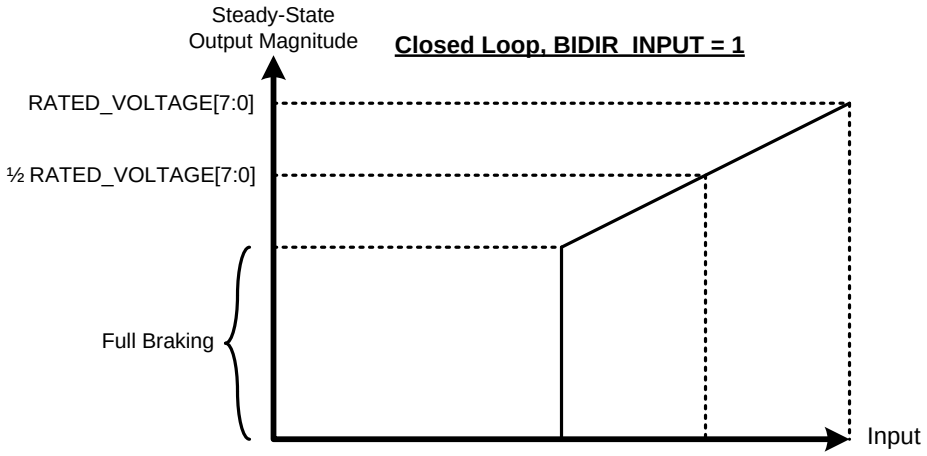
## Programming (continued)

#### 7.5.7.1.3 Closed-Loop Mode, Bidirectional

In closed-loop bidirectional mode, the DRV2605L-Q1 device provides automatic overdrive and braking for both ERM and LRA devices. Closed-loop bidirectional mode preserves compatibility with data created in open-loop signaling by maintaining zero drive-strength at the mid-scale value. When input values less than the mid-scale value are given, the DRV2605L-Q1 device interprets them as the same as the mid-scale with zero drive.

The reference level for steady-state full-scale drive is set by the RATED_VOLTAGE[7:0] bit (when auto calibration is performed). The output voltage can momentarily exceed the rated voltage for automatic overdrive and braking, but does not exceed the OD_CLAMP[7:0] voltage. Braking occurs automatically based on the input signal when the back-EMF feedback determines that braking is necessary. Although the Closed-Loop mode preserves compatibility with existing device data formats, it provides closed loop benefits and is the default configuration at power up.

The RTP mode has 8 bits of resolution over the $I^2C$ bus. The RTP data can either be in signed (2s complement) or unsigned format as defined by the DATA_FORMAT_RTP bit.




| Input Interface | | | | |
|---|---|---|---|---|
| PWM | 0% | 50% | 75% | 100% |
| RTP (8-bit) DATA_FORMAT_RTP = 0 | 0x81 | 0x00 | 0x3F | 0x7F |
| RTP (8-bit) DATA_FORMAT_RTP = 1 | 0x00 | 0x7F | 0xBF | 0xFF |

**Figure 27.**

**NOTE**

Closed-loop bidirectional mode is compatible with all DRV2605L-Q1 interfaces except for TS2200 Library A (with fixed overdrive programming). Library A should only be used in open-loop mode. Libraries B through F (no overdrive) can take advantage of the automatic overdrive and braking of closed-loop bidirectional mode.

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## Programming (continued)

### 7.5.7.2 Waveform Setup and Playback

Playback of a haptic effect can occur in multiple ways. Using the PWM mode, RTP mode, audio-to-vibe mode, and analog-input mode can provide the waveform in real time. The waveforms can also be played from the ROM in which case the waveform playback engine is used and the waveform is either played by an internal GO bit (register 0x0C), or by an external trigger.

#### 7.5.7.2.1 Waveform Playback Using RTP Mode

The user can enter the RTP mode by writing the MODE[2:0] bit to 5 in register 0x01. When in RTP mode, the DRV2605L-Q1 device drives the actuator continuously with the amplitude specified in the RTP_INPUT[7:0] bit (in register 0x02). Because the amplitude tracks the value specified in the RTP_INPUT[7:0] bit, the $I^2C$ bus can stream waveforms.

#### 7.5.7.2.2 Waveform Playback Using the Analog-Input Mode

The user can enter the analog-input mode by setting the MODE[2:0] bit to 3 in register 0x01 and by setting the N_PWM_ANALOG bit to 1 in register 0x1D. When in analog-input mode, the DRV2605L-Q1 device accepts an analog voltage at the IN/TRIG pin. The DRV2605L-Q1 device drives the actuator continuously in analog-input mode until the user sets the device into STANDBY mode or enters another interface mode. The reference voltage in analog-input mode is 1.8 V. Therefore a 1.8-V reference voltage is interpreted as a 100% input value, a 0.9-V reference voltage is interpreted as 50%, and a 0-V reference voltage is interpreted as 0%. The input value is analogous to the duty-cycle percentage in PWM mode. The interpretation of these percentages varies according to the selected mode of operation. See the *Data Formats for Waveform Playback* section for details.

#### 7.5.7.2.3 Waveform Playback Using PWM Mode

The user can enter the PWM mode by setting the MODE[2:0] bit to 3 in register 0x01 and by setting the N_PWM_ANALOG bit to 0 in register 0x1D. When in PWM mode, the DRV2605L-Q1 device accepts PWM data at the IN/TRIG pin. The DRV2605L-Q1 device drives the actuator continuously in PWM mode until the user sets the device to STANDBY mode or to enter another interface mode. The interpretation of the duty-cycle information varies according to the selected mode of operation. See the *Data Formats for Waveform Playback* section for details.

#### 7.5.7.2.4 Waveform Playback Using Audio-to-Vibe Mode

To take advantage of the audio-to-vibe feature, connect the DRV2605L-Q1 device to a line-out source as shown in Figure 58. The full-scale range of the IN/TRIG pin in the audio-to-vibe mode is 1.8 $V_{PP}$. A 1-µF capacitor is recommended to AC couple the audio source and the IN/TRIG pin. For sources smaller than 1.8 $V_{PP}$, the ATH_MAX_INPUT bit in register 0x13 can scale down the input range.

The device enters audio-to-vibe mode when the MODE[2:0] bit is set to 4 in register 0x01 and when the AC_COUPLE bit in register 0x1B and the N_PWM_ANALOG bit in register 0x1D are set to 1. See the *Register Map* section for details.

#### 7.5.7.2.5 Waveform Sequencer

If the user uses library effects, the effects must first be loaded into the waveform sequencer, and then the effects can be launched by using any of the trigger options (see the *Waveform Triggers* section for details).

The waveform sequencer (see the *Waveform Sequencer (Address: 0x04 to 0x0B)* section) queues waveform-library identifiers for playback. Eight sequence registers queue up to eight library waveforms for sequential playback. A waveform identifier is an integer value referring to the index position of a waveform in the ROM library. Playback begins at register address 0x04 when the user asserts the GO bit (register 0x0C). When playback of that waveform ends, the waveform sequencer plays the next waveform identifier held in register 0x05, if the next waveform is non-zero. The waveform sequencer continues in this way until the sequencer reaches an identifier value of zero or until all eight identifiers are played (register addresses 0x04 through 0x0B), whichever comes first.

The waveform identifier range is 1 to 123. The MSB of each sequence register can be used to implement a delay between sequence waveforms. When the MSB is high, bits 6-0 indicate the length of the wait time. The wait time for that step then becomes WAV_FRM_SEQ[6:0] × 10 ms.


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## Programming (continued)

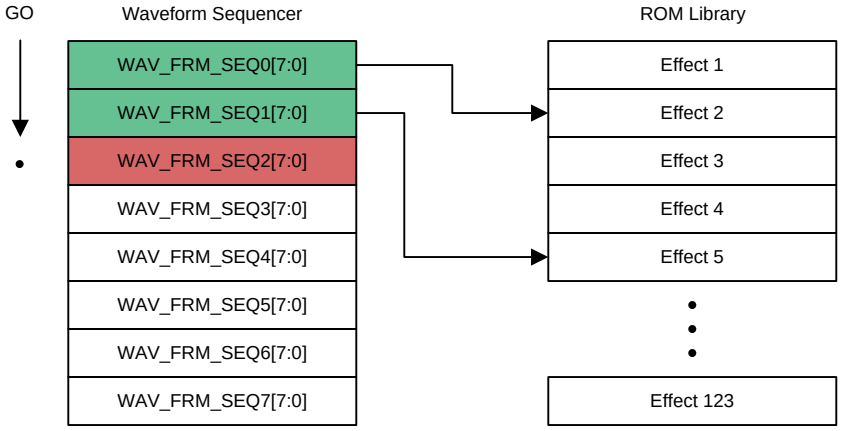



**Figure 28. Waveform Sequencer Programming**

#### 7.5.7.2.6 Waveform Triggers

When the waveform sequencer has the effect (or effects) loaded, the waveform sequencer can be triggered by an internal trigger, external trigger (edge), or external trigger (level). To trigger using the internal trigger set the MODE[2:0] bit to 0 in register 0x01. To trigger using the external trigger (edge), set the MODE[2:0] bit to 1 and then follow the trigger instructions listed in the *Edge Trigger* section. To trigger using the external trigger (level), set the MODE[2:0] bit to 2 and then follow the trigger instructions listed in the *Level Trigger* section.

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## 7.6 Register Map

**Table 3. Register Map Overview**

| REG NO. | DEFAULT | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x00 | 0xE0 | DEVICE_ID[2:0] | | | Reserved | DIAG_RESULT | Reserved | OVER_TEMP | OC_DETECT |
| 0x01 | 0x40 | DEV_RESET | STANDBY | Reserved | | | MODE[2:0] | | |
| 0x02 | 0x00 | RTP_INPUT[7:0] | | | | | | | |
| 0x03 | 0x01 | Reserved | | | HI_Z | Reserved | LIBRARY_SEL[2] | LIBRARY_SEL[1] | LIBRARY_SEL[0] |
| 0x04 | 0x01 | WAIT1 | WAV_FRM_SEQ1[6:0] | | | | | | |
| 0x05 | 0x00 | WAIT2 | WAV_FRM_SEQ2[6:0] | | | | | | |
| 0x06 | 0x00 | WAIT3 | WAV_FRM_SEQ3[6:0] | | | | | | |
| 0x07 | 0x00 | WAIT4 | WAV_FRM_SEQ4[6:0] | | | | | | |
| 0x08 | 0x00 | WAIT5 | WAV_FRM_SEQ5[6:0] | | | | | | |
| 0x09 | 0x00 | WAIT6 | WAV_FRM_SEQ6[6:0] | | | | | | |
| 0x0A | 0x00 | WAIT7 | WAV_FRM_SEQ7[6:0] | | | | | | |
| 0x0B | 0x00 | WAIT8 | WAV_FRM_SEQ8[6:0] | | | | | | |
| 0x0C | 0x00 | Reserved | | | | | | | GO |
| 0x0D | 0x00 | ODT[7:0] | | | | | | | |
| 0x0E | 0x00 | SPT[7:0] | | | | | | | |
| 0x0F | 0x00 | SNT[7:0] | | | | | | | |
| 0x10 | 0x00 | BRT[7:0] | | | | | | | |
| 0x11 | 0x05 | Reserved | | | | ATH_PEAK_TIME[1:0] | | ATH_FILTER[1:0] | |
| 0x12 | 0x19 | ATH_MIN_INPUT[7:0] | | | | | | | |
| 0x13 | 0xFF | ATH_MAX_INPUT[7:0] | | | | | | | |
| 0x14 | 0x19 | ATH_MIN_DRIVE[7:0] | | | | | | | |
| 0x15 | 0xFF | ATH_MAX_DRIVE[7:0] | | | | | | | |
| 0x16 | 0x3E | RATED_VOLTAGE[7:0] | | | | | | | |
| 0x17 | 0x8C | OD_CLAMP[7:0] | | | | | | | |
| 0x18 | 0x0C | A_CAL_COMP[7:0] | | | | | | | |
| 0x19 | 0x6C | A_CAL_BEMF[7:0] | | | | | | | |
| 0x1A | 0x36 | N_ERM_LRA | FB_BRAKE_FACTOR[2:0] | | | LOOP_GAIN[1:0] | | BEMF_GAIN[1:0] | |
| 0x1B | 0x93 | STARTUP_BOOST | Reserved | AC_COUPLE | DRIVE_TIME[4:0] | | | | |
| 0x1C | 0xF5 | BIDIR_INPUT | BRAKE_STABILIZER | SAMPLE_TIME[1:0] | | BLANKING_TIME[1:0] | | IDISS_TIME[1:0] | |
| 0x1D | 0xA0 | NG_THRESH[1:0] | | ERM_OPEN_LOOP | SUPPLY_COMP_DIS | DATA_FORMAT_RTP | LRA_DRIVE_MODE | N_PWM_ANALOG | LRA_OPEN_LOOP |
| 0x1E | 0x20 | ZC_DET_TIME[1:0] | | AUTO_CAL_TIME[1:0] | | Reserved | | | |
| 0x1F | 0x80 | AUTO_OL_CNT[1:0] | | LRA_AUTO_OPEN_LOOP | PLAYBACK_INTERVAL | BLANKING_TIME[3:2] | | IDISS_TIME[3:2] | |
| 0x20 | 0x33 | Reserved | OL_LRA_PERIOD[6:0] | | | | | | |
| 0x21 | 0x00 | VBAT[7:0] | | | | | | | |
| 0x22 | 0x00 | LRA_PERIOD[7:0] | | | | | | | |


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### 7.6.1 Status (Address: 0x00)

**Figure 29. Status Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DEVICE_ID[2:0] | | | Reserved | DIAG_RESULT | Reserved | OVER_TEMP | OC_DETECT |
| RO-1 | RO-1 | RO-1 | | RO-0 | | RO-0 | RO-0 |

**Table 4. Status Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-5 | DEVICE_ID[2:0] | RO | 7 | Device identifier. The DEVICE_ID bit indicates the part number to the user. The user software can ascertain the device capabilities by reading this register.<br>3: DRV2605 (contains licensed ROM library, does not contain RAM)<br>4: DRV2604 (contains RAM, does not contain licensed ROM library)<br>6: DRV2604L (low-voltage version of the DRV2604 device)<br>7: DRV2605L (low-voltage version of the DRV2605 device) |
| 4 | Reserved | | | |
| 3 | DIAG_RESULT | RO | 0 | This flag stores the result of the auto-calibration routine and the diagnostic routine. The flag contains the result for whichever routine was executed last. The flag clears upon read. Test result is not valid until the GO bit self-clears at the end of the routine.<br>Auto-calibration mode:<br>0: Auto-calibration passed (optimum result converged)<br>1: Auto-calibration failed (result did not converge)<br>Diagnostic mode:<br>0: Actuator is functioning normally<br>1: Actuator is not present or is shorted, timing out, or giving out–of-range back-EMF |
| 2 | Reserved | | | |
| 1 | OVER_TEMP | RO | 0 | Latching overtemperature detection flag. If the device becomes too hot, it shuts down. This bit clears upon read.<br>0: Device is functioning normally<br>1: Device has exceeded the temperature threshold |
| 0 | OC_DETECT | RO | 0 | Latching overcurrent detection flag. If the load impedance is below the load-impedance threshold, the device shuts down and periodically attempts to restart until the impedance is above the threshold.<br>0: No overcurrent event is detected<br>1: Overcurrent event is detected |

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### 7.6.2 Mode (Address: 0x01)

**Figure 30. Mode Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DEV_RESET | STANDBY | Reserved | | | MODE[2:0] | | |
| R/W-0 | R/W-1 | | | | R/W-0 | | |

**Table 5. Mode Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7 | DEV_RESET | R/W | 0 | Device reset. Setting this bit performs the equivalent operation of power cycling the device. Any playback operations are immediately interrupted, and all registers are reset to the default values. The DEV_RESET bit self-clears after the reset operation is complete. |
| 6 | STANDBY | R/W | 1 | Software standby mode<br>0: Device ready<br>1: Device in software standby |
| 5-3 | Reserved | | | |
| 2-0 | MODE | R/W | 0 | 0: Internal trigger<br>Waveforms are fired by setting the GO bit in register 0x0C.<br>1: External trigger (edge mode)<br>A rising edge on the IN/TRIG pin sets the GO Bit. A second rising edge on the IN/TRIG pin cancels the waveform if the second rising edge occurs before the GO bit has cleared.<br>2: External trigger (level mode)<br>The GO bit follows the state of the external trigger. A rising edge on the IN/TRIG pin sets the GO bit, and a falling edge sends a cancel. If the GO bit is already in the appropriate state, no change occurs.<br>3: PWM input and analog input<br>A PWM or analog signal is accepted at the IN/TRIG pin and used as the driving source. The device actively drives the actuator while in this mode. The PWM or analog input selection occurs by using the N_PWM_ANALOG bit.<br>4: Audio-to-vibe<br>An AC-coupled audio signal is accepted at the IN/TRIG pin. The device converts the audio signal into meaningful haptic vibration. The AC_COUPLE and N_PWM_ANALOG bits should also be set.<br>5: Real-time playback (RTP mode)<br>The device actively drives the actuator with the contents of the RTP_INPUT[7:0] bit in register 0x02.<br>6: Diagnostics<br>Set the device in this mode to perform a diagnostic test on the actuator. The user must set the GO bit to start the test. The test is complete when the GO bit self-clears. Results are stored in the DIAG_RESULT bit in register 0x00.<br>7: Auto calibration<br>Set the device in this mode to auto calibrate the device for the actuator. Before starting the calibration, the user must set the all required input parameters. The user must set the GO bit to start the calibration. Calibration is complete when the GO bit self-clears. For more information see the *Auto Calibration Procedure* section. |


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### 7.6.3 Real-Time Playback Input (Address: 0x02)

**Figure 31. Real-Time Playback Input Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RTP_INPUT[7:0] | | | | | | | |
| R/W-0 | | | | | | | |

**Table 6. Real-Time Playback Input Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-0 | RTP_INPUT[7:0] | R/W | 0 | This field is the entry point for real-time playback (RTP) data. The DRV2605L-Q1 playback engine drives the RTP_INPUT[7:0] value to the load when MODE[2:0] = 5 (RTP mode). The RTP_INPUT[7:0] value can be updated in real-time by the host controller to create haptic waveforms. The RTP_INPUT[7:0] value is interpreted as signed by default, but can be set to unsigned by the DATA_FORMAT_RTP bit in register 0x1D. When the haptic waveform is complete, the user can idle the device by setting MODE[2:0] = 0, or alternatively by setting STANDBY = 1. |

### 7.6.4 (Address: 0x03)

**Figure 32. Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | HI_Z | Reserved | LIBRARY_SEL[2:0] | | |
| | | | R/W-0 | | R/W-0 | R/W-0 | R/W-1 |

**Table 7. Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-5 | Reserved | | | |
| 4 | HI_Z | R/W | 0 | This bit sets the output driver into a true high-impedance state. The device must be enabled to go into the high-impedance state. When in hardware shutdown or standby mode, the output drivers have 15 kO to ground. When the HI_Z bit is asserted, the hi-Z functionality takes effect immediately, even if a transaction is taking place. |
| 3 | Reserved | | | |
| 2-0 | LIBRARY_SEL | R/W | 1 | Waveform library selection value. This bit determines which library the playback engine selects when the GO bit is set. For additional details on the ERM libraries see the *Table 1* section.<br>0: Empty<br>1: TS2200 Library A<br>2: TS2200 Library B<br>3: TS2200 Library C<br>4: TS2200 Library D<br>5: TS2200 Library E<br>6: LRA Library<br>7: TS2200 Library F |

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### 7.6.5 Waveform Sequencer (Address: 0x04 to 0x0B)

**Figure 33. Waveform Sequencer Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| WAIT | WAV_FRM_SEQ[6:0] | | | | | | |
| R/W-0 | R/W-0 | | | | | | |

**Table 8. Waveform Sequencer Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7 | WAIT | R/W | 0 | When this bit is set, the WAV_FRM_SEQ[6:0] bit is interpreted as a *wait time* in which the playback engine idles. This bit is used to insert timed delays between sequentially played waveforms.<br>Delay time = 10 ms × WAV_FRM_SEQ[6:0]<br>If WAIT = 0, then WAV_FRM_SEQ[6:0] is interpreted as a waveform identifier for sequence playback. |
| 6-0 | WAV_FRM_SEQ | R/W | 0 | Waveform sequence value. This bit holds the waveform identifier of the waveform to be played. A waveform identifier is an integer value referring to the index position of a waveform in a ROM library. Playback begins at register address 0x04 when the user asserts the GO bit (register 0x0C). When playback of that waveform ends, the waveform sequencer plays the next waveform identifier held in register 0x05, if the next waveform identifier is non-zero. The waveform sequencer continues in this way until the sequencer reaches an identifier value of zero, or all eight identifiers are played (register addresses 0x04 through 0x0B), whichever comes first. |

### 7.6.6 GO (Address: 0x0C)

**Figure 34. GO Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | GO |
| | | | | | | | R/W-0 |

**Table 9. GO Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-1 | Reserved | | | |
| 0 | GO | R/W | 0 | This bit is used to fire processes in the DRV2605L-Q1 device. The process fired by the GO bit is selected by the MODE[2:0] bit (register 0x01). The primary function of this bit is to fire playback of the waveform identifiers in the waveform sequencer (registers 0x04 to 0x0B), in which case, this bit can be thought of a *software trigger* for haptic waveforms. The GO bit remains high until the playback of the haptic waveform sequence is complete. Clearing the GO bit during waveform playback cancels the waveform sequence. Using one of the external trigger modes can cause the GO bit to be set or cleared by the external trigger pin. This bit can also be used to fire the auto-calibration process or the diagnostic process. |


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### 7.6.7 Overdrive Time Offset (Address: 0x0D)

**Figure 35. Overdrive Time Offset Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ODT[7:0] | | | | | | | |
| R/W-0 | | | | | | | |

**Table 10. Overdrive Time Offset Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-0 | ODT | R/W | 0 | This bit adds a time offset to the overdrive portion of the library waveforms. Some motors require more overdrive time than others, therefore this register allows the user to add or remove overdrive time from the library waveforms. The maximum voltage value in the library waveform is automatically determined to be the overdrive portion. This register is only useful in open-loop mode. Overdrive is automatic for closed-loop mode. The offset is interpreted as 2s complement, therefore the time offset can be positive or negative.<br>Overdrive Time Offset (ms) = ODT[7:0] × PLAYBACK_INTERVAL |

### 7.6.8 Sustain Time Offset, Positive (Address: 0x0E)

**Figure 36. Sustain Time Offset, Positive Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SPT[7:0] | | | | | | | |
| R/W-0 | | | | | | | |

**Table 11. Sustain Time Offset, Positive Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-0 | SPT | R/W | 0 | This bit adds a time offset to the positive sustain portion of the library waveforms. Some motors have a faster or slower response time than others, therefore this register allows the user to add or remove positive sustain time from the library waveforms. Any positive voltage value other than the overdrive portion is considered as a sustain positive value. The offset is interpreted as 2s complement, therefore the time offset can positive or negative.<br>Sustain-Time Positive Offset (ms) = SPT[7:0] × PLAYBACK_INTERVAL |

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### 7.6.9 Sustain Time Offset, Negative (Address: 0x0F)

**Figure 37. Sustain Time Offset, Negative Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SNT[7:0] | | | | | | | |
| R/W-0 | | | | | | | |

**Table 12. Sustain Time Offset, Negative Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-0 | SNT | R/W | 0 | This bit adds a time offset to the negative sustain portion of the library waveforms. Some motors have a faster or slower response time than others, therefore this register allows the user to add or remove negative sustain time from the library waveforms. Any negative voltage value other than the overdrive portion is considered as a sustaining negative value. The offset is interpreted as two's complement, therefore the time offset can be positive or negative.<br>Sustain-Time Negative Offset (ms) = SNT[7:0] × PLAYBACK_INTERVAL |

### 7.6.10 Brake Time Offset (Address: 0x10)

**Figure 38. Brake Time Offset Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BRT[7:0] | | | | | | | |
| R/W-0 | | | | | | | |

**Table 13. Brake Time Offset Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-0 | BRT | R/W | 0 | This bit adds a time offset to the braking portion of the library waveforms. Some motors require more braking time than others, therefore this register allows the user to add or take away brake time from the library waveforms. The most negative voltage value in the library waveform is automatically determined to be the braking portion. This register is only useful in open-loop mode. Braking is automatic for closed-loop mode. The offset is interpreted as 2s complement, therefore the time offset can be positive or negative.<br>Brake Time Offset (ms) = BRT[7:0] × PLAYBACK_INTERVAL |


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### 7.6.11 Audio-to-Vibe Control (Address: 0x11)

**Figure 39. Audio-to-Vibe Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | ATH_PEAK_TIME[1:0] | | ATH_FILTER[1:0] | |
| | | | | R/W-0 | R/W-1 | R/W-0 | R/W-1 |

**Table 14. Audio-to-Vibe Control Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-4 | Reserved | | | |
| 3-2 | ATH_PEAK_TIME[1:0] | R/W | 1 | This bit sets the peak detection time for the audio-to-vibe signal path:<br>0: 10 ms<br>1: 20 ms<br>2: 30 ms<br>3: 40 ms |
| 1-0 | ATH_FILTER[1:0] | R/W | 1 | This bit sets the low-pass filter frequency for the audio-to-vibe signal path:<br>0: 100 Hz<br>1: 125 Hz<br>2: 150 Hz<br>3: 200 Hz |

### 7.6.12 Audio-to-Vibe Minimum Input Level (Address: 0x12)

**Figure 40. Audio-to-Vibe Minimum Input Level Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ATH_MIN_INPUT[7:0] | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-1 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 15. Audio-to-Vibe Minimum Input Level Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-0 | ATH_MIN_INPUT[7:0] | R/W | 0x19 | This bit sets the minimum voltage level at the IN/TRIG pin that is detected by the audio-to-vibe engine. Levels below this are ignored.<br>ATH_MIN_INPUT Voltage ($V_{PP}$) = ATH_MIN_INPUT[7:0] × 1.8 V / 255 |

### 7.6.13 Audio-to-Vibe Maximum Input Level (Address: 0x13)

**Figure 41. Audio-to-Vibe Maximum Input Level Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ATH_MAX_INPUT[7:0] | | | | | | | |
| R/W-1 | | | | | | | |

**Table 16. Audio-to-Vibe Maximum Input Level Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-0 | ATH_MAX_INPUT[7:0] | R/W | 0xFF | This bit sets the full-scale voltage level at the IN/TRIG pin for audio-to-vibe mode.<br>ATH_MAX_INPUT Voltage ($V_{PP}$) = ATH_MAX_INPUT[7:0] × 1.8 V / 255 |

### 7.6.14 Audio-to-Vibe Minimum Output Drive (Address: 0x14)

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**Figure 42. Audio-to-Vibe Minimum Output Drive Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ATH_MIN_DRIVE[7:0] | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-1 |

**Table 17. Audio-to-Vibe Minimum Output Drive Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-0 | ATH_MIN_DRIVE[7:0] | R/W | 0x19 | This bit sets the minimum output level that is applied to the actuator drive engine.<br>ATH_MIN_DRIVE (%) = ATH_MIN_DRIVE[7:0] / 255 × 100% |

### 7.6.15 Audio-to-Vibe Maximum Output Drive (Address: 0x15)

**Figure 43. Audio-to-Vibe Maximum Output Drive Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ATH_MAX_DRIVE[7:0] | | | | | | | |
| R/W-1 | | | | | | | |

**Table 18. Audio-to-Vibe Maximum Output Drive Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-0 | ATH_MAX_DRIVE[7:0] | R/W | 0xFF | This bit sets the maximum output level that is applied to the actuator drive engine.<br>ATH_MAX_DRIVE (%) = ATH_MAX_DRIVE[7:0] / 255 × 100% |


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### 7.6.16 Rated Voltage (Address: 0x16)

**Figure 44. Rated Voltage Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RATED_VOLTAGE[7:0] | | | | | | | |
| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 |

**Table 19. Rated Voltage Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-0 | RATED_VOLTAGE[7:0] | R/W | 0x3E | This bit sets the reference voltage for full-scale output during closed-loop operation. The auto-calibration routine uses this register as an input, therefore this register must be written with the rated voltage value of the motor before calibration is performed. This register is ignored for open-loop operation because the overdrive voltage sets the reference for that case. Any modification of this register value should be followed by calibration to set A_CAL_BEMF appropriately.<br>See the *Rated Voltage Programming* section for calculating the correct register value. |

### 7.6.17 Overdrive Clamp Voltage (Address: 0x17)

**Figure 45. Overdrive Clamp Voltage Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OD_CLAMP[7:0] | | | | | | | |
| R/W-1 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |

**Table 20. Overdrive Clamp Voltage Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7 | OD_CLAMP[7:0] | R/W | 0x8C | During closed-loop operation the actuator feedback allows the output voltage to go above the rated voltage during the automatic overdrive and automatic braking periods. This register sets a clamp so that the automatic overdrive is bounded. This bit also serves as the full-scale reference voltage for open-loop operation.<br>See the *Overdrive Voltage-Clamp Programming* section for calculating the correct register value. |

### 7.6.18 Auto-Calibration Compensation Result (Address: 0x18)

**Figure 46. Auto-Calibration Compensation-Result Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| A_CAL_COMP[7:0] | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |

**Table 21. Auto-Calibration Compensation-Result Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-0 | A_CAL_COMP[7:0] | R/W | 0x0C | This register contains the voltage-compensation result after execution of auto calibration. The value stored in the A_CAL_COMP bit compensates for any resistive losses in the driver. The calibration routine checks the impedance of the actuator to automatically determine an appropriate value. The auto-calibration compensation-result value is multiplied by the drive gain during playback.<br>Auto-calibration compensation coefficient = 1 + A_CAL_COMP[7:0] / 255 |

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### 7.6.19 Auto-Calibration Back-EMF Result (Address: 0x19)

**Figure 47. Auto-Calibration Back-EMF Result Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| A_CAL_BEMF[7:0] | | | | | | | |
| R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |

**Table 22. Auto-Calibration Back-EMF Result Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-0 | A_CAL_BEMF[7:0] | R/W | 0x6F | This register contains the rated back-EMF result after execution of auto calibration. The A_CAL_BEMF[7:0] bit is the level of back-EMF voltage that the actuator gives when the actuator is driven at the rated voltage. The DRV2605L-Q1 playback engine uses this the value stored in this bit to automatically determine the appropriate feedback gain for closed-loop operation.<br>Auto-calibration back-EMF (V) = (A_CAL_BEMF[7:0] / 255) × 1.22 V / BEMF_GAIN[1:0] |


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### 7.6.20 Feedback Control (Address: 0x1A)

**Figure 48. Feedback Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| N_ERM_LRA | FB_BRAKE_FACTOR[2:0] | | | LOOP_GAIN[1:0] | | BEMF_GAIN[1:0] | |
| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-1 | R/W-1 | R/W-0 |

**Table 23. Feedback Control Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7 | N_ERM_LRA | R/W | 0 | This bit sets the DRV2605L-Q1 device in ERM or LRA mode. This bit should be set prior to running auto calibration.<br>0: ERM Mode<br>1: LRA Mode |
| 6-4 | FB_BRAKE_FACTOR[2:0] | R/W | 3 | This bit selects the feedback gain ratio between braking gain and driving gain. In general, adding additional feedback gain while braking is desirable so that the actuator brakes as quickly as possible. Large ratios provide less-stable operation than lower ones. The advanced user can select to optimize this register. Otherwise, the default value should provide good performance for most actuators. This value should be set prior to running auto calibration.<br>0: 1x<br>1: 2x<br>2: 3x<br>3: 4x<br>4: 6x<br>5: 8x<br>6: 16x<br>7: Braking disabled |
| 3-2 | LOOP_GAIN[1:0] | R/W | 1 | This bit selects a loop gain for the feedback control. The LOOP_GAIN[1:0] bit sets how fast the loop attempts to make the back-EMF (and thus motor velocity) match the input signal level. Higher loop-gain (faster settling) options provide less-stable operation than lower loop gain (slower settling). The advanced user can select to optimize this register. Otherwise, the default value should provide good performance for most actuators. This value should be set prior to running auto calibration.<br>0: Low<br>1: Medium (default)<br>2: High<br>3: Very High |
| 1-0 | BEMF_GAIN[1:0] | R/W | 2 | This bit sets the analog gain of the back-EMF amplifier. This value is interpreted differently between ERM mode and LRA mode. Auto calibration automatically populates the BEMF_GAIN bit with the most appropriate value for the actuator. |

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### 7.6.21 Control1 (Address: 0x1B)

**Figure 49. Control1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| STARTUP_BOOST | Reserved | AC_COUPLE | DRIVE_TIME[4:0] | | | | |
| R/W-1 | | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-1 | R/W-1 |

**Table 24. Control1 Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7 | STARTUP_BOOST | R/W | 1 | This bit applies higher loop gain during overdrive to enhance actuator transient response. |
| 6 | Reserved | | | |
| 5 | AC_COUPLE | R/W | 0 | This bit applies a 0.9-V common mode voltage to the IN/TRIG pin when an AC-coupling capacitor is used. This bit is only useful for analog input mode. This bit should not be asserted for PWM mode or external trigger mode.<br>0: Common-mode drive disabled for DC-coupling or digital inputs modes<br>1: Common-mode drive enabled for AC coupling |
| 4-0 | DRIVE_TIME[4:0] | R/W | 0x13 | **LRA Mode:** Sets initial *guess* for LRA drive-time in LRA mode. Drive time is automatically adjusted for optimum drive in real time; however, this register should be optimized for the approximate LRA frequency. If the bit is set too low, it can affect the actuator startup time. If the bit is set too high, it can cause instability.<br>Optimum drive time (ms) ≈ 0.5 × LRA Period<br>Drive time (ms) = DRIVE_TIME[4:0] × 0.1 ms + 0.5 ms<br>**ERM Mode:** Sets the sample rate for the back-EMF detection. Lower drive times cause higher peak-to-average ratios in the output signal, requiring more supply headroom. Higher drive times cause the feedback to react at a slower rate.<br>Drive Time (ms) = DRIVE_TIME[4:0] × 0.2 ms + 1 ms |


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### 7.6.22 Control2 (Address: 0x1C)

**Figure 50. Control2 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BIDIR_INPUT | BRAKE_STABILIZER | SAMPLE_TIME[1:0] | | BLANKING_TIME[1:0] | | IDISS_TIME[1:0] | |
| R/W-1 | R/W-1 | R/W-1 | | R/W-0 | R/W-1 | R/W-0 | R/W-1 |

**Table 25. Control2 Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7 | BIDIR_INPUT | R/W | 1 | The BIDIR_INPUT bit selects how the engine interprets data.<br>0: Unidirectional input mode<br>Braking is automatically determined by the feedback conditions and is applied when required. Use of this mode also recovers an additional bit of vertical resolution. This mode should only be used for closed-loop operation.<br>**Examples:**:<br>0% Input ? No output signal<br>50% Input ? Half-scale output signal<br>100% Input ? Full-scale output signal<br>1: Bidirectional input mode (default)<br>This mode is compatible with traditional open-loop signaling and also works well with closed-loop mode. When operating closed-loop, braking is automatically determined by the feedback conditions and applied when required. When operating open-loop modes, braking is only applied when the input signal is less than 50%.<br>**Open-loop mode (ERM and LRA) examples:**<br>0% Input ? Negative full-scale output signal (braking)<br>25% Input ? Negative half-scale output signal (braking)<br>50% Input ? No output signal<br>75% Input ? Positive half-scale output signal<br>100% Input ? Positive full-scale output signal<br>**Closed-loop mode (ERM and LRA) examples:**<br>0% to 50% Input ? No output signal<br>50% Input ? No output signal<br>75% Input ? Half-scale output signal<br>100% Input ? Full-scale output signal |
| 6 | BRAKE_STABILIZER | R/W | 1 | When this bit is set, loop gain is reduced when braking is almost complete to improve loop stability |
| 5-4 | SAMPLE_TIME[1:0] | R/W | 1 | LRA auto-resonance sampling time (Advanced use only)<br>0: 150 µs<br>1: 200 µs<br>2: 250 µs<br>3: 300 µs |

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**Table 25. Control2 Register Field Descriptions (continued)**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 3-2 | BLANKING_TIME[1:0] | R/W | 2 | Blanking time before the back-EMF AD makes a conversion. (Advanced use only)<br>Blanking time for LRA has an additional 2 bits (BLANKING_TIME[3:2]) located in register 0x1F. Depending on the status of N_ERM_LRA the blanking time represents different values.<br>N_ERM_LRA = 0 (ERM mode)<br>0: 45 µs<br>1: 75 µs<br>2: 150 µs<br>3: 225 µs<br>N_ERM_LRA = 1(LRA mode)<br>0: 15 µs<br>1: 25 µs<br>2: 50 µs<br>3: 75 µs<br>4: 90 µs<br>5: 105 µs<br>6: 120 µs<br>7: 135 µs<br>8: 150 µs<br>9: 165 µs<br>10: 180 µs<br>11: 195 µs<br>12: 210 µs<br>13: 235 µs<br>14: 260 µs<br>15: 285 µs |


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**Table 25. Control2 Register Field Descriptions (continued)**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 1-0 | IDISS_TIME[1:0] | R/W | 2 | Current dissipation time. This bit is the time allowed for the current to dissipate from the actuator between PWM cycles for flyback mitigation. (Advanced use only)<br>the current dissipation time for LRA has an additional 2 bits (IDISS_TIME[3:2]) located in register 0x1F. Depending on the status of N_ERM_LRA the idiss time represents different values<br>N_ERM_LRA = 0 (ERM mode)<br>0: 45 µs<br>1: 75 µs<br>2: 150 µs<br>3: 225 µs<br>N_ERM_LRA = 1(LRA mode)<br>0: 15 µs<br>1: 25 µs<br>2: 50 µs<br>3: 75 µs<br>4: 90 µs<br>5: 105 µs<br>6: 120 µs<br>7: 135 µs<br>8: 150 µs<br>9: 165 µs<br>10: 180 µs<br>11: 195 µs<br>12: 210 µs<br>13: 235 µs<br>14: 260 µs<br>15: 285 µs |

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### 7.6.23 Control3 (Address: 0x1D)

**Figure 51. Control3 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| NG_THRESH[1:0] | | ERM_OPEN_LOOP | SUPPLY_COMP_DIS | DATA_FORMAT_RTP | LRA_DRIVE_MODE | N_PWM_ANALOG | LRA_OPEN_LOOP |
| R/W-1 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 26. Control3 Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-6 | NG_THRESH[1:0] | R/W | 2 | This bit is the noise-gate threshold for PWM and analog inputs.<br>0: Disabled<br>1: 2%<br>2: 4% (Default)<br>3: 8% |
| 5 | ERM_OPEN_LOOP | R/W | 1 | This bit selects mode of operation while in ERM mode. Closed-loop operation is usually desired for because of automatic overdrive and braking properties. However, many existing waveform libraries were designed for open-loop operation, therefore open-loop operation can be required for compatibility.<br>0: Closed Loop<br>1: Open Loop |
| 4 | SUPPLY_COMP_DIS | R/W | 0 | This bit disables supply compensation. The DRV2605L-Q1 device generally provides constant drive output over variation in the power supply input ($V_{DD}$). In some systems, supply compensation can have already been implemented upstream, therefore disabling the DRV2605L-Q1 supply compensation can be useful.<br>0: Supply compensation enabled<br>1: Supply compensation disabled |
| 3 | DATA_FORMAT_RTP | R/W | 0 | This bit selects the input data interpretation for RTP (Real-Time Playback) mode.<br>0: Signed<br>1: Unsigned |
| 2 | LRA_DRIVE_MODE | R/W | 0 | This bit selects the drive mode for the LRA algorithm. This bit determines how often the drive amplitude is updated. Updating once per cycle provides a symmetrical output signal, while updating twice per cycle provides more precise control.<br>0: Once per cycle<br>1: Twice per cycle |
| 1 | N_PWM_ANALOG | R/W | 0 | This bit selects the input mode for the IN/TRIG pin when MODE[2:0] = 3. In PWM input mode, the duty cycle of the input signal determines the amplitude of the waveform. In analog input mode, the amplitude of the input determines the amplitude of the waveform.<br>0: PWM Input<br>1: Analog Input |
| 0 | LRA_OPEN_LOOP | R/W | 0 | This bit selects an open-loop drive option for LRA Mode. When asserted, the playback engine drives the LRA at the selected frequency independently of the resonance frequency. In PWM input mode, the playback engine recovers the LRA commutation frequency from the PWM input, dividing the frequency by 128. Therefore the PWM input frequency must be equal to 128 times the resonant frequency of the LRA.<br>In RTP, ROM and audio-to-vibe mode, the frequency is set by the OL_LRA_PERIOD[6:0] bit. Open-loop mode is not supported if analog input mode is selected.<br>0: Auto-resonance mode<br>1: LRA open-loop mode |


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### 7.6.24 Control4 (Address: 0x1E)

**Figure 52. Control4 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ZC_DET_TIME[1] | ZC_DET_TIME[0] | AUTO_CAL_TIME[1:0] | | Reserved | | | |
| R/W-0 | R/W-0 | R/W-1 | R/W-0 | | | | |

**Table 27. Control4 Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-6 | ZC_DET_TIME[1:0] | R/W | 0 | This bit sets the minimum length of time devoted for detecting a zero crossing (advanced use only).<br>0: 100 µs<br>1: 200 µs<br>2: 300 µs<br>3: 390 µs |
| 5-4 | AUTO_CAL_TIME[1:0] | R/W | 2 | This bit sets the length of the auto calibration time. The AUTO_CAL_TIME[1:0] bit should be enough time for the motor acceleration to settle when driven at the RATED_VOLTAGE[7:0] value.<br>0: 150 ms (minimum), 350 ms (maximum)<br>1: 250 ms (minimum), 450 ms (maximum)<br>2: 500 ms (minimum), 700 ms (maximum)<br>3: 1000 ms (minimum), 1200 ms (maximum) |
| 3-0 | Reserved | | | |

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### 7.6.25 Control5 (Address: 0x1F)

**Figure 53. Control5 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AUTO_OL_CNT[1:0] | | LRA_AUTO_OPEN_LOOP | PLAYBACK_INTERVAL | BLANKING_TIME[3:2] | | IDISS_TIME[3:2] | |
| R/W-1 | R/W-0 | R/W-0 | R/W-0 | RW-0 | RW-0 | RW-0 | |

**Table 28. Control5 Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-6 | AUTO_OL_CNT[1:0] | R/W | 2 | This bit selects number of cycles required to attempt synchronization before transitioning to open loop when the LRA_AUTO_OPEN_LOOP bit is asserted,<br>0: 3 attempts<br>1: 4 attempts<br>2: 5 attempts<br>3: 6 attempts |
| 5 | LRA_AUTO_OPEN_LOOP | R/W | 0 | This bit selects the automatic transition to open-loop drive when a back-EMF signal is not detected (LRA only).<br>0: Never transitions to open loop<br>1: Automatically transitions to open loop |
| 4 | PLAYBACK_INTERVAL | R/W | 0 | This bit selects the memory playback interval.<br>0: 5 ms<br>1: 1 ms |
| 3-2 | BLANKING_TIME[3:2] | R/W | 0 | This bit sets the MSB for the BLANKING_TIME[3:0]. See the BLANKING_TIME[3:0] bit in the *Control2 (Address: 0x1C)* section for details. Advanced use only. |
| 1-0 | IDISS_TIME[3:2] | R/W | 0 | This bit sets the MSB for IDISS_TIME[3:0]. See the IDISS_TIME[1:0] bit in the *Control2 (Address: 0x1C)* section for details. Advanced use only. |

### 7.6.26 LRA Open Loop Period (Address: 0x20)

**Figure 54. LRA Open Loop Period Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | OL_LRA_PERIOD[6:0] | | | | | | |
| R/W-0 | | | | | | | |

**Table 29. LRA Open Loop Period Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-0 | OL_LRA_PERIOD[6:0] | R/W | 0 | This bit sets the period to be used for driving an LRA when open-loop mode is selected.<br>LRA open-loop period (µs) = OL_LRA_PERIOD[6:0] × 98.46 µs |

### 7.6.27 $V_{(BAT)}$ Voltage Monitor (Address: 0x21)

**Figure 55. $V_{(BAT)}$ Voltage-Monitor Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VBAT[7:0] | | | | | | | |
| R/W-0 | | | | | | | |


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**Table 30. $V_{(BAT)}$ Voltage-Monitor Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-0 | VBAT[7:0] | R/W | 0 | This bit provides a real-time reading of the supply voltage at the $V_{DD}$ pin. The device must be actively sending a waveform to take a reading.<br>$V_{DD}$ (V) = VBAT[7:0] × 5.6V / 255 |

### 7.6.28 LRA Resonance Period (Address: 0x22)

**Figure 56. LRA Resonance-Period Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LRA_PERIOD[7:0] | | | | | | | |
| R/W-0 | | | | | | | |

**Table 31. LRA Resonance-Period Register Field Descriptions**

| BIT | FIELD | TYPE | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 7-0 | LRA_PERIOD[7:0] | R/W | 0 | This bit reports the measurement of the LRA resonance period. The device must be actively sending a waveform to take a reading.<br>LRA period (us) = LRA_Period[7:0] × 98.46 µs |

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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The typical application for a haptic driver is in a touch-enabled system that already has an application processor which makes the decision on when to execute haptic effects.

The DRV2605L-Q1 device can be used fully with $I^2C$ communications (either using RTP or the memory interface). A system designer can chose to use external triggers to play low-latency effects (such as from a physical button) or can decide to use the PWM interface. Figure 57 shows a typical haptic system implementation. The system designer should not use the internal regulator (REG) to power any external load.

A system designer can also implement audio-to-vibe. Figure 58 shows a typical haptic system implementation supporting audio-to-vibe.

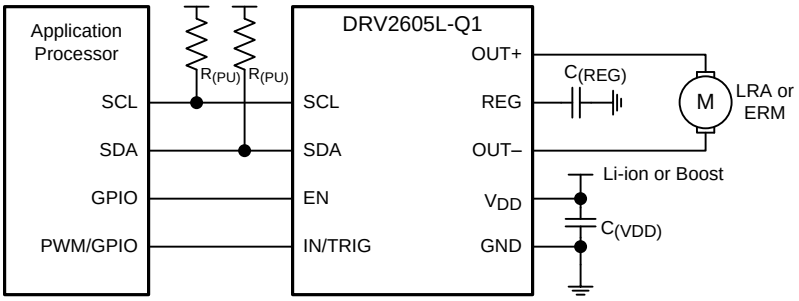



**Figure 57. $I^2C$ Control with Optional PWM Input or External Trigger**

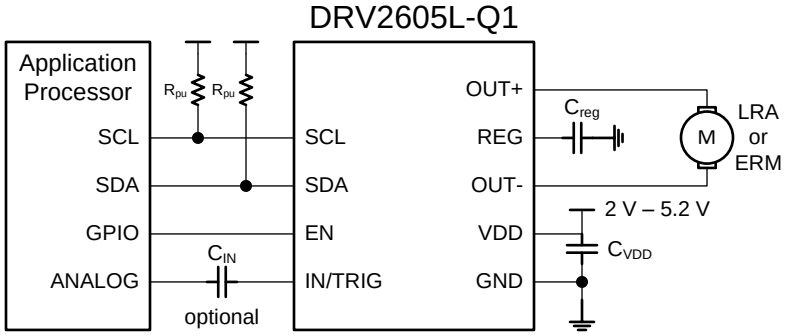



**Figure 58. $I^2C$ Control With Audio-to-Vibe Input and Optional AC Coupling**

**Table 32. Recommended External Components**

| COMPONENT | DESCRIPTION | SPECIFICATION | TYPICAL VALUE |
|---|---|---|---|
| $C_{(VDD)}$ | Input capacitor | Capacitance | 0.1 µF |
| $C_{(REG)}$ | Regulator capacitor | Capacitance | 1 µF |
| $C_{(IN)}$ | AC coupling capacitor (optional) | Capacitance | 1 µF |
| $R_{(PU)}$ | Pullup resistor | Resistance | 2.2 kΩ |


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## 8.2 Typical Application

A typical application of the DRV2605L-Q1 device is in a system that has external buttons which fire different haptic effects when pressed. Figure 59 shows a typical schematic of such a system. The buttons can be physical buttons, capacitive-touch buttons, or GPIO signals coming from the touch-screen system.

Effects in this type of system are programmable.

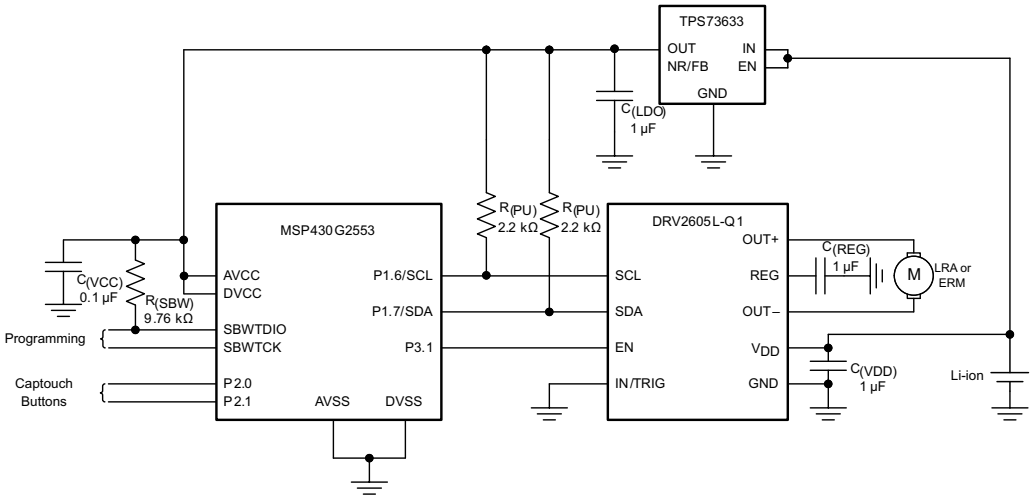



**Figure 59. Typical Application Schematic**

### 8.2.1 Design Requirements

For this design example, use the values listed in Table 33 as the input parameters.

**Table 33. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Interface | $I^2C$, external trigger |
| Actuator type | LRA, ERM |
| Input power source | Li-ion/Li-polymer, 5-V boost |

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Actuator Selection*

The actuator decision is based on many factors including cost, form factor, vibration strength, power-consumption requirements, haptic sharpness requirements, reliability, and audible noise performance. The actuator selection is one of the most important design considerations of a haptic system and therefore the actuator should be the first component to consider when designing the system. The following sections list the basics of ERM and LRA actuators.

##### 8.2.2.1.1 Eccentric Rotating-Mass Motors (ERM)

Eccentric rotating-mass motors (ERMs) are typically DC-controlled motors of the bar or coin type. ERMs can be driven in the clockwise direction or counter-clockwise direction depending on the polarity of voltage across the two pins. Bidirectional drive is made possible in a single-supply system by differential outputs that are capable of sourcing and sinking current. The bidirectional drive feature helps eliminate long vibration tails which are undesirable in haptic feedback systems.

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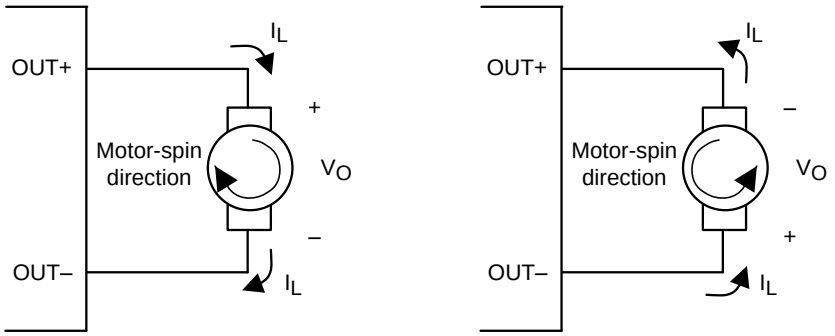



**Figure 60. Motor Spin Direction in ERM Motors**

Another common approach to driving DC motors is the concept of overdrive voltage. To overcome the inertia of the mass of the motor, the DC motors are often *overdriven* for a short amount of time before returning to the rated voltage of the motor to sustain the rotation of the motor. Overdrive is also used to stop (or brake) a motor quickly. Refer to the data sheet of the particular motor used with the DRV2605L-Q1 device for safe and reliable overdrive voltage and duration.

#### 8.2.2.1.2 Linear Resonance Actuators (LRA)

Linear resonant actuators (LRAs) vibrate optimally at the resonant frequency. LRAs have a high-Q frequency response because of a rapid drop in vibration performance at the offsets of 3 to 5 Hz from the resonant frequency. Many factors also cause a shift or drift in the resonant frequency of the actuator such as temperature, aging, the mass of the product to which the LRA is mounted, and in the case of a portable product, the manner in which the product is held. Furthermore, as the actuator is driven to the maximum allowed voltage, many LRAs will shift several hertz in frequency because of mechanical compression. All of these factors make a real-time tracking auto-resonant algorithm critical when driving LRA to achieve consistent, optimized performance.

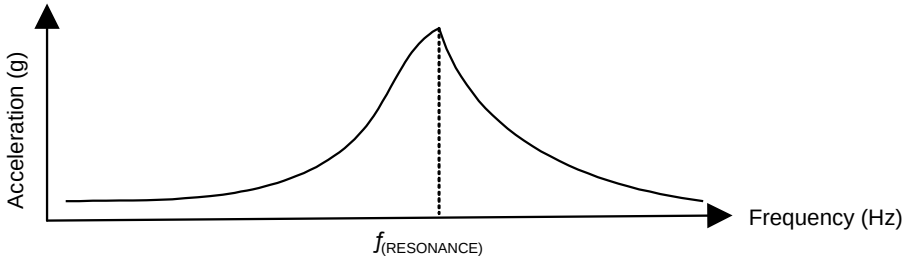



**Figure 61. Typical LRA Response**

##### *8.2.2.1.2.1 Auto-Resonance Engine for LRA*

The DRV2605L-Q1 auto-resonance engine tracks the resonant frequency of an LRA in real time effectively locking into the resonance frequency after half a cycle. If the resonant frequency shifts in the middle of a waveform for any reason, the engine tracks the frequency from cycle to cycle. The auto resonance engine accomplishes this tracking by constantly monitoring the back-EMF of the actuator. Note that the auto resonance engine is not affected by the auto-calibration process which is only used for level calibration. No calibration is required for the auto resonance engine.

### *8.2.2.2 Capacitor Selection*

The DRV2605L-Q1 device has a switching output stage which pulls transient currents through the $V_{DD}$ pin. TI recommends placing a 0.1-µF low equivalent-series-resistance (ESR) supply-bypass capacitor of the X5R or X7R type near the $V_{DD}$ supply pin for proper operation of the output driver and the digital portion of the device. Place a 1-µF X5R or X7R-type capacitor from the REG pin to ground.


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#### 8.2.2.3 Interface Selection

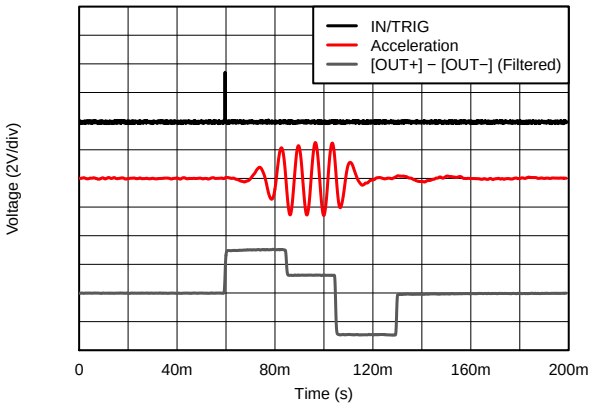
The $I^2C$ interface is required to configure the device. The device can be used fully with the $I^2C$ interface and with either RTP or internal memory. The advantage of using the $I^2C$ interface is that no additional GPIO (for the IN/TRIG pin) is required for firing effects, and no PWM signal is required to be generated. Therefore the IN/TRIG pin can be connected to GND. Using the external trigger pin has the advantage that no $I^2C$ transaction is required to fire the pre-loaded effect, which is a good choice for interfacing with a button. The PWM interface is available for backward compatibility. If audio-to-vibe is desired, then use $C_{(IN)}$ as shown in Figure 58.

#### 8.2.2.4 Power Supply Selection

The DRV2605L-Q1 device supports a wide range of voltages in the input. Ensuring that the battery voltage is high enough to support the desired vibration strength with the selected actuator is an important design consideration. The typical application uses Li-ion or Li-polymer batteries which provide enough voltage headroom to drive most common actuators.

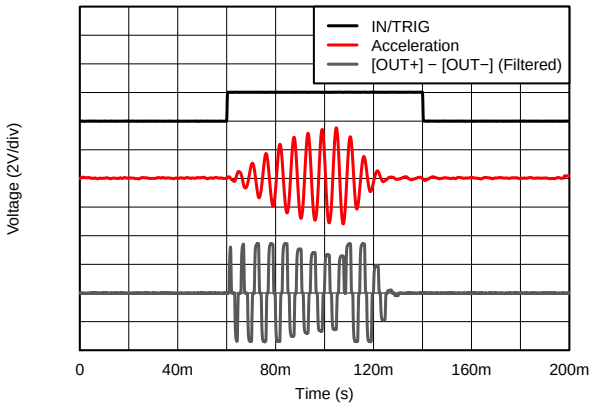
If very strong vibrations are desired, a boost converter can be placed between the power supply and the $V_{DD}$ pin to provide a constant voltage with a healthy headroom (5-V rails are common in some systems) which is particularly true if two AA batteries in series are being used to power the system.

### 8.2.3 Application Curves




$V_{DD}$ = 3.6 V ERM open loop
Strong click - 60% External edge trigger

**Figure 62. ERM Click with and without Braking**




$V_{DD}$ = 3.6 V LRA closed loop
Strong click - 100% External level trigger

**Figure 63. LRA Click With and Without Braking**

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## 8.3 Initialization Setup

### 8.3.1 Initialization Procedure

1. After powerup, wait at least 250 µs before the DRV2605L-Q1 device accepts $I^2C$ commands.
2. Assert the EN pin (logic high). The EN pin can be asserted any time during or after the 250-µs wait period.
3. Write the MODE register (address 0x01) to value 0x00 to remove the device from standby mode.
4. If the nonvolatile auto-calibration memory has been programmed as described in the *Auto Calibration Procedure* section, skip Step 5 and proceed to Step 6.
5. Perform the steps as described in the *Auto Calibration Procedure* section. Alternatively, rewrite the results from a previous calibration.
6. If using the embedded ROM library, write the library selection register (address 0x03) to select a library.
7. The default setup is closed-loop bidirectional mode. To use other modes and features, write Control1 (0x1B), Control2 (0x1C), and Control3 (0x1D) as required. Open-loop operation is recommended for ERM mode when using the ROM libraries.
8. Put the device in standby mode or deassert the EN pin, whichever is the most convenient. Both settings are low-power modes. The user can select the desired MODE (address 0x01) at the same time the STANDBY bit is set.

### 8.3.2 Typical Usage Examples

#### *8.3.2.1 Play a Waveform or Waveform Sequence from the ROM Waveform Memory*

1. Initialize the device as listed in the *Initialization Procedure* section.
2. Assert the EN pin (active high) if it was previously deasserted.
3. If register 0x01 already holds the desired value and the STANDBY bit is low, the user can skip this step. Select the desired MODE[2:0] value of 0 (internal trigger), 1 (external edge trigger), or 2 (external level trigger) in the MODE register (address 0x01). If the STANDBY bit was previously asserted, this bit should be deasserted (logic low) at this time.
4. Select the waveform index to be played and write it to address 0x04. Alternatively, a sequence of waveform indices can be written to register 0x04 through 0x0B. See the *Waveform Sequencer* section for details.
5. If using the internal trigger mode, set the GO bit (in register 0x0C) to fire the effect or sequence of effects. If using an external trigger mode, send an appropriate trigger pulse to the IN/TRIG pin. See the *Waveform Triggers* section for details.
6. If desired, the user can repeat Step 5 to fire the effect or sequence again.
7. Put the device in low-power mode by deasserting the EN pin or setting the STANDBY bit.

#### *8.3.2.2 Play a Real-Time Playback (RTP) Waveform*

1. Initialize the device as shown in the *Initialization Procedure* section.
2. Assert the EN pin (active high) if it was previously deasserted.
3. Set the MODE[2:0] value to 5 (RTP Mode) at address 0x01. If the STANDBY bit was previously asserted, this bit should be deasserted (logic low) at this time. If register 0x01 already holds the desired value and the STANDBY bit is low, the user can skip this step.
4. Write the desired drive amplitude to the real-time playback input register (address 0x02).
5. When the desired sequence of drive amplitudes is complete, put the device in low-power mode by deasserting the EN pin or setting the STANDBY bit.


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## Initialization Setup (continued)

#### *8.3.2.3 Play a PWM or Analog Input Waveform*

1. Initialize the device as shown in the *Initialization Procedure* section.
2. Assert the EN pin (active high) if it was previously deasserted.
3. If register 0x01 already holds the desired value and the STANDBY bit is low, the user can skip this step. Set the MODE value to 3 (PWM/Analog Mode) at address 0x01. If the STANDBY bit was previously asserted, this bit should be deasserted (logic low) at this time.
4. Select the input mode (PWM or analog) in the Control3 register (address 0x1D). If this mode was selected during the initialization procedure, the user can skip this step.
5. Send the desired PWM or analog input waveform sequence from the external source. See the *Data Formats for Waveform Playback* section for drive amplitude scaling.
6. When the desired drive sequence is complete, put the device in low-power mode by deasserting the EN pin or setting the STANDBY bit.

# 9 Power Supply Recommendations

The DRV2605L-Q1 device is designed to operate from an input-voltage supply range between 2 V to 5.2 V. The decoupling capacitor for the power supply should be placed closed to the device pin.

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# 10 Layout

## 10.1 Layout Guidelines

Use the following guidelines for the DRV2605L-Q1 layout:

- The decoupling capacitor for the power supply ($V_{DD}$) should be placed closed to the device pin.
- The filtering capacitor for the regulator (REG) should be placed close to the device REG pin.
- When creating the pad size for the WCSP pins, TI recommends that the PCB layout use nonsolder mask-defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area and the opening size is defined by the copper pad width. Figure 64 shows and Table 34 lists appropriate diameters for a wafer-chip scale package (WCSP) layout.

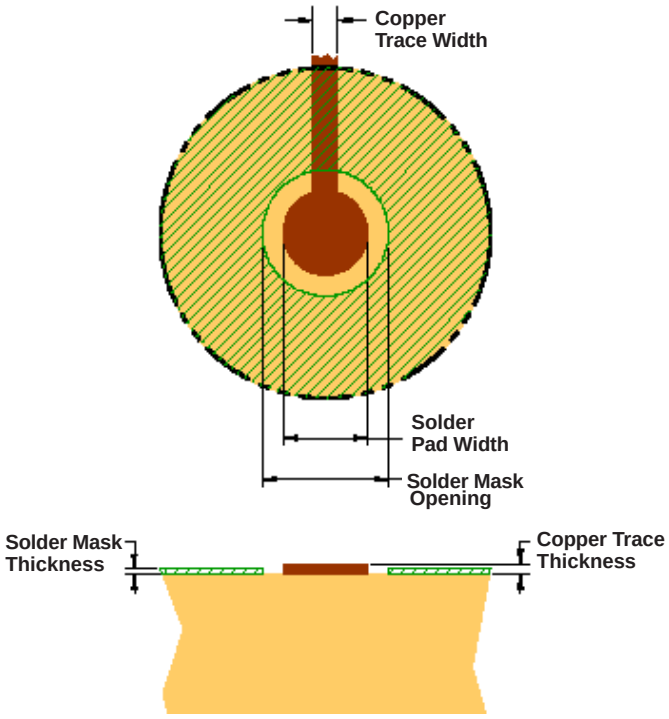



**Figure 64. Land Pattern Dimensions**

**Table 34. Land Pattern Dimensions**

| SOLDER PAD DEFINITIONS | COPPER PAD | SOLDER MASK OPENING | COPPER THICKNESS | STENCIL OPENING | STENCIL THICKNESS |
|---|---|---|---|---|---|
| Nonsolder mask defined (NSMD) | 275 µm (0, –25 µm) | 375 µm (0, –25 µm) | 1-oz maximum (32 µm) | 275 µm × 275 µm$^2$ (rounded corners) | 125-µm thick |

1. Circuit traces from NSMD defined PWB lands should be 75-µm to 100-µm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand-off and impact reliability.
2. The recommended solder paste is Type 3 or Type 4.
3. The best reliability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application.
4. For a PWB using a Ni/Au surface finish, the gold thickness should be less than 0.5 µm to avoid a reduction in thermal fatigue performance.
5. Solder mask thickness should be less than 20 µm on top of the copper circuit pattern.
6. The best solder stencil performance is achieved using laser-cut stencils with electro polishing. Use of chemically-etched stencils results in inferior solder paste volume control.
7. Trace routing away from the WCSP device should be balanced in *X* and *Y* directions to avoid unintentional component movement because of solder-wetting forces.


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### 10.1.1 Trace Width

The recommended trace width at the solder pins is 75 µm to 100 µm to prevent solder wicking onto wider PCB traces. Maintain this trace width until the pin pattern has escaped, then the trace width can be increased for improved current flow. The width and length of the 75-µm to 100-µm traces should be as symmetrical as possible around the device to provide even solder reflow on each of the pins.

## 10.2 Layout Example

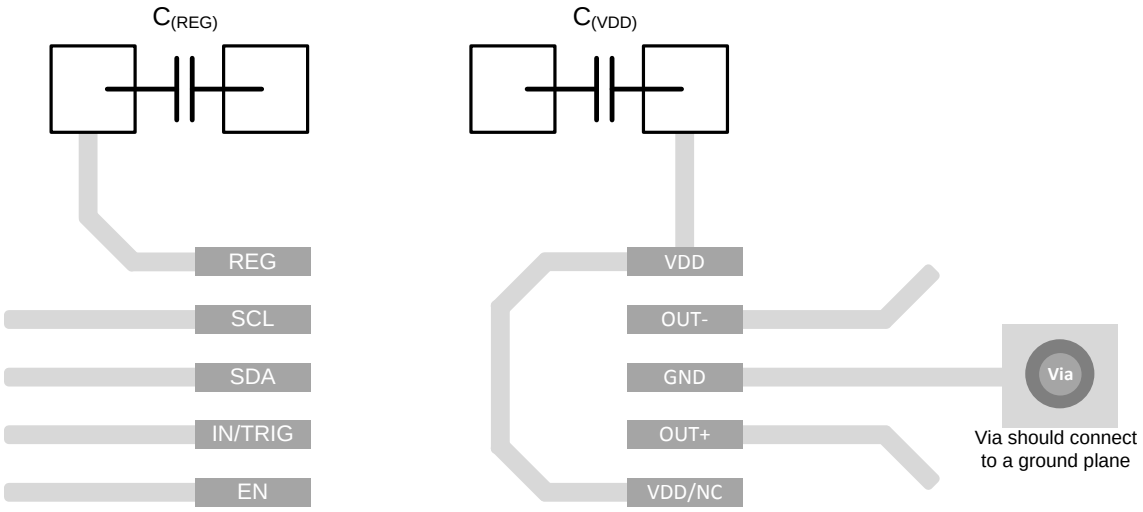



**Figure 65. DRV2605L-Q1 Layout Example VSSOP**

# 11 器件和文档支持

## 11.1 器件支持

### 11.1.1 法律声明

为帮助德州仪器 (TI) DRV2605L-Q1 产品的购买者和用户，TI 已向 Immersion 公司代付版税，保证您有权使用 TI DRV2605L-Q1 产品特定的内置（或专门设计的内置）Immersion 公司软件（仅限 TI DRV2605L-Q1 产品中包含的软件），同时要求遵守 TI 与 Immersion 公司达成的许可条款、条件和限制。根据 TI 与 Immersion 公司达成的许可条款、条件和限制，(1) 用户不得使用或分发 TI DRV2605L-Q1 产品中包含的任何 Immersion 公司软件，除非 TI DRV2605L-Q1 产品中包含的内容符合 TI 发布的适用规范和 DRV2605L-Q1 产品数据表，(2) 不得修改任何 Immersion 软件，(3) 不得更改或删除任何 Immersion 版权声明，(4) 不得反向工程设计或反汇编任何 Immersion 软件，或以其他方式尝试了解 Immersion 软件的内部工作原理或设计，(5) 不得将 Immersion 软件作为标准分析程序包发布。

### 11.1.2 波形库效果列表

| 效果 ID 号 | 波形名称 | 效果 ID 号 | 波形名称 | 效果 ID 号 | 波形名称 |
|---|---|---|---|---|---|
| 1 | 强力点击 - 100% | 42 | 长时间双次中度猛击 2 – 80% | 83 | 长时间平缓斜升转换 2 – 0 至 100% |
| 2 | 强力点击 - 60% | 43 | 长时间双次中度猛击 3 – 60% | 84 | 中等时间平缓斜升转换 1 – 0 至 100% |
| 3 | 强力点击 - 30% | 44 | 长时间双次猛击节拍 1 – 100% | 85 | 中等时间平缓斜升转换 2 – 0 至 100% |
| 4 | 猛击 - 100% | 45 | 长时间双次猛击节拍 2 – 80% | 86 | 短时间平缓斜升转换 1 – 0 至 100% |
| 5 | 猛击 - 60% | 46 | 长时间双次猛击节拍 3 – 60% | 87 | 短时间平缓斜升转换 2 – 0 至 100% |
| 6 | 猛击 - 30% | 47 | 蜂鸣 1 – 100% | 88 | 长时间剧烈斜升转换 1 – 0 至 100% |
| 7 | 软冲击 - 100% | 48 | 蜂鸣 2 – 80% | 89 | 长时间剧烈斜升转换 2 – 0 至 100% |
| 8 | 软冲击 - 60% | 49 | 蜂鸣 3 – 60% | 90 | 中等时间剧烈斜升转换 1 – 0 至 100% |
| 9 | 软冲击 - 30% | 50 | 蜂鸣 4 – 40% | 91 | 中等时间剧烈斜升转换 2 – 0 至 100% |
| 10 | 双次点击 - 100% | 51 | 蜂鸣 5 – 20% | 92 | 短时间剧烈斜升转换 1 – 0 至 100% |
| 11 | 双次点击 - 60% | 52 | 强脉冲 1 – 100% | 93 | 短时间剧烈斜升转换 2 – 0 至 100% |
| 12 | 三次点击 - 100% | 53 | 强脉冲 2 – 60% | 94 | 长时间平缓斜降转换 1 – 50 至 0% |
| 13 | 小毛刺 - 60% | 54 | 中等脉冲 1 – 100% | 95 | 长时间平缓斜降转换 2 – 50 至 0% |
| 14 | 剧烈蜂鸣 - 100% | 55 | 中等脉冲 2 – 60% | 96 | 中等时间平缓斜降转换 1 – 50 至 0% |
| 15 | 750ms 报警 100% | 56 | 剧烈脉冲 1 – 100% | 97 | 中等时间平缓斜降转换 2 – 50 至 0% |
| 16 | 1000ms 报警 100% | 57 | 剧烈脉冲 2 – 60% | 98 | 短时间平缓斜降转换 1 – 50 至 0% |
| 17 | 强力点击 1 - 100% | 58 | 转换点击 1 - 100% | 99 | 短时间平缓斜降转换 2 – 50 至 0% |
| 18 | 强力点击 2 - 80% | 59 | 转换点击 2 - 80% | 100 | 长时间剧烈斜降转换 1 – 50 至 0% |
| 19 | 强力点击 3 - 60% | 60 | 转换点击 3 - 60% | 101 | 长时间剧烈斜降转换 2 – 50 至 0% |
| 20 | 强力点击 4 - 30% | 61 | 转换点击 4 - 40% | 102 | 中等时间剧烈斜降转换 1 – 50 至 0% |
| 21 | 中等力度点击 1 - 100% | 62 | 转换点击 5 - 20% | 103 | 中等时间剧烈斜降转换 2 – 50 至 0% |
| 22 | 中等力度点击 2 - 80% | 63 | 转换点击 6 - 10% | 104 | 短时间剧烈斜降转换 1 – 50 至 0% |
| 23 | 中等力度点击 3 - 60% | 64 | 转换噪声 1 - 100% | 105 | 短时间剧烈斜降转换 2 – 50 至 0% |
| 24 | 猛击节拍 1 - 100% | 65 | 转换噪声 2 - 80% | 106 | 长时间平缓斜升转换 1 – 0 至 50% |
| 25 | 猛击节拍 2 - 80% | 66 | 转换噪声 3 - 60% | 107 | 长时间平缓斜升转换 2 – 0 至 50% |
| 26 | 猛击节拍 3 - 60% | 67 | 转换噪声 4 - 40% | 108 | 中等时间平缓斜升转换 1 – 0 至 50% |
| 27 | 短时间强力双击 1 – 100% | 68 | 转换噪声 5 - 20% | 109 | 中等时间平缓斜升转换 2 – 0 至 50% |
| 28 | 短时间强力双击 2 – 80% | 69 | 转换噪声 6 - 10% | 110 | 短时间平缓斜升转换 1 – 0 至 50% |
| 29 | 短时间强力双击 3 – 60% | 70 | 长时间平缓斜降转换 1 – 100 至 0% | 111 | 短时间平缓斜升转换 2 – 0 至 50% |
| 30 | 短时间强力双击 4 – 30% | 71 | 长时间平缓斜降转换 2 – 100 至 0% | 112 | 长时间剧烈斜升转换 1 – 0 至 50% |
| 31 | 短时间中等强度双击 1 – 100% | 72 | 中等时间平缓斜降转换 1 – 100 至 0% | 113 | 长时间剧烈斜升转换 2 – 0 至 50% |
| 32 | 短时间中等强度双击 2 – 80% | 73 | 中等时间平缓斜降转换 2 – 100 至 0% | 114 | 中等时间剧烈斜升转换 1 – 0 至 50% |
| 33 | 短时间中等强度双击 3 – 60% | 74 | 短时间平缓斜降转换 1 – 100 至 0% | 115 | 中等时间剧烈斜升转换 2 – 0 至 50% |
| 34 | 短时间双次猛击节拍 1 – 100% | 75 | 短时间平缓斜降转换 2 – 100 至 0% | 116 | 短时间剧烈斜升转换 1 – 0 至 50% |
| 35 | 短时间双次猛击节拍 2 – 80% | 76 | 长时间剧烈斜降转换 1 – 100 至 0% | 117 | 短时间剧烈斜升转换 2 – 0 至 50% |
| 36 | 短时间双次猛击节拍 3 – 60% | 77 | 长时间剧烈斜降转换 2 – 100 至 0% | 118 | 编程停止导致长时间蜂鸣 – 100% |
| 37 | 长时间双次强力猛击 1 – 100% | 78 | 中等时间剧烈斜降转换 1 – 100 至 0% | 119 | 平缓噪声 1（无回弹或制动脉冲） – 50% |
| 38 | 长时间双次强力猛击 2 – 80% | 79 | 中等时间剧烈斜降转换 2 – 100 至 0% | 120 | 平缓噪声 2（无回弹或制动脉冲） – 40% |
| 39 | 长时间双次强力猛击 3 – 60% | 80 | 短时间剧烈斜降转换 1 – 100 至 0% | 121 | 平缓噪声 3（无回弹或制动脉冲） – 30% |
| 40 | 长时间双次强力猛击 4 – 30% | 81 | 短时间剧烈斜降转换 2 – 100 至 0% | 122 | 平缓噪声 4（无回弹或制动脉冲） – 20% |
| 41 | 长时间双次中度猛击 1 – 100% | 82 | 长时间平缓斜升转换 1 – 0 至 100% | 123 | 平缓噪声 5（无回弹或制动脉冲） – 10% |


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## 11.2 文档支持

### 11.2.1 相关文档

如需相关文档，请参阅：

- *《触觉能耗》*，SLOA194
- *《关于移动设备和可穿戴设备的触觉实现注意事项》*，SLOA207
- *《LRA 致动器：如何移动它们？》*，SLOA209

## 11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

## 11.4 社区资源

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 11.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

# 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| DRV2605LTDGSRQ1 | Active | Production | VSSOP (DGS) \| 10 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 105 | 05LQ |
| DRV2605LTDGSRQ1.A | Active | Production | VSSOP (DGS) \| 10 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 105 | 05LQ |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF DRV2605L-Q1 :**

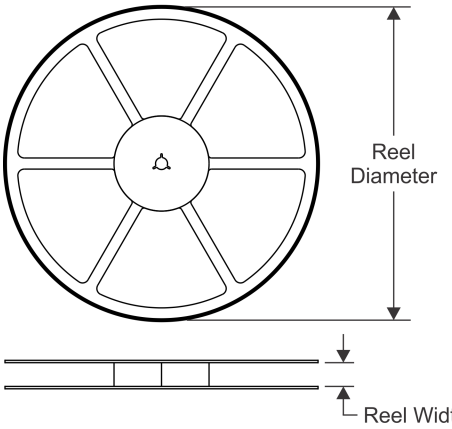
- Catalog : DRV2605L

NOTE: Qualified Version Definitions:

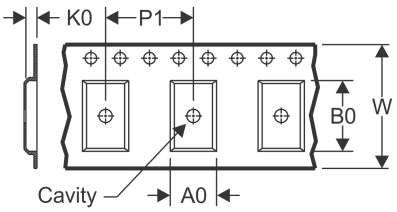
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

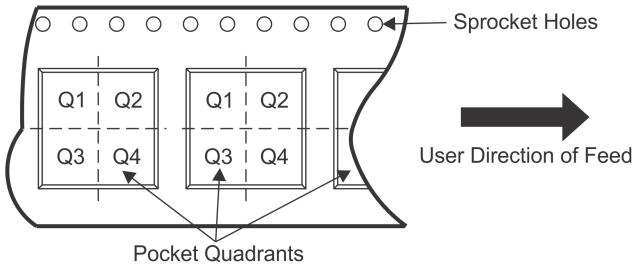



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

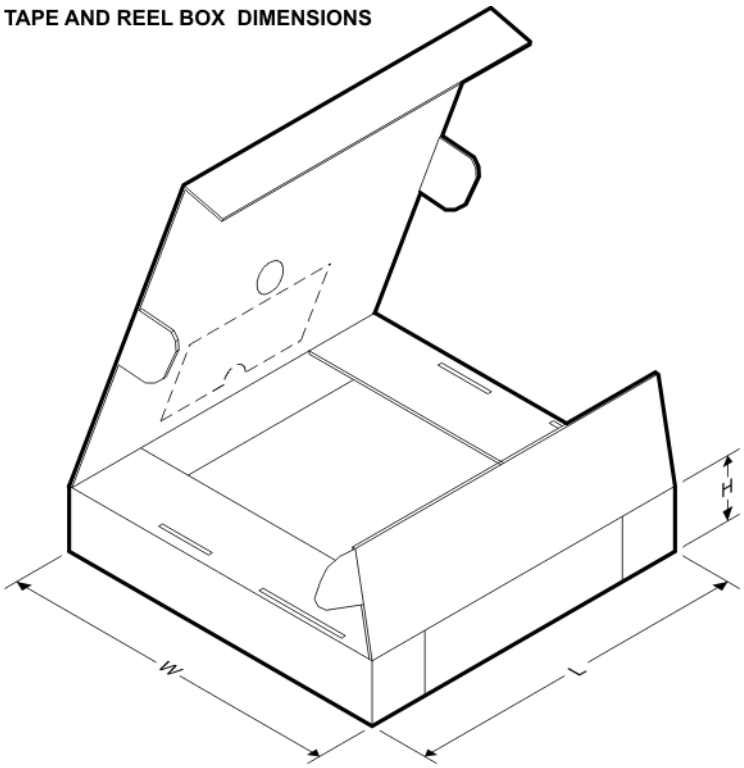
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV2605LTDGSRQ1 | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

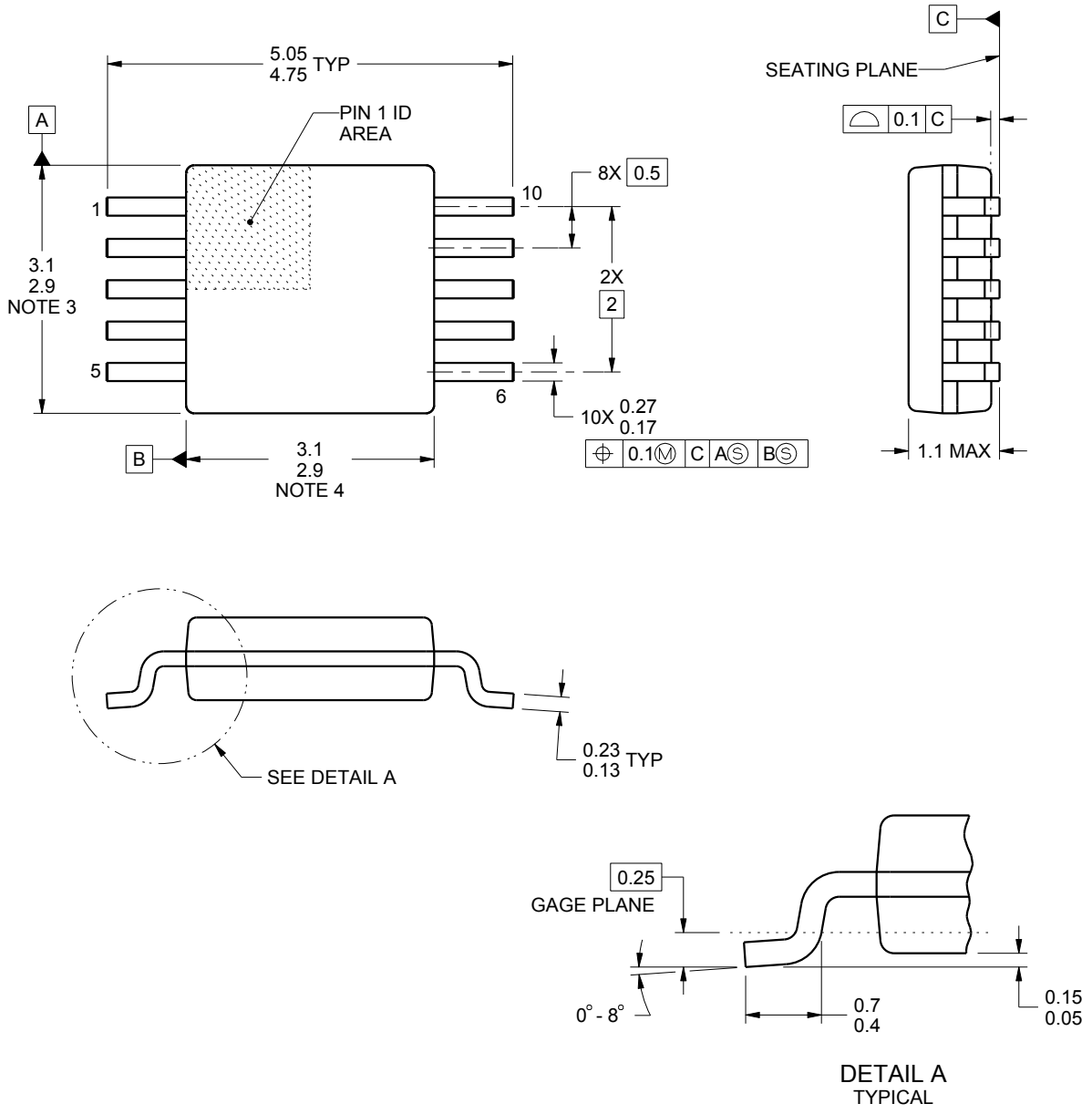
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DRV2605LTDGSRQ1 | VSSOP | DGS | 10 | 2500 | 366.0 | 364.0 | 50.0 |

# PACKAGE OUTLINE

## DGS0010A

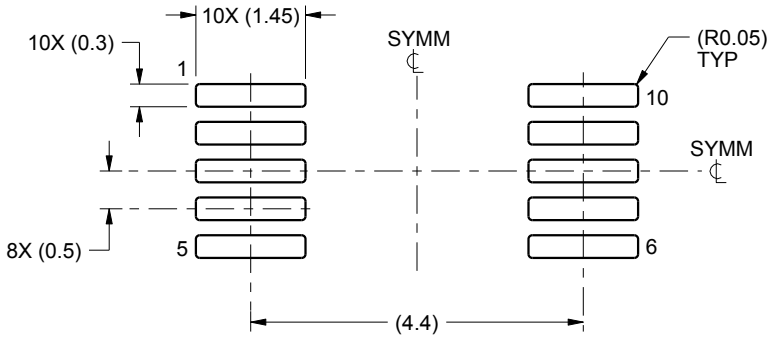
## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

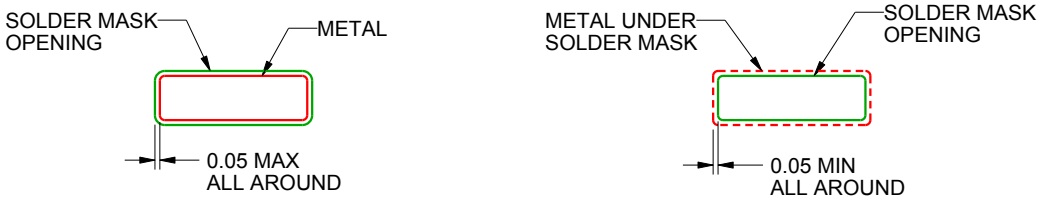



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.




LAND PATTERN EXAMPLE
SCALE:10X

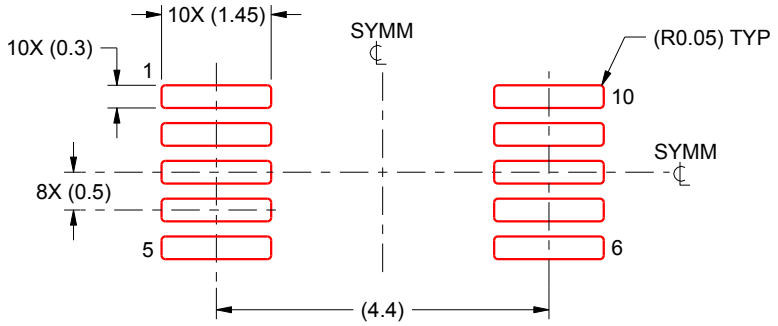



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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