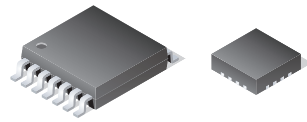


具有可编程固定增益的 2Vrms DirectPath™ 线路驱动器

查询样品: **DRV612**

特性

- **DirectPath™**
  - 消除了噼啪声/喀哒声
  - 免除了输出隔直流电容器
  - **3V** 至 **3.6V** 电源电压
- 低噪声及**THD**
  - **SNR > 105dB** （在—**1x** 增益条件下）
  - 典型 **Vn < 12μVms** （在 **20Hz** 至 **20kHz** 频率范围内和—**1x** 增益条件下）
  - **THD + N < 0.003%** （在 **10kΩ** 负载和—**1x** 增益条件下）
- 可为 **600Ω** 负载提供 **2Vrms** 输出电压
- 单端输入和输出
- 可编程增益选择减少了组件的数量
  - **13x** 增益值
- 具有大于 **80 dB** 衰减的有源静音
- 具短路和热保护功能
- **±8 kV HBM ESD** 保护输出

应用

- **PDP / LCD TV**
- **DVD** 播放机
- 迷你型/微型组合音响系统
- 声卡

说明

DRV612 是一款单端、2Vrms 立体声线路驱动器，专为缩减组件数量、板级空间和成本而设计。 对于那些将尺寸和成本作为关键设计参数的单电源电子产品而言，该器件是理想的选择。

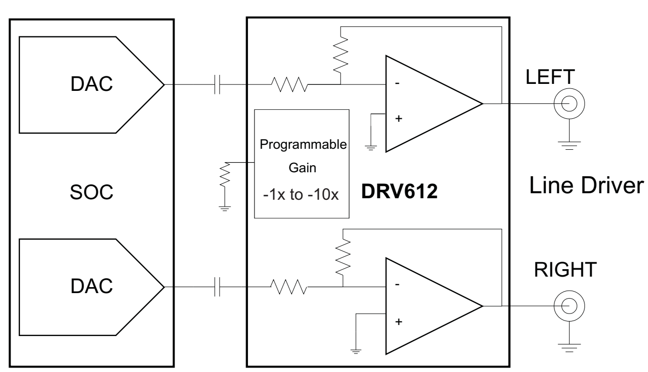
DRV612 既不需要采用一个高于 3.3V 的电源来产生其 $5.6V_{pp}$ 输出，也不需要一个分离轨电源。

DRV612 的设计运用了 TI 的 DirectPath 专利技术，集成了一个充电泵以产生一个负电源轨，可提供一个干净、无噼啪声的接地偏置输出。 DRV612 能够向一个 600Ω 负载输送 2Vrms 驱动电压。 另外，DirectPath 技术还允许去除昂贵的输出隔直流电容器。

该器件具有固定增益单端输入和一个增益选择引脚。 通过在该引脚上使用单个电阻器，设计人员就能够从 13 种内部可编程增益设定值中进行选择，以使线路驱动器与编解码器输出电平相匹配。 另外，它还削减了组件数量和板级空间。

线路输出具有 ±8 kV HBM ESD 保护等级，从而实现了简单的 ESD 保护电路。 DRV612 内置了具有大于 80 dB 衰减的有源静音控制功能电路，用于实现无噼啪声的静音接通/关断控制。

DRV612 采用 14 引脚 TSSOP 封装和 16 引脚 QFN 封装。 如需一款具有兼容焊脚的立体声头戴式耳机驱动器，请查阅 TPA6139A2 的文档资料 (SLOS700)。



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DirectPath is a trademark of Texas Instruments.

English Data Sheet: SLOS690B

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

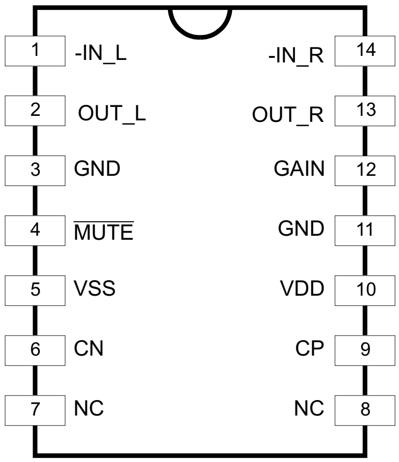
GENERAL INFORMATION

TERMINAL ASSIGNMENT

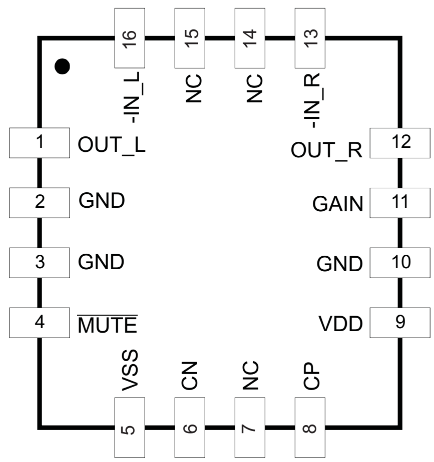
The DRV612 is available in package:

- 14-pin TSSOP package (PW) or 16-pin QFN package (RGT)

PW PACKAGE
TSSOP
(TOP VIEW)



RGT PACKAGE
QFN
(TOP VIEW)

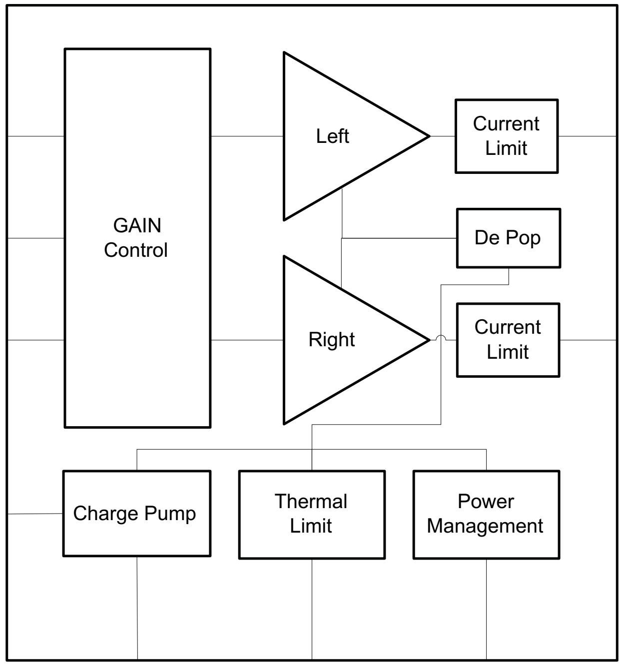


PIN FUNCTIONS

PIN			FUNCTION(1)	DESCRIPTION
NAME	PW NO.	RGT NO.		
-IN_L	1	16	I	Negative input, left channel
OUT_L	2	1	O	Output, left channel
GND	3, 11	2, 3, 10	P	Ground
$\overline{\text{MUTE}}$	4	4	I	MUTE, active low
VSS	5	5	O	Change Pump negative supply voltage
CN	6	6	I/O	Charge Pump flying capacitor negative connection
NC	7, 8	7. 14, 15		No internal connection
CP	9	8	I/O	Charge Pump flying capacitor positive connection
VDD	10	9	P	Supply voltage, connect to positive supply
GAIN	12	11	I	Gain set programming pin; connect a resistor to ground. See 表 1 for recommended resistor values
OUT_R	13	12	O	Output, right channel
-IN_R	14	13	I	Negative input, right channel
Thermal Pad	n/a	Thermal Pad	P	Connect to ground

(1) I = input, O = output, P = power

SYSTEM BLOCK DIAGRAM



ORDERING INFORMATION(1)

T_A	PACKAGE	DESCRIPTION
–40°C to 85°C	DRV612PW	14-pin TSSOP
	DRV612RGT	16-pin QFN

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV612 RGT (16-Pin)	DRV612 PW (14-Pin)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	52	130	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	71	49	
θ_{JB}	Junction-to-board thermal resistance	26	63	
ψ_{JT}	Junction-to-top characterization parameter	3.0	3.6	
ψ_{JB}	Junction-to-board characterization parameter	26	62	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

		VALUE MIN	VALUE MAX	UNIT
Voltage range	VDD to GND	–0.3	4	V
	V_I , Input voltage	VSS – 0.3	VDD + 0.3	V
	$\overline{\text{MUTE}}$ to GND	–0.3	VDD + 0.3	V
Temperature	Maximum operating junction temperature range, T_J	–40	150	°C
	Storage temperature	–65	150	°C
Electrostatic discharge (HBM) QSS 009-105 (JESD22-A114A)	OUT_L, OUT_R	8		kV
	All other pins	2		kV

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range unless otherwise noted

			MIN	NOM	MAX	UNIT
VDD	Supply voltage	DC supply voltage	3.0	3.3	3.6	V
R_L			600	10k		Ω
V_{IL}	Low-level input voltage	$\overline{\text{MUTE}}$	38	40	43	%VDD
V_{IH}	High-level input voltage	$\overline{\text{MUTE}}$	57	60	66	%VDD
T_A	Free-air temperature		–0	25	85	°C

ELECTRICAL CHARACTERISTICS

VDD = 3.3V, R_{LD} = 5 kΩ, T_A = 25°C, Charge pump: C_{CP} = 1 μF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output offset voltage	VDD = 3.3 V, input ac-coupled		0.5	1	mV
PSRR	Power-supply rejection ratio		70	80		dB
V_{OH}	High-level output voltage	VDD = 3.3 V	3.1			V
V_{OL}	Low-level output voltage	VDD = 3.3 V			–3.05	V
Vuvp_on	VDD, undervoltage detection				2.8	V
Vuvp_hysteresis	VDD, undervoltage detection, hysteresis			200		mV
F_{CP}	Charge-pump switching frequency			350		kHz
$\|I_{IH}\|$	High-level input current, $\overline{\text{MUTE}}$	VDD = 3.3 V, V_{IH} = VDD			1	μA
$\|I_{IL}\|$	Low-level input current, $\overline{\text{MUTE}}$	VDD = 3.3 V, V_{IL} = 0 V			1	μA
$I_{(VDD)}$	Supply current, no load	VDD, $\overline{\text{MUTE}}$ = 3.3 V		18		mA
	Supply current, MUTED	VDD = 3.3 V, $\overline{\text{MUTE}}$ = GND		18		mA
T_{SD}	Thermal shutdown			150		°C
	Thermal shutdown hysteresis			15		°C

ELECTRICAL CHARACTERISTICS, LINE DRIVER

VDD = 3.3 V, R_{LOAD} = 10 kΩ, T_A = 25°C, Charge pump: C_{CP} = 1 μF, 1× gain select (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage, outputs in phase	1% THD+N, f = 1 kHz, 10 -kΩ load		2.2		V_{rms}
THD+N	Total harmonic distortion plus noise	f = 1 kHz, 10-kΩ load, V_O = 2 V_{rms}		0.007%		
SNR	Signal-to-noise ratio	A-weighted, AES17 filter, 2 V_{rms} ref		105		dB
DNR	Dynamic range	A-weighted, AES17 filter, 2 V_{rms} ref		105		dB
Vn	Noise voltage	A-weighted, AES17 filter		12		μV
Zo	Output impedance when muted	$\overline{\text{MUTE}}$ = GND		0.07	1	Ω
	Input-to-output attenuation when muted	1 Vrms, 1-kHz input		80		dB
	Slew rate			4.5		V/μs
G_{BW}	Unity-gain bandwidth			8		MHz
	Crosstalk – Line L-R and R-L	10-kΩ load, V_O = 2 Vrms		–91		dB
I_{limit}	Current limit	VDD = 3.3 V		25		mA

PROGRAMMABLE GAIN SETTINGS(1)(2)

VDD = 3.3 V, R_{load} = 10 kΩ, T_A = 25°C, Charge pump: C_{CP} = 1 μF, 1× gain select, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_Tol	Gain programming resistor tolerance				2%	
ΔA_V	Gain matching	Between left and right channels		0.25		dB
	Gain step tolerance			0.1		dB
	Gain steps	Gain resistor 2% tolerance 249k or higher 82k5 51k1 34k8 27k4 20k5 15k4 11k5 9k09 7k50 6k19 5k11 4k22		 –2 –1 –1.5 –2.3 –2.5 –3 –3.5 –4 –5 –5.6 –6.4 –8.3 –10		V/V
	Input impedance	Gain resistor 2% tolerance 249k or higher 82k5 51k1 34k8 27k4 20k5 15k4 11k5 9k09 7k50 6k19 5k11 4k22		 37 55 44 33 31 28 24 22 18 17 15 12 10		kΩ

(1) If the GAIN pin is left floating, an internal pullup sets the gain to –2×.
(2) Gain setting is latched during power up.

TYPICAL CHARACTERISTICS, LINE DRIVER

V_{DD} = 3.3 V, T_A = 25°C, R_L = 2.5 kΩ, C_{PUMP} = $C_{(VSS)}$ = 1 μF, Gain = -2V/V (unless otherwise noted)

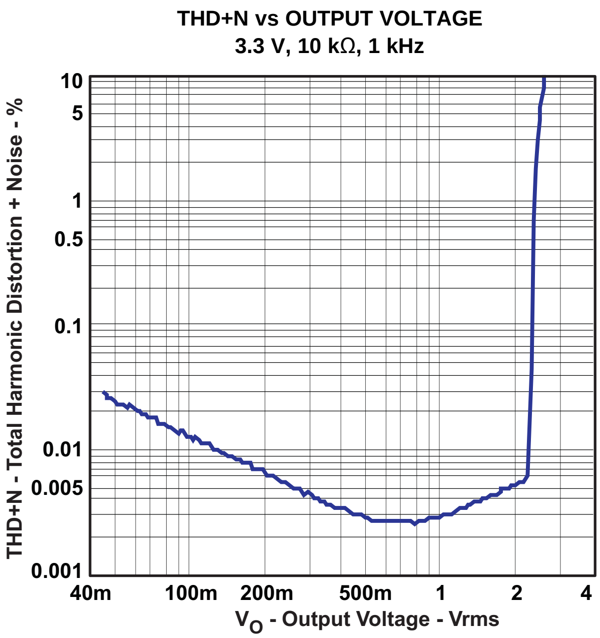


图 1.

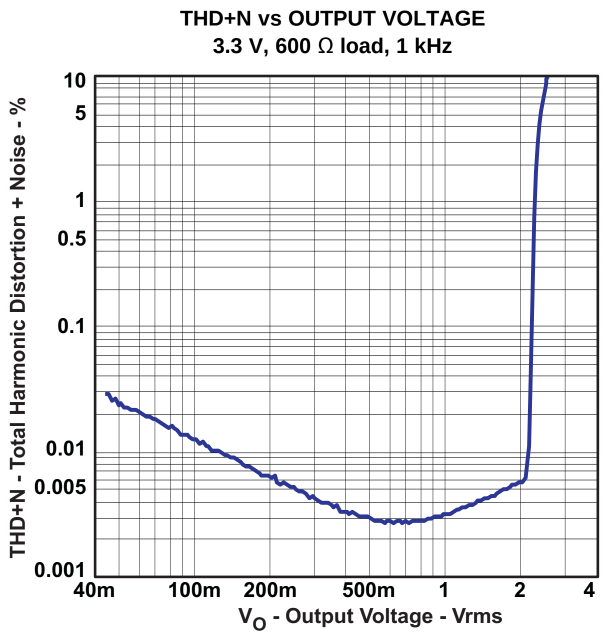
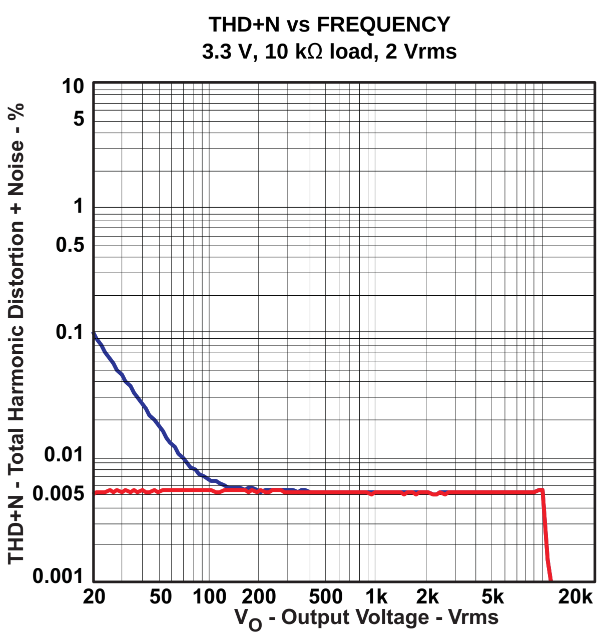


图 2.



Blue: 10-μF ceramic ac-coupling capacitor.

Red: 10-μF electrolytic ac-coupling capacitor

图 3.

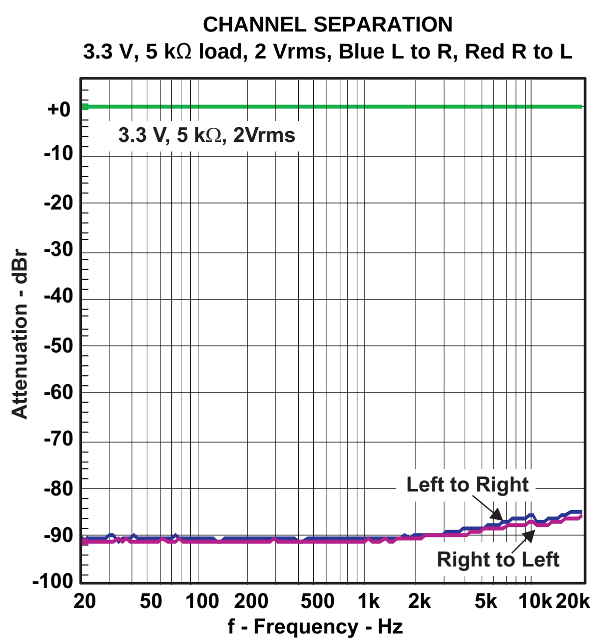


图 4.

TYPICAL CHARACTERISTICS, LINE DRIVER (接下页)

V_{DD} = 3.3 V, T_A = 25°C, R_L = 2.5 kΩ, C_{PUMP} = $C_{(VSS)}$ = 1 μF, Gain = -2V/V (unless otherwise noted)

Gain vs Frequency
For the Different Gain Settings

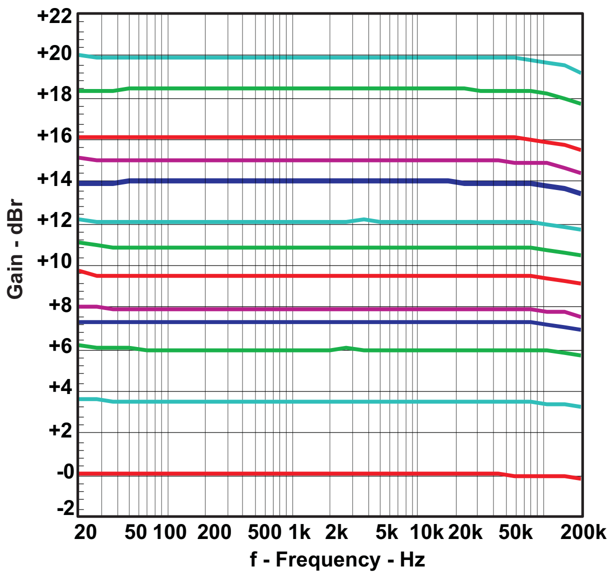


图 5.

Mute to Play

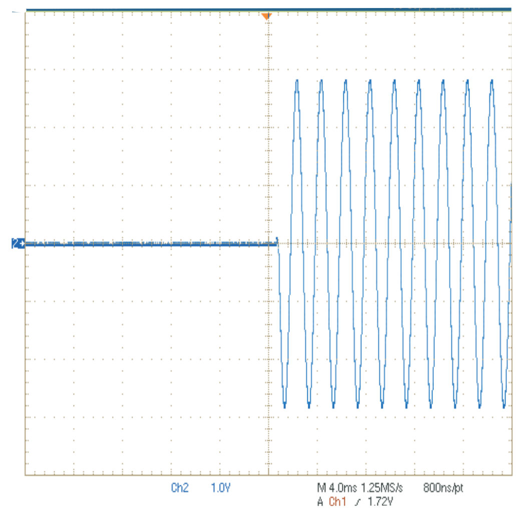


图 6.

Play to Mute

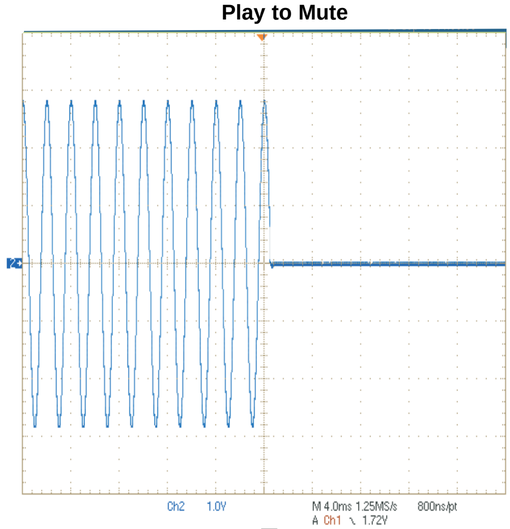


图 7.

APPLICATION INFORMATION

LINE DRIVER AMPLIFIERS

Single-supply line-driver amplifiers typically require dc-blocking capacitors. The top drawing in 图 8 illustrates the conventional line-driver amplifier connection to the load and output signal.

DC blocking capacitors are often large in value, and a mute circuit is needed during power up to minimize click and pop. The output capacitor and mute circuit consume PCB area and increase cost of assembly, and can reduce the fidelity of the audio output signal.

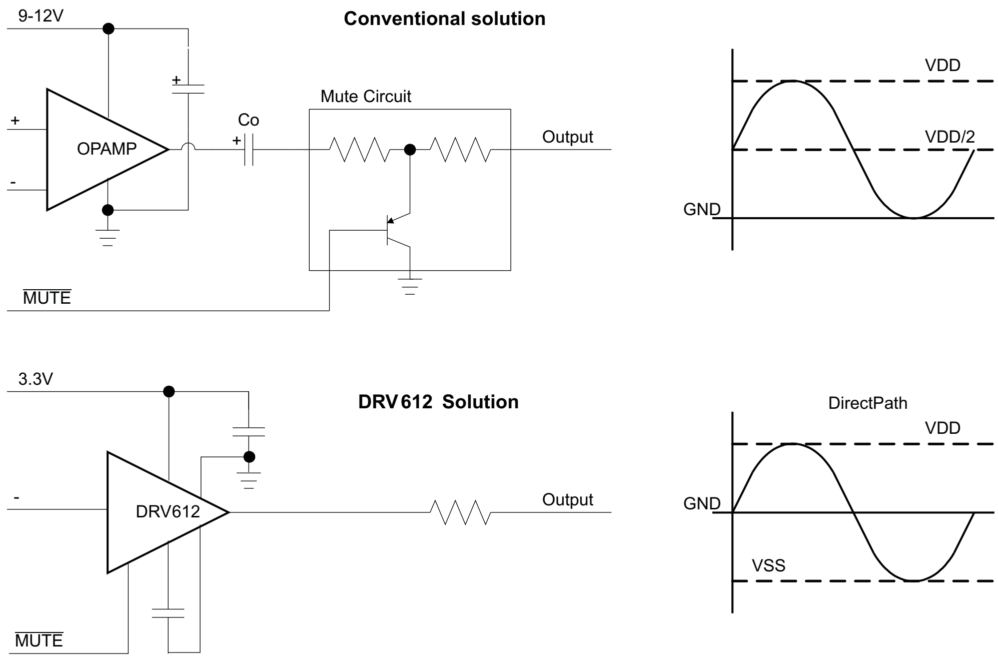


图 8. Conventional and DirectPath Line Driver

The DirectPath amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail.

Combining the user-provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode.

The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. Combining this with the built-in click- and pop-reduction circuit, the DirectPath amplifier requires no output dc-blocking capacitors.

The bottom block diagram and waveform of 图 8 illustrate the ground-referenced line-driver architecture. This is the architecture of the DRV612.

COMPONENT SELECTION

Charge Pump Flying Capacitor and VSS Capacitor

The charge-pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The VSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low-ESR capacitors are an ideal selection, and a value of 1 μF is typical.

Decoupling Capacitors

The DRV612 is a DirectPath line-driver amplifier that requires adequate power-supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 μF, placed as close as possible to the device VDD lead works best. Placing this decoupling capacitor close to the DRV612 is important for the performance of the amplifier. For filtering lower-frequency noise signals, a 10-μF or greater capacitor placed near the audio power amplifier also helps, but it is not required in most applications because of the high PSRR of this device.

Gain-Setting

The gain setting is programmed with the GAIN pin. Gain setting is latched durning power on. 表 1 lists the gain settings.

NOTE: If gain pin is left unconnected (open) default gain of –2× is selected.

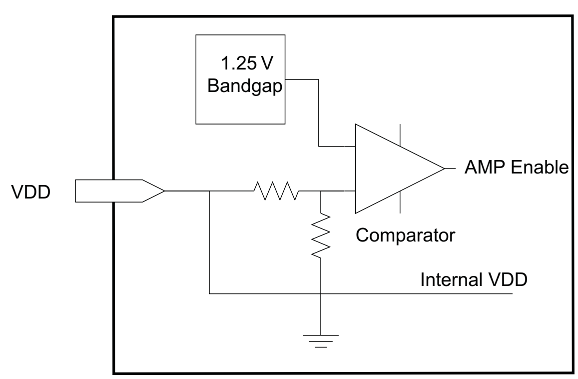
表 1. Gain Settings

Gain_set RESISTOR	GAIN	GAIN (dB)	INPUT RESISTANCE
249 kΩ(1)	–2×	6	37 kΩ
82k5	–1×	0.0	55 kΩ
51k1	–1.5×	3.5	44 kΩ
34k8	–2.3×	7.2	33 kΩ
27k4	–2.5×	8	31 kΩ
20k5	–3×	9.5	28 kΩ
15k4	–3.5×	10.9	24 kΩ
11k5	–4.0×	12	22 kΩ
9k09	–5×	14	18 kΩ
7k5	–5.6×	15	17 kΩ
6k19	–6.4×	16.1	15 kΩ
5k11	–8.3×	18.4	12 kΩ
4k22	–10×	20	10 kΩ

(1) or higher

Internal Undervoltage Detection

The DRV612 contains an internal precision band-gap reference voltage and a comparator used to monitor the supply voltage, VDD. The internal VDD monitor is set at 2.8 V with 200-mV hysteresis.



Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the DRV612. These capacitors block the dc portion of the audio source and allow the DRV612 inputs to be properly biased to provide maximum performance. The input blocking capacitors also limit the dc gain to 1, limiting the dc-offset voltage at the output.

These capacitors form a high-pass filter with the input resistor, R_{IN}. The cutoff frequency is calculated using 公式 1. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input resistor chosen from 表 2. Then the frequency and/or capacitance can be determined when one of the two values is given.

$$fc_{IN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{or} \quad C_{IN} = \frac{1}{2\pi fc_{IN} R_{IN}} \tag{1}$$

For a fixed cutoff frequency of 2 Hz, the size of the input capacitance is shown in 表 2 with the capacitors rounded up to nearest E6 values. For 20-Hz cutoff, simply divide the capacitor values with 10; e.g., for 1× gain, 150 nF is needed.

表 2. Input Capacitor for Different Gain and Cutoff

Gain_set RESISTOR	GAIN	Gain (dB)	INPUT RESISTANCE	2 Hz Cutoff
249 kΩ	–2 ×	6	37 kΩ	2.2 µF
82k5	–1 ×	0.0	55 kΩ	1.5 µF
51k1	–1.5×	3.5	44 kΩ	2.2 µF
34k8	–2.3×	7.2	33 kΩ	3.3 µF
27k4	–2.5×	8	31 kΩ	3.3 µF
20k5	–3×	9.5	28 kΩ	3.3 µF
15k4	–3.5×	10.9	24 kΩ	3.3 µF
11k5	–4×	12	22 kΩ	4.7 µF
9k09	–5×	14	18 kΩ	4.7 µF
7k5	–5.6×	15	17 kΩ	4.7 µF
6k19	–6.4×	16.1	15 kΩ	6.8 µF
5k11	–8.3×	18.4	12 kΩ	6.8 µF
4k22	–10×	20	10 kΩ	10 µF

Pop-Free Power Up

Pop-free power up is ensured by keeping the $\overline{\text{MUTE}}$ pin low during power-supply ramp-up and -down. The pins should be kept low until the input ac-coupling capacitors are fully charged before asserting the $\overline{\text{MUTE}}$ pin high, this way proper pre-charge of the ac-coupling is performed and pop-less power up is achieved. 图 9 illustrates the preferred sequence.

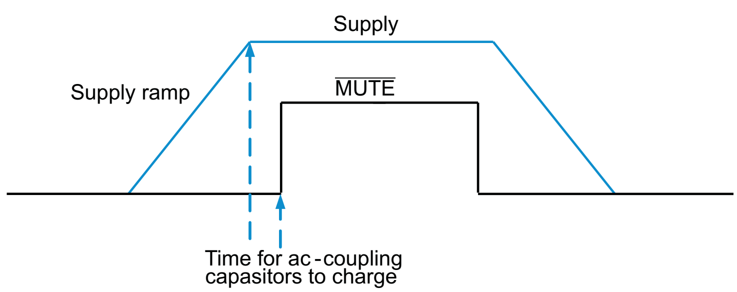


图 9. Power-Up/Down Sequence

CAPACITIVE LOAD

The DRV612 has the ability to drive a high capacitive load up to 220 pF directly. Higher capacitive loads can be accepted by adding a series resistor of 47 Ω or larger for the line driver output.

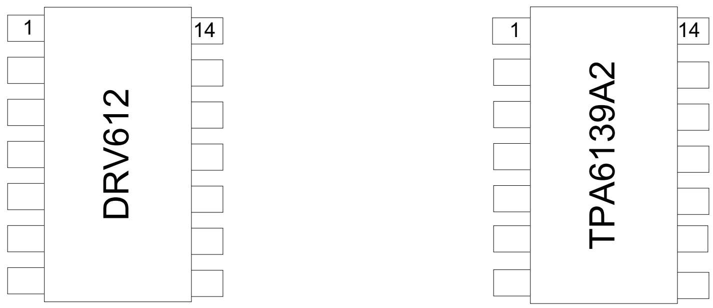
LAYOUT RECOMMENDATIONS

A proposed layout for the DRV612 can be seen in the DRV612EVM User's Guide (SLOU248), and the Gerber files can be downloaded from http://focus.ti.com/docs/toolsw/folders/print/DRV612evm.html. To access this information, open the DRV612 product folder and look in the Tools and Software folder.

Ground traces are recommended to be routed as a star ground to minimize hum interference. VDD, VSS decoupling capacitors and the charge-pump capacitors should be connected with short traces.

FOOTPRINT COMPATIBLE WITH TPA6139A2

The DRV612 stereo line driver is pin compatible with the headphone amplifier TPA6139A2. Therefore, a single PCB layout can be used with stuffing options for different board configurations.



APPLICATION CIRCUIT

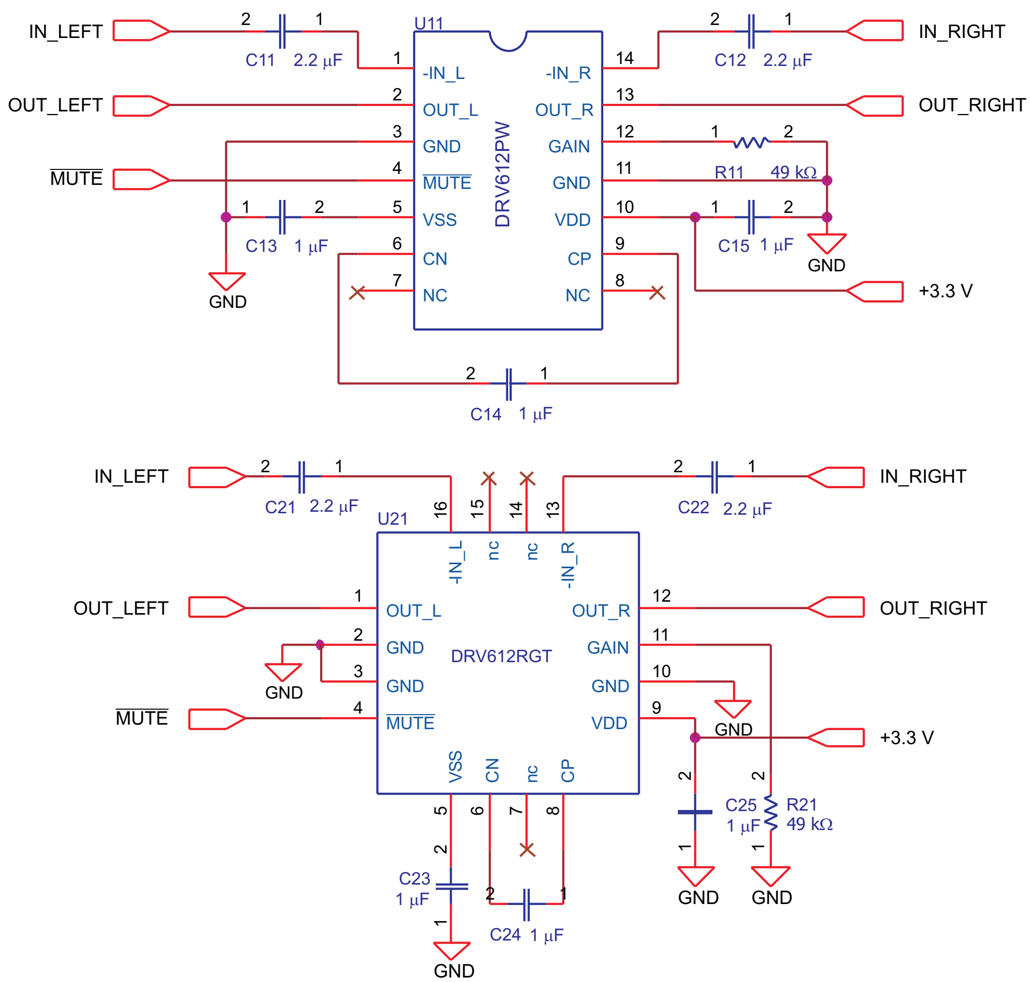


图 10. Single-Ended Input and Output, Gain Set to –1.5×

REVISION HISTORY

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV612PW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV612
DRV612PW.A	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV612
DRV612PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV612
DRV612PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV612
DRV612RGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D612
DRV612RGTR.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D612
DRV612RGTT	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D612
DRV612RGTT.A	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D612

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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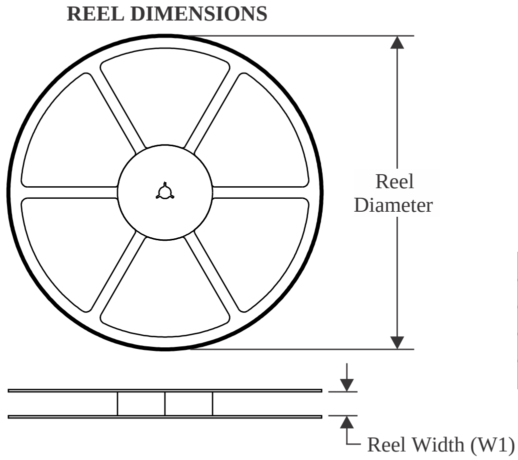
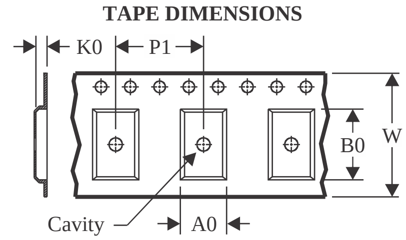
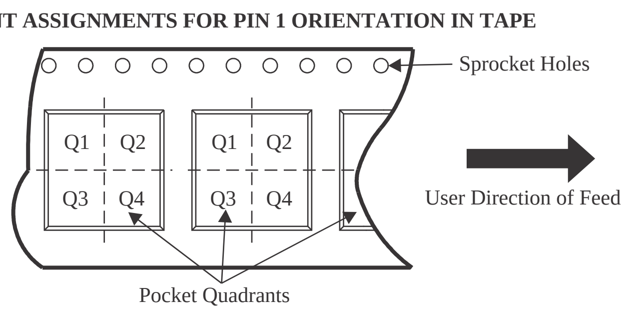
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





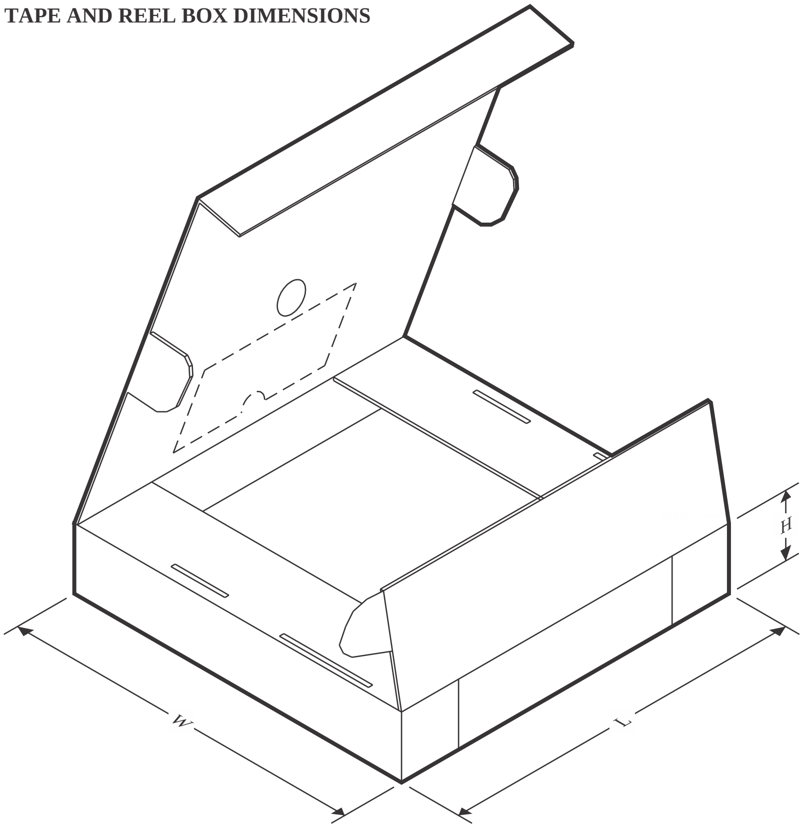
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV612PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV612RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DRV612RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DRV612RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

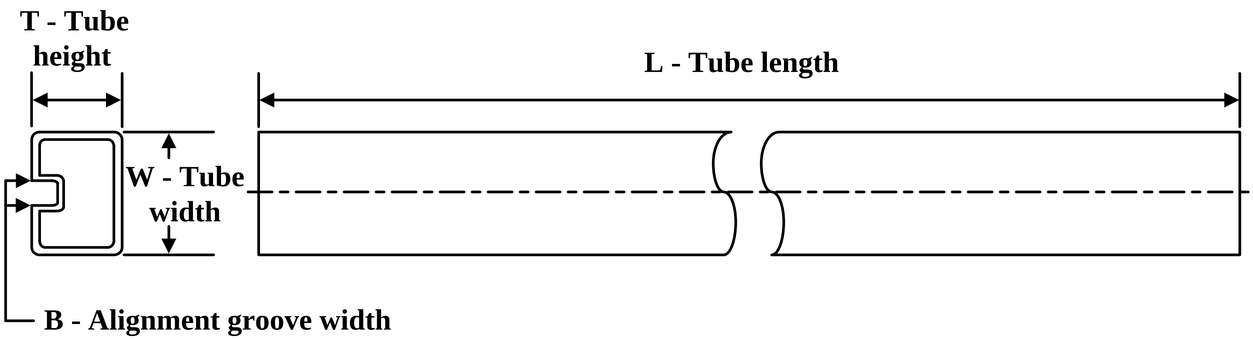
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

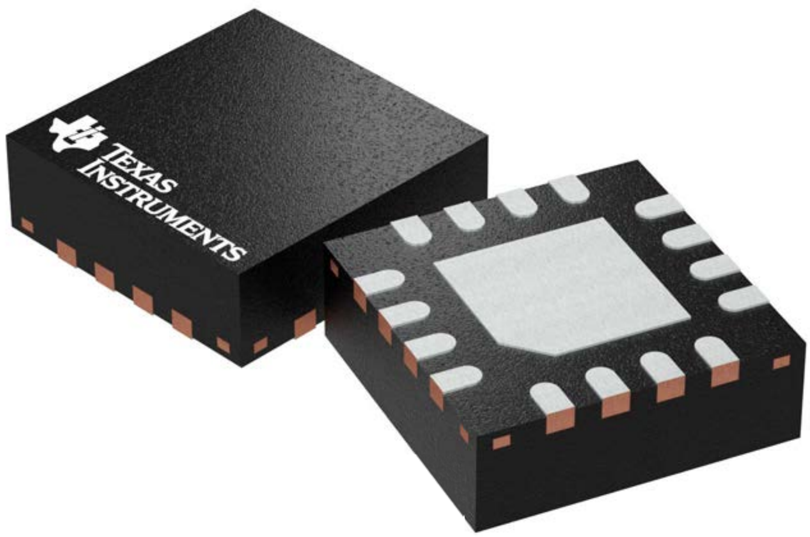
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV612PWR	TSSOP	PW	14	2000	350.0	350.0	43.0
DRV612RGTR	VQFN	RGT	16	3000	346.0	346.0	33.0
DRV612RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
DRV612RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

TUBE

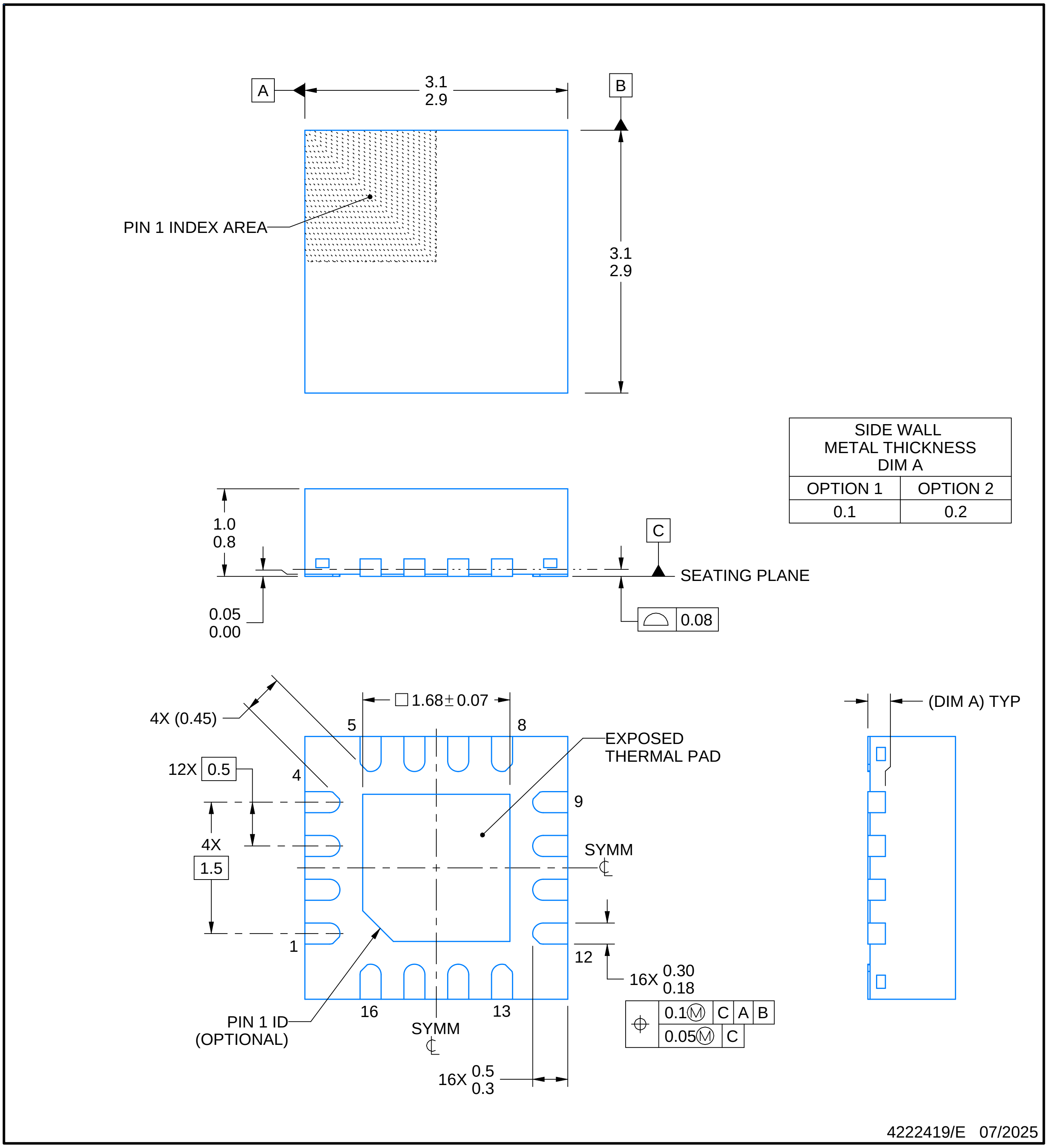


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DRV612PW	PW	TSSOP	14	90	530	10.2	3600	3.5
DRV612PW.A	PW	TSSOP	14	90	530	10.2	3600	3.5



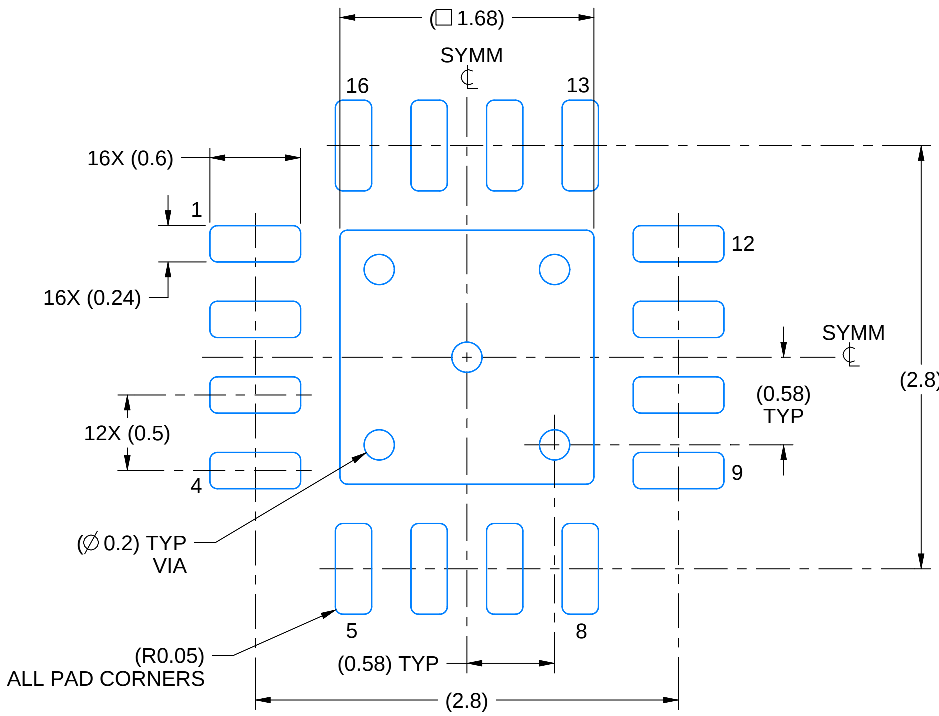
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



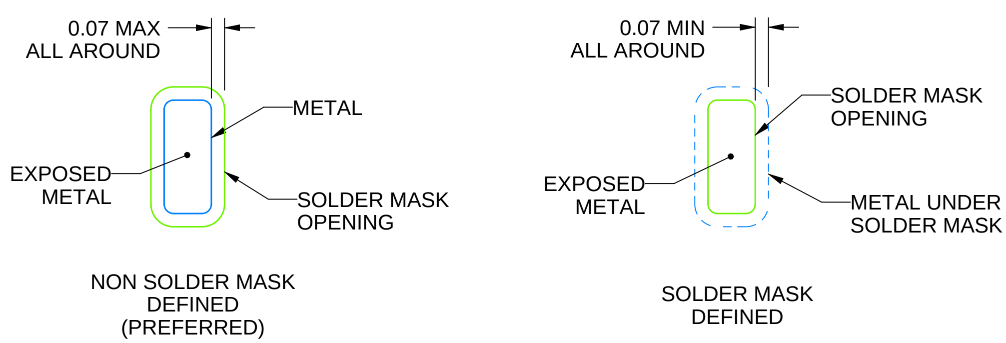
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

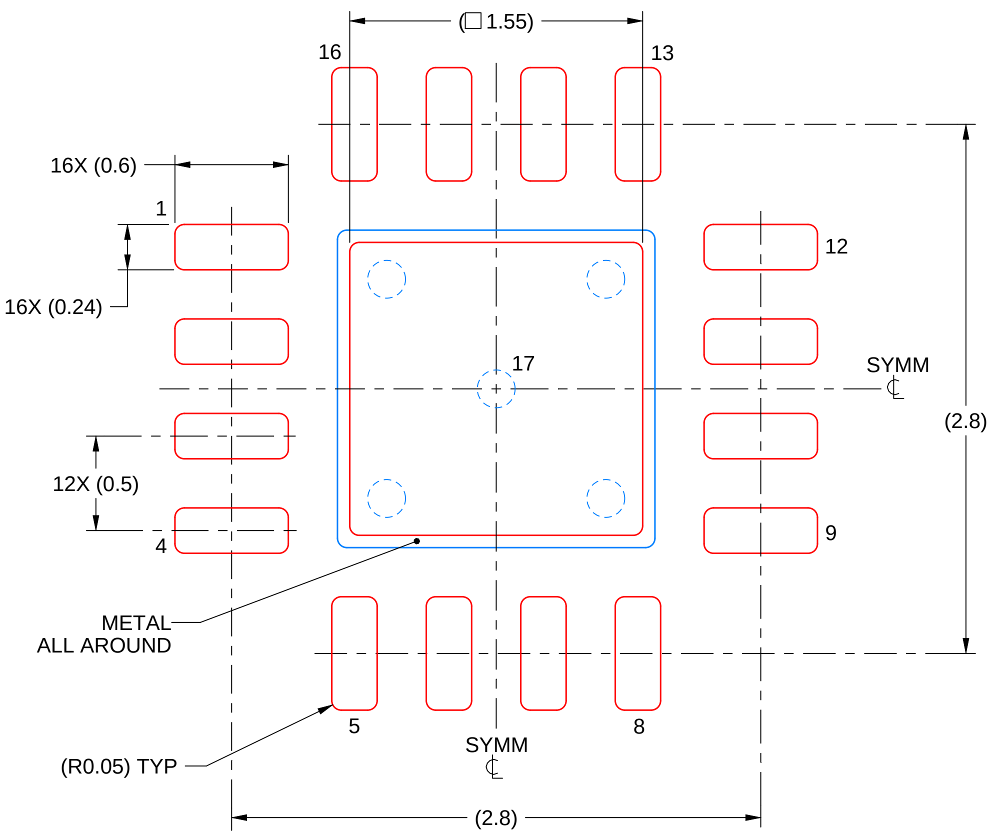


SOLDER MASK DETAILS

4222419/E 07/2025

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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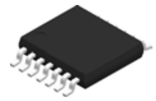
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

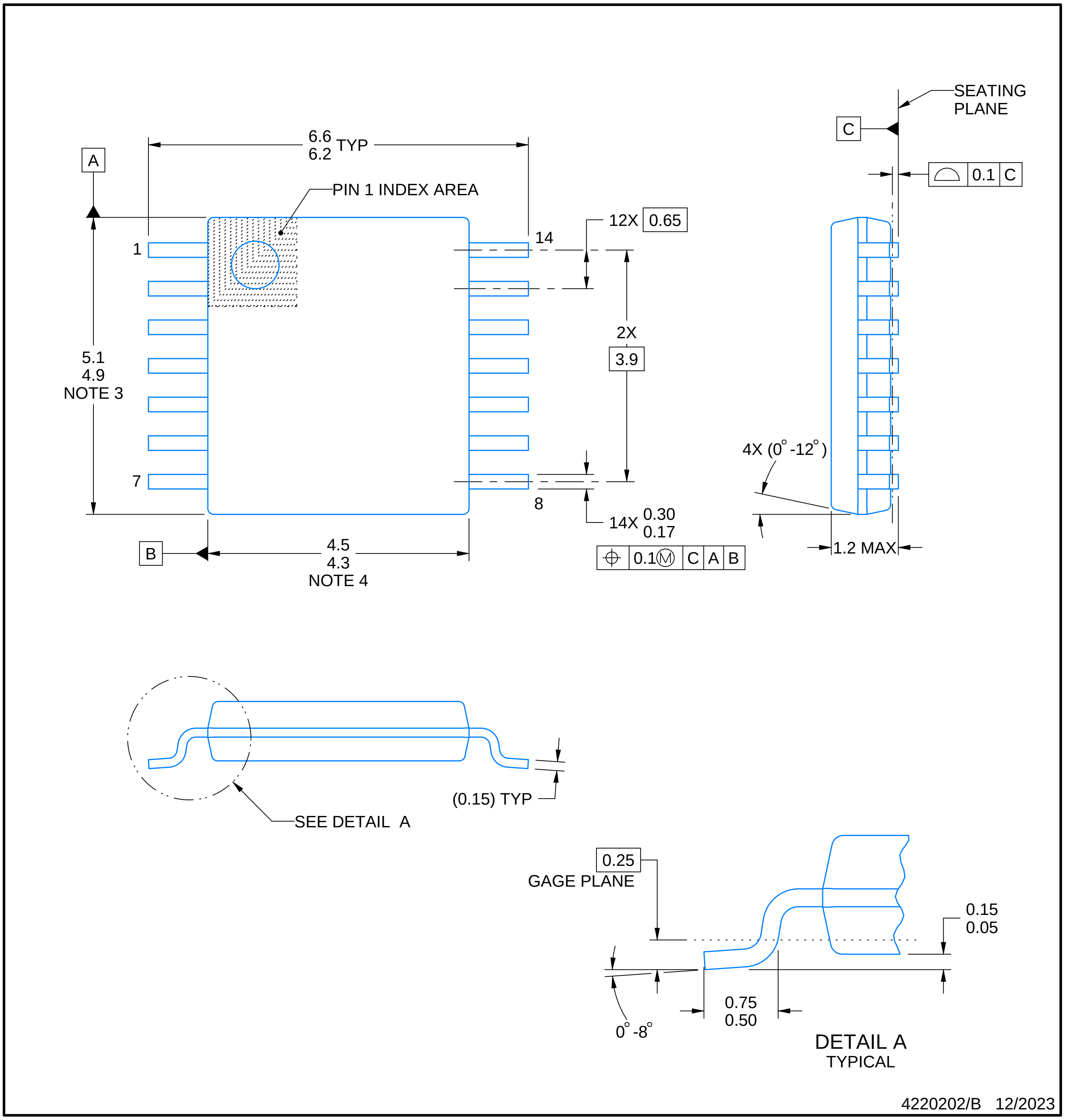


PACKAGE OUTLINE

PW0014A

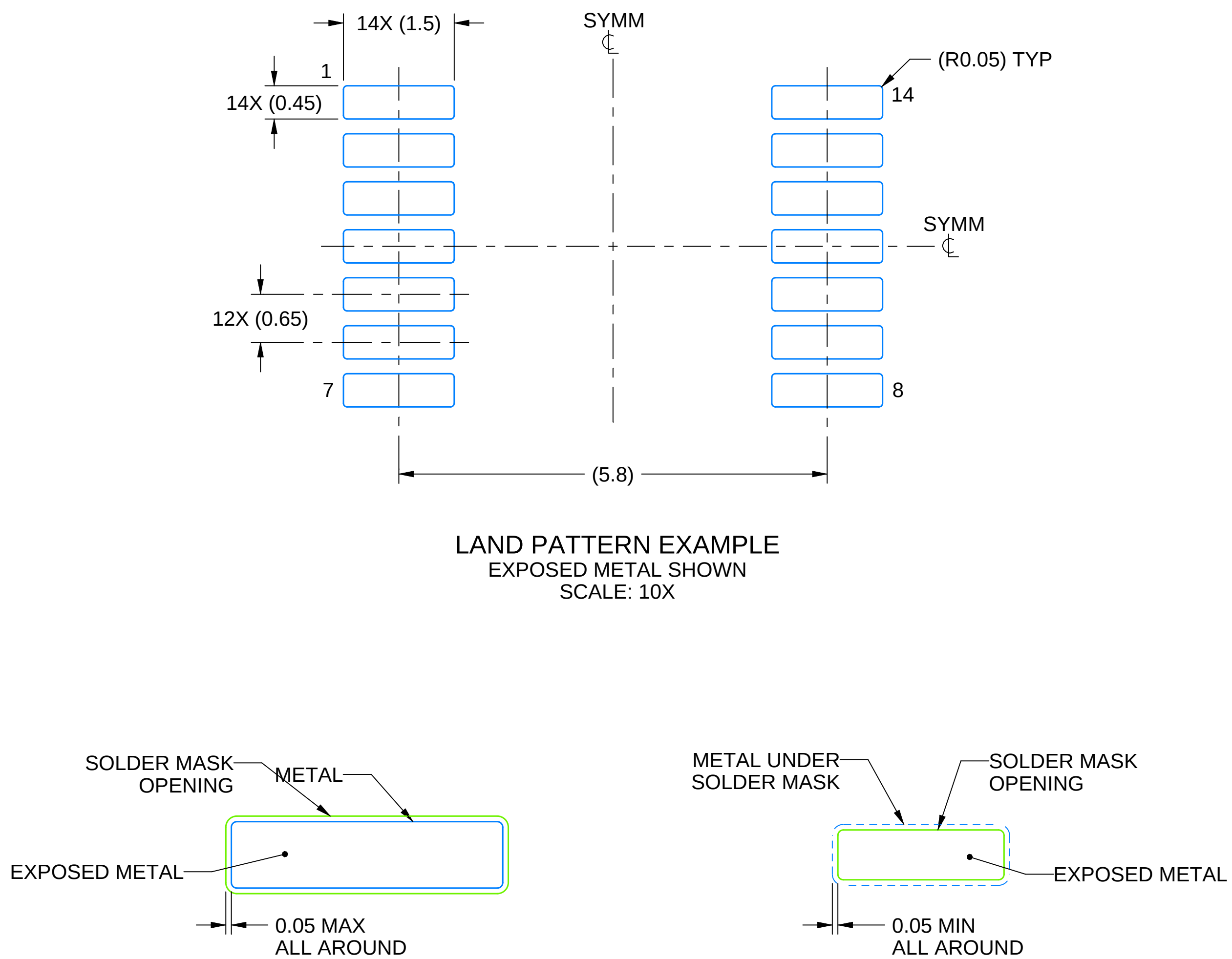
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK
DEFINED
(PREFERRED)

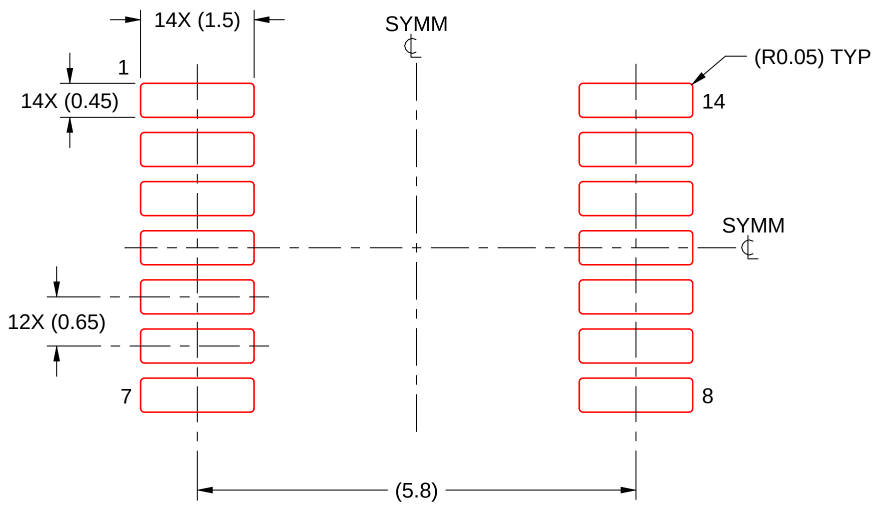
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月