DRV8305 具有分流放大器和稳压器的三相栅极驱动器

1 特性

- 4.4V 至 45V 工作电压范围
- 1.25A/1A 峰值栅极驱动器电流
- 可编程的独立高速 (HS)/低速 (LS) 转换率/斜率控制
- 支持 100% 占空比的电荷泵栅极驱动器
- 三个集成分流放大器
- 50mA 集成低压降稳压器 (LDO)（3.3V/5V 选项）
- 可控制 3 个脉宽调制 (PWM) 或 6 个 PWM 输入，频率最高可达 200kHz
- 内置用于单 PWM 情况的换向表
- 可编程死区时间
- 金属氧化物半导体场效应晶体管 (MOSFET) 击穿保护
- MOSFET 的可编程 V_{DS} 保护
- 支持电池反向保护
- 支持 3.3V/5V 数字接口
- SPI 接口
- 耐热增强型 48 引脚四方扁平无引线 (QFN) 封装 (7mm × 7mm)
- 保护特性
- VM 欠压锁定 (UVLO2)
- 逻辑欠压 (UVLO1)
- 电荷泵欠压 (CPUVL)
- 过热警告和关断
- 看门狗定时器

2 应用

- 三相无刷直流 (BLDC) 电机和永磁同步电机 (PMSM)
- 持续正压通气 (CPAP) 和泵
- 机器人和遥控 (RC) 玩具
- 电动工具
- 工业自动化

3 说明

DRV8305 是一款针对三相电机驱动应用的栅极驱动器集成电路 (IC)。 该器件提供了三个经高精度调节和温度补偿的半桥驱动器，每个驱动器能够驱动一个高侧和低侧 N 型 MOSFET。

电荷泵驱动器支持占空比为 100% 的低压操作。 该栅极驱动器还能够处理最高达 45V 的负载突降脉冲。

栅极驱动器在切换时使用自动握手，以防止发生电流击穿。 该器件可精确感测高侧和低侧 MOSFET 的 V_{DS}，以在过流状态期间保护外部 MOSFET。

DRV8305 提供三个分流放大器进行精确的电流测量，支持增益可调节的双向电流感测。

DRV8305 具有一个集成稳压器和控制器，可满足微控制器 (MCU) 或附加系统的电源要求。

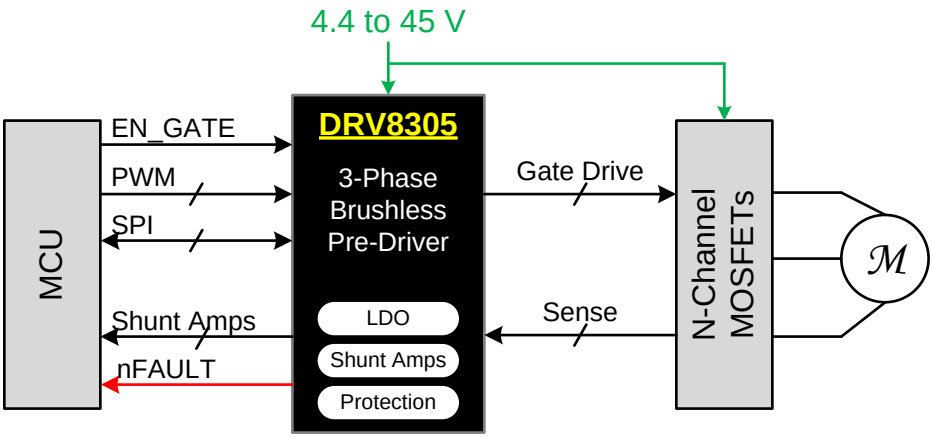
SPI 提供详细的故障报告以及灵活的参数设置，例如针对分流放大器的增益选项、栅极驱动器的转换率控制以及多种保护功能。

器件信息 (1)

部件号	封装	封装尺寸（标称值）
DRV8305	HTQFP (48)	7.00mm x 7.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



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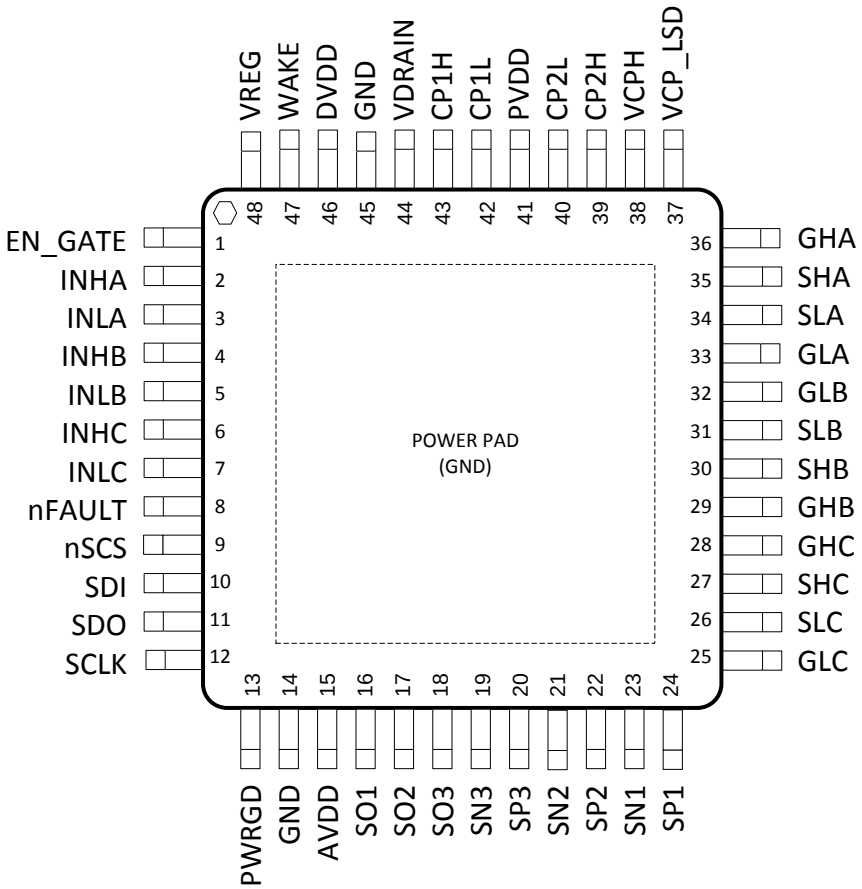
4 修订历史记录

日期	修订版本	注释
2015 年 8 月	*	首次发布。

5 Pin Configuration and Functions

PHP Package
48-Pin HTQFP
Top View



Pin Functions

PIN		I/O	DESCRIPTION	
NO.	NAME			
1	EN_GATE	I	Enable gate	Enables the gate driver and current shunt amplifiers; internal pulldown
2	INHA	I	Bridge PWM input	PWM input signal for bridge A high-side
3	INLA	I	Bridge PWM input	PWM input signal for bridge A low-side
4	INHB	I	Bridge PWM input	PWM input signal for bridge B high-side
5	INLB	I	Bridge PWM input	PWM input signal for bridge B low-side
6	INHC	I	Bridge PWM input	PWM input signal for bridge C high-side
7	INLC	I	Bridge PWM input	PWM input signal for bridge C low-side
8	nFAULT	OD	Fault indicator	When low indicates a fault has occurred; open drain; external pullup to MCU power supply needed (1 kΩ to 10 kΩ)
9	nSCS	I	SPI chip select	Select/enable for SPI; active low
10	SDI	I	SPI input	SPI input signal
11	SDO	O	SPI output	SPI output signal; referred to VREG
12	SCLK	I	SPI clock	SPI clock signal
13	PWRGD	OD	Power Good	VREG and MCU watchdog fault indication; open drain; external pullup to MCU power supply needed (1 kΩ to 10 kΩ)

Pin Functions (continued)

PIN		I/O	DESCRIPTION	
NO.	NAME			
14	GND	P	Device ground	Must be connected to ground
45				
PPAD				
15	AVDD	P	Analog regulator	5.0 V analog internal supply regulator; bypass to GND with a 6.3-V, 1-µF ceramic capacitor
16	SO1	O	Current amplifier output	Output of current sense amplifier 1
17	SO2	O	Current amplifier output	Output of current sense amplifier 2
18	SO3	O	Current amplifier output	Output of current sense amplifier 3
19	SN3	I	Current amplifier negative input	Negative input of current sense amplifier 3
20	SP3	I	Current amplifier positive input	Positive input of current sense amplifier 3
21	SN2	I	Current amplifier negative input	Negative input of current sense amplifier 2
22	SP2	I	Current amplifier positive input	Positive input of current sense amplifier 2
23	SN1	I	Current amplifier negative input	Negative input of current sense amplifier 1
24	SP1	I	Current amplifier positive input	Positive input of current sense amplifier 1
25	GLC	O	Low-side gate driver	Low-side gate driver output for half-bridge C
26	SLC	I	Low-side source connection	Low-side source connection for half-bridge C
27	SHC	I	High-side source connection	High-side source connection for half-bridge C
28	GHC	O	High-side gate driver	High-side gate driver output for half-bridge C
29	GHB	O	High-side gate driver	High-side gate driver output for half-bridge B
30	SHB	I	High-side source connection	High-side source connection for half-bridge B
31	SLB	I	Low-side source connection	Low-side source connection for half-bridge B
32	GLB	O	Low-side gate driver	Low-side gate driver output for half-bridge B
33	GLA	O	Low-side gate driver	Low-side gate driver output for half-bridge A
34	SLA	I	Low-side source connection	Low-side source connection for half-bridge A
35	SHA	I	High-side source connection	High-side source connection for half-bridge A
36	GHA	O	High-side gate driver	High-side gate driver output for half-bridge A
37	VCP_LSD	P	Low-side gate driver regulator	Internal voltage regulator for low-side gate driver; connect 1-µF capacitor to GND
38	VCPH	P	High-side gate driver regulator	Internal voltage regulator for high-side gate driver; connect 2.2-µF capacitor to PVDD
39	CP2H	P	Charge pump flying capacitor	Flying capacitor for charge pump; connect 0.047-µF capacitor between CP2H and CP2L
40	CP2L	P		

External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{PVDD}	PVDD	GND	4.7-µF ceramic capacitor rated for 50 V
C_{AVDD}	AVDD	GND	1.0-µF ceramic capacitor rated for 6.3 V
C_{DVDD}	DVDD	GND	1.0-µF ceramic capacitor rated for 6.3 V
C_{VCPH}	VCPH	PVDD	2.2-µF ceramic capacitor rated for 16 V
C_{VCP_LSD}	VCP_LSD	GND	1.0-µF ceramic capacitor rated for 16 V
C_{CP1}	CP1H	CP1L	0.047-µF ceramic capacitor rated for 16 V
C_{CP2}	CP2H	CP2L	0.047-µF ceramic capacitor rated for 16 V
C_{VREG}	VREG	GND	1.0-µF ceramic capacitor rated for 6.3 V
R_{VDRAIN}	VDRAIN	PVDD	100-Ω series resistor
R_{nFAULT}	nFAULT	VCC (1)	1 to 10 kΩ pulled up the MCU power supply

(1) VCC is not a pin on the DRV8305, but a VCC supply voltage pullup is required for open-drain output nFAULT

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range referenced with respect to GND (unless otherwise noted) (1)

	MIN	MAX	UNIT
Power supply voltage (PVDD)	–0.3	45	V
Power supply voltage ramp rate (VM)	0	2	V/µs
Charge pump voltage (CP1H,CP1L, CP2L,CP2H, VCPH, VCP_LSD)	–0.3	PVDD + 12	V
High side gate driver voltage (GHA, GHB, GHC)	–3	57	V
Low-side gate driver voltage (GHA, GHB, GHC)	–2	12	V
High side gate driver source pin voltage (SHA, SHB, SHC)	–5	45	V
Low-side gate driver source pin voltage (SLA, SLB, SLC)	–3	5	V
Internal phase clamp pin voltage difference {(GHA-SHA), (GHB-SHB), (GHC-SHC), (GLA-SLA), (GLB-SLB), (GLC-SLC)}	–0.3	15	V
Drain pin voltage drain (VDRAIN)	–0.3	45	V
Max source current (VDRAIN) – limit current with external series resistor	–20		mA
Max sink current (VDRAIN)		2	mA
Voltage difference between supply and VDRAIN (PVDD-VDRAIN)	–10	10	V
Control pin voltage range (INHA, INLA, INHB, INLB, INHC, INLC, EN_GATE, SCLK, SDI, SCS, SDO, nFAULT, PWRGD)	–0.3	5.5	V
Open drain pins skink current (nFAULT, PWRGD)		7	mA
Wake pin voltage (WAKE)	–0.3	45	V
Wake pin sink current (WAKE) – limit with external series resistor		1	mA
Sense amp voltage (SPA, SNA, SPB, SNB, SPC, SNC)	–2	5	V
Externally applied reference voltage (VREG) – when vreg_vref = 1	–0.3	5.5	V
Externally applied reference sink current (VREG) – when vreg_vref = 1		100	µA
Operating ambient temperature, T_A	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{PVDD}	Power supply voltage range	4.4	45 (1)	V
V_{PVDD}	Power supply voltage range for voltage regulator operation	4.3	45 (2)	V
$V_{PVDDRAMP}$	Power supply voltage ramp rate (PVDD = 0 to 20 V rising <3-mA pin sink current)		1	V/µs
$V_{PVDD-SH\_X}$	Total voltage drop from PVDD to SH_X pins		4.5	V
I_{SRC_VCPH}	External load on VCPH pin (current limit resistor in series to load)		10	mA
C_{O_OPA}	Maximum external capacitive load on shunt amplifier (no external resistor on output, excluding internal pin capacitance)		60	pF
I_{nFAULT}	nFAULT sink current (VnFAULT = 0.3 V)		7	mA
F_{gate}	Operating switching frequency of gate driver		200	kHz
I_{GATE}	Total average gate driver current (HS + LS) – charge pump limited		30	mA
T_A	Operating ambient temperature	-40	125	°C

(1) IC is fully functional and tested in the range 4.4 to 45 V.
(2) Subject to thermal dissipation limits.

6.4 Thermal Information

THERMAL METRIC (1)		DRV8305 PHP (HTQFP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

PVDD = 4.4 to 45 V, T_J = –40°C to 150°C, unless specified under test condition

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (PVDD, DVDD, AVDD)						
V_{PVDD}	PVDD operating voltage		4.4		45	V
		VREG (voltage regulator) operational	4.3		45	
$I_{PVDD\_Operating}$	PVDD operating supply current	EN_GATE = enabled; LDO reg = enabled at no load; outputs HiZ		15		mA
$I_{PVDD\_Standby}$	PVDD standby supply current	EN_GATE = disabled; LDO reg = enabled at no load		4	7	mA
I_{PVDD_Sleep}	PVDD sleep supply current	EN_GATE = disabled; LDO reg = disabled; ready for WAKE		60	175	µA
V_{AVDD}	Internal regulator voltage	PVDD = 5.3 to 45 V	4.85	5	5.15	V
		PVDD = 4.4 to 5.3 V	PVDD – 0.22	PVDD		
V_{DVDD}	Internal regulator voltage			3.3		V
VOLTAGE REGULATOR (VREG)						
VVREG	VREG DC output voltage	PVDD = 5.3 to 45 V	VSET – (0.03 × VSET)	VSET	VSET + (0.03 × VSET)	V
		PVDD = 4.3 to 5.3 V; 5-V regulator	PVDD – 0.4 V		PVDD	
		PVDD = 4.3 to 5.3 V; 3.3-V regulator	VSET – (0.03 × VSET)	VSET	VSET + (0.03 × VSET)	
$V_{LineReg}$	Line regulation $\Delta V_{OUT}/\Delta V_{IN}$	5.3 V ≤ V_{IN} ≤ 12 V; I_O = 1 mA		10	30	mV
$V_{LoadReg}$	Load regulation $\Delta V_{OUT}/\Delta I_{OUT}$	100 µA ≤ I_{OUT} ≤ 50 mA			30	mV
V_{do}	Dropout voltage	I_{OUT} = 100 µA; 3.3 V		0.05	0.1	V
		I_{OUT} = 50 mA; 3.3 V		0.2	0.4	
LOGIC-LEVEL INPUTS (INHA, INLA, INHB, INLB, INHC, INLC, EN_GATE, SCLK, nSCS)						
V_{IL}	Input logic low voltage		0		0.8	V
V_{IH}	Input logic high voltage		2		5	V
R_{PD}	Internal pull down resistor	To GND		100		kΩ
CONTROL OUTPUTS (nFAULT, SDO, PWRGD)						
V_{OL}	Output logic low voltage	I_O = 5 mA			0.5	V
V_{OH}	Output logic high voltage		2.4			V
I_{OH}	Output logic high leakage	V_O = 3.3 V	–1		1	µA
HIGH VOLTAGE TOLERANT LOGIC INPUT (WAKE)						
V_{IL_WAKE}	Output logic low voltage		1.1		1.41	V
V_{IH_WAKE}	Output logic high voltage		1.42		1.75	V
GATE DRIVE OUTPUT (GHA, GHB, GHC, GLA, GLB, GLC)						
V_{GHS}	High side gate driver Vgs voltage	V_{PVDD} = 8 to 45 V; I_{GATE} < 30 mA, C_{VCPH} = 2.2 µF, $C_{CP1/CP2}$ = 0.047 µF, C_{VCP_LSD} = 1 µF	9	10	10.5	V
		V_{PVDD} = 5.5 to 8 V; I_{GATE} < 6 mA, C_{VCPH} = 2.2 µF, $C_{CP1/CP2}$ = 0.047 µF, C_{VCP_LSD} = 1 µF	7.2		9	
		V_{PVDD} = 4.4 to 5.5 V; I_{GATE} < 6 mA, C_{VCPH} = 2.2 µF, $C_{CP1/CP2}$ = 0.047 µF, C_{VCP_LSD} = 1 µF	5		7.2	

Electrical Characteristics (continued)

PVDD = 4.4 to 45 V, T_J = –40°C to 150°C, unless specified under test condition

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{GLS}	Low-side gate driver Vgs voltage	V_{PVDD} = 8 to 45 V; I_{GATE} < 30 mA, C_{VCPH} = 2.2 µF, $C_{CP1/CP2}$ = 0.047 µF, C_{VCP_LSD} = 1 µF	9	10	10.5	V
		V_{PVDD} = 5.5 to 8 V; I_{GATE} < 6 mA, C_{VCPH} = 2.2 µF, $C_{CP1/CP2}$ = 0.047 µF, C_{VCP_LSD} = 1 µF	9		10.5	
		V_{PVDD} = 4.4 to 5.5 V; I_{GATE} < 6 mA, C_{VCPH} = 2.2 µF, $C_{CP1/CP2}$ = 0.047 µF, C_{VCP_LSD} = 1 µF	8		9	
PEAK CURRENT DRIVE TIMES						
t_{DRIVE}	Peak sink or source current drive time	TDRIVEP = 00; TDRIVEN = 00		220		ns
		TDRIVEP = 01; TDRIVEN = 01		440		
		TDRIVEP = 10; TDRIVEN = 10		880		
		TDRIVEP = 11; TDRIVEN = 11		1660		
HIGH SIDE (GHA, GHB, GHC) PEAK CURRENT GATE DRIVE						
I_{DRIVEP_HS}	High side peak source current	IDRIVEP_HS = 0000		0.01		A
		IDRIVEP_HS = 0001		0.02		
		IDRIVEP_HS = 0010		0.03		
		IDRIVEP_HS = 0011		0.04		
		IDRIVEP_HS = 0100		0.05		
		IDRIVEP_HS = 0101		0.06		
		IDRIVEP_HS = 0110		0.07		
		IDRIVEP_HS = 0111		0.125		
		IDRIVEP_HS = 1000		0.25		
		IDRIVEP_HS = 1001		0.5		
		IDRIVEP_HS = 1010		0.75		
		IDRIVEP_HS = 1011		1		
		IDRIVEP_HS = 1100, 1101, 1110, 1111		0.05		
I_{DRIVEN_HS}	High side peak sink current	IDRIVEN_HS = 0000		0.02		A
		IDRIVEN_HS = 0001		0.03		
		IDRIVEN_HS = 0010		0.04		
		IDRIVEN_HS = 0011		0.05		
		IDRIVEN_HS = 0100		0.06		
		IDRIVEN_HS = 0101		0.07		
		IDRIVEN_HS = 0110		0.08		
		IDRIVEN_HS = 0111		0.25		
		IDRIVEN_HS = 1000		0.5		
		IDRIVEN_HS = 1001		0.75		
		IDRIVEN_HS = 1010		1		
		IDRIVEN_HS = 1011		1.25		
		IDRIVEN_HS = 1100, 1101, 1110, 1111		0.06		

Electrical Characteristics (continued)

PVDD = 4.4 to 45 V, T_J = –40°C to 150°C, unless specified under test condition

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOW SIDE (GLA, GLB, GLC) PEAK CURRENT GATE DRIVE						
I_{DRIVEP_LS}	Low-side peak source current	IDRIVEP_HS = 0000		0.01		A
		IDRIVEP_HS = 0001		0.02		
		IDRIVEP_HS = 0010		0.03		
		IDRIVEP_HS = 0011		0.04		
		IDRIVEP_HS = 0100		0.05		
		IDRIVEP_HS = 0101		0.06		
		IDRIVEP_HS = 0110		0.07		
		IDRIVEP_HS = 0111		0.125		
		IDRIVEP_HS = 1000		0.25		
		IDRIVEP_HS = 1001		0.5		
		IDRIVEP_HS = 1010		0.75		
		IDRIVEP_HS = 1011		1		
		IDRIVEP_HS = 1100, 1101, 1110, 1111		0.05		
LOW SIDE (GLA, GLB, GLC) PEAK CURRENT GATE DRIVE						
I_{DRIVEN_LS}	Low-side peak sink current	IDRIVEN_HS = 0000		0.02		A
		IDRIVEN_HS = 0001		0.03		
		IDRIVEN_HS = 0010		0.04		
		IDRIVEN_HS = 0011		0.05		
		IDRIVEN_HS = 0100		0.06		
		IDRIVEN_HS = 0101		0.07		
		IDRIVEN_HS = 0110		0.08		
		IDRIVEN_HS = 0111		0.25		
		IDRIVEN_HS = 1000		0.5		
		IDRIVEN_HS = 1001		0.75		
		IDRIVEN_HS = 1010		1		
		IDRIVEN_HS = 1011		1.25		
		IDRIVEN_HS = 1100, 1101, 1110, 1111		0.06		
GATE PULL DOWN, MOTOR OFF STATE (BRIDGE IN HI-Z)						
R_{SLEEP_PD}	Gate pull down resistance, SLEEP, under voltage and sleep mode	2 V < PVDD < PVDD_UVLO2 GHX to GND; GLX to GND		2000		Ω
$R_{STANDBY\_PD}$	Gate pull down resistance, STANDBY, standby mode (Parallel with $I_{STANDBY\_PD}$)	PVDD > PVDD_UVLO2; EN_GATE = low; GHX to GND; GLX to GND		750		Ω
$I_{OPERATING\_PD}$	Gate pull down current, OPERATING, operating mode	PVDD > PVDD_UVLO2; EN_GATE = high; GHX to SHX; GLX to SLX		50		mA
GATE PULL DOWN, MOTOR ON STATE (IDRIVE/tdrive)						
I_{HOLD}	Gate pull down current, holding	PVDD > PVDD_UVLO2; EN_GATE = high; GHX to SHX; GLX to SLX		50		mA
$I_{PULLDOWN}$	Gate pull down current, strong	PVDD > PVDD_UVLO2; EN_GATE = high; GHX to SHX; GLX to SLX		1.25		A

Electrical Characteristics (continued)

PVDD = 4.4 to 45 V, T_J = –40°C to 150°C, unless specified under test condition

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE TIMING						
t_{pd_lf-O}	Positive input falling to GHS_x falling	PVDD = 12 V; CL = 1 nF; 50% to 50%		200		ns
t_{pd_lr-O}	Positive input rising to GHS_x rising	PVDD = 12 V; CL = 1 nF; 50% to 50%		200		ns
t_{d_min}	Minimum dead time after hand shaking			280		ns
t_{dtp}	Dead time in addition to t_{d_min}	DEAD_TIME = 000		35		ns
		DEAD_TIME = 001		52		
		DEAD_TIME = 010		88		
		DEAD_TIME = 011		440		
		DEAD_TIME = 100		880		
		DEAD_TIME = 101		1760		
		DEAD_TIME = 110		3520		
		DEAD_TIME = 111		5280		
t_{PD_MATCH}	Propagation delay matching between high-side and low-side			50		ns
t_{DT_MATCH}	Dead time matching			50		ns
CURRENT SHUNT AMPLIFIER						
G_{CSA}	Current sense amplifier gain	GAIN_CSx = 00		10		V/V
		GAIN_CSx = 01		20		
		GAIN_CSx = 10		40		
		GAIN_CSx = 11		80		
G_{ERR}	Current sense amplifier gain error	Input differential > 0.025 V	–3%		3%	
$t_{SETTLING}$	Current sense amplifier settling time	Settling time to 1%; no blanking; T_J = -40 – 150°C, G_{CSA} = 10; Vstep = 0.46 V		300		ns
		Settling time to 1%; no blanking; T_J = -40 – 150°C, G_{CSA} = 20; Vstep = 0.46 V		600		
		Settling time to 1%; no blanking; T_J = -40 – 150°C, G_{CSA} = 40; Vstep = 0.46 V		1.2		µs
		Settling time to 1%; no blanking; T_J = -40 – 150°C, G_{CSA} = 80; Vstep = 0.46 V		2.4		
V_{IOS}	DC input offset	G_{CSA} = 10; input shorted; RTI	–4		4	mV
V_{VREF_ERR}	Reference buffer error (DC)	Internal or external VREF	–2%		2%	
$V_{DRIFTOS}$	Input offset error drift	G_{CSA} = 10; input shorted; RTI		10		µV/C
I_{BIAS}	Input bias current	VIN_COM = 0; SOx open			100	µA
I_{OFFSET}	Input bias current offset	IBIAS (SNx-SPx); VIN_COM = 0; SOx open		1		µA
V_{IN_COM}	Common input mode range		–0.15		0.15	V
V_{IN_DIFF}	Differential input range		-0.48		0.48	V
CMRR	Common mode rejection ration	External input resistance matched; DC; GCSA = 10	60	80		dB
		External input resistance matched; 20 kHz; GCSA = 10	60	80		
PSRR	Power supply rejection ratio	DC (<120 Hz); GCSA = 10		150		dB
		20 kHz; GCSA = 10		90		
V_{SWING}	Output voltage swing	PVDD > 5.3 V	0.3		4.7	V
V_{SLEW}	Output slew rate	GCSA = 10; R_L = 0 Ω; CL = 60 pF	5.2	10		V/µs

Electrical Characteristics (continued)

PVDD = 4.4 to 45 V, T_J = –40°C to 150°C, unless specified under test condition

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VO}	Output short circuit current	SOx shorted to ground		20		mA
UGB	Unity gain bandwidth product	GCSA = 10		2		MHz
VOLTAGE PROTECTION						
V_{AVDD_UVLO}	AVDD undervoltage Fault	Relative to GND	3.3		3.5	V
V_{VREG_UV}	VREG undervoltage Fault	VREG_UV_LEVEL = 00			VSET-10%	V
		VREG_UV_LEVEL = 01			VSET-20%	
		VREG_UV_LEVEL = 10			VSET-30%	
		VREG_UV_LEVEL = 11			VSET-30%	
$V_{VREG\_UV\_DGL}$	VREG undervoltage monitor deglitch time		1.5		2	µs
V_{PVDD_UVFL}	Undervoltage protection Warning, PVDD	PVDD falling	7.7		8.1	V
		PVDD rising	7.9		8.3	
V_{PVDD_UVLO1}	Undervoltage protection lockout, PVDD	PVDD falling			4.1	V
		PVDD rising			4.3	
V_{PVDD_UVLO2}	Undervoltage protection Fault, PVDD	PVDD falling	4.2		4.4	V
		PVDD rising	4.4		4.6	
V_{PVDD_OVFL}	Overvoltage protection Warning, PVDD	PVDD falling	33.5		36	V
		PVDD rising	32.5		35	
V_{VCPH_UVFL}	Charge pump under voltage protection Warning, VCPH	Relative to PVDD			8	V
V_{VCPH_UVLO}	Charge pump under voltage protection Fault, VCPH	Relative to PVDD, SET_VCPH_UV = 0	4.5		4.9	V
		Relative to PVDD, SET_VCPH_UV = 1	4.2		4.6	
$V_{VCP\_LSD\_UVLO}$	Low-side charge pump under voltage Fault, VCP_LSD	Relative to PVDD	6.4		7.5	V
V_{VCPH_OVLO}	Charge pump over voltage protection FAULT, VCPH	Relative to PVDD	14		18	V
$V_{VCPH\_OVLO\_ABS}$	Charge pump over voltage protection FAULT, VCPH	Relative to GND		60		V
TEMPERATURE PROTECTION						
OTW_CLR	Junction temperature for resetting over temperature (OT) warning(1)			140		°C
OTW_SET/ OTSD_CLR	Junction temperature for over temperature warning and resetting over temperature shutdown(1)			155		°C
OTSD_SET	Junction temperature for over temperature shutdown(1)			175		°C
$TEMP_{FLAG1}$	Junction temperature flag setting 1 (no warning)(1)			105		°C
$TEMP_{FLAG2}$	Junction temperature flag setting 2 (no warning)(1)			125		°C
$TEMP_{FLAG3}$	Junction temperature flag setting 3 (no warning)(1)			135		°C
$TEMP_{FLAG4}$	Junction temperature flag setting 4 (no warning)(1)			175		°C

(1) Specified by design and characterization data

Electrical Characteristics (continued)

PVDD = 4.4 to 45 V, T_J = –40°C to 150°C, unless specified under test condition

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION CONTROL						
$t_{pd,E-L}$	Delay, error event to all gates low			24		µs
$t_{pd,E-SD}$	Delay, error event to nFAULTx low			7		µs
FET CURRENT PROTECTION (VDS SENSING)						
V_{DS_TRIP}	Drain-source voltage protection limit	VDS_LEVEL = 00000		0.06		V
		VDS_LEVEL = 00001		0.068		
		VDS_LEVEL = 00010		0.076		
		VDS_LEVEL = 00011		0.086		
		VDS_LEVEL = 00100		0.097		
		VDS_LEVEL = 00101		0.109		
		VDS_LEVEL = 00110		0.123		
		VDS_LEVEL = 00111		0.138		
		VDS_LEVEL = 01000		0.155		
		VDS_LEVEL = 01001		0.175		
		VDS_LEVEL = 01010		0.197		
		VDS_LEVEL = 01011		0.222		
		VDS_LEVEL = 01100		0.25		
		VDS_LEVEL = 01101		0.282		
		VDS_LEVEL = 01110		0.317		
		VDS_LEVEL = 01111		0.358		
		VDS_LEVEL = 10000		0.403		
		VDS_LEVEL = 10001		0.454		
		VDS_LEVEL = 10010		0.511		
		VDS_LEVEL = 10011		0.576		
		VDS_LEVEL = 10100		0.648		
		VDS_LEVEL = 10101		0.73		
		VDS_LEVEL = 10110		0.822		
		VDS_LEVEL = 10111		0.926		
		VDS_LEVEL = 11000		1.043		
		VDS_LEVEL = 11001		1.175		
		VDS_LEVEL = 11010		1.324		
		VDS_LEVEL = 11011		1.491		
		VDS_LEVEL = 11100		1.679		
		VDS_LEVEL = 11101		1.892		
		VDS_LEVEL = 11110		2.131		
		VDS_LEVEL = 11111		2.131		
t_{VDS}	VDS sense deglitch time	TVDS = 00		0		µs
		TVDS = 01		1.75		
		TVDS = 10		3.5		
		TVDS = 11		7		
t_{BLANK}	VDS sense blanking time	TBLANK = 00		0		µs
		TBLANK = 01		1.75		
		TBLANK = 10		3.5		
		TBLANK = 11		7		

Electrical Characteristics (continued)

PVDD = 4.4 to 45 V, T_J = –40°C to 150°C, unless specified under test condition

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{VDS_PULSE}	nFAULT pin reporting pulse stretch length for V_{DS} event			56		µs
PHASE SHORT PROTECTION						
V_{SNSOCP_TRIP}	Phase short protection limit	Fixed voltage		2		V

6.6 SPI Timing Requirements (Slave Mode Only)

			MIN	NOM	MAX	UNIT
t_{SPI_READY}	SPI read after power on	PVDD > V_{PVDD_UVLO1}		5	10	ms
t_{CLK}	Minimum SPI clock period		100			ns
t_{CLKH}	Clock high time		40			ns
t_{CLKL}	Clock low time		40			ns
t_{SU_SDI}	SDI input data setup time		20			ns
t_{HD_SDI}	SDI input data hold time		30			ns
t_{D_SDO}	SDO output data delay time, CLK high to SDO valid	C_L = 20 pF			20	ns
t_{HD_SDO}	SDO output hold time		40			ns
t_{SU_SCS}	SCS setup time		50			ns
t_{HD_SCS}	SCS hold time		50			ns
t_{HI_SCS}	SCS minimum high time before SCS active low		400			ns
tACC	SCS access time, SCS low to SDO out of high impedance			10		ns
t_{DIS}	SCS disable time, SCS high to SDO high impedance			10		ns

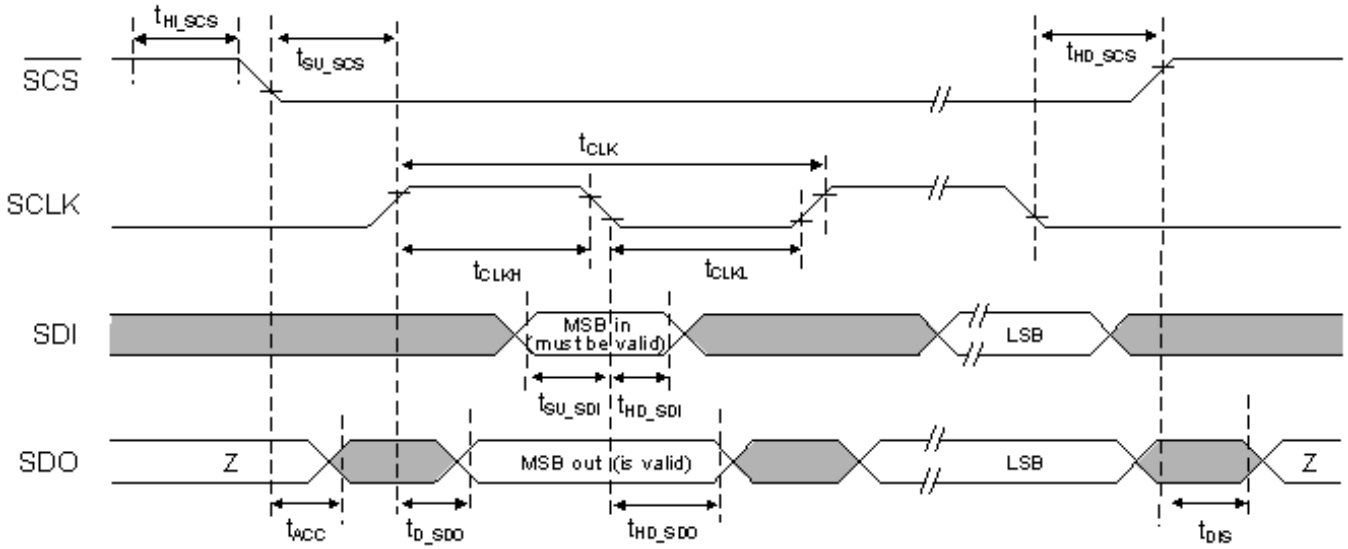


Figure 1. SPI Slave Mode Timing Definition

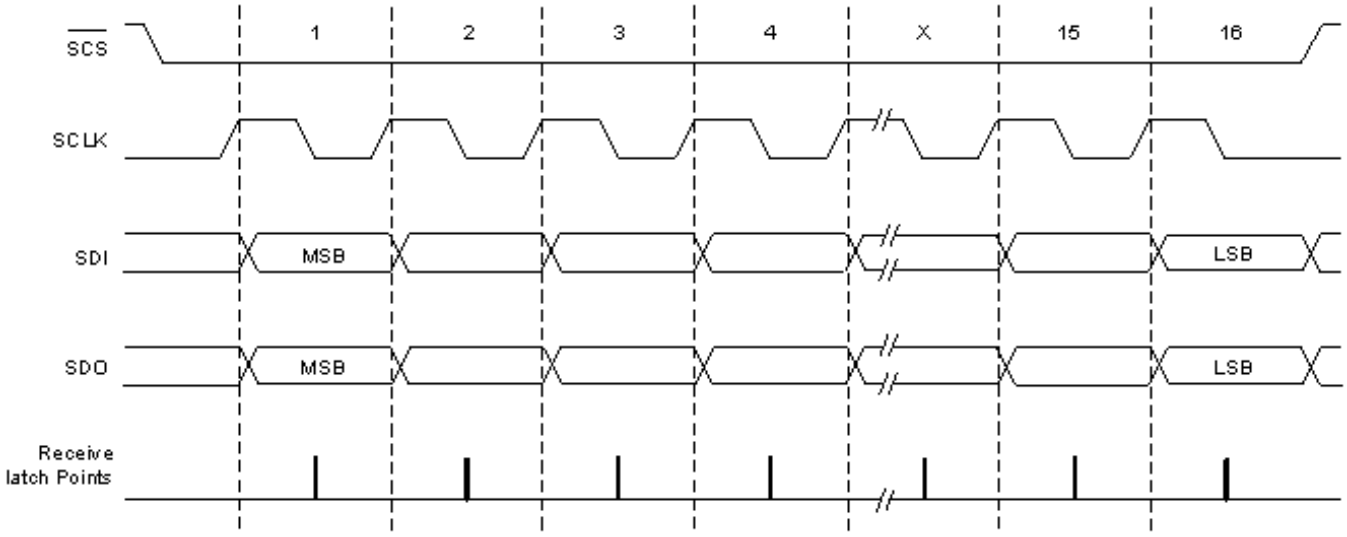


Figure 2. SPI Slave Mode Timing Diagram

6.7 Typical Characteristics

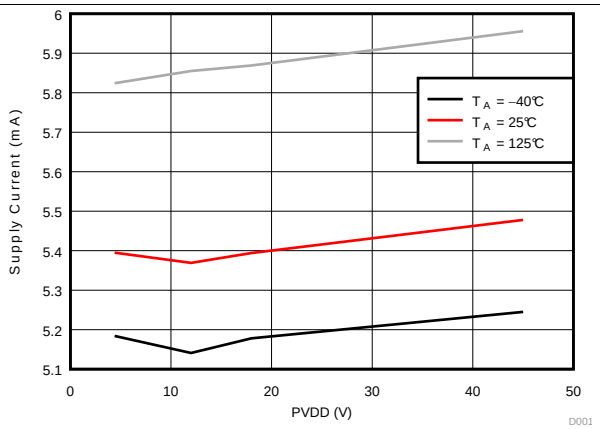


Figure 3. Standby Current

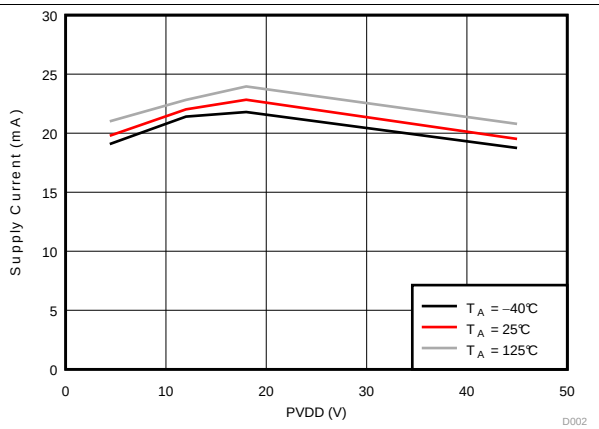


Figure 4. Operating Current

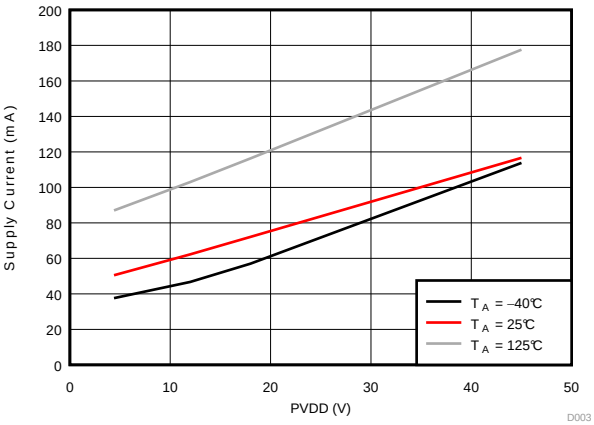


Figure 5. Sleep Current

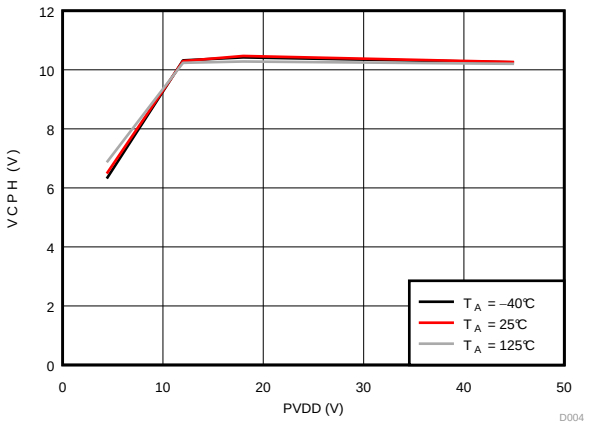


Figure 6. VCPH Voltage

7 Detailed Description

7.1 Overview

The DRV8305 is a 4.4-V to 45-V gate driver IC for three-phase motor driver applications. This device reduces external component count by integrating three half-bridge drivers, three current shunt amplifiers, and a LDO. The DRV8305 provides overcurrent, overtemperature, and undervoltage protection. Fault conditions are indicated by the nFAULT pin and specific fault indication can be read back from the SPI registers.

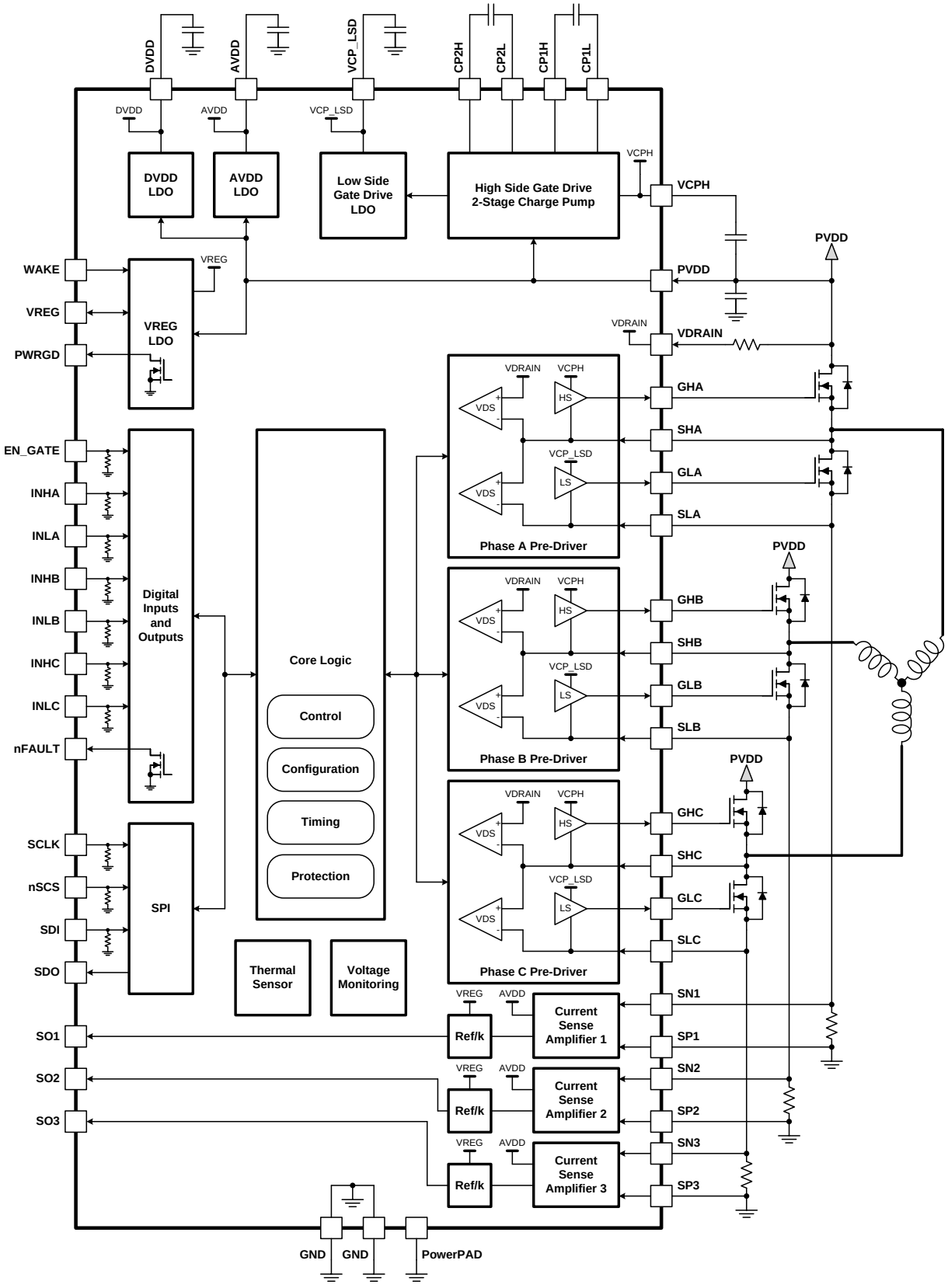
Adjustable dead time control and peak gate drive current allows for finely tuning the switching of the external MOSFETs. Internal hand-shaking is used to prevent FET shoot through.

V_{DS} sensing of the external MOSFETs allows for the DRV8305 to detect overcurrent conditions and respond appropriately. Individual MOSFET overcurrent conditions are reported through the SPI status registers.

There are three versions of DRV8305 with separate part numbers:

- DRV8305N – VREG pin is used as input that supplies the reference for the CSA and SPI.
- DRV83053 – VREG is a 3.3-V LDO output pin.
- DRV83055 – VREG is a 5.0-V LDO output pin.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Three-Phase Gate Driver

The DRV8305 provides three half-bridge drivers, each driver is capable of driving two N-type MOSFETs, one for the high side and one for the low side.

Both the high side (GHX to SHX) and the low side (GLX to SLX) are implemented as floating gate drivers.

The gate driver uses a charge pump architecture which enables an extended voltage operating range to support a variety of application requirements.

7.3.2 Operating Modes

The DRV8305 can be operated in three modes, to support various commutation schemes.

- Table 1 shows six independent PWM inputs with the truth table.

Table 1. 6-PWM Truth Table

INHX	INLX	GHX	GLX
1	1	L	L
1	0	H	L
0	1	L	H
0	0	L	L

- Three independent high-side PWM inputs (low-side complimentary PWMs generated internally).
  In this mode all activity on INLA, INLB and INLC is ignored.

Table 2. 3-PWM Truth Table

INHX	INLX	GHX	GLX
1	X	H	L
0	X	L	H

- One single PWM that uses internally stored 6-step block commutation tables. In this mode of operation, DRV8305 can be operated using a single PWM sourced from a low cost microcontroller. The PWM is applied on pin PWM_IN (INHA) from the microcontroller along with three GPIO pins PHC_0 (INLA), PHC_1 (INHB), PHC_2 (INLB) that serve to set the bits of a three bit register. The PWM may be operated from 0-100% duty cycle. The three bit register is used to select the state of each of the phases for a total of eight states including an align and stop state. The 1-PWM mode tables will use all the applicable settings from the control registers as set up by the user.
  An additional and optional GPIO (INHC) can be used to facilitate the insertion of *dwell states* or *phase current overlap* states between the six commutation steps. This may be used to reduce acoustic noise and improve motion through the reduction of abrupt current direction changes when switching between states. INHC must be high when the states are changed and the dwell state will exist until INHC is taken low. If the dwell states are not being used, the INHC pin can be simply tied low.
  In this mode all activity on INLC is always ignored.
  The commutation tables (Table 3 and Table 4) may be selected through the appropriate SPI register.

Table 3. 1-PWM Active Freewheeling

	INLA : INHB : INLB : INHC	AH	AL	BH	BL	CH	CL
AB	0110	PWM	!PWM	LOW	HIGH	LOW	LOW
AB_CB	0101	PWM	!PWM	LOW	HIGH	PWM	!PWM
CB	0100	LOW	LOW	LOW	HIGH	PWM	!PWM
CB_CA	1101	LOW	HIGH	LOW	HIGH	PWM	!PWM
CA	1100	LOW	HIGH	LOW	LOW	PWM	!PWM
CA_BA	1001	LOW	HIGH	PWM	!PWM	PWM	!PWM
BA	1000	LOW	HIGH	PWM	!PWM	LOW	LOW
BA_BC	1011	LOW	HIGH	PWM	!PWM	LOW	HIGH
BC	1010	LOW	LOW	PWM	!PWM	LOW	HIGH
BC_AC	0011	PWM	!PWM	PWM	!PWM	LOW	HIGH
AC	0010	PWM	!PWM	LOW	LOW	LOW	HIGH
AC_AB	0111	PWM	!PWM	LOW	HIGH	LOW	HIGH
Align	1110	PWM	!PWM	LOW	HIGH	LOW	HIGH
Stop	0000	LOW	LOW	LOW	LOW	LOW	LOW

Table 4. 1-PWM Diode Freewheeling

	INLA : INHB : INLB : INHC	AH	AL	BH	BL	CH	CL
AB	0110	PWM	LOW	LOW	HIGH	LOW	LOW
AB_CB	0101	PWM	LOW	LOW	HIGH	PWM	LOW
CB	0100	LOW	LOW	LOW	HIGH	PWM	LOW
CB_CA	1101	LOW	HIGH	LOW	HIGH	PWM	LOW
CA	1100	LOW	HIGH	LOW	LOW	PWM	LOW
CA_BA	1001	LOW	HIGH	PWM	LOW	PWM	LOW
BA	1000	LOW	HIGH	PWM	LOW	LOW	LOW
BA_BC	1011	LOW	HIGH	PWM	LOW	LOW	HIGH
BC	1010	LOW	LOW	PWM	LOW	LOW	HIGH
BC_AC	0011	PWM	LOW	PWM	LOW	LOW	HIGH
AC	0010	PWM	LOW	LOW	LOW	LOW	HIGH
AC_AB	0111	PWM	LOW	LOW	HIGH	LOW	HIGH
Align	1110	PWM	LOW	LOW	HIGH	LOW	HIGH
Stop	0000	LOW	LOW	LOW	LOW	LOW	LOW

7.3.3 Charge Pump

A regulated triple charge pump scheme is used to create sufficient V_{GS} to drive standard FETs under low voltage operation.

The high-side FETs are directly driven by the tripler charge pump output while the low-side FETs are driven by a voltage that is internally regulated but derived from the tripler charge pump. This allows both the high side and low side to maintain sufficient V_{GS} through low voltage transients. This topology also supports 100% duty cycle operation.

Between 4.4 to 18 V the charge pump regulates the voltage in tripler mode; beyond 4.4 to 18 V, it switches over to doubler mode until the operating max voltage. The charge pump is monitored for undervoltage and overvoltage conditions to prevent underdriven or overdriven FET conditions.

7.3.4 Gate Driver Architecture

The DRV8305 gate driver is a complimentary push-pull topology for both the high-side and the low-side drivers. The peak currents for the drivers are adjustable; their benefits are described in detail in the *Slew Rate/Slope Control* section.

The gate driver is implemented as constant current sources for up to 80 mA (sink)/70 mA (source) currents in order to maintain the accuracy required for precise slew rate control. Beyond that, resistors are switched to create the desired settings up to 1.25 A (sink)/1 A (source).

7.3.5 IDRIVE/TDRIVE

The DRV8305 gate driver has an integrated state machine (TDRIVE/IDRIVE scheme) to protect against high current events on the outputs (shorts or inadvertent clamp activation) and also dV/dt turn on due to switching on the phase nodes.

When changing the state of the gate driver, the peak current (source or sink, IDRIVE) is applied for a fixed period of time (TDRIVE) until the gate capacitances are charged or discharged completely. After this time has expired, a fixed current source of I_{HOLD} is used to hold the gate at the desired state (pulled up or pulled down).

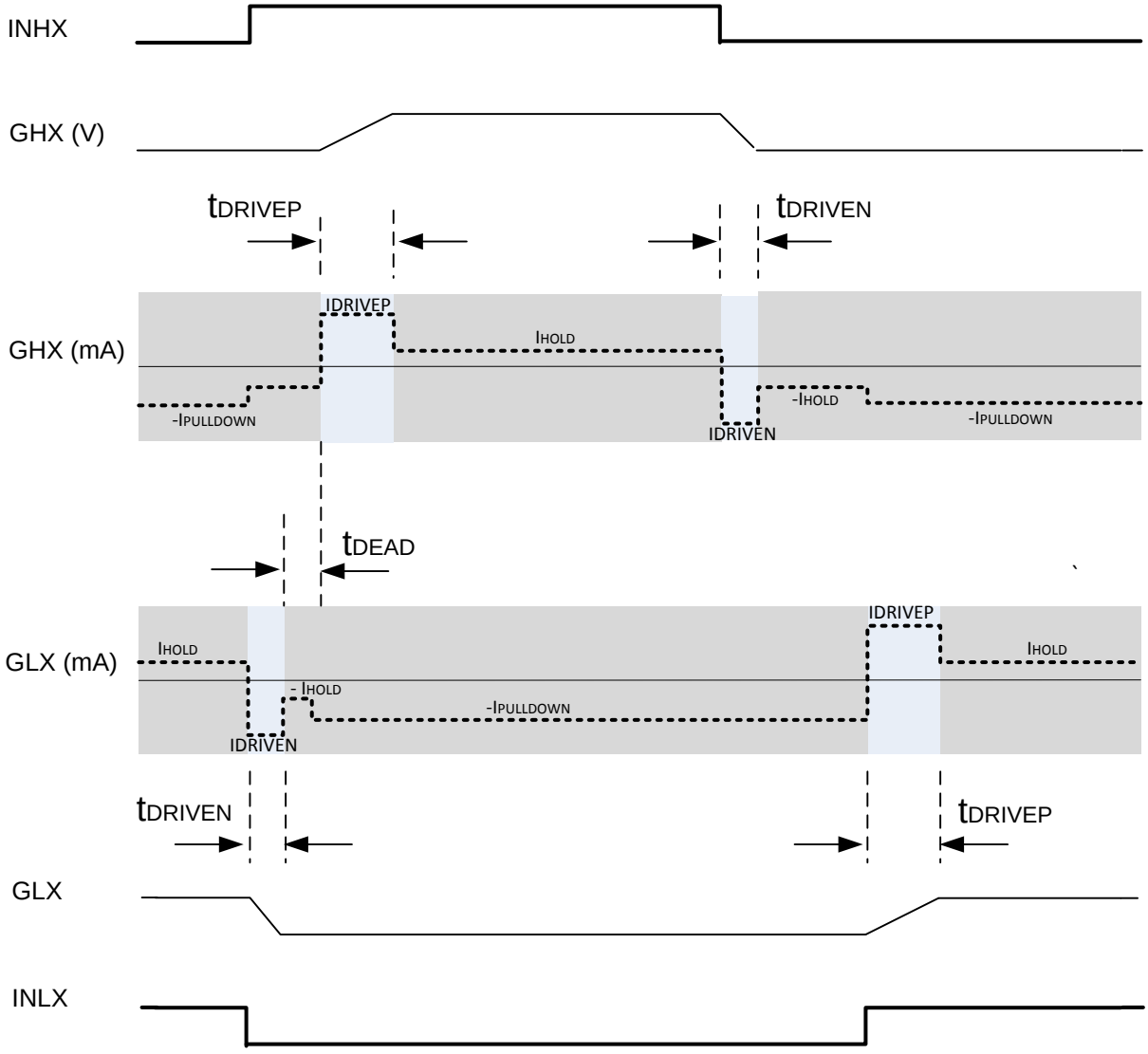


Figure 7. TDRIVE/IDRIVE Waveforms

This fixed TDRIVE time ensures that under abnormal circumstances like a short on the FET gate, or the inadvertent turning on of a FET V_{GS} clamp, the high peak current through the DRV8305 gate drivers is limited to the energy of the peak current during TDRIVE. Limiting this energy helps to prevent the gate driver from damage.

Select a TDRIVE time that is longer than the time needed to charge or discharge the gate capacitances. IDRIVE and TDRIVE are selected based on the size of external FETs used and the desired rise and fall times. These registers must be configured so that the FET gates are charged completely during TDRIVE. If IDRIVE and TDRIVE are too low for a given FET, then the FET may not turn on completely. TI suggests to adjust these values in-system with the required external FETs to determine the best possible setting for any application.

Note that TDRIVE will not increase the PWM time and will simply terminate if a PWM command is received while it is active. A good starting point is to select a TDRIVE that is about 2× longer than the external FET switching rise (turn ON) and fall (turn OFF) times.

The IDRIVE/TDRIVE state machine protects against dV/dt turn on of a FET due to switching of the phase nodes. A strong pulldown current source of value $I_{PULLDOWN}$ is switched on between (GHX to SHX) or (GLX to SLX), every time an opposing FET is commanded to turn on.

7.3.6 Slew Rate/Slope Control

Control of the FET VDS rise and fall times during the Miller region of the FET is one of the most important parameters for optimizing emitted radiations and power. The rise and fall times also influence the energy and duration of the diode recovery inductive spikes and also dV/dt turn on of the LS FET.

The ability of a driver to control the rise and fall times across the entire range of gate drive temperature, voltage, and process variation is essential to design robust systems. The key control knob is the ability to turn on and turn off the external FET with the least amount of variation.

The DRV8305 uses temperature compensated *constant current* sources up to 80-mA (sink) and 70-mA (source) current. The current source architecture helps eliminate the temperature, process, and load-dependent variation associated with internal and external series limiting resistors.

For higher currents, internal series resistors are used to minimize the power losses associated with mirroring such large currents.

The 12 settings that are available on the DRV8305 allow the user to optimize the system using only SPI commands. This flexibility allows the system designer to tune the performance of the driver for different operating conditions through software alone.

The slew rate settings may be set separately for source and sink values and can also be set separately for the high-side FETs (the high sides of all three phases share the same setting) and the low-side FETs (the low sides of all three phases share the same settings)

7.3.7 Current Shunt Amplifiers

The DRV8305 includes three high performance low-side current shunt amplifiers for accurate current measurement. The current amplifiers provide output bias up to 2.5 V to support bidirectional current sensing.

Current shunt amplifier has following features:

- Each of the three current sense amplifiers can be programmed and calibrated independently.
- The independent current shunt amplifiers may be used either for sensing current through individual phase shunt resistors or the total current delivered to the motor through a single shunt resistor.
- Programmable gain: four gain settings through SPI command
- Internally or externally provided reference voltage to set output bias for amplifiers. Reference voltage is internally sourced from DRV8305 voltage regulator VREG, if also used to power microcontroller. It can alternatively be applied externally on the VREG pin.
- Programmable output bias scaling. The scaling factor k can be programmed through SPI to be equal to, half or a fourth of the reference voltage.
- Programmable blanking time (delay) of the amplifier outputs. The blanking time is implemented from any rising or falling edge (any of the outputs) of the internal gate driver gate signals. The blanking time is applied to all three current sense amplifiers equally. In case the current sense amplifiers are already being blanked when another gate driver rising or falling edge is seen, the blanking interval will be restarted at the edge.

  Note that the blanking time options do not include delay from internal amplifier loading or delays from the trace or component loads on the amplifier output. The programmable blanking time may be overridden to have no delay (default value).
- Minimize DC offset and drift through temperature with DC calibrating through SPI command. When DC calibration is enabled, device will short input of current shunt amplifier and disconnect the load. DC calibrating

can be done at anytime, even when the FET is switching because the load is disconnected. For best result, perform the DC calibrating during switching off period when no load is present to reduce the potential noise impact to the amplifier.

The output of current shunt amplifier can be calculated as:

$$V_O = \frac{V_{VREF}}{k} - G \times (SN_X - SP_X) \quad (1)$$

where

- VREF is the reference voltage.
- G is the gain of the amplifier.
- k = 2, or 4
- SNx and SPx are the inputs of channel x. SPx should connect to resistor ground for the best common mode rejection.

Figure 8 shows current amplifier simplified block diagram.

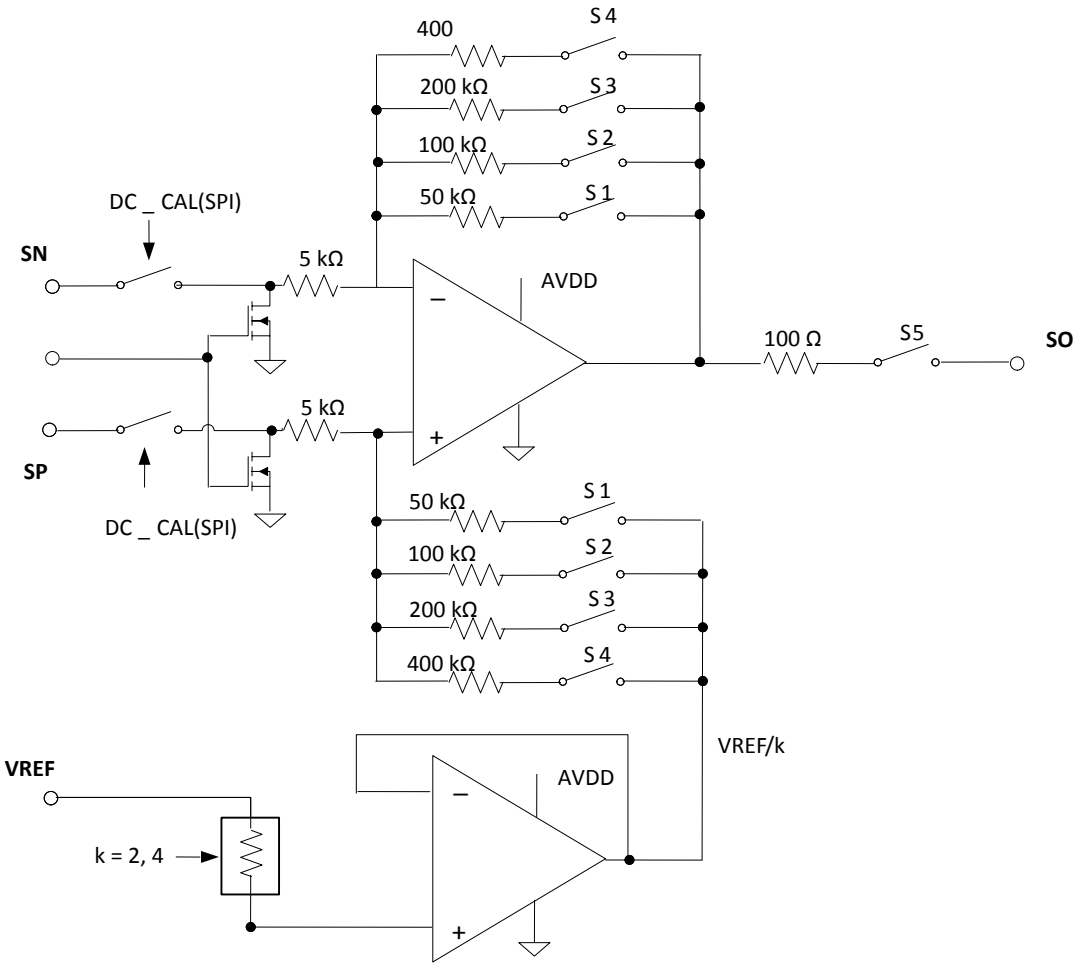


Figure 8. Current Shunt Amplifier Simplified Block Diagram

7.3.8 Internal Regulators (DVDD and AVDD)

The DRV8305 has two internal regulators, DVDD and AVDD, that power internal circuits. These regulators cannot be used to drive external loads and may not be supplied externally.

DVDD is the voltage regulator for the internal logic circuits and is maintained at a value of about 3.3 V through the entire operating range of the device. DVDD is derived from the PVDD supply.

AVDD is the voltage regulator that provides the voltage rail for the internal analog circuit blocks including the current sense amplifiers. AVDD is derived from the PVDD voltage supply.

Because the allowed operating range of the device permits operation below the nominal value of AVDD, this regulator operates in two regimes: namely a linear regulating regime and a dropout region. In the dropout region, the AVDD will simply track the PVDD voltage minus a voltage drop.

If the device is expected to operate within the dropout region, take care while selecting current sense amplifier components and settings to accommodate this reduced voltage rail.

7.3.9 Voltage Regulator Output for Driving External Loads (VREG)

The DRV8305 integrates an LDO voltage regulator (VREG) that is dedicated for driving external loads like an MCU directly. The two versions of the device provide different voltages: DRV83053 provides 3.3 V, DRV83055 provides 5.0 V. Because the user can supply microcontroller and other system power from the DRV8305, the user does not need to add an external regulator IC for system power.

The DRV8305 voltage regulator is standalone, uncommitted, and is not used internally.

The DRV8305 voltage regulator also features a PWRGD pin to protect against brownouts on externally driven devices. The PWRGD pin is often tied to a reset pin on a microcontroller to ensure that the microcontroller is always reset when the voltage is outside of its recommended operation area.

When the voltage output of the LDO drops or exceeds the set threshold (programmable).

- The PWRGD pin will go low for a period of 64 µs.
- After the 64-µs period has expired, the LDO voltage will be checked and PWRGD will be held low until the LDO voltage has recovered.

The voltage regulator also has undervoltage protection implemented for both the input voltage (PVDD) and output voltage (VREG).

7.3.10 Protection Features

Fault / Warning Classes and Recovery summarizes the protection features, fault responses, and recovery sequences.

7.3.10.1 Fault and Protection Handling

The DRV8305 handles fault (latched fault) and warnings (unlatched faults) separately. Both latched and unlatched faults are reported in status registers and can be read through SPI.

- A latched nFAULT pin indicates an error event has occurred that has caused part of the gate driver to shut down and force outputs to a safe state (external FETs in high impedance).
  - A latched fault is indicated by the nFAULT pin going low (and staying low) and reporting the details of the fault in the status registers (0x02 and 0x03). The appropriate recovery sequence must be performed in order to reset the latched fault. In addition, the register (0x01) contains a single status bit if any latched faults are detected.
  - The nFAULT pin will stay low until the appropriate recovery sequence is performed.

TI recommends to inspect the system and board when a latched nFAULT faults occurs.

- An unlatched warning on nFAULT pin indicates that an event that requires a warning to be communicated has occurred.
  - An unlatched fault is indicated by the nFAULT pin going low for a period of 64 µs, reporting the warning and then recovering back high for a period of 64 µs before reporting any subsequent errors.
  - When a warning has been read by SPI through the warning register (0x01), that same warning will not be reported through nFAULT again unless that warning or condition passes and then reoccurs.

    However, the SPI registers will continue to report the latest status of the condition even after it has been cleared by the read, that is, if the condition has cleared, then the warning will clear in the SPI registers.

    Note that if the microprocessor does not read the warning, then the nFAULT pin will continue to toggle.
  - In case another warning or warnings are received during the 64-µs period but after the warning register has been read, then after the expiration of 64 µs, the nFAULT pin will go high for another 64 µs and then report those warning or warnings by going low for another 64 µs.
  - If a latched fault occurs during a period where nFAULT is low, then the nFAULT pin will stay low.

Note that nFAULT is an open-drain signal and must be pulled up through an external resistor.

7.3.10.2 Shoothrough Protection

DRV8305 integrates analog and digital monitors to prevent shoot-through in the external FETs.

- An Internal handshake through analog comparators is performed between high-side and low-side FETs during switching transition.
- A minimum dead time (digital) of 40 ns is always inserted after a successful handshake. This digital dead-time is programmable and is in addition to the time taken for the handshake.

7.3.10.3 VDS Sensing – External FET Protection and Reporting (OC Event)

To protect the external FETs from damage due to high currents, V_{DS} sensing circuitry is implemented in the DRV8305.

The V_{DS} sensing is implemented for both the high-side and low-side MOSFET through these pins:

- High-side MOSFET: V_{DS} measured between VDRAIN and SHX pins
- Low-side MOSFET: V_{DS} measured between SHX and SLX pins

Based on $R_{DS(on)}$ of the power MOSFETs and the maximum allowed I_{DS}, a voltage threshold can be calculated, which when exceeded, triggers the V_{DS} protection feature.

This voltage threshold level is programmable through SPI command and may be programmed during operation if needed.

The V_{DS} protection logic also has an adjustable blanking time and deglitch time to prevent false trips.

V_{DS} blanking time (t_{BLANK}): This time is inserted digitally and is programmable. The t_{BLANK} time is a delay inserted at each output after that particular output has been commanded to turn ON. During t_{BLANK} time, the VDS comparators are not being monitored in order to prevent false trips when the FETs first turn ON.

V_{DS} deglitch time (t_{VDS}): This time is inserted digitally and is programmable. The t_{VDS} time is a delay inserted after the VDS sensing comparators have tripped to when the protection logic is informed that a VDS event has occurred.

Note that the dead time and blanking time are overlapping counters as shown in Figure 9

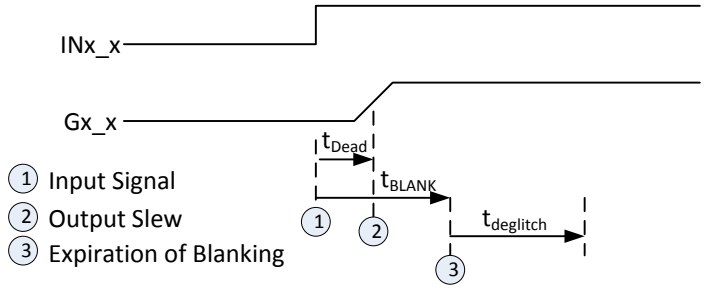


Figure 9. VDS Protection Timing

Three overcurrent responses are possible depending on the configuration option selected through SPI.

- V_{DS} event latch shutdown mode
  When a VDS event occurs, device will pull all outputs low in order to take all six external FETs into high-impedance mode. The Fault will be reported on nFAULT and details of the FET that reported the fault can be read back through SPI.
- V_{DS} event Reporting only mode
  In this mode, VDS event will be reported on the nFAULT pin and the SPI register. Gate drivers will continue to operate.
- V_{DS} event disable mode
  Device ignores all the V_{DS} event detections and does not report them.

7.3.10.4 Low-Side Source Monitoring (SNS_OCP)

The DRV8305 monitors the voltage on the SLX pins for high-current events like phase shorts that may cause the voltage on those pins to exceed 2 V. The device will put the FETs into a high-impedance state to avoid damage.

7.3.11 Undervoltage Reporting and Undervoltage Lockout (UVLO) Protection

The DRV8305 implements appropriate undervoltage responses in order to protect the system. *Fault / Warning Classes and Recovery* lists the details of the monitors and their response and recovery sequences.

Under-voltage is monitored on PVDD, AVDD, VCPH, and VCP_LSD.

The UVLO protection fault may be completely disabled for the PVDD undervoltage condition using a SPI register command. In this case, the fault is still reported in the register.

The UVLO protection may never be completely disabled for the VCPH or VCP_LSD in OPERATING mode because this may indicate a short condition that could damage the DRV8305.

7.3.11.1 Battery Overvoltage Protection (PVDD_OV)

The DRV8305 implements appropriate overvoltage responses in order to protect the system.

PVDD is monitored for overvoltage conditions. If the overvoltage threshold is tripped, a warning is issued and the event is reported in the status registers. The device takes no action.

7.3.11.2 Charge Pump Overvoltage Protection (VCPH_OV/VCP_LSD_OV)

If VCPH or VCP_LSD exceed the overvoltage threshold due to potential issue related to the charge pumps (for example, short of external charge pump capacitor or charge pump, an overvoltage fault is triggered).

7.3.11.3 Overtemperature (OT) Warning and Protection

A multi-level temperature detection circuit is implemented:

- Flag Level 1: Level 1 overtemperature flag. No warning is reported on nFAULT. A real-time register bit is set to indicate flag and can be read through SPI.
- Flag Level 2: Level 2 overtemperature flag. No warning is reported on nFAULT. A real-time register bit is set to indicate flag and can be read through SPI.
- Flag Level 3: Level 3 overtemperature flag. No warning is reported on nFAULT. A real-time register bit is set to indicate flag and can be read through SPI.
- Flag Level 4: Level 4 overtemperature flag. No warning is reported on nFAULT. A real-time register bit is set to indicate flag and can be read through SPI.
- Warning Level: Overtemperature warning only. Warning is reported on nFAULT for 64 µs and can be read through SPI.
- Fault Level: Overtemperature fault and latched shut down of gate driver and charge pump Fault will be reported to nFAULT pin.

SPI operation is still available and register settings will be retained in the device during OTSD operation as long as PVDD is still within defined operation range.

The details of the fault will be reported into a register that can be read back through SPI.

7.3.11.4 dV/dt Protection

The DRV8305 gate driver implements a strong pulldown scheme for preventing dV/dt turn on of external FETs. After a FET has been turned off using the selected sink slew rate setting, the internal state machine will turn on a stronger pulldown if it senses that the opposite FET on that phase has been commanded to turn on. This allows the systems designer to decouple the optimum slew rate setting selection for EMI and power from the pull down required to prevent dV/dt turn on.

7.3.11.5 VGS Protection

The DRV8305 gate driver uses a multilevel level protection scheme to protect the external FET from VGS voltages that may damage the gate of the external FET.

The device integrates VGS clamps inside the gate driver that will turn on when the GHX voltage exceeds SHX voltage by a value that could be damaging to the FETs. If the voltage continues to rise, in spite of the clamps turning on, the TDRIVE architecture ensures that the energy through the clamps is limited. If the high VGS voltage is due to an abnormal condition on the charge pump, the charge pump overvoltage fault will trip in order to protect the FETs from damage.

7.3.11.6 Gate Driver Faults

The DRV8305 protects against abnormal short to battery or short to ground conditions on the gate driver outputs that could result in an incorrect state of the gate driver outputs. The gate driver integrates VGS comparators that check the status of the gate driver output against the commanded PWM signal to ensure that they match. This comparison occurs shortly after the expiration of the TDRIVE time. If the comparison indicates a mismatch, a gate driver fault is indicated.

7.3.11.7 Reverse Battery Protection

The VCPH pin on the DRV8305 is designed to be able to supply an external load of up to 10 mA. This feature allows implementation of an external reverse battery protection scheme using a MOS and a BJT. The MOS gate can be driven through VCP through a current limiting resistor to limit the current drawn from VCP. The current limit resistor must be sized not to exceed the maximum external load on VCPH.

The VDRAIN pin (sense) may also be protected against negative transients on it by use of a current limiting resistor. The current limit resistor must be sized not to exceed the maximum current load on the VDRAIN pin.

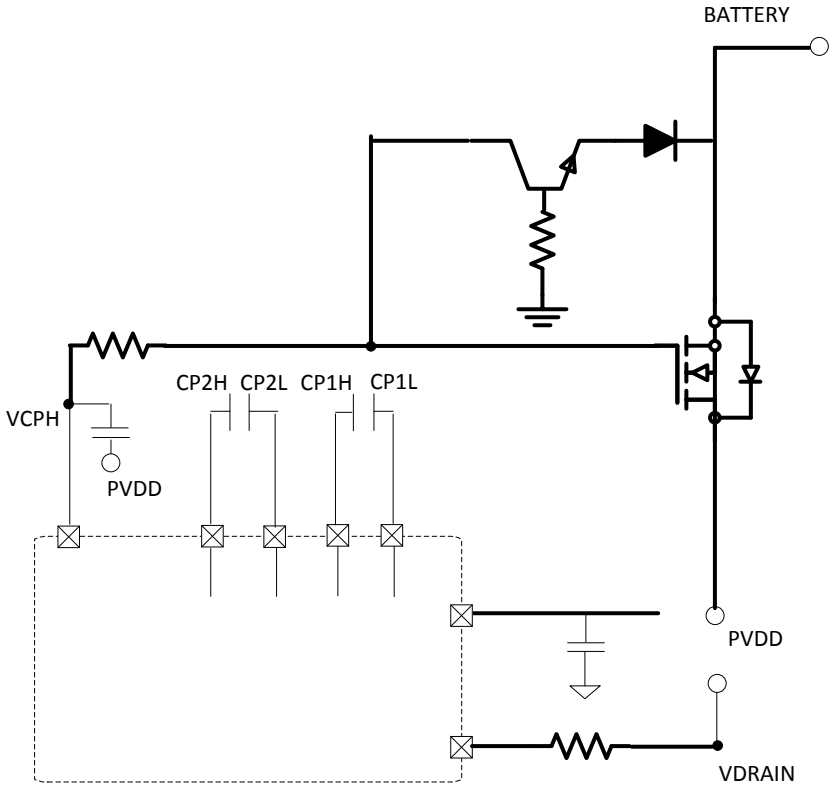


Figure 10. Typical Scheme for Reverse Battery Protection Using VCPH

7.3.11.8 MCU Watchdog

An MCU watchdog function may be enabled to ensure that the external controller that is instructing the DRV8305 is active and not in an unknown state.

SPI Watchdog must be enabled by writing a 1 to the WD_EN bit through SPI (default is disabled = 0).

When the SPI watchdog is enabled, an internal timer starts to countdown to an interval set by WD_dly bit.

To reset the watchdog, the address 0x01 (Status register) must be read by the microcontroller within the interval set by the register WD_dly.

If the timer is allowed to expire without the address 0x01 being read, the WD fault will get enabled.

Response to this fault is as follows:

- A Latched + PWRGD fault occurs on the DRV8305 and gate drivers are put into a safe state. The appropriate recovery sequence must be performed.
- PWRGD pin is taken low for 64 µs and then back high in order to reset the microcontroller.
- nFAULT is asserted
- WD_EN bit is cleared
- Report that the watchdog had expired through SPI bit WD_FAULT
- TI recommends that if the watchdog function is being used, the MCU software routine reads the status registers as part of its recovery or power-up routine in order to know whether a WD_FAULT had previously occurred.

Note that the fault results in clearing of the WD_EN bit and it will have to be set again to resume watchdog functionality.

7.3.12 Pin Control Functions

7.3.12.1 EN_GATE

EN_GATE low is used to put the gate driver into standby mode. Note that EN_GATE has no effect on the LDO voltage regulator. When EN_GATE is low, the device will always put the MOSFET output stage to high impedance as long as PVDD is still present. EN_GATE is also used to reset the IC.

It is not possible to enter SLEEP mode without taking EN_GATE low and entering STANDBY mode first.

TI recommends to take EN_GATE for at least greater than 25 µs when it is asserted low to go into standby mode.

7.3.12.2 SPI Pins

SDO pin has to be tri-state, so a data bus line can be connected to multiple SPI slave devices. SCS pin is active low. When SCS is high, SDO is at high-impendence mode.

Ensure that SDO pin is always configured in the system as an output from DRV8305.

SDO pin must never be driven to ensure correct operation of DRV8305. SDO is referrenced to the VREG voltage.

Table 5. Fault / Warning Device Status

CONDITION	CLASS	OUTPUTS PD – PULL DOWN O – OPERATING	CHARGE PUMP O – OPERATING SD – SHUTDOWN	AVDD / DVDD O – OPERATING SD – SHUTDOWN	VOLTAGE REGULATOR O – OPERATING SD – SHUTDOWN
PVDD undervoltage (V_{PVDD_UVLO1}) falling	None	PD	SD	SD	SD
PVDD undervoltage (V_{PVDD_UVLO2}) falling	Latched	PD	SD	O	O
PVDD undervoltage (V_{PVDD_UVFL}) falling	Warning	O	O	O	O
PVDD overvoltage (V_{PVDD_OVFL}) rising	Warning	O	O	O	O
Charge pump undervoltage (VVCPH_UVFL) falling	Warning	O	O	O	O
Charge pump undervoltage (V_{VCPH_UVLO} / $V_{VCP\_LSD\_UVLO}$)	Latched	PD	SD	O	O
Charge pump overvoltage (V_{VCPH_OVLO}, $V_{VCPH\_OVLO\_ABS}$)	Latched	PD	SD	O	O
AVDD undervoltage	Latched	PD	SD	SD	O
TEMP FLAG 1/2/3/4	Real time	O	O	O	O
OT warning (OTW)	Warning	O	O	O	O
OT shutdown (OTS)	Latched	PD	SD	O	O
VDS event – latch mode (FETxx_VDS)	Latched	PD	O	O	O
VDS event – report mode (FETxx_VDS)	Report only	O	O	O	O
VDS event – disable mode (FETxx_VDS)	Not reported	O	O	O	O
SNS OCP	Latched	PD	O	O	O
Gate driver fault VGS event	Latched	PD	SD	O	O
MCU watchdog	Latched + PWRGD	PD	O	O	O
VREG_UV	Latched + PWRGD	PD	O	O	O

7.3.13 Fault / Warning Classes and Recovery

7.3.13.1 Reg 09h CLR_FLTS

When CLR_FLTS bit is set to 1, all expired faults (latch/warn) will be cleared from the SPI status register. Also, the nFAULT pin will be released on the event of an expired Latched fault. CLR_FLTS provides a software reset option to DRV8305. The effect on nFAULT pin and SPI status registers is the same as pulling EN_GATE pin low and taking it HIGH.

CLR_FLTS bit self clears to 0 after SPI status register is reset and nFAULT pin is released.

Table 6. Fault / Warning Reporting and Handling

CLASS	nFAULT	PWRGD	SPI REPORT	DEVICE RECOVERY SEQUENCE	SPI REPORT RECOVERY
Latched	Low	No action	Yes	Toggle EN_GATE (Faults clear on rising edge of EN_GATE) OR Write Reg 09h CLR_FLTS bit set 1	Bit clears only on successful fault recovery
Warning	Toggles with 64-µs period	No action	Yes	Read SPI status register 0x01 to acknowledge warning (otherwise nFAULT will continue to toggle)	Bit clears on register read only if condition has passed
Report only (VDS mode)	Toggles with 64-µs period	No action	Yes	Read SPI status register 0x01 to acknowledge warning (otherwise nFAULT will continue to toggle)	Bit clears on register read only if condition has passed
Real time	No action	No action	Yes	Read SPI register to capture real time status	Bit clears after condition has passed
Not reported	No action	No action	No	None	None
Latched + PWRGD	Low	Low for minimum of 64 µs	Yes	Toggle EN_GATE (Faults clear on rising edge of EN_GATE) OR Write Reg 09h CLR_FLTS bit set 1	Bit clears only on successful fault recovery

7.4 Device Functional Modes

7.4.1 Power-Up and Operating States Hardware Configuration for VREG/VREF

Hardware configuration is not required. Voltage regulator voltage (3.3 or 5 V or disabled) is based on orderable part number.

7.4.1.1 POWER Up

During power-up, all internal circuits are enabled. The VREG will also be enabled based on the hardware configuration (see *Voltage Regulator Control (address = 0xB)* section). All gate drive outputs are held low and the nFAULT pin is taken low by the IC while power up is being executed.

7.4.1.2 STANDBY State

After the startup sequence is completed and the PVDD voltage is above V_{PVDD_UVLO2}, the DRV8305 will indicate successful and fault-free power up of all circuits by releasing the nFAULT pin.

The device will also enter STANDBY state any time that EN_GATE is taken low or a latched fault occurs.

Gate driver always has control of the power FETs even in STANDBY state.

TI recommends to set up the device control registers through SPI in the STANDBY state.

7.4.1.3 OPERATING State

Normal operation of the gate driver and current shunt amplifiers can be initiated by taking EN_GATE from a low state to a high state. In this state the charge pump is powered up and the driver is ready for operation.

Device Functional Modes (continued)

7.4.1.4 SLEEP State

The SLEEP state is invoked by issuing a SLEEP command through SPI. After the SLEEP command is received, the VREG and the gate driver safely power down internally after a programmable delay.

The DRV8305 can then only be enabled through the WAKE pin which is a high-voltage-tolerant input pin.

For the DRV8305 to be brought out of SLEEP, the WAKE pin must be at a voltage greater than 3 V. This allows the WAKE to be driven, for example, directly by the battery through a switch, through the inhibit pin (INH) on standard LIN interface or through standard digital logic. The WAKE pin will only react to a wake-up command if PVDD > V_{PVDD_UVLO2}.

After the DRV8305 is out of SLEEP mode, all activity on the WAKE pin is ignored.

SLEEP state erases the values in the SPI control registers. TI does not recommend to write through SPI in SLEEP state.

7.5 Programming

7.5.1 SPI Communication

7.5.1.1 SPI

SPI is used to set device configuration, operating parameters, and read out diagnostic information. The DRV8305 SPI operates in slave mode.

The SPI input data (SDI) word consists of a 16-bit word with 11-bit data and 5-bit (MSB) command. The SPI output data (SDO) word consists of 11-bit register data. (The first 5 bits (MSB) are to be ignored.)

A valid frame must meet following conditions:

- Clock must be low when nSCS goes low.
- It should have 16 full clock cycles.
- Clock must be low when nSCS goes high.

Data is always shifted out on the rising edge of the clock in the same frame following the 5-bit MSB.

Data is always sampled on the falling edge of the clock in the same frame following the 5-bit MSB.

When SCS is asserted high, any signals at the SCLK and SDI pins are ignored, and SDO is forced into a high-impedance state. When SCS transitions from HIGH to LOW, SDO is enabled and the SPI response word loads into the shift register based on 5-bit command.

The SCLK pin must be low when SCS transitions low. While SCS is low, at each rising edge of the clock, the response bit is serially shifted out on the SDO pin with MSB shifted out first.

While SCS is low, at each falling edge of the clock, the new control bit is sampled on the SDI pin. The SPI command bits are decoded to determine the register address and access type (read or write). The MSB will be shifted in first. If the word sent to SDI is less than 16 bits or more than 16 bits, it is considered a frame error and the data will not be written into the destination address. If it is a write command, the data will be ignored.

For a write command, the existing data in the register being written to is shifted out on SDO following the 5-bit MSB.

SCS should be taken high for at least 500 ns between frames.

7.5.1.2 SPI Format

SPI input data control word is 16-bit long, consisting of:

- 1 read or write bit W [15]
- 4 address bits A [14:11]
- 11 data bits D [10:0]

SPI output data response word is 11-bit long (first 5 bits are ignored) and its content is the content of the register being accessed

For a Write transaction: The response word is the data currently in the register being written to.

For a Read Command: The response word is the data currently in the register being read.

Table 7. SPI Input Data Control Word Format

	R/W	ADDRESS				DATA										
Word Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Command	W0	A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 8. SPI Output Data Response Word Format

	DATA															
Word Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Command	X	X	X	X	X	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

7.6 Register Maps

Table 9. Register Map

ADDRESS	NAME	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x1	Warning & Watch Dog	FAULT	Reserved	TEMP_FLAG4	PVDD_UVFL	PVDD_OVFL	VDS_STATUS	VCPH_UVFL	TEMP_FLAG1	TEMP_FLAG2	TEMP_FLAG3	OTW
0x2	OV/VDS Faults	FETHA_VDS	FETLA_VDS	FETHB_VDS	FETLB_VDS	FETHC_VDS	FETLC_VDS	Reserved	Reserved	SNS_C_OCP	SNS_B_OCP	SNS_A_OCP
0x3	IC Faults	PVDD_UVLO2	WD_FAULT	OTS	Reserved	VREG_UV	AVDD_UVLO	VCP_LSD_UVLO	Reserved	VCPH_UVLO	VCPH_OVLO	VCPH_OVLO_ABS
0x4	Gate drvier VGS Faults	FETHA_VGS	FETLA_VGS	FETHB_VGS	FETLB_VGS	FETHC_VGS	FETLC_VGS	Reserved	Reserved	Reserved	Reserved	Reserved
0x5	HS Gate Driver Control	Reserved	TDRIVEN[1]	TDRIVEN[0]	IDRIVEN_HS[3]	IDRIVEN_HS[2]	IDRIVEN_HS[1]	IDRIVEN_HS[0]	IDRIVEP_HS[3]	IDRIVEP_HS[2]	IDRIVEP_HS[1]	IDRIVEP_HS[0]
0x6	LS Gate Driver Control	Reserved	TDRIVEP[1]	TDRIVE[0]	IDRIVEN_LS[3]	IDRIVEN_LS[2]	IDRIVEN_LS[1]	IDRIVEN_LS[0]	IDRIVEP_LS[3]	IDRIVEP_LS[2]	IDRIVEP_LS[1]	IDRIVEP_LS[0]
0x7	Gate Drive Control	Reserved	COMM_OPTION	PWM_MODE[1]	PWM_MODE[0]	DEAD_TIME[2]	DEAD_TIME[1]	DEAD_TIME[0]	TBLANK[1]	TBLANK[0]	TVDS[1]	TVDS[0]
0x8	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x9	IC Operation	FLIP_OTS	DISABLE VPVDD_UVLO2	DIS_GDRV FAULT	EN_SNS_CLAMP	WD_DLY[1]	WD_DLY[0]	DIS_SNS_OCP	WD_EN	SLEEP	CLR_FLTS	SET_VCPH_UV
0xA	Shunt Amplifier Control	DC_CAL_CH3	DC_CAL_CH2	DC_CAL_CH1	CS_BLANK[1]	CS_BLANK[0]	GAIN_CS3[1]	GAIN_CS3[0]	GAIN_CS2[1]	GAIN_CS2[0]	GAIN_CS1[1]	GAIN_CS1[0]
0xB	Voltage Regulator Control	Reserved	VREF_SCALE[1]	VREF_SCALE[0]	Reserved	Reserved	Reserved	SLEEP_DLY[1]	SLEEP_DLY[0]	DIS_VREG_PWRGD	VREG_UV_LEVEL[1]	VREG_UV_LEVEL[0]
0xC	VDS Sense Control	Reserved	Reserved	Reserved	VDS_LEVEL[4]	VDS_LEVEL[3]	VDS_LEVEL[2]	VDS_LEVEL[1]	VDS_LEVEL[0]	VDS_MODE[2]	VDS_MODE[1]	VDS_MODE[0]

7.6.1 Read / Write Bit

The MSB bit of SDI word (W0) is read/write bit. When W0 = 0, input data is a write command; when W0 = 1, input data is a read command, and the register value will send out on the same word cycle from SDO from D10 to D0.

7.6.2 Status Registers

Status registers are used to report warning, fault conditions and provide a means to prevent timing out of the watchdog timer. Status registers are read only registers.

7.6.3 0x1 Warning and Watchdog Reset

Table 10. Warning and Watchdog Reset Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION
10	R	FAULT	0x0	0 - Warning, 1 - Latched fault
9	R	Reserved	0x0	
8	R	TEMP_Flag4	0x0	Temperature flag setting for about 175°C
7	R	PVDD_UVFL	0x0	PVDD undervoltage flag warning
6	R	PVDD_OVFL	0x0	PVDD overvoltage flag warning
5	R	VDS_STATUS	0x0	Real time or of all VDS sensors (0x2[D10:5])
4	R	VCHP_UVFL	0x0	Charge pump undervoltage flag warning
3	R	TEMP_Flag1	0x0	Temperature flag setting for about 105°C
2	R	TEMP_Flag2	0x0	Temperature flag setting for about 125°C
1	R	TEMP_Flag3	0x0	Temperature flag setting for about 135°C
0	R	OTW	0x0	Overtemperature warning

7.6.4 0x2 OV/VDS Faults

Table 11. OV/VDS Faults Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION
10	R	FETHA_VDS	0x0	VDS monitor fault for high-side FET A
9	R	FETLA_VDS	0x0	VDS monitor fault for low-side FET A
8	R	FETHB_VDS	0x0	VDS monitor fault for high-side FET B
7	R	FETLB_VDS	0x0	VDS monitor fault for low-side FET B
6	R	FETHC_VDS	0x0	VDS monitor fault for high-side FET C
5	R	FETLC_VDS	0x0	VDS monitor fault for low-side FET C
4:3	R	Reserved	0x0	
2	R	SNS_C_OCP	0x0	Sense C overcurrent protection flag
1	R	SNS_B_OCP	0x0	Sense B overcurrent protection flag
0	R	SNS_A_OCP	0x0	Sense A overcurrent protection flag

7.6.5 0x3 IC Faults

Table 12. IC Faults Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION
10	R	PVDD_UVLO2	0x0	PVDD undervoltage 2 fault
9	R	WD_FAULT	0x0	Watchdog fault
8	R	OTS	0x0	Overtemperature fault
7	R	Reserved	0x0	
6	R	VREG_UV	0x0	VREG undervoltage fault
5	R	AVDD_UVLO	0x0	AVDD undervoltage fault
4	R	VCP_LSD_UVLO	0x0	Charge pump low-side gate driver fault
3	R	Reserved	0x0	
2	R	VCPH_UVLO	0x0	Charge pump high-side undervoltage 2 fault
1	R	VCPH_OVLO	0x0	Charge pump high-side overvoltage fault
0	R	VCPH_OVLO_ABS	0x0	Charge pump high-side overvoltage ABS fault

7.6.6 0x4 Gate Driver VGS Faults

Table 13. Gate Driver VGS Faults Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION
10	R	FETHA_VGS	0x0	VGS monitor fault for high-side FET A
9	R	FETLA_VGS	0x0	VGS monitor fault for low-side FET A
8	R	FETHB_VGS	0x0	VGS monitor fault for high-side FET B
7	R	FETLB_VGS	0x0	VGS monitor fault for low-side FET B
6	R	FETHC_VGS	0x0	VGS monitor fault for high-side FET C
5	R	FETLC_VGS	0x0	VGS monitor fault for low-side FET C
4:0	R	Reserved	0x0	

7.6.7 Control Registers

Control registers are used to set the user parameter for DRV8305. The default values are shown in bold.

- Control registers may be read and do not clear on read or EN_GATE resets
- Control registers are cleared to default values on power up
- Control registers are cleared to default values when the device enters SLEEP mode

7.6.7.1 HS Gate Driver Control (address = 0x5)

Table 14. HS Gate Driver Control Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION			
10	R/W	Reserved	0x0				
9:8	R/W	TDRIVEN	0x3	High-side gate driver peak source time b'00 - 250 ns b'01 - 500 ns b'10 - 1000 ns **b'11 - 2000 ns**			
7:4	R/W	IDRIVEN_HS	0x4	High-side gate driver peak sink current			
				b'0000 - 20 mA **b'0100 - 60 mA** b'1000 - 0.50 A b'1100 - 60 mA	b'0001 - 30 mA b'0101 - 70 mA b'1001 - 0.75 A b'1101 - 60 mA	b'0010 - 40 mA b'0110 - 80 mA b'1010 - 1.00 A b'1110 - 60 mA	b'0011 - 50 mA b'0111 - 0.25 A b'1011 - 1.25 A b'1111 - 60 mA
3:0	R/W	IDRIVEP_HS	0x4	High-side gate driver peak source current			
				b'0000 - 10 mA **b'0100 - 50 mA** b'1000 - 0.25 A b'1100 - 50 mA	b'0001 - 20 mA b'0101 - 60 mA b'1001 - 0.50 A b'1101 - 50 mA	b'0010 - 30 mA b'0110 - 70 mA b'1010 - 0.75 A b'1110 - 50 mA	b'0011 - 40 mA b'0111 - 0.125 A b'1011 - 1.00 A b'1111 - 50 mA

7.6.7.2 LS Gate Driver Control (address = 0x6)

Table 15. LS Gate Driver Control Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION			
10	R/W	Reserved	0x0				
9:8	R/W	TDRIVEP	0x3	Low-side gate driver peak source time b'00 - 250 ns b'01 - 500 ns b'10 - 1000 ns **b'11 - 2000 ns**			
7:4	R/W	IDRIVEN_LS	0x4	Low-side gate driver peak sink current			
				b'0000 - 20 mA **b'0100 - 60 mA** b'1000 - 0.50 A b'1100 - 60 mA	b'0001 - 30 mA b'0101 - 70 mA b'1001 - 0.75 A b'1101 - 60 mA	b'0010 - 40 mA b'0110 - 80 mA b'1010 - 1.00 A b'1110 - 60 mA	b'0011 - 50 mA b'0111 - 0.25 A b'1011 - 1.25 A b'1111 - 60 mA
3:0	R/W	IDRIVEP_LS	0x4	Low-side gate driver peak source current			
				b'0000 - 10 mA **b'0100 - 50 mA** b'1000 - 0.25 A b'1100 - 50 mA	b'0001 - 20 mA b'0101 - 60 mA b'1001 - 0.50 A b'1101 - 50 mA	b'0010 - 30 mA b'0110 - 70 mA b'1010 - 0.75 A b'1110 - 50 mA	b'0011 - 40 mA b'0111 - 0.125 A b'1011 - 1.00 A b'1111 - 50 mA

7.6.7.3 Gate Drive Control (address = 0x7)

Table 16. Gate Drive Control Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION
10	R/W	Reserved	0x0	
9	R/W	COMM_OPTION	0x1	Rectification control (PWM_MODE = b'10 only) b'0 - diode freewheeling **b'1 - active freewheeling**
8:7	R/W	PWM_MODE	0x0	PWM Mode **b'00 - PWM with 6 independent inputs** b'01 - PWM with 3 independent inputs b'10 - PWM with one input b'11 - PWM with 6 independent inputs
6:4	R/W	DEAD_TIME	0x1	Dead time
				b'000 - 40 ns b'011 - 500 ns b'110 - 4000 ns **b'001 - 60 ns** b'100 - 1000 ns b'111 - 6000 ns b'010 - 100 ns b'101 - 2000 ns
3:2	R/W	TBLANK	0x1	VDS sense blanking b'00 - 0 µs **b'01 - 2 µs** b'10 - 4 µs b'11 - 8 µs
1:0	R/W	TVDS	0x2	VDS sense deglitch b'00 - 0 µs b'01 - 2 µs **b'10 - 4 µs** b'11 - 8 µs

7.6.7.4 IC Operation (address = 0x9)

Table 17. IC Operation Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION
10	R/W	Flip_OTS	0x0	Enable OTS **b'0 - Disable OTS** b'1 - Enable OTS
9	R/W	DIS_VPVDD_UVLO2	0x0	Disable PVDD_UVLO2 fault and reporting **b'0 - PVDD_UVLO2 enabled** b'1 - PVDD_UVLO2 disabled
8	R/W	DIS_GDRV_FAULT	0x0	Disable gate driver fault and reporting **b'0 - Gate driver fault enabled** b'1 - Gate driver fault disabled
7	R/W	EN_SNS_CLAMP	0x0	Enable sense amplifier clamp **b'0 - sense amplifier clamp is not enabled** b'1 - sense amplifier clamp is enabled limiting output to about 3.3 V
6:5	R/W	WD_DLY	0x1	Watch dog delay b'00 - 10 ms **b'01 - 20 ms** b'10 - 50 ms b'11 - 100 ms
4	R/W	DIS_SNS_OCP	0x0	Disable SNS overcurrent protection fault and reporting **b'0 - SNS OCP enabled** b'1 - SNS OCP disabled
3	R/W	WD_EN	0x0	Watch dog enable **b'0 - Watch dog disabled** b'1 - Watch dog enabled
2	R/W	SLEEP	0x0	Put device into sleep mode **b'0 - Device awake** b'1 - Device asleep
1	R/W	CLR_FLTS	0x0	Clear faults **b'0 - Normal operation** b'1 - Clear fault bits
0	R/W	SET_VCPH_UV	0x0	Set charge pump undervoltage threshold level **b'0 - 4.9 V** b'1 - 4.6 V

7.6.7.5 Shunt Amplifier Control (address = 0xA)

Table 18. Shunt Amplifier Control Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION
10	R/W	DC_CAL_CH3	0x1	DC Calibration of CS amplifier 3 **b'0 - Normal operation** b'1 - DC calibration mode
9	R/W	DC_CAL_CH2	0x1	DC Calibration of CS amplifier 2 **b'0 - Normal operation** b'1 - DC calibration mode
8	R/W	DC_CAL_CH1	0x1	DC Calibration of CS amplifier 1 **b'0 - Normal operation** b'1 - DC calibration mode
7:6	R/W	CS_BLANK	0x0	Current shunt amplifier blanking time **b'00 - 0 ns** b'01 - 500 ns b'10 - 2.5 µs b'11 - 10 µs
5:4	R/W	GAIN_CS3	0x0	Gain of CS amplifier 3 **b'00 - 10 V/V** b'01 - 20 V/V b'10 - 40 V/V b'11 - 80 V/V
3:2	R/W	GAIN_CS2	0x0	Gain of CS amplifier 2 **b'00 - 10 V/V** b'01 - 20 V/V b'10 - 40 V/V b'11 - 80 V/V
1:0	R/W	GAIN_CS1	0x0	Gain of CS amplifier 1 **b'00 - 10 V/V** b'01 - 20 V/V b'10 - 40 V/V b'11 - 80 V/V

7.6.7.6 Voltage Regulator Control (address = 0xB)

Table 19. Voltage Regulator Control Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION
10	R/W	Reserved	0x0	
9:8	R/W	VREF_SCALING	0x1	VREF Scaling b'00 - RSVD **b'01 - k = 2** b'10 - k = 4 b'11 - RSVD
7:5	R/W	Reserved	0x0	
4:3	R/W	SLEEP_DLY	0x1	Delay to power down VREG after SLEEP b'00 - 0 µs **b'01 - 10 µs** b'10 - 50 µs b'11 - 1 ms
2	R/W	DIS_VREG_PWRGD	0x0	
0:1	R/W	VREG_UV_LEVEL	0x2	VREG undervoltage set point b'00 - VSET-10% b'01 - VSET-20% **b'10 - VSET-30%** b'11 - VSET-30%

7.6.7.7 VDS Sense Control (address = 0xC)

Table 20. VDS Sense Control Register Description

BIT	R/W	NAME	DEFAULT	DESCRIPTION			
10:8	R/W	Reserved	0x0				
7:3	R/W	VDS_LEVEL	0x19	VDS comparator threshold			
				b'00000 - 0.060 V b'00100 - 0.097 V b'01000 - 0.155 V b'01100 - 0.250 V b'10000 - 0.403 V b'10100 - 0.648 V b'11000 - 1.043 V b'11100 - 1.679 V	b'00001 - 0.068 V b'00101 - 0.109 V b'01001 - 0.175 V b'01101 - 0.282 V b'10001 - 0.454 V b'10101 - 0.730 V **b'11001 - 1.175 V** b'11101 - 1.892 V	b'00010 - 0.076 V b'00110 - 0.123 V b'01010 - 0.197V b'01110 - 0.317 V b'10010 - 0.511 V b'10110 - 0.822 V b'11010 - 1.324 V b'11110 - 2.131 V	b'00011 - 0.086 V b'00111 - 0.138 V b'01011 - 0.222 V b'01111 - 0.358 V b'10011 - 0.576 V b'10111 - 0.926 V b'11011 - 1.491 V b'11111 - 2.131 V
2:0	R/W	VDS_MODE	0x0	VDS mode **b'000 - Latched shut down when over-current detected** b'001 - Report only when over current detected b'010 - VDS protection disabled (no overcurrent sensing or reporting)			

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8305 is a gate driver IC designed to drive a 3-phase BLDC motor in combination with external power MOSFETs. The device provides a high level of integration with three half-bridge gate drivers, three current shunt amplifiers, adjustable slew rate control, logic LDO, and a suite of protection features.

8.2 Typical Application

The following design is a common application of the DRV8305.

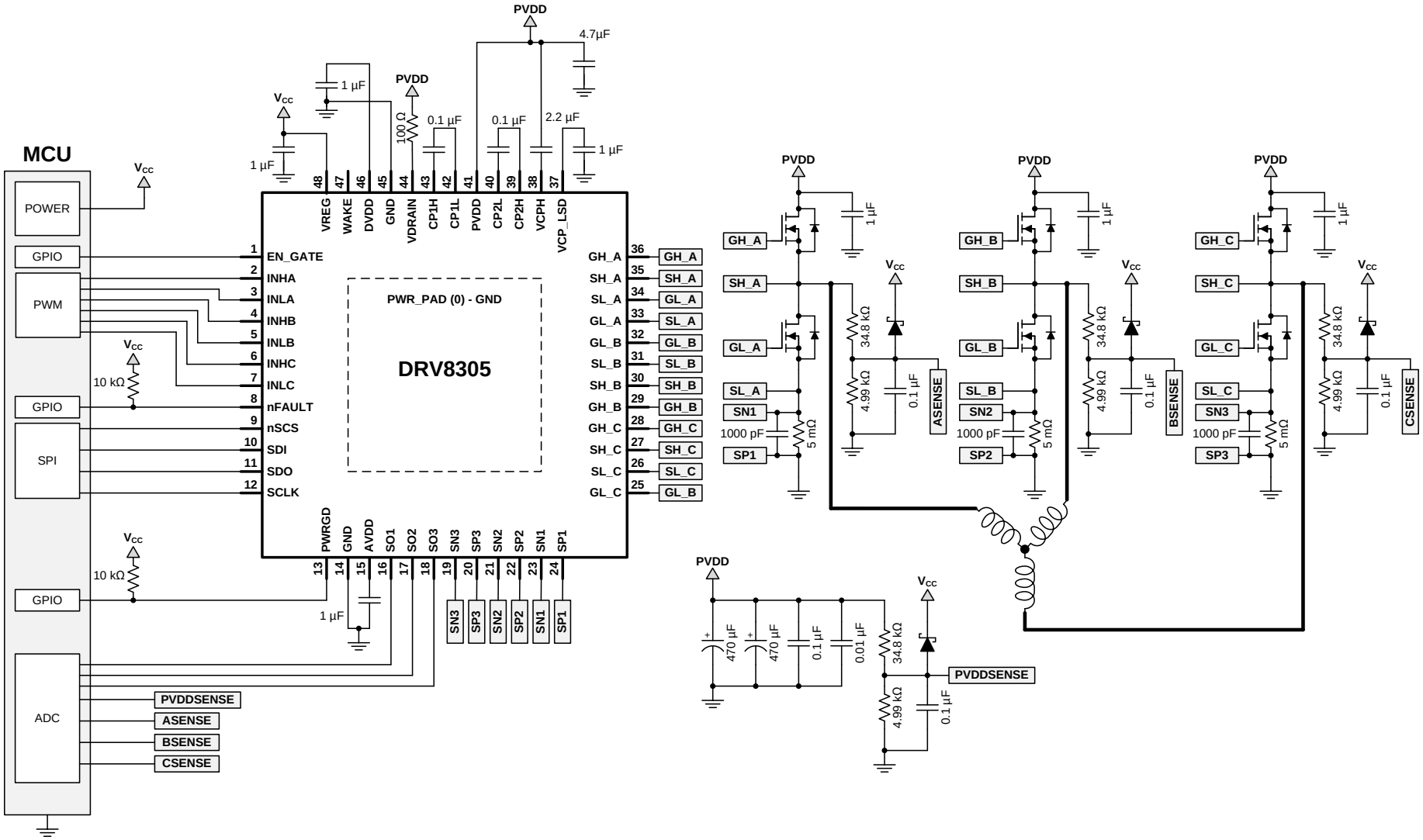


Figure 11. Typical Application Schematic

8.2.1 Design Requirements

Table 21. Design Parameters

DESIGN PARAMETER	REFERENCE	VALUE
Supply voltage	PVDD	12 V
Motor winding resistance	M_R	0.5 Ω
Motor winding inductance	M_L	0.28 mH
Motor poles	M_P	16 poles
Motor rated RPM	M_{RPM}	2000 RPM
Number of MOSFETs switching	N_{SW}	6
Switching frequency	f_{SW}	45 kHz
IDRIVEP	I_{DRIVEP}	50 mA
IDRIVEN	I_{DRIVEN}	60 mA
MOSFET Q_G	Q_g	36 nC
MOSFET Q_{GD}	Q_{GD}	9 nC
MOSFET $R_{DS(on)}$	$R_{DS(on)}$	4.1 mΩ
Target full-scale current	I_{MAX}	30 A
Sense resistor	R_{SENSE}	0.005 Ω
V_{DS} trip level	V_{DS_LVL}	0.197 V
Amplifier bias	V_{BIAS}	1.65 V
Amplifier gain	Gain	10 V/V

8.2.2 Detailed Design Procedure

8.2.2.1 Gate Drive Average Current

The gate drive supply (VCP) of the DRV8305 is capable of delivering up to 30 mA (RMS) of current to the external power MOSFETs. The charge pump directly supplies the high-side N-channel MOSFETs and a 10-V LDO powered from VCP supplies the low-side N-channel MOSFETs. The designer can determine the approximate RMS load on the gate drive supply through the following equation.

$$\text{Gate Drive RMS Current} = \text{MOSFET } Q_g \times \text{Number of Switching MOSFETs} \times \text{Switching Frequency} \quad (2)$$

Example: 36 nC (Q_G) × 6 (N_{SW}) × 45 kHz (f_{SW}) = 9.72 mA

Note that this is only a first-order approximation.

8.2.2.2 MOSFET Slew Rates

The rise and fall times of the external power MOSFET can be adjusted through the use of the DRV8305 IDRIVE setting. A higher IDRIVE setting will charge the MOSFET gate more rapidly where a lower IDRIVE setting will charge the MOSFET gate more slowly. System testing requires fine tuning to the desired slew rate, but a rough first-order approximation can be calculated as shown in the following.

$$\text{MOSFET Slew Rate} = \text{MOSFET } Q_{GD} / \text{IDRIVE Setting} \quad (3)$$

Example: 9 nC (Q_{GD}) / 50 mA (IDRIVEP) = 180 ns

8.2.2.3 Overcurrent Protection

The DRV8305 provides overcurrent protection for the external power MOSFETs through the use of VDS monitors for both the high-side and low-side MOSFETs. These are intended for protecting the MOSFET in overcurrent conditions and are not for precise current regulation.

The overcurrent protection works by monitoring the VDS voltage drop of the external MOSFETs and comparing it against the internal VDS_LEVEL set through the SPI registers. The high-side VDS is measured across the VDRAIN and SH_X pins. The low-side VDS is measured across the SH_X and SL_X pins. If the VDS voltage exceeds the VDS_LEVEL value, the DRV8305 will take action according to the VDS_MODE register.

The overcurrent trip level can be determined with the MOSFET $R_{DS(on)}$ and the VDS_LEVEL setting.

$$\text{Overcurrent Trip} = \text{VDS Level (VDS\_LVL)} / \text{MOSFET } R_{DS(on)} \ (R_{DS(on)}) \quad (4)$$

Example: 0.197 V (VDS_LVL) / 4.1 mΩ ($R_{DS(ON)}$) = 48 A

8.2.2.4 Current Sense Amplifiers

The DRV8305 provides three bidirectional low-side current shunt amplifiers. These can be used to sense the current flowing through each half-bridge. If individual half-bridge sensing is not required, a single current shunt amplifier can be used to measure the sum of the half-bridge current. Use this simple procedure to correctly configure the current shunt amplifiers.

1. Determine the peak current that the motor will demand (IMAX). This demand depends on the motor parameters and the application requirements. IMAX in this example is 14 A.
2. Determine the available voltage output range for the current shunt amplifiers. This will be the ± voltage around the amplifier bias voltage (VBIAS). In this case VBIAS = 1.65 V and a valid output voltage is 0 to 3.3 V. This gives an output range of ±1.65 V.
3. Determine the sense resistor value and amplifier gain settings. The sense resistor value and amplifier gain have common tradeoffs. The larger the sense resistor value, the better the resolution of the half-bridge current. This comes at the cost of additional power dissipated from the sense resistor. A larger gain value allows for the use of a smaller resolution, but at the cost of increased noise in the output signal and a longer settling time. This example uses a 5-mΩ sense resistor and the minimum gain setting of the DRV8305 (10 V/V). These values allow the current shunt amplifiers to measure ±33 A across the sense resistor.

8.2.3 Application Curves

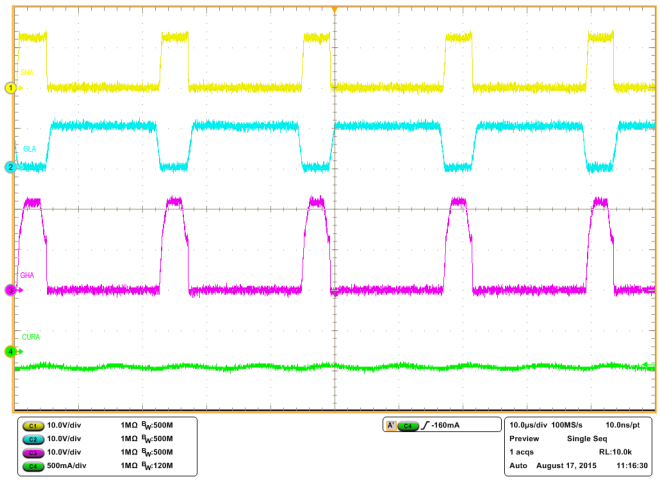


Figure 12. Gate Drive 20% Duty Cycle

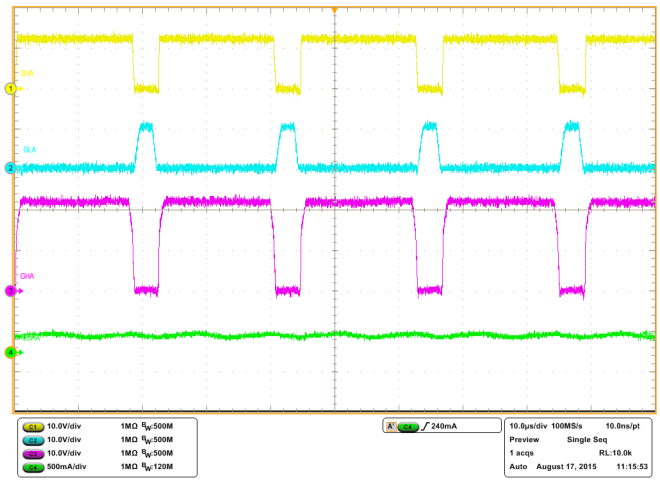


Figure 13. Gate Drive 80% Duty Cycle

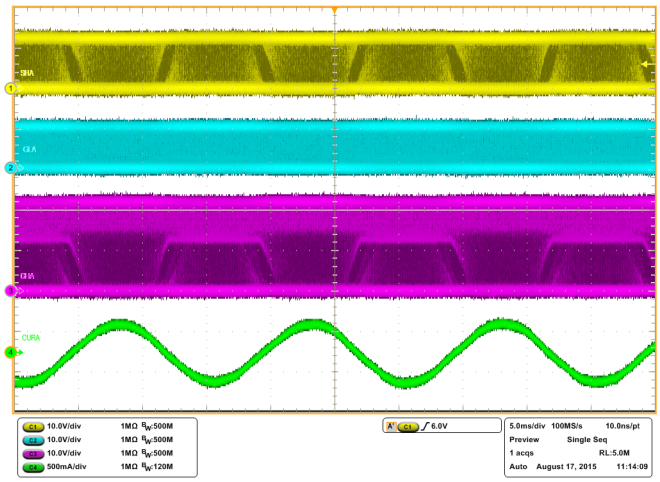


Figure 14. Motor Spinning 1000 RPM

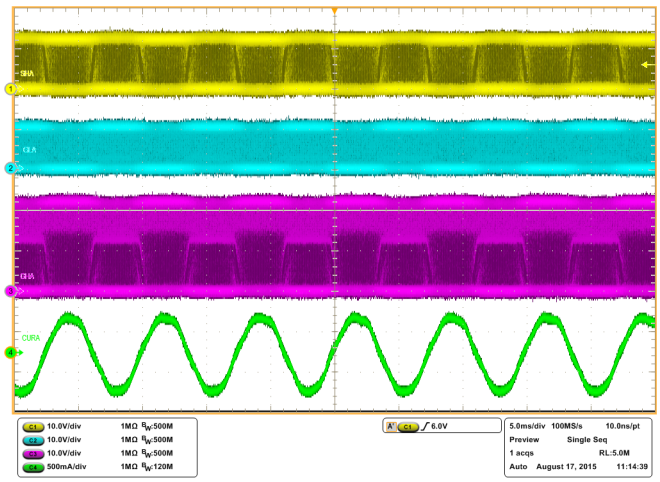


Figure 15. Motor Spinning 2000 RPM

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including the:

- Highest current required by the motor system
- Power supply's capacitance and ability to source or sink current
- Amount of parasitic inductance between the power supply and motor system
- Acceptable voltage ripple
- Type of motor used (brushed DC, brushless DC, stepper)
- Motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate-sized bulk capacitor.

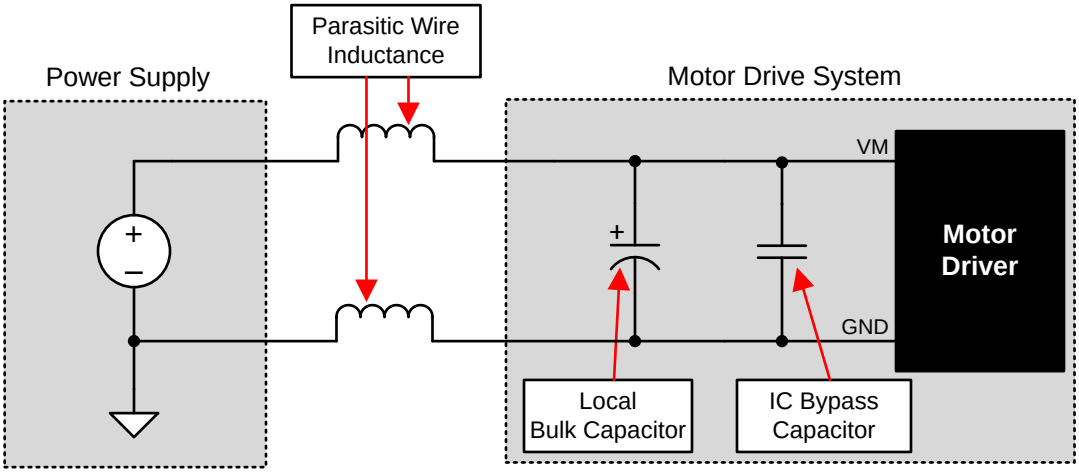


Figure 16. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

Use the following layout recommendations when designing a PCB for the DRV8305.

- The DVDD and AVDD 1-µF bypass capacitors should connect directly to the adjacent GND pin to minimize loop impedance for the bypass capacitor.
- The CP1 and CP2 0.047-µF flying capacitors should be placed directly next to the DRV8305 charge pump pins.
- The VCPH 2.2-µF and VCP_LSD 1-µF bypass capacitors should be placed close to their corresponding pins with a direct path back to the DRV8305 GND net.
- The PVDD 4.7-µF bypass capacitor should be placed as close as possible to the DRV8305 PVDD supply pin.
- Use the proper footprint as shown in the *机械、封装和可订购信息* section.
- Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the DRV8305 GH_X to the power MOSFET and returns through SH_X. The low-side loop is from the DRV8305 GL_X to the power MOSFET and returns through SL_X.

10.2 Layout Example

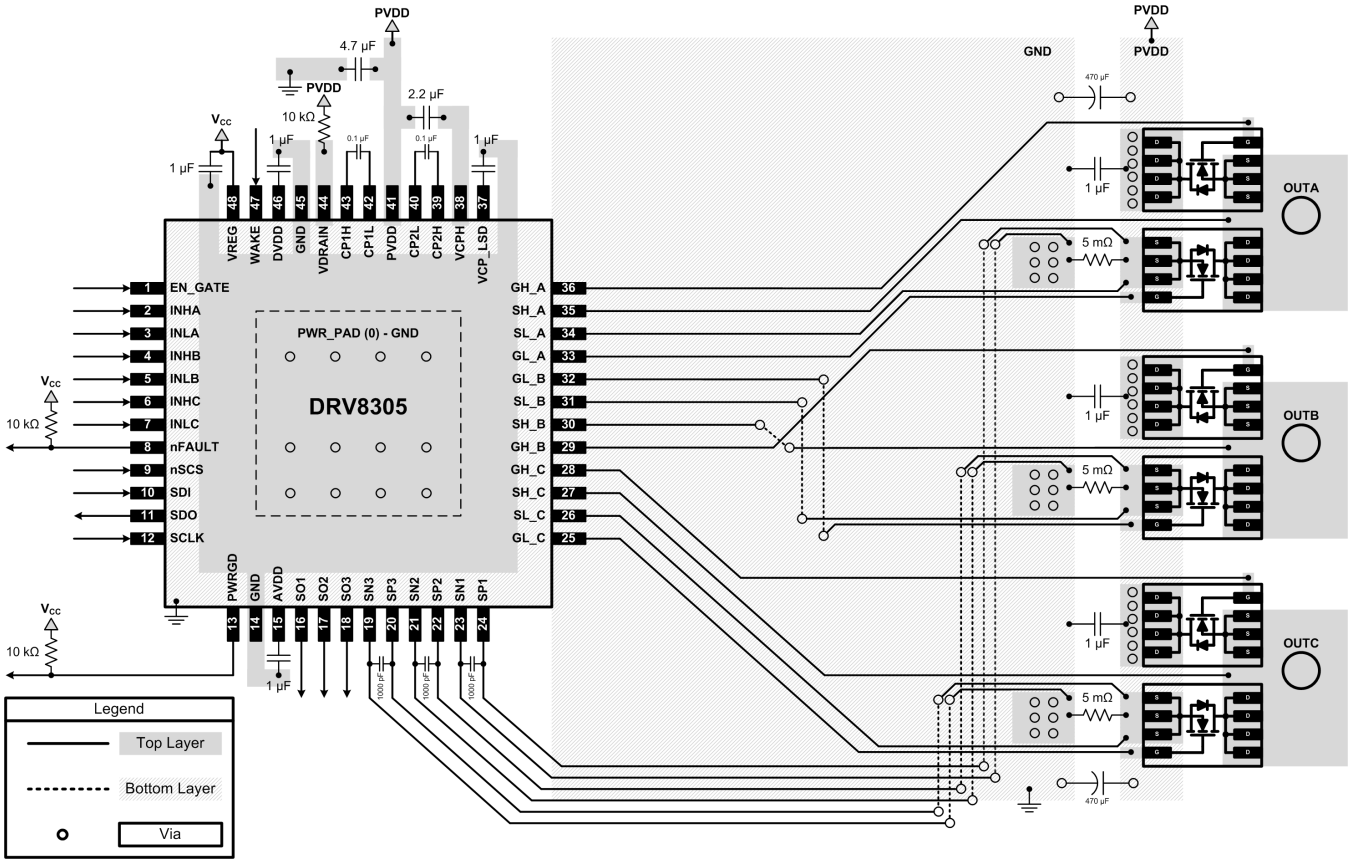


Figure 17. Layout Recommendation

11 器件和文档支持

11.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV83053PHP	ACTIVE	HTQFP	PHP	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV83053	Samples
DRV83053PHPR	ACTIVE	HTQFP	PHP	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV83053	Samples
DRV83055PHP	ACTIVE	HTQFP	PHP	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV83055	Samples
DRV83055PHPR	ACTIVE	HTQFP	PHP	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV83055	Samples
DRV8305NPHP	ACTIVE	HTQFP	PHP	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8305N	Samples
DRV8305NPHPR	ACTIVE	HTQFP	PHP	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8305N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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GENERIC PACKAGE VIEW

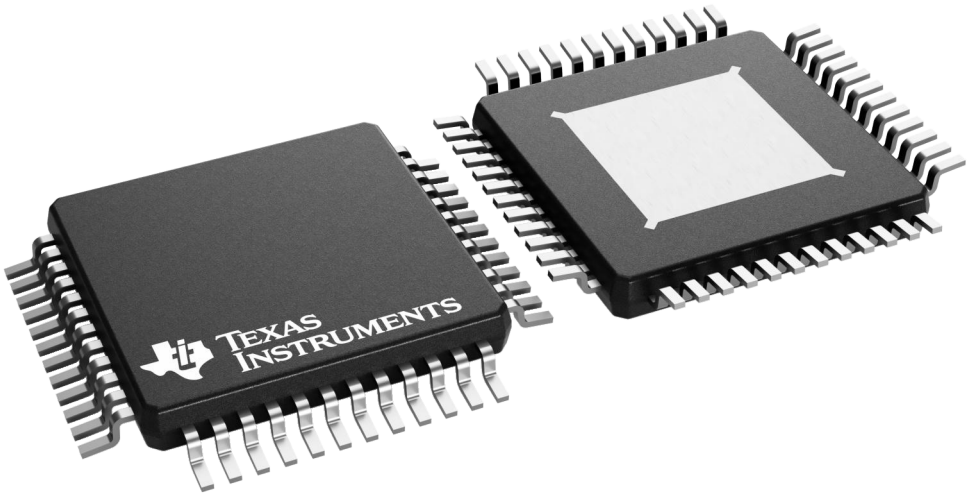
PHP 48

TQFP - 1.2 mm max height

7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



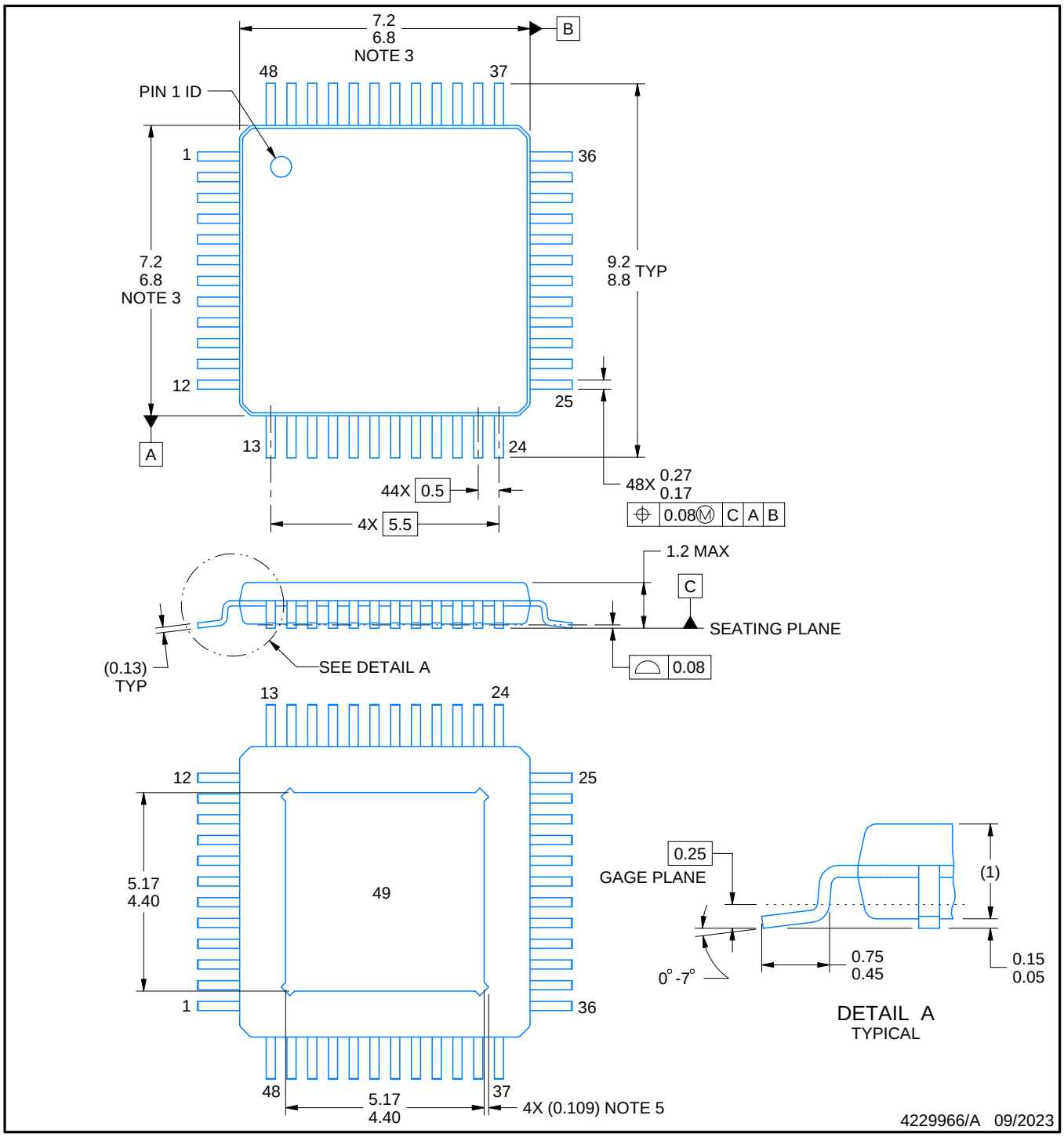
4226443/A

PACKAGE OUTLINE

PHP0048N

PowerPAD™ HTQFP - 1.2 mm max height

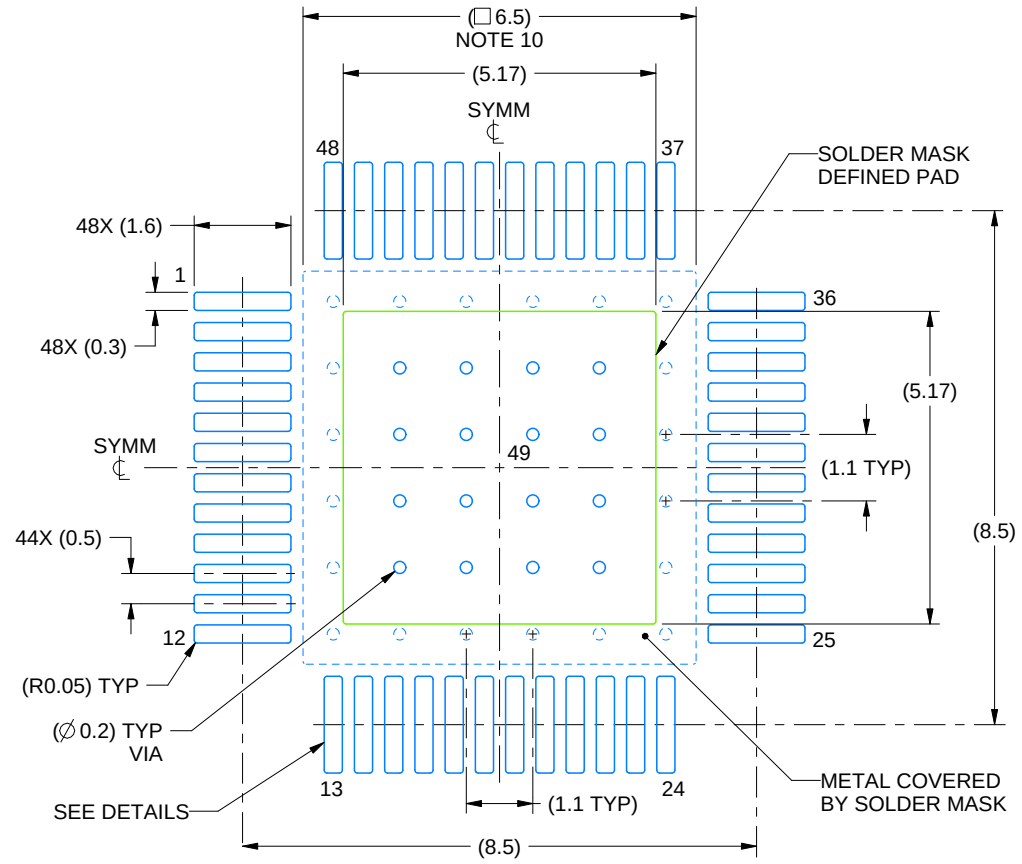
PLASTIC QUAD FLATPACK



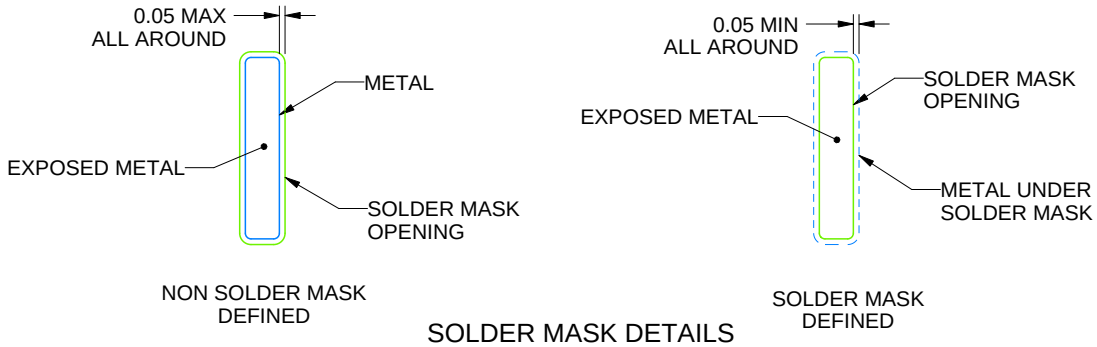
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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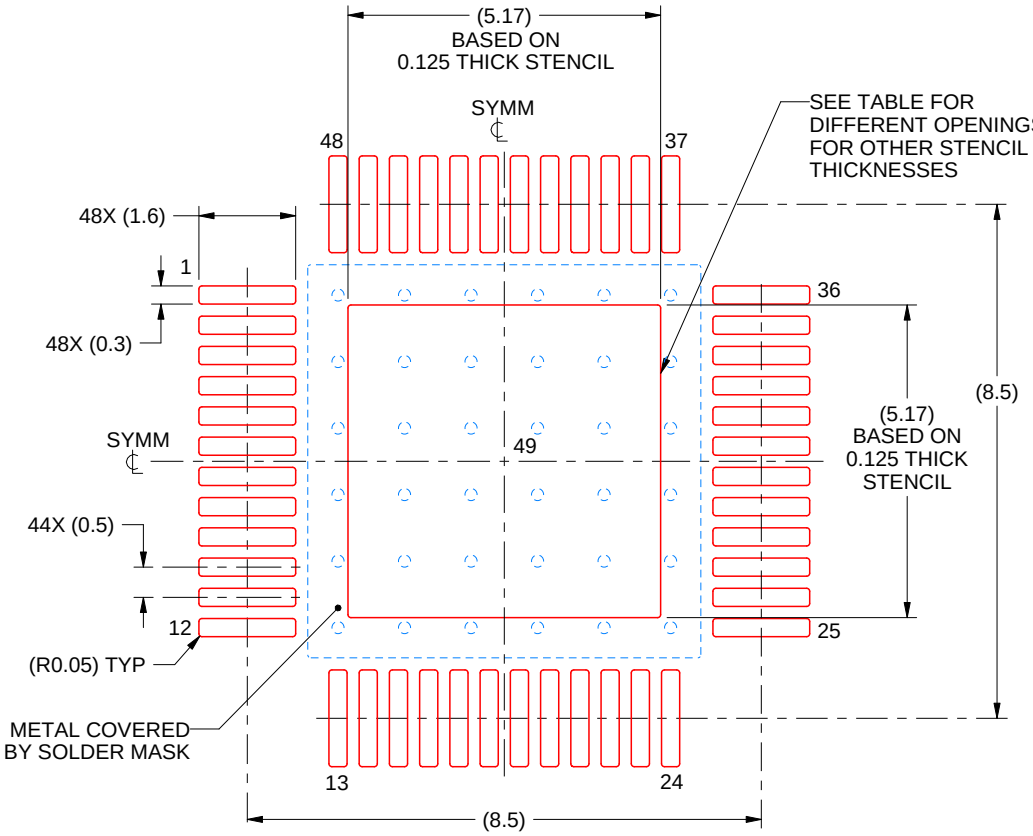
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5.78 X 5.78
0.125	5.17 X 5.17 (SHOWN)
0.150	4.72 X 4.72
0.175	4.37 X 4.37

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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