

DRV8806 四通道串行接口低侧驱动器 IC

1 特性

- 4 通道受保护低侧驱动器
 - 4 个具有过流保护功能的 NMOS 场效应晶体管 (FET)
 - 集成感应钳位二极管
 - 串行接口
 - 开路/短路负载检测
- 每通道最大 2A 驱动电流（单通道打开）/ 1A（所有通道打开）（25°C 时）
- 8.2V 至 40V 运行电源电压范围
- 耐热增强型表面贴装

2 应用

- 继电器驱动器
- 单极步进电机驱动器
- 螺线管驱动器
- 常见低侧开关 应用

3 说明

DRV8806 提供了一个具有过流保护的 4 通道低侧驱动器。它具有内置的用来钳制由电感负载生成的关闭瞬态的二极管，可被用于驱动单极步进电机、直流电机、继电器、螺线管、或者其它负载。

DRV8806 能够提供高达 2A（单通道打开）或者 1A（所有通道打开）持续输出电流（25°C 时有足够的印刷电路板 (PCB) 散热）

提供一个用于控制输出驱动器的串行接口。可通过串行接口读取故障状态。多个 DRV8806 器件可被连在一起共同使用一个单一串行串口。

内置的关断功能可提供过流保护、短路保护、欠压闭锁和过热保护，具体故障由故障输出引脚来指示。

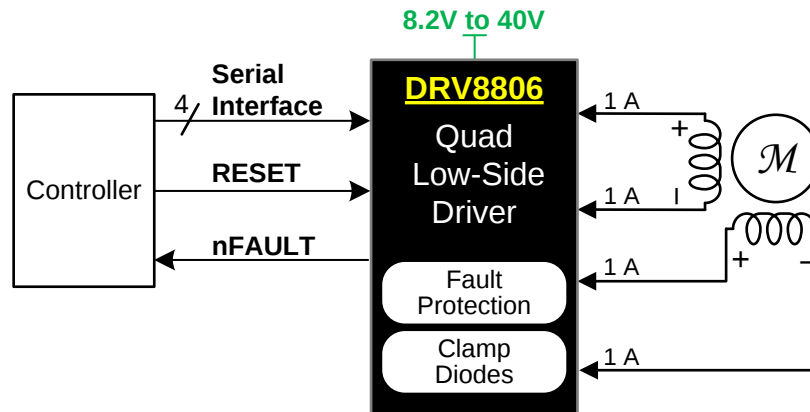
DRV8806 采用 16 引脚散热薄型小外形尺寸 (HTSSOP) 封装（环境友好型：符合 RoHS 标准且无镉/无溴）。

器件信息⁽¹⁾

器件型号	封装	封装尺寸（标称值）
DRV8806	HTSSOP (16)	5.00mm x 4.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (December 2013) to Revision C Page

• 已添加 ESD 额定值表，特性 描述 部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分	1
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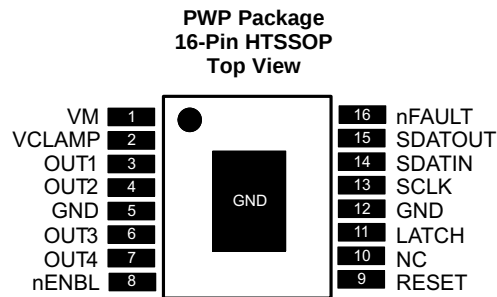
Changes from Revision A (November 2013) to Revision B Page

• Changed (OPEN-DRAIN to PUSH-PULL in the elec chara table section SDATAOUT OUTPUT	5
• Added another row below V_{OH} - merge the first two columns together (V_{OH} and Output high voltage). The second row should have test condition " $I_o = 100 \mu A$, $V_M = 8.2 V$ " and be specified as 2.5 V MIN	5
• Added two new rows, I_{SRC} and I_{SNK} in elec chara table, section SDATAOUT OUTPUT	5
• Changed NO. 6 in Timing Requirements table	6
• Added a sentence in second paragraph below Figure 2: A pullup resistor.....1 kohm is recommended.	10

Changes from Original (June 2012) to Revision A Page

• Added comment to Timing Requirements section.....	6
• Changed Functional Block Diagram at SDATOUT	8
• Changed Figure 6 at SDATOUT	10
• Changed SDATOUT description in Serial Interface Operation section	10

5 Pin Configuration and Functions



Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
POWER AND GROUND				
GND	5, 12, PowerPAD™	—	Device ground	All pins must be connected to GND.
VM	1	—	Device power supply	Connect to motor supply (8.2 V - 40 V).
CONTROL				
LATCH	11	I	Latch input	Rising edge latches shift register to output stage, falling edge latches fault data into output shift register – internal pulldown
nENBL	8	I	Enable input	Active low enables outputs – internal pulldown
RESET	9	I	Reset input	Active-high reset input initializes internal logic – internal pulldown
SCLK	13	I	Serial clock	Serial clock input – internal pulldown
SDATIN	14	I	Serial data input	Serial data input – internal pulldown
SDATOUT	15	OD	Serial data output	Serial data output; push-pull structure; see serial interface section for details
STATUS				
nFAULT	16	OD	Fault	Logic low when in fault condition (overtemperature, overcurrent, open load) - open-drain output
OUTPUT				
OUT1	3	O	Output 1	Connect to load 1
OUT2	4	O	Output 2	Connect to load 2
OUT3	6	O	Output 3	Connect to load 3
OUT4	7	O	Output 4	Connect to load 4
VCLAMP	2	—	Output clamp voltage	Connect to VM supply, or zener diode to VM supply

(1) Directions: I = input, O = output, OD = open-drain output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
V _M	Power supply voltage	–0.3	43	V
V _{OUTx}	Output voltage	–0.3	43	V
V _{CLAMP}	Clamp voltage	–0.3	43	V
SDATOUT, nFAULT	Output current		20	mA
	Peak clamp diode current ⁽³⁾		2	A
	DC or RMS clamp diode current ⁽³⁾		1	A
	Digital input pin voltage	–0.5	7	V
SDATOUT, nFAULT	Digital output pin voltage	–0.5	7	V
	Peak motor drive output current, t < 1 μS	Internally limited		A
	Continuous total power dissipation ⁽³⁾	See Thermal Information		
T _J	Operating virtual junction temperature ⁽³⁾	–40	150	°C
T _{stg}	Storage temperature	–60	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) Power dissipation and thermal limits must be observed.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge		
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±6000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V _M	Power supply voltage	8.2		40	V
V _{CLAMP}	Output clamp voltage ⁽¹⁾	0		40	V
I _{OUT}	Continuous output current, single channel on, T _A = 25°C ⁽²⁾			2	A
	Continuous output current, four channels on, T _A = 25°C ⁽²⁾			1	A

- (1) V_{CLAMP} is not a power supply input pin - it only connects to the output clamp diodes.
- (2) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DRV8806	UNIT
		PWP (HTSSOP)	
		16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	39.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	24.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	20.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ _{JB}	Junction-to-board characterization parameter	20.1	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES					
I _{VM}	VM operating supply current V _M = 24 V		1.6	3	mA
V _{UVLO}	VM undervoltage lockout voltage V _M rising			8.2	V
LOGIC-LEVEL INPUTS (SCHMITT TRIGGER INPUTS WITH HYSTERESIS)					
V _{IL}	Input low voltage			0.8	V
V _{IH}	Input high voltage	2			V
V _{HYS}	Input hysteresis		0.45		V
I _{IL}	Input low current V _{IN} = 0	–20		20	μA
I _{IH}	Input high current V _{IN} = 3.3 V			100	μA
R _{PD}	Pulldown resistance		100		kΩ
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)					
V _{OL}	Output low voltage I _O = 5 mA			0.5	V
I _{OH}	Output high leakage current V _O = 3.3 V			1	μA
SDATOUT OUTPUT (PUSH-PULL OUTPUT WITH INTERNAL PULLUP)					
V _{OL}	Output low voltage I _O = 5 mA		0.5		V
V _{OH}	Output high voltage I _O = 100 μA, V _M = 11 V - 60 V, peak			6.5	V
	I _O = 100 μA, V _M = 11 V - 60 V, steady state	3.3	4.5	5.6	
	I _O = 100 μA, V _M = 8.2 V - 11 V, steady state	2.5			V
I _{SRC}	Output source current V _M = 24 V			1	mA
I _{SNK}	Output sink current V _M = 24 V			5	mA
LOW-SIDE FETS					
R _{DS(ON)}	FET on resistance V _M = 24 V, I _O = 700 mA, T _J = 25°C		0.5		Ω
	V _M = 24 V, I _O = 700 mA, T _J = 85°C		0.75	0.8	
I _{OFF}	Open load detect current	0	25	50	μA
HIGH-SIDE DIODES					
V _F	Diode forward voltage V _M = 24 V, I _O = 700 mA, T _J = 25°C		0.9		V
I _{OFF}	Off state leakage current V _M = 24 V, T _J = 25°C	–50		50	μA
OUTPUTS					
t _R	Rise time V _M = 24 V, I _O = 700 mA, Resistive load	50		300	ns
t _F	Fall time V _M = 24 V, I _O = 700 mA, Resistive load	50		150	ns
PROTECTION CIRCUITS					
I _{OC}	Overcurrent protection trip level	3		5	A

Electrical Characteristics (continued)

$T_A = 25^\circ\text{C}$, over recommended operating conditions (unless otherwise noted)

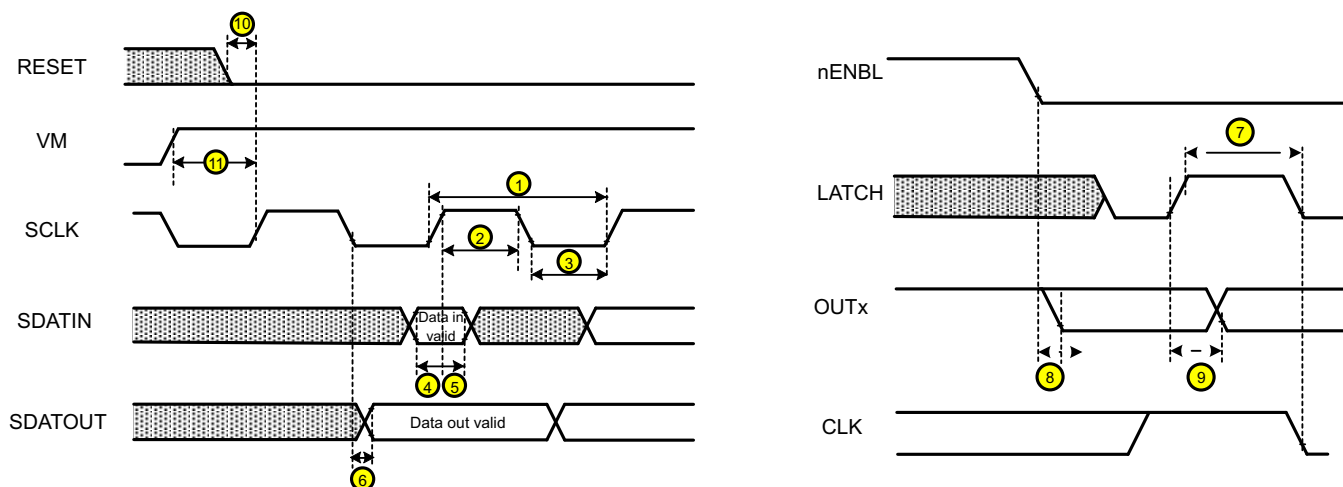
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OCP} Overcurrent protection deglitch time			3.5		μs
t_{OL} Open load detect deglitch time			15		μs
t_{RETRY} Overcurrent protection re-try time			1.2		ms
T_{TSD} Thermal shutdown temperature	Die temperature	150	160	180	$^\circ\text{C}$

6.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	NOM	MAX	UNIT
1	t_{CYC} Clock cycle time	62			ns
2	t_{CLKH} Clock high time	25			ns
3	t_{CLKL} Clock low time	25			ns
4	$t_{\text{SU}}(\text{SDATIN})$ Setup time, SDATIN to SCLK	5			ns
5	$t_{\text{H}}(\text{SDATIN})$ Hold time, SDATIN to SCLK	1			ns
6	$t_{\text{D}}(\text{SDATOUT})$ Delay time, SCLK to SDATOUT, no external pullup resistor, $C_{\text{OUT}} = 100 \text{ pF}$		50	100	ns
7	$t_{\text{W}}(\text{LATCH})$ Pulse width, LATCH	200			ns
8	$t_{\text{OE}}(\text{ENABLE})$ Enable time, nENBL to output low		60		ns
9	$t_{\text{D}}(\text{LATCH})$ Delay time, LATCH to output change		200		ns
—	t_{RESET} RESET pulse width	20			μs
10	$t_{\text{D}}(\text{RESET})$ Reset delay before clock	20			μs
11	t_{STARTUP} Start-up delay VM applied before clock	55			μs

(1) Not production tested.



More than 400 ns of delay should exist between the final SCLK rising edge and the LATCH rising edge. This ensures that the last data bit is shifted into the device properly.

Figure 1. DRV8806 Timing Requirements

6.7 Typical Characteristics

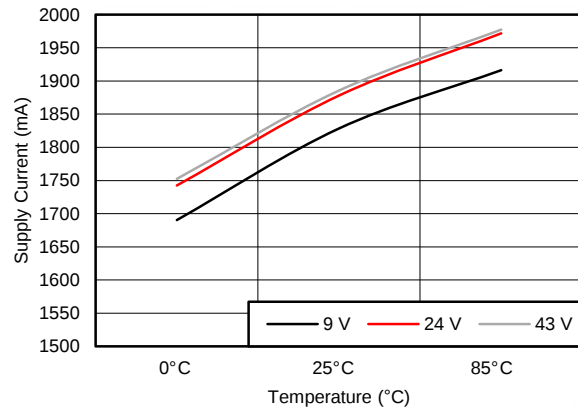


Figure 2. Supply Current vs Temperature

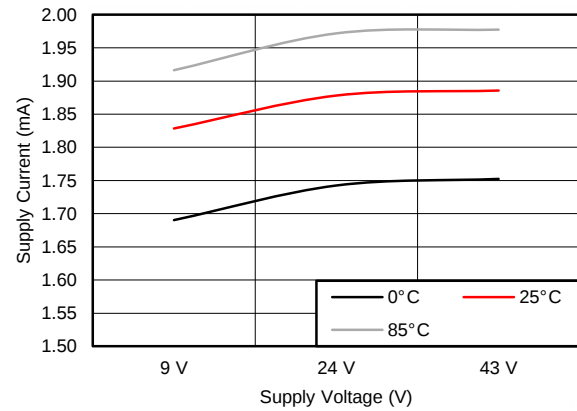


Figure 3. Supply Current vs Supply Voltage

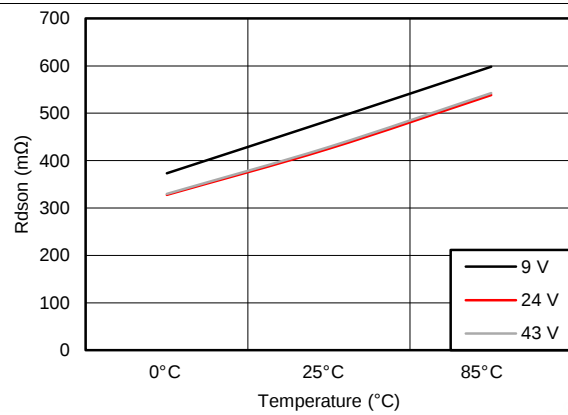


Figure 4. $R_{DS(ON)}$ vs Temperature

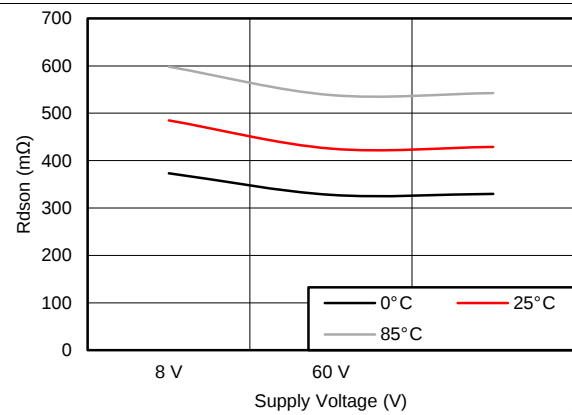


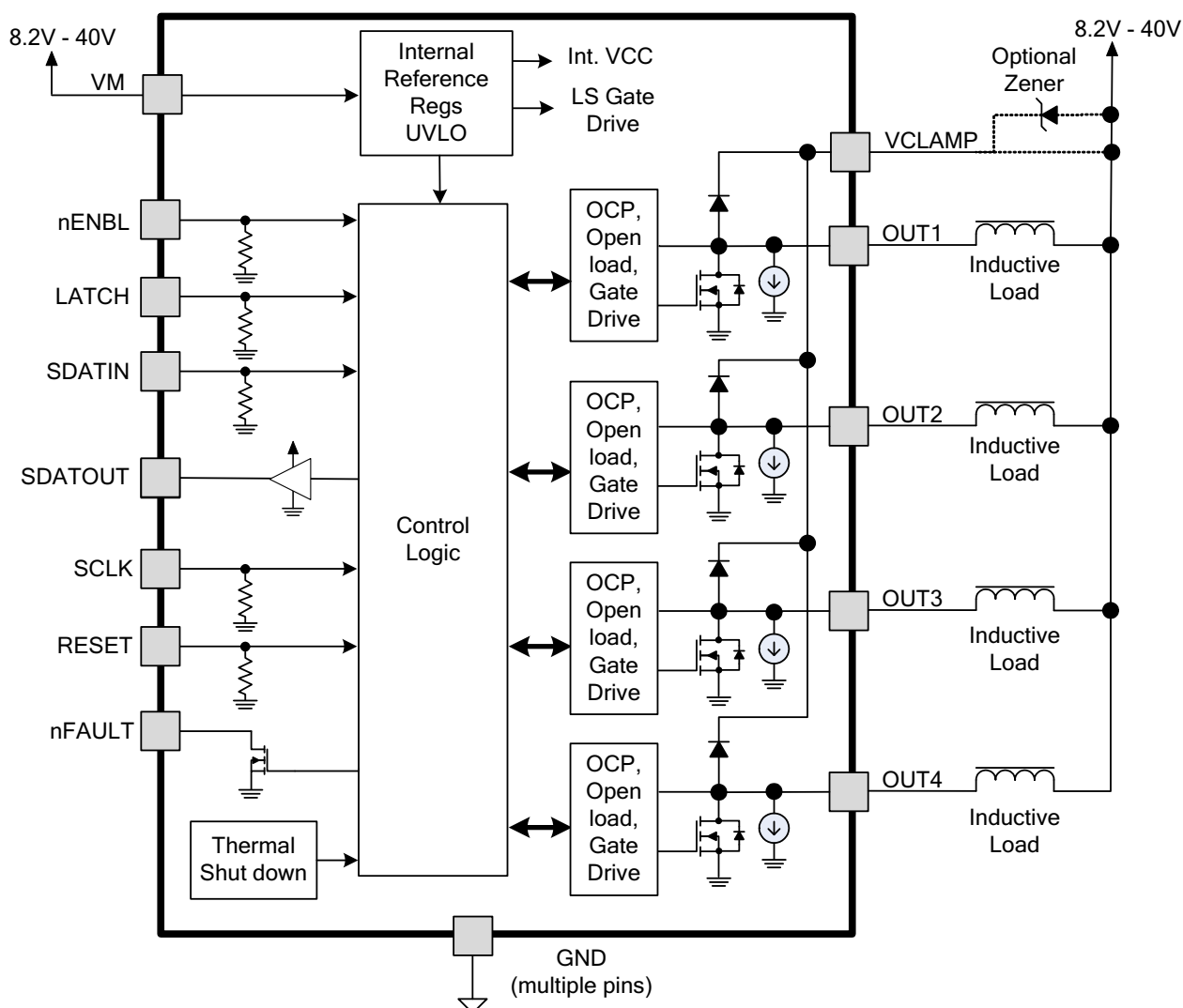
Figure 5. $R_{DS(ON)}$ vs Supply Voltage

7 Detailed Description

7.1 Overview

The DRV8806 is an integrated 4-channel low-side driver controlled using a serial interface to change the state of the low-side driver outputs. The low-side driver outputs consist of four N-channel MOSFETs that have a typical $R_{DS(ON)}$ of 500 m Ω . A single motor supply input VM serves as device power and is internally regulated to power the low-side gate drive. Data is shifted into a temporary data register in the device through the SDATIN pin, one bit at each rising edge of SCLK, while LATCH is held low. The outputs of the device can be disabled by pulling nENBL logic high. Several safety features are integrated in the device including overcurrent protection, thermal shutdown, undervoltage lockout, and open load protection. The overcurrent protection and open load faults share a fault bit per channel that is set when one of these conditions occurs.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Drivers

The DRV8806 contains four protected low-side drivers. Each output has an integrated clamp diode connected to a common pin, VCLAMP.

VCLAMP can be connected to the main power supply voltage, V_M . It can also be connected to a Zener or TVS diode to V_M , allowing the switch voltage to exceed the main supply voltage V_M . This connection can be beneficial when driving loads that require very fast current decay, such as unipolar stepper motors.

In all cases, the voltage on the outputs must not be allowed to exceed the maximum output voltage specification.

7.3.2 Protection Circuits

The DRV8806 is fully protected against undervoltage, overcurrent and overtemperature events.

7.3.2.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the t_{OCP} deglitch time (approximately 3.5 μ s), the driver will be disabled and the nFAULT pin will be driven low. The driver will remain disabled for the t_{RETRY} retry time (approximately 1.2 ms), then the fault will be automatically cleared. The fault will be cleared immediately if either RESET pin is activated or V_M is removed and reapplied.

7.3.2.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all output FETs will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level, operation will automatically resume.

7.3.2.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the V_M pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and internal logic will be reset. Operation will resume when V_M rises above the UVLO threshold.

7.4 Device Functional Modes

7.4.1 Serial Interface Operation

The DRV8806 is controlled with a simple serial interface. Logically, the interface is shown in [Figure 6](#).

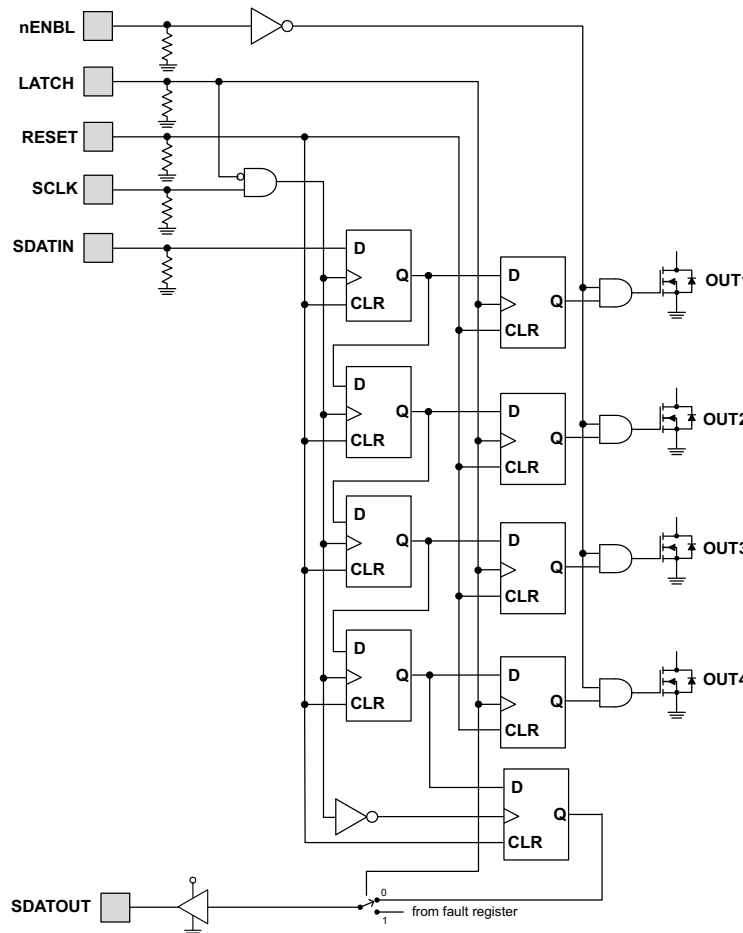


Figure 6. Serial Interface Operation

Data is shifted into a temporary holding shift register in the part using the SDATIN pin, one bit at each rising edge of the SCLK pin, while LATCH is low. Data is shifted from the last bit to the SDATOUT pin, so multiple devices may be daisy-chained together using a single serial interface.

Note that the SDATOUT pin has a push-pull driver, which can support driving another DRV8806 SDATIN pin at clock frequencies of up to 1 MHz without an external pullup. A pullup resistor can be used between SDATOUT and an external 5-V logic supply to support higher clock frequencies. TI recommends a resistor value of approximately 1 k Ω . The SDATOUT pin is capable of approximately 1-mA source and 5-mA sink. To supply logic signals to a lower-voltage microcontroller, use a resistor divider from SDATOUT to GND.

A rising edge on the LATCH pin latches the data from the temporary shift register into the output stage.

Device Functional Modes (continued)

7.4.2 Fault Output Register

The DRV8806 contains circuitry to detect open or shorted loads. The status of the loads can be read through the serial interface. The logic is shown in Figure 7.

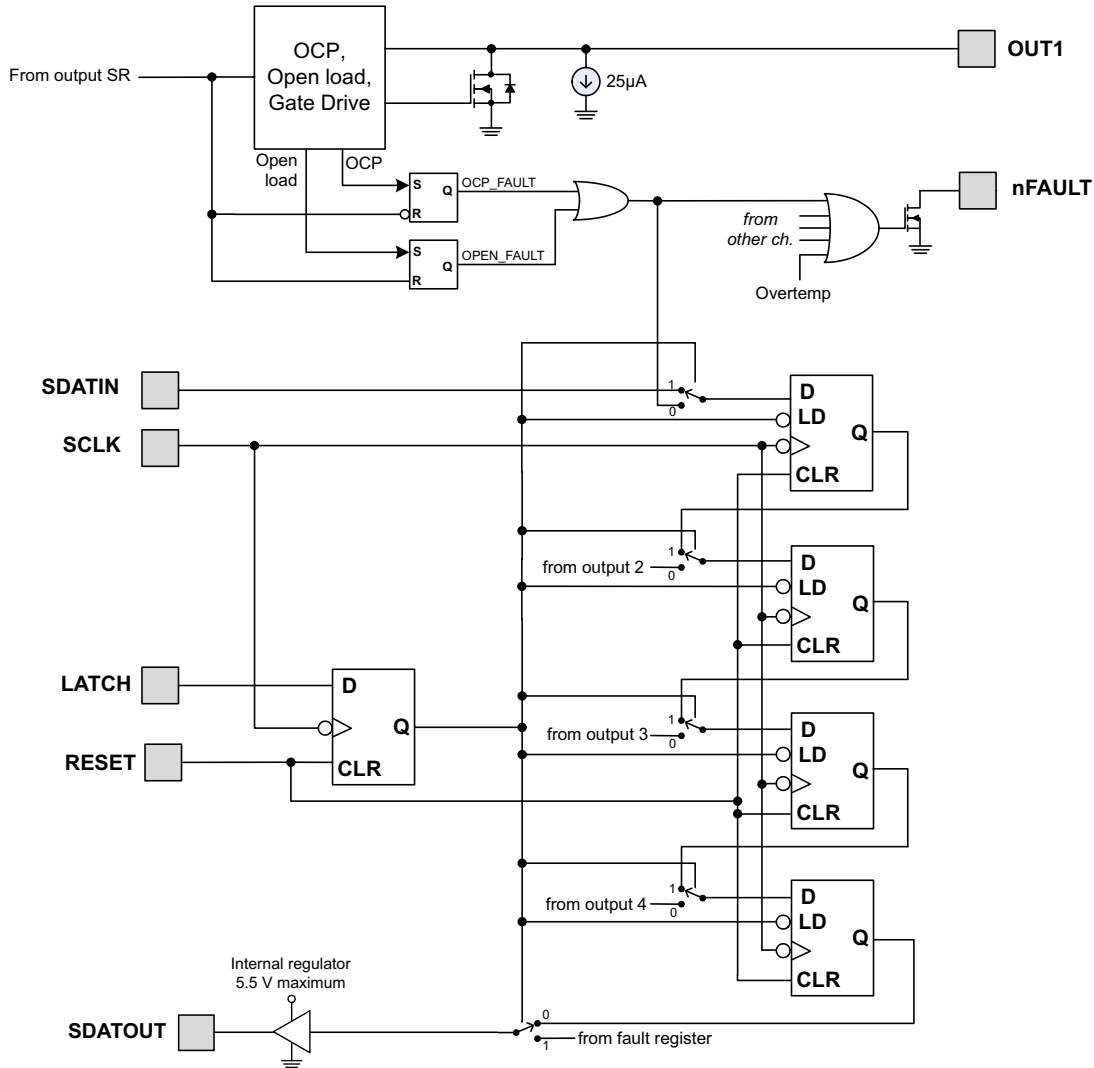


Figure 7. Fault Output

To overcome any leakage currents to accurately sense an open load, a small current source is connected to each output pin. This source pulls approximately 25-µA of current to ground. The voltage on the output pin is sensed during the time that the output is off, and if the voltage on the pin is less than 1.2 V (indicating that there is no load connected) after the open load deglitch time, the OPEN_FAULT latch is set. This latch is cleared whenever the output bit is set.

When the output is turned on, if an overcurrent (OCP) fault is detected, the channel will be turned off and the OCP_FAULT latch is set. This latch will be cleared whenever the output bit is cleared.

The state of the OCP_FAULT and OPEN_FAULT signals is combined into a single fault bit per channel, and loaded into a shift register while the LATCH pin is low. When the LATCH pin is taken high, the fault data is latched into the shift register at the first falling edge of SCLK. Data may then be shifted out on the SDATOUT pin on each falling edge of the SCLK pin.

Note that the LATCH signal must be high for a minimum of 200 ns before valid data can be clocked out.

Device Functional Modes (continued)

The nFAULT pin will be driven active low whenever any of the OCP_FAULT or OPEN_FAULT latches are set, as well as whenever there is an overtemperature condition.

7.4.3 Daisy-Chain Connection

Two or more DRV8806 devices may be connected together to use a single serial interface. The SDATOUT pin of the first device in the chain is connected to the SDATIN pin of the next device. The SCLK, LATCH, RESET, and nFAULT pins are connected together.

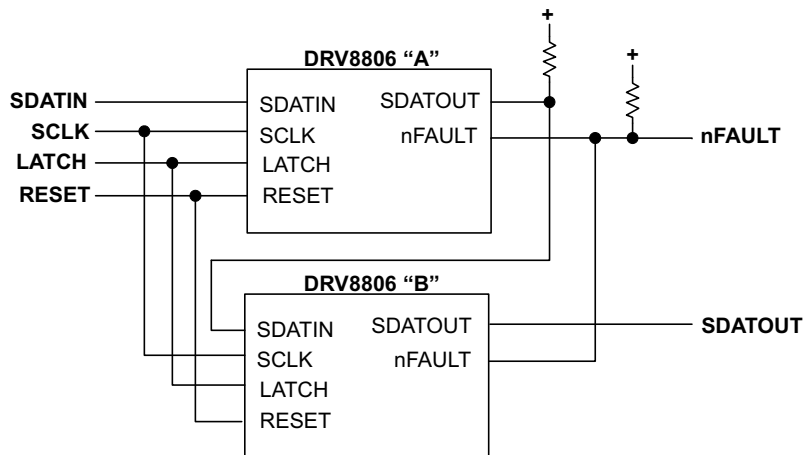


Figure 8. Daisy-Chain Connection

Figure 9 shows an example of a serial transaction, writing the output bits, and then reading the fault status bits, using two devices connected together in a daisy-chain.

Note that the LATCH signal must be high for a minimum of 200 ns before valid data can be clocked out.

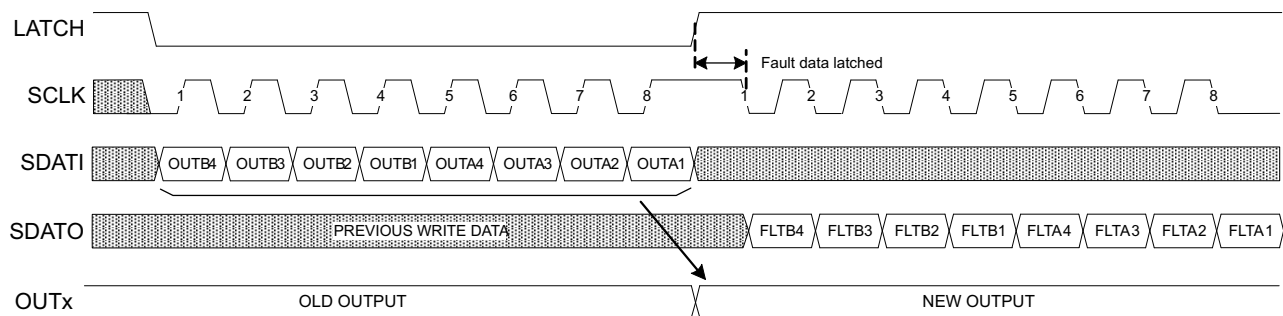


Figure 9. Daisy-Chain Serial Transaction

7.4.4 nENBL and RESET Operation

The nENBL pin enables or disables the output drivers. nENBL must be low to enable the outputs. nENBL does not affect the operation of the serial interface logic. Note that nENBL has an internal pulldown.

The RESET pin, when driven active high, resets internal logic, including the OCP fault. All serial interface registers are cleared. Note that RESET has an internal pulldown. An internal power-up reset is also provided, so it is not required to drive RESET at power up.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8806 can be used to drive one unipolar stepper motor.

8.2 Typical Application

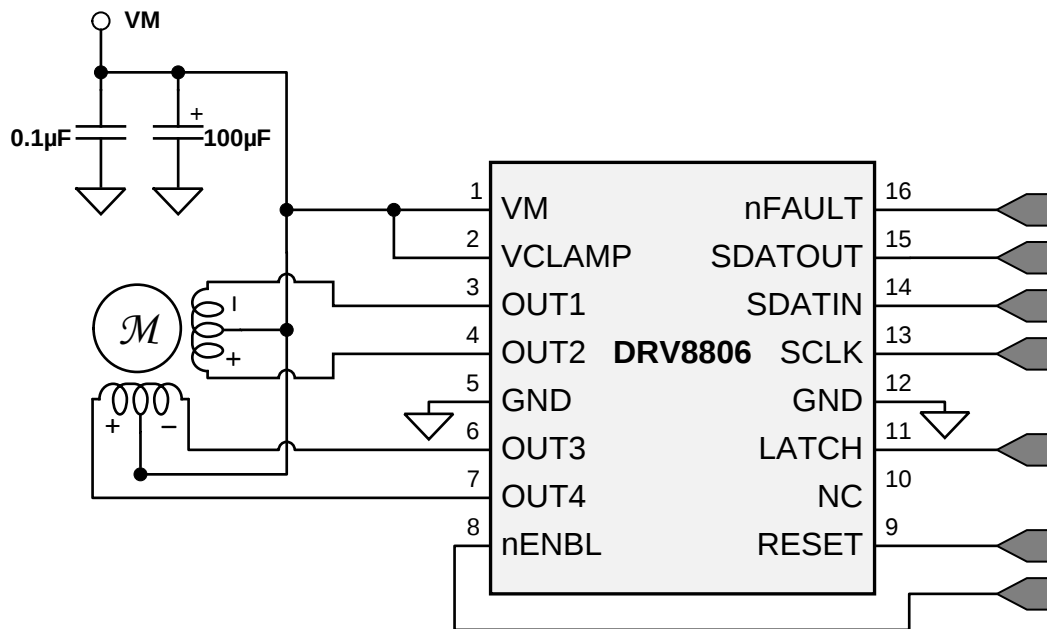


Figure 10. DRV8806 Typical Application

8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage, V_M	24 V
Motor winding resistance, R_L	7.4 Ω /phase
Motor full step angle, θ_{step}	1.8°/step
Motor rated current, I_{RATED}	0.75 A
SCLK frequency, f_{SCLK}	1 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The motor voltage to use will depend on the ratings of the motor selected and the desired torque. A higher voltage shortens the current rise time in the coils of the stepper motor allowing the motor to produce a greater average torque. Using a higher voltage also allows the motor to operate at a faster speed than a lower voltage.

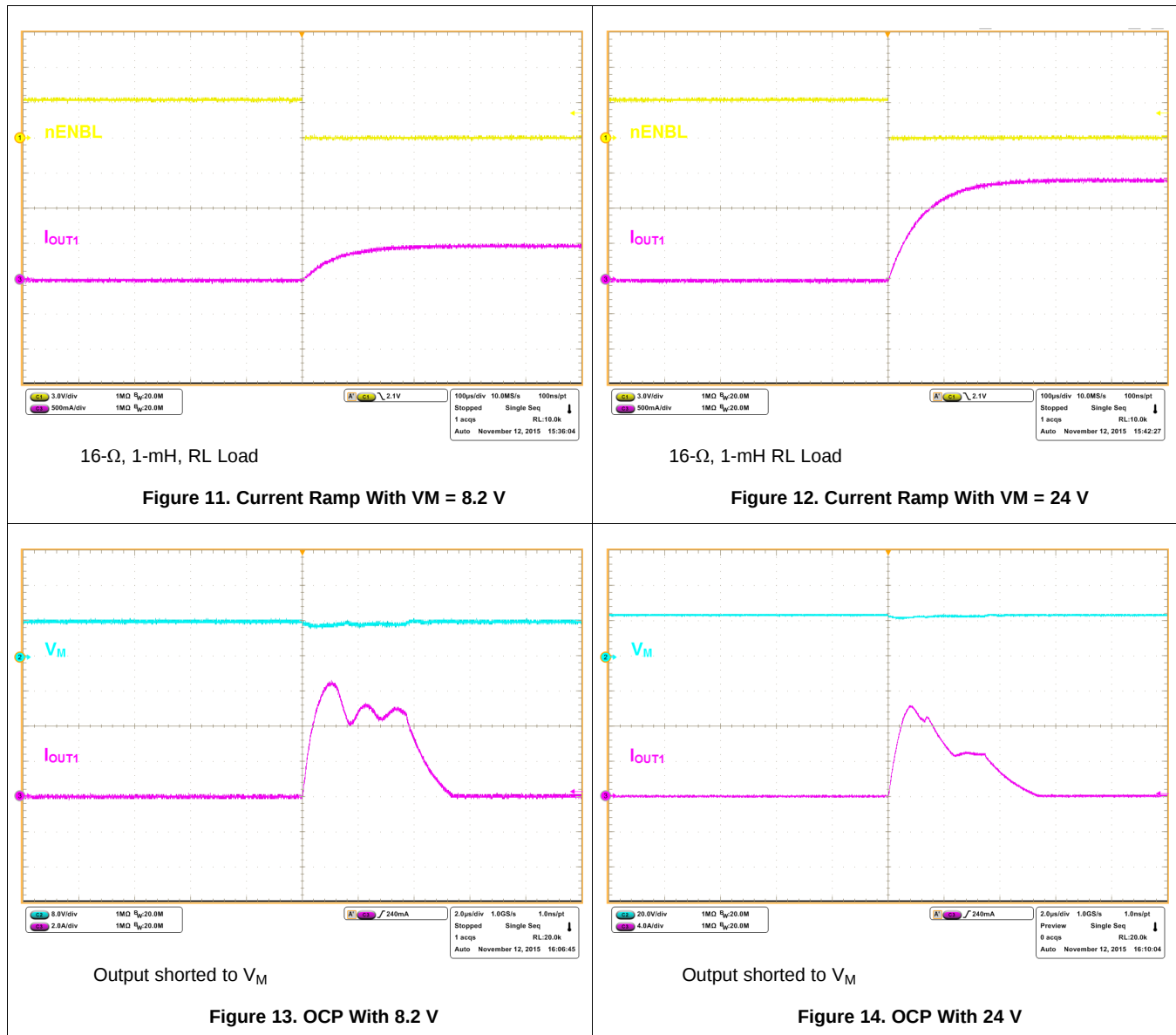
8.2.2.2 Drive Current

The current path starts from the supply V_M , moves through the inductive winding load, and low-side sinking NMOS power FET. Power dissipation losses in one sink NMOS power FET are shown in Equation 1.

$$P = I^2 \times R_{DS(on)} \quad (1)$$

The DRV8806 has been measured to be capable of 2-A Single Channel or 1-A Four Channels in a HTSSOP package at 25°C on standard FR-4 PCBs. The maximum RMS current varies based on PCB design and the ambient temperature.

8.2.3 Application Curves



9 Power Supply Recommendations

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size. The amount of local capacitance needed depends on a variety of factors, including

- Highest current required by the motor system
- Power supply's capacitance and ability to source current
- Amount of parasitic inductance between the power supply and motor system
- Acceptable voltage ripple
- Type of motor used (Brushed DC, Brushless DC, Stepper)
- Motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

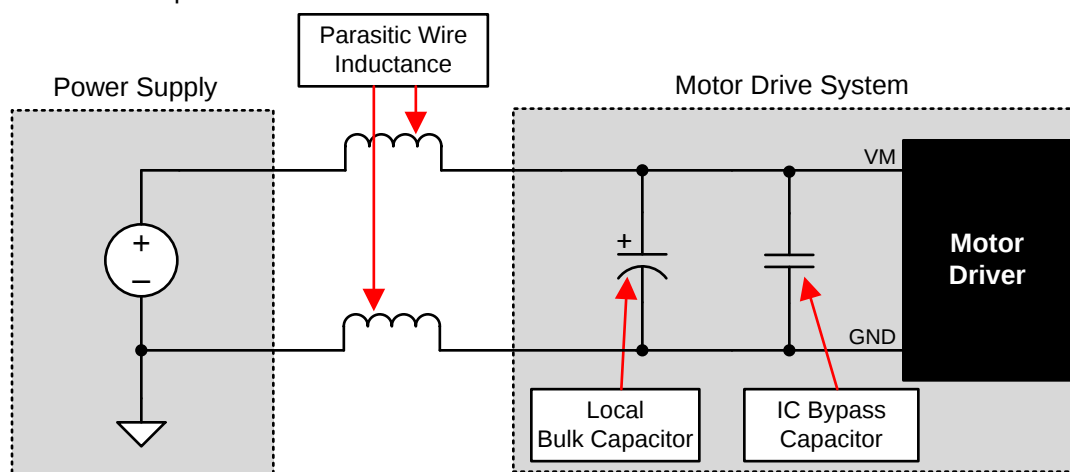


Figure 15. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

10.2 Layout Example

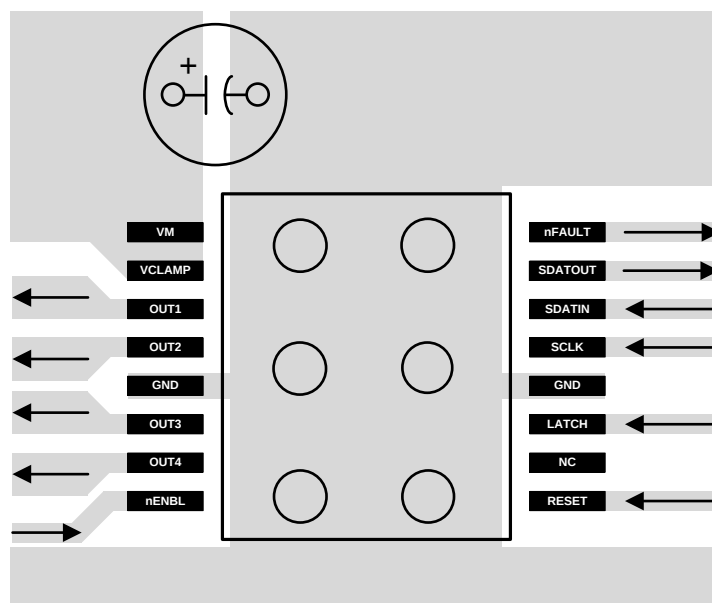


Figure 16. Layout Recommendation

10.3 Thermal Considerations

The DRV8806 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.3.1 Power Dissipation

Power dissipation in the DRV8806 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation of each FET when running a static load can be roughly estimated by [Equation 2](#):

$$P = R_{DS(ON)} \cdot (I_{OUT})^2$$

where

- P is the power dissipation of one FET
- $R_{DS(ON)}$ is the resistance of each FET
- I_{OUT} is equal to the average current drawn by the load

(2)

Thermal Considerations (continued)

Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and their duration also must be considered. When driving more than one load simultaneously, the power in all active output stages must be summed.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

10.3.2 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, see the TI application report, *PowerPAD™ Thermally Enhanced Package* (SLMA002), and TI application brief, *PowerPAD™ Made Easy* (SLMA004), available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

- 《PowerPAD™ 耐热增强型封装》 [SLMA002](#)
- 《PowerPAD™ 速成》 [SLMA004](#)

11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8806PWP	Obsolete	Production	HTSSOP (PWP) 16	-	-	Call TI	Call TI	-40 to 85	DRV8806
DRV8806PWPR	Active	Production	HTSSOP (PWP) 16	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8806
DRV8806PWPR.A	Active	Production	HTSSOP (PWP) 16	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8806

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

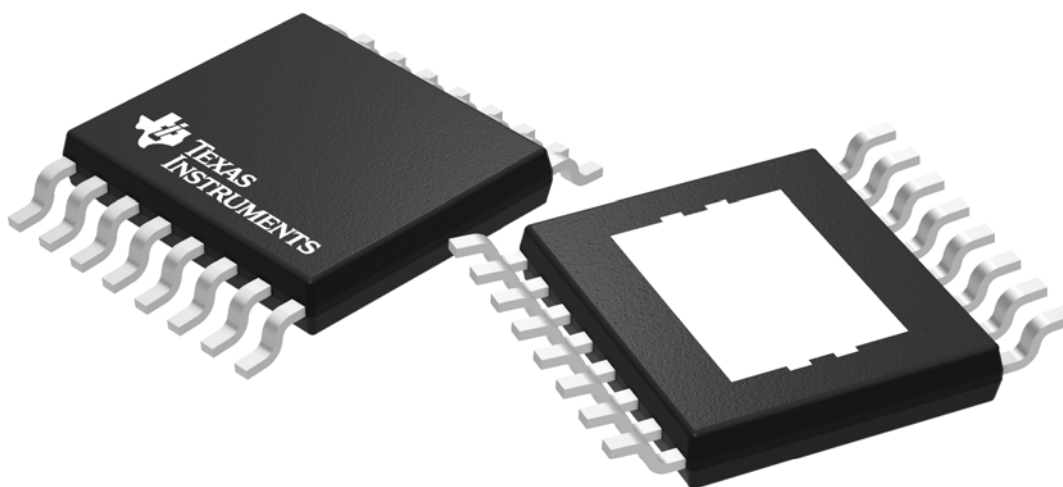
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8806PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

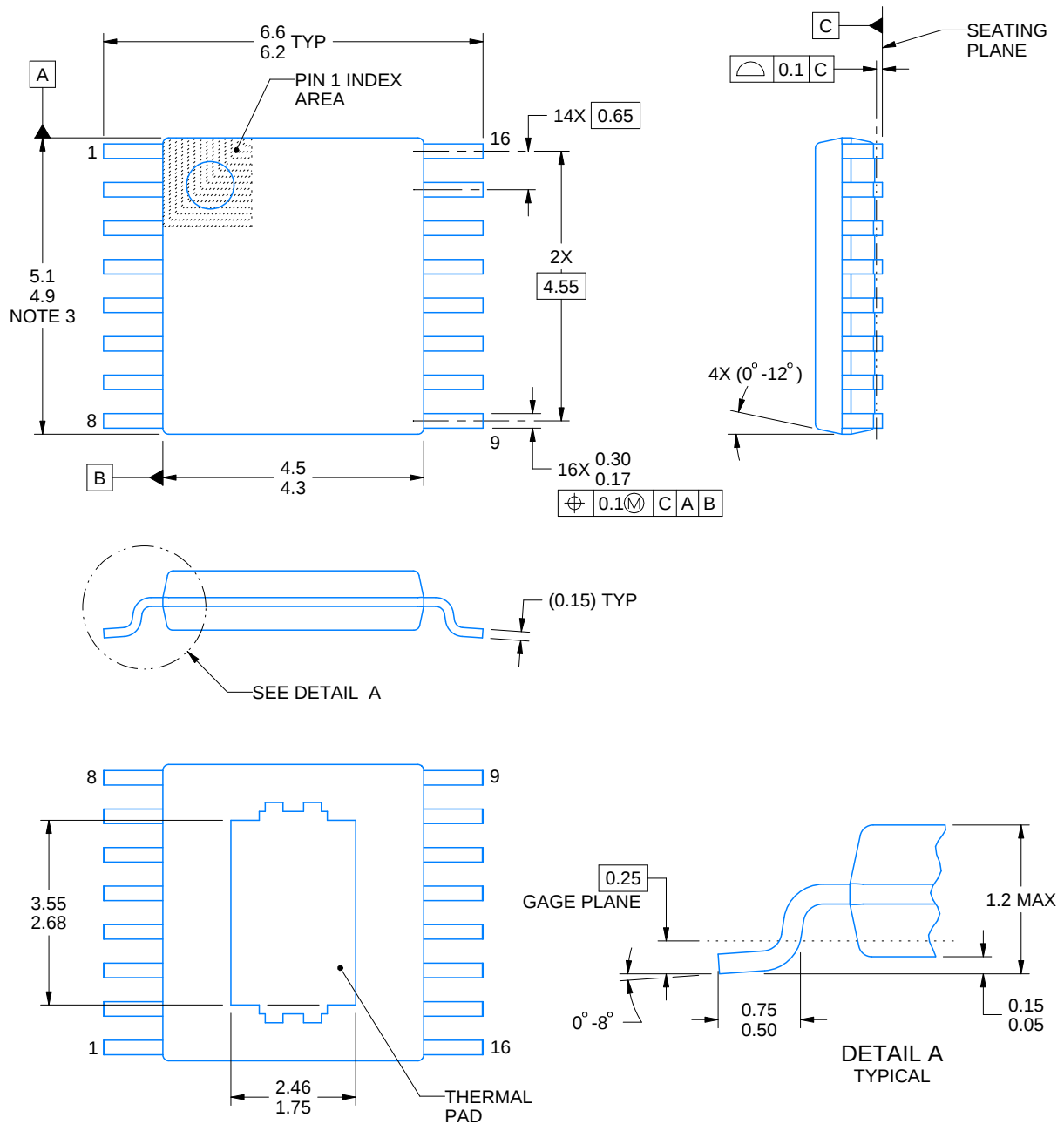
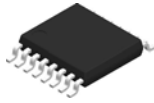


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8806PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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NOTES:

PowerPAD is a trademark of Texas Instruments.

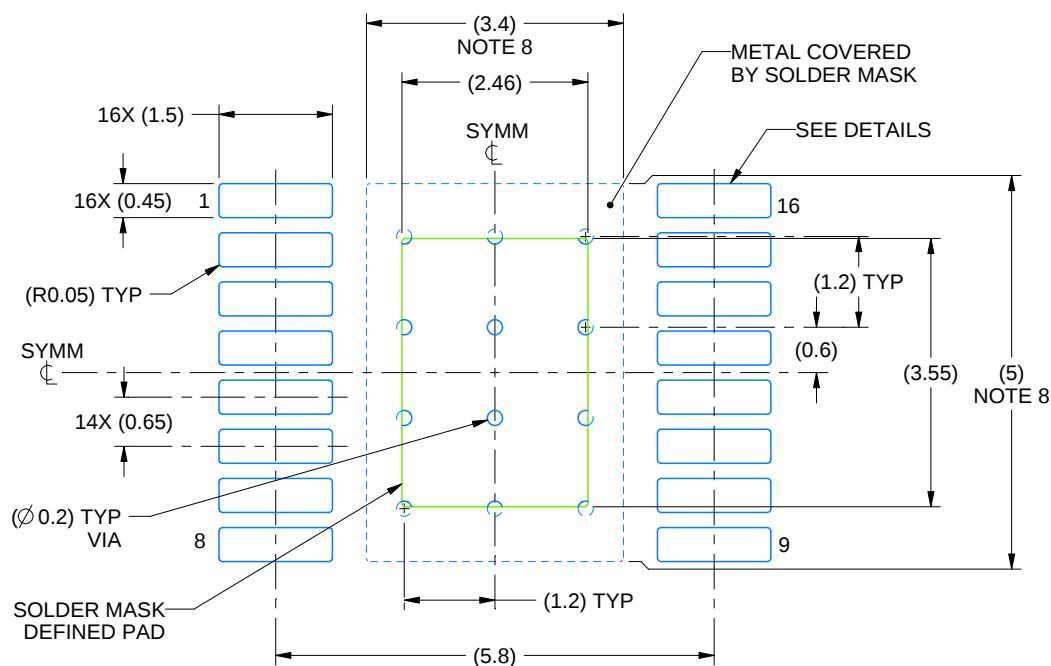
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

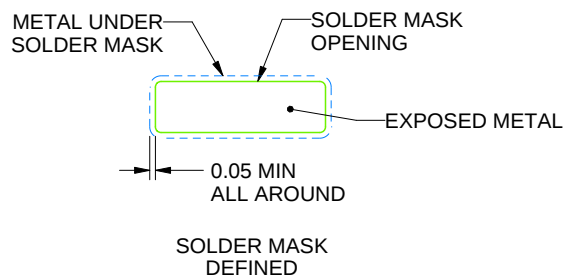
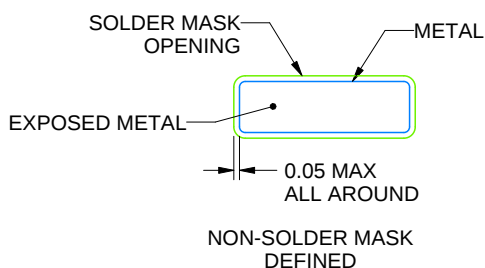
PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

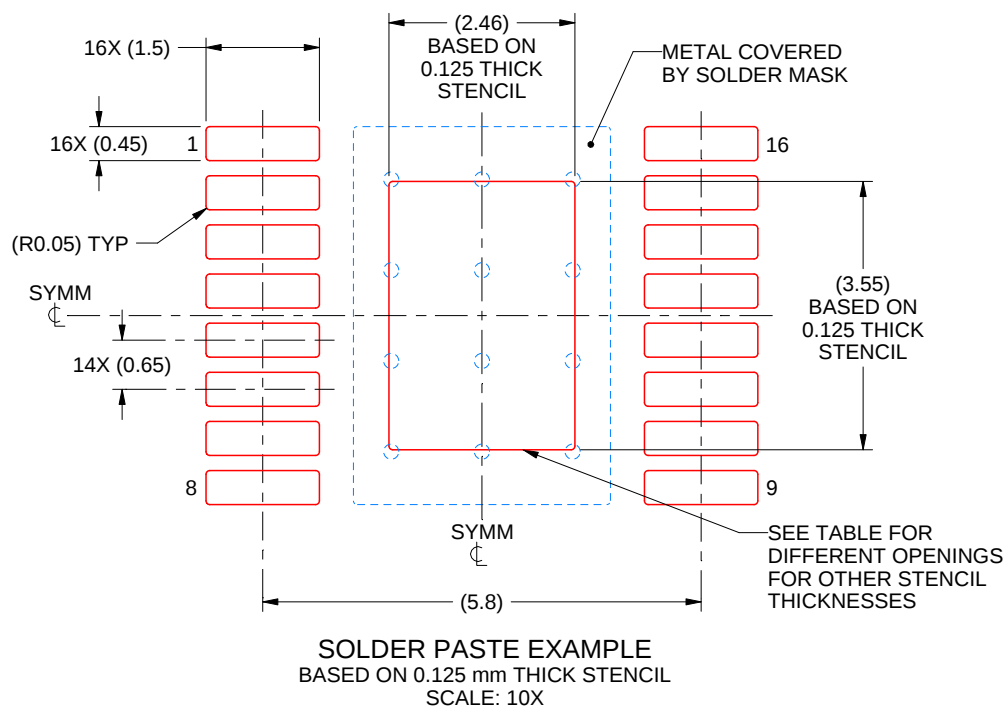
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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