DRV8872具有故障报告功能的 3.6A 刷式直流电机驱动器（PWM 控制）

1 特性

- H 桥电机驱动器
  - 驱动一个直流电机、一个步进电机的绕组或其他负载
- 6.5V 至 45V 宽工作电压范围
- 565mΩ（典型值）$R_{DS(on)}$ (HS + LS)
- 3.6A 峰值电流驱动能力
- 脉宽调制 (PWM) 控制接口
- 集成电流调节功能
- 低功耗休眠模式
- 故障状态输出引脚
- 小型封装尺寸
  - 8 引脚 HSOP 封装，带有 PowerPAD™
  - 4.9mm × 6mm
- 集成保护 功能
  - VM 欠压闭锁 (UVLO)
  - 过流保护 (OCP)
  - 热关断 (TSD)
  - 故障报告 (nFAULT)
  - 自动故障恢复

2 应用范围

- 打印机
- 电器
- 工业设备
- 其他机电 应用

3 说明

DRV8872 器件是一款刷式直流 (BDC) 电机驱动器，适用于打印机、电器、工业设备和其他小型机器。两个逻辑输入控制 H 桥驱动器，该驱动器由四个 N 沟道金属氧化物半导体场效应晶体管 (MOSFET) 组成，能够以高达 3.6A 的峰值电流执行双向电机控制。利用电流衰减模式，可通过对输入进行脉宽调制 (PWM) 来控制电机转速。如果将两个输入均置为低电平，则电机驱动器将进入低功耗休眠模式。

DRV8872 器件 具备 集成电流调节功能。该功能基于内部基准电压以及 ISEN 引脚电压（与流经外部感测电阻的电机电流成正比）。该器件能够将电流限制在某一已知水平，这可显著降低系统功耗要求，并且无需大容量电容来维持稳定电压，尤其是在电机启动和停转时。

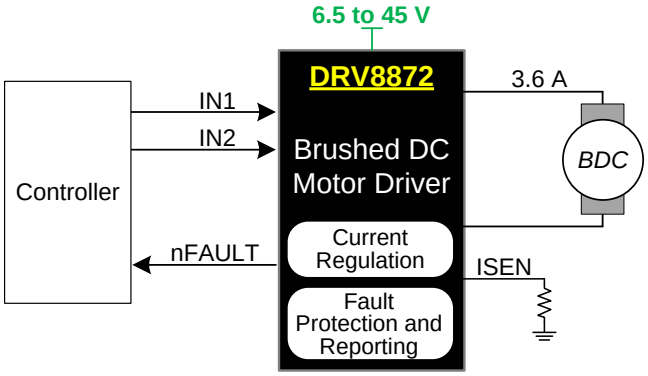
该器件针对故障和短路问题提供了全面保护，包括欠压锁定 (UVLO)、过流保护 (OCP) 和热关断 (TSD)。通过将 nFAULT 输出拉为低电平来报告故障。故障排除后，器件自动恢复正常状态。

器件信息(1)

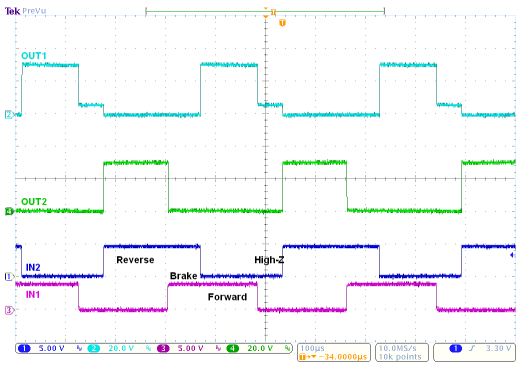
器件型号	封装	封装尺寸（标称值）
DRV8872	HSOP (8)	4.90mm x 6.00mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

简化电路原理图



H 桥状态



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (January 2016) to Revision C **Page**

- Deleted the power supply voltage ramp rate (VM) parameter from the *Absolute Maximum Ratings* table ... 3
- Added the output current parameter to the *Absolute Maximum Ratings* table ... 3
- 已添加 *接收文档更新通知*部分 ... 17

Changes from Revision A (August 2015) to Revision B **Page**

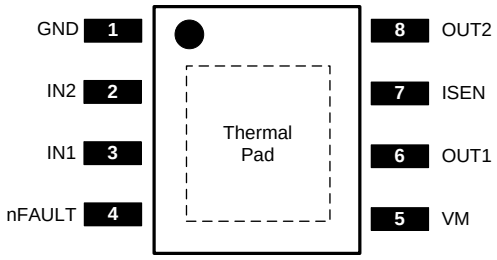
- Updated the f_{PWM} max value and added a note ... 4
- Removed the redundant T_A condition and added f_{PWM} = 24 kHz ... 5
- Added more information to clarify how the max RMS current varies for different applications ... 12

Changes from Original (August 2015) to Revision A **Page**

- Updated conditions for 图 12 ... 13

5 Pin Configuration and Functions

DDA Package
8-Pin HSOP With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION	
NAME	NO.			
GND	1	PWR	Logic ground	Connect to board ground.
IN1	3	I	Logic inputs	Controls the H-bridge output. Has internal pulldowns. (See 表 1.)
IN2	2			
ISEN	7	PWR	High-current ground path	If using current regulation, connect ISEN to a resistor (low-value, high-power-rating) to ground. If not using current regulation, connect ISEN directly to ground.
nFAULT	4	OD	Fault status (open-drain)	Low-level indicates UVLO, TSD, or OCP fault. Connect to a pullup resistor.
OUT1	6	O	H-bridge outputs	Connect directly to the motor, or other inductive load.
OUT2	8			
VM	5	PWR	6.5-V to 45-V power supply	Connect a 0.1-µF bypass capacitor to ground, as well as sufficient bulk capacitance, rated for the VM voltage.
PAD	—	—	Thermal pad	Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	50	V
Logic input voltage (IN1, IN2)	–0.3	7	V
Fault pin (nFAULT)	–0.3	6	V
Continuous phase node pin voltage (OUT1, OUT2)	–0.7	VM + 0.7	V
Current sense input pin voltage (ISEN)(2)	–0.5	1	V
Output current (100% duty cycle)	0	3.5	A
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transients of ±1 V for less than 25 ns are acceptable

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±6000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VM	Power supply voltage	6.5		45	V
V_I	Logic input voltage (IN1, IN2)	0		5.5	V
f_{PWM}	Logic input PWM frequency (IN1, IN2)	0		200 (1)	kHz
I_{peak}	Peak output current (2)	0		3.6	A
T_A	Operating ambient temperature	–40		125	°C

(1) The voltages applied to the inputs should have at least 800 ns of pulse width to ensure detection. Typical devices require at least 400 ns. If the PWM frequency is 200 kHz, the usable duty cycle range is 16% to 84%
(2) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC (1)		DRV8872 DDA (HSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VM)						
VM	VM operating voltage		6.5		45	V
I_{VM}	VM operating supply current	VM = 12 V		3	10	mA
$I_{VMSLEEP}$	VM sleep current	VM = 12 V			10	µA
t_{ON}	Turn-on time(1)	VM > V_{UVLO} with IN1 or IN2 high		40	50	µs
LOGIC-LEVEL INPUTS (IN1, IN2)						
V_{IL}	Input logic low voltage				0.5	V
V_{IH}	Input logic high voltage		1.5			V
V_{HYS}	Input logic hysteresis			0.5		V
I_{IL}	Input logic low current	V_{IN} = 0 V	–1		1	µA
I_{IH}	Input logic high current	V_{IN} = 3.3 V		33	100	µA
R_{PD}	Pulldown resistance	To GND		100		kΩ
t_{PD}	Propagation delay	INx to OUTx change (see 图 6)		0.7	1	µs
t_{sleep}	Time to sleep	Inputs low to sleep		1	1.5	ms
MOTOR DRIVER OUTPUTS (OUT1, OUT2)						
$R_{DS(ON)}$	High-side FET on resistance	VM = 24 V, I = 1 A, f_{PWM} = 25 kHz		307	360	mΩ
$R_{DS(ON)}$	Low-side FET on resistance	VM = 24 V, I = 1 A, f_{PWM} = 25 kHz		258	320	mΩ
t_{DEAD}	Output dead time			220		ns
V_d	Body diode forward voltage	I_{OUT} = 1 A		0.8	1	V
CURRENT REGULATION						
V_{TRIP}	ISEN voltage for current chopping		0.32	0.35	0.38	V
t_{OFF}	PWM off-time			25		µs
t_{BLANK}	PWM blanking time			2		µs
PROTECTION CIRCUITS						
V_{UVLO}	VM undervoltage lockout	VM falls until UVLO triggers		6.1	6.4	V
		VM rises until operation recovers		6.3	6.5	
$V_{UV,HYS}$	VM undervoltage hysteresis	Rising to falling threshold	100	180		mV
I_{OCP}	Overcurrent protection trip level		3.7	4.5	6.4	A
t_{OCP}	Overcurrent deglitch time			1.5		µs
t_{RETRY}	Overcurrent retry time			3		ms
T_{SD}	Thermal shutdown temperature		150	175		°C
T_{HYS}	Thermal shutdown hysteresis			40		°C
nFAULT OPEN DRAIN OUTPUT						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA

(1) t_{ON} applies when the device initially powers up, and when it exits sleep mode.

6.6 Typical Characteristics

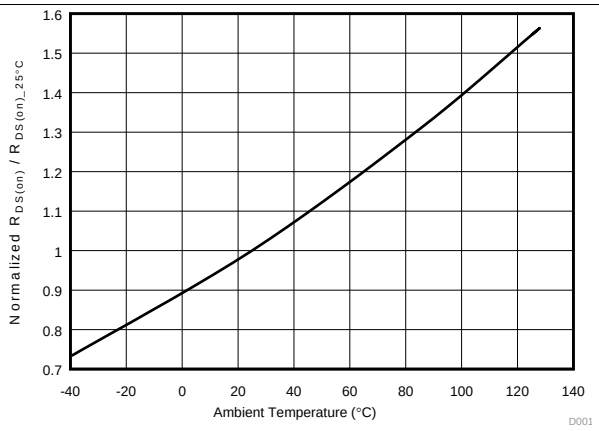


图 1. $R_{DS(on)}$ vs Temperature

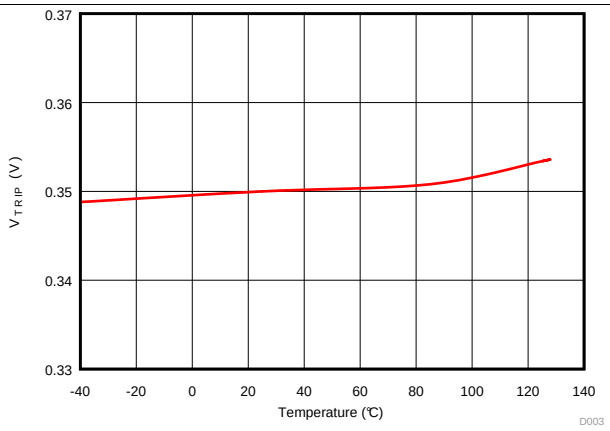


图 2. V_{TRIP} vs Temperature

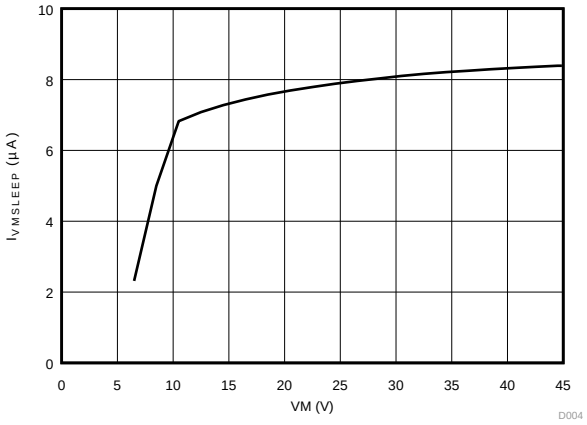


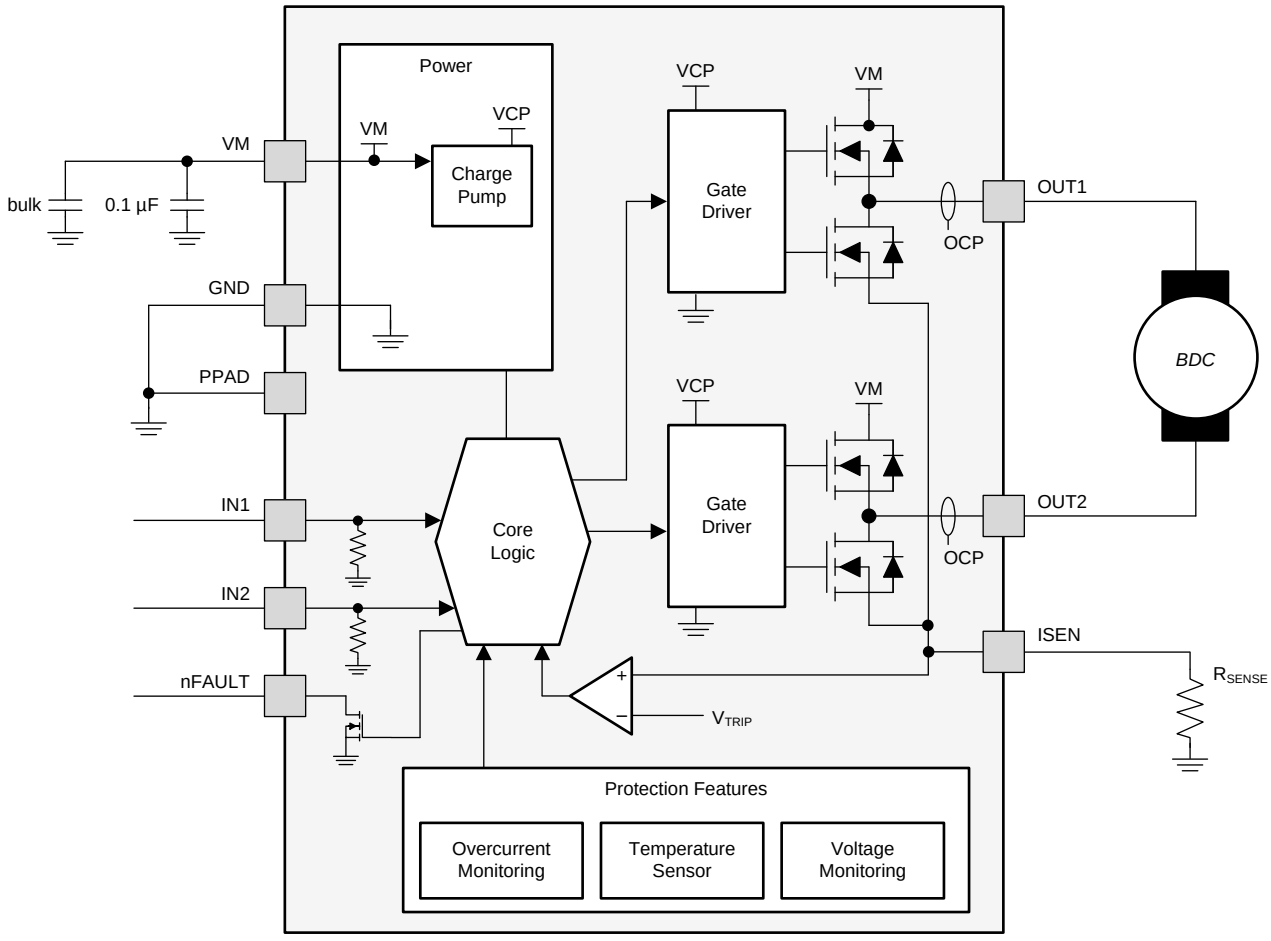
图 3. $I_{VMSLEEP}$ vs VM at 25°C

7 Detailed Description

7.1 Overview

The DRV8872 device is an optimized 8-pin device for driving brushed DC motors with 6.5 to 45 V and up to 3.6-A peak current. The integrated current regulation restricts motor current to a predefined maximum. Two logic inputs control the H-bridge driver, which consists of four N-channel MOSFETs that have a typical $R_{ds(on)}$ of 565 mΩ (including one high-side and one low-side FET). A single power input, VM, serves as both device power and the motor winding bias voltage. The integrated charge pump of the device boosts VM internally and fully enhances the high-side FETs. Motor speed can be controlled with pulse-width modulation, at frequencies between 0 to 100 kHz. The device has an integrated sleep mode that is entered by bringing both inputs low. An assortment of protection features prevent the device from being damaged if a system fault occurs.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Bridge Control

The DRV8872 output consists of four N-channel MOSFETs that are designed to drive high current. These MOSFETs are controlled by the two logic inputs IN1 and IN2, according to 表 1.

表 1. H-Bridge Control

IN1	IN2	OUT1	OUT2	DESCRIPTION
0	0	High-Z	High-Z	Coast; H-bridge disabled to High-Z (sleep entered after 1 ms)
0	1	L	H	Reverse (current OUT2 → OUT1)
1	0	H	L	Forward (current OUT1 → OUT2)
1	1	L	L	Brake; low-side slow decay

The inputs can be set to static voltages for 100% duty-cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. When using PWM, switching between driving and braking typically works best. For example, to drive a motor forward with 50% of its max RPM, IN1 = 1 and IN2 = 0 during the driving period, and IN1 = 1 and IN2 = 1 during the other period. Alternatively, the coast mode (IN1 = 0, IN2 = 0) for *fast current decay* is also available. The input pins can be powered before VM is applied.

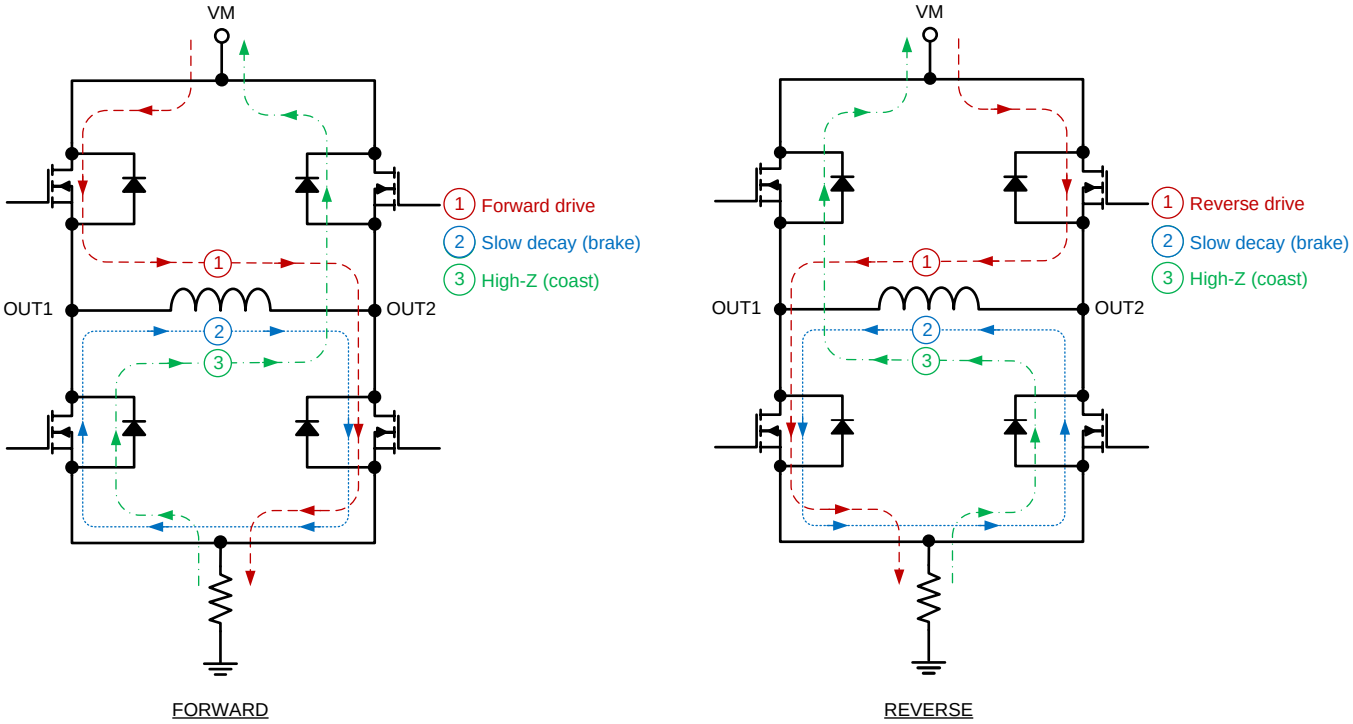


图 4. H-Bridge Current Paths

7.3.2 Sleep Mode

When IN1 and IN2 are both low for time t_{SLEEP} (typically 1 ms), the DRV8872 device enters a low-power sleep mode, where the outputs remain High-Z and the device uses $I_{VMSLEEP}$ (microamps) of current. If the device is powered up while both inputs are low, sleep mode is immediately entered. After IN1 or IN2 are high for at least 5 µs, the device is operational 50 µs (t_{ON}) later.

7.3.3 Current Regulation

The DRV8872 device limits the output current based on the resistance of an external sense resistor on pin ISEN, according to 公式 1.

$$I_{TRIP}\ (A) = \frac{V_{TRIP}\ (V)}{R_{ISEN}\ (\Omega)} = \frac{0.35\ (V)}{R_{ISEN}\ (\Omega)} \quad (1)$$

For example, if R_{ISEN} = 0.16 Ω, the DRV8872 device limits motor current to 2.2 A no matter how much load torque is applied. For guidelines on selecting a sense resistor, see the *Sense Resistor* section.

When I_{TRIP} has been reached, the device enforces slow current decay by enabling both low-side FETs, and it does this for time t_{OFF} (typically 25 µs).

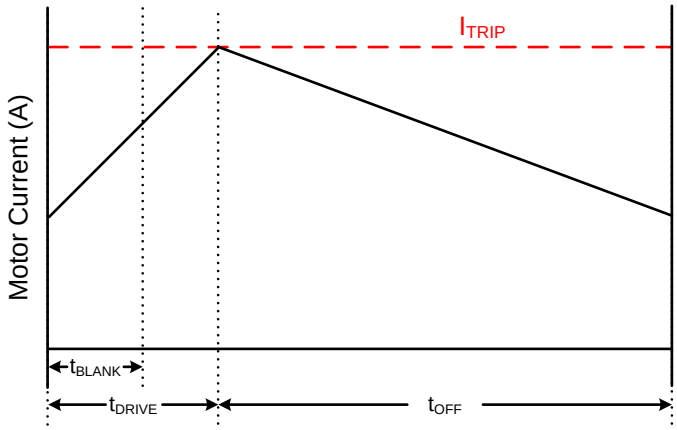


图 5. Current Regulation Time Periods

After t_{OFF} has elapsed, the output is re-enabled according to the two inputs INx. The drive time (t_{DRIVE}) until reaching another I_{TRIP} event heavily depends on the VM voltage, the back-EMF of the motor, and the inductance of the motor.

7.3.4 Dead Time

When an output changes from driving high to driving low, or driving low to driving high, dead time is automatically inserted to prevent shoot-through. t_{DEAD} is the time in the middle when the output is High-Z. If the output pin is measured during t_{DEAD}, the voltage will depend on the direction of current. If current is leaving the pin, the voltage is a diode drop below ground. If current is entering the pin, the voltage is a diode drop above VM. This diode is the body diode of the high-side or low-side FET.

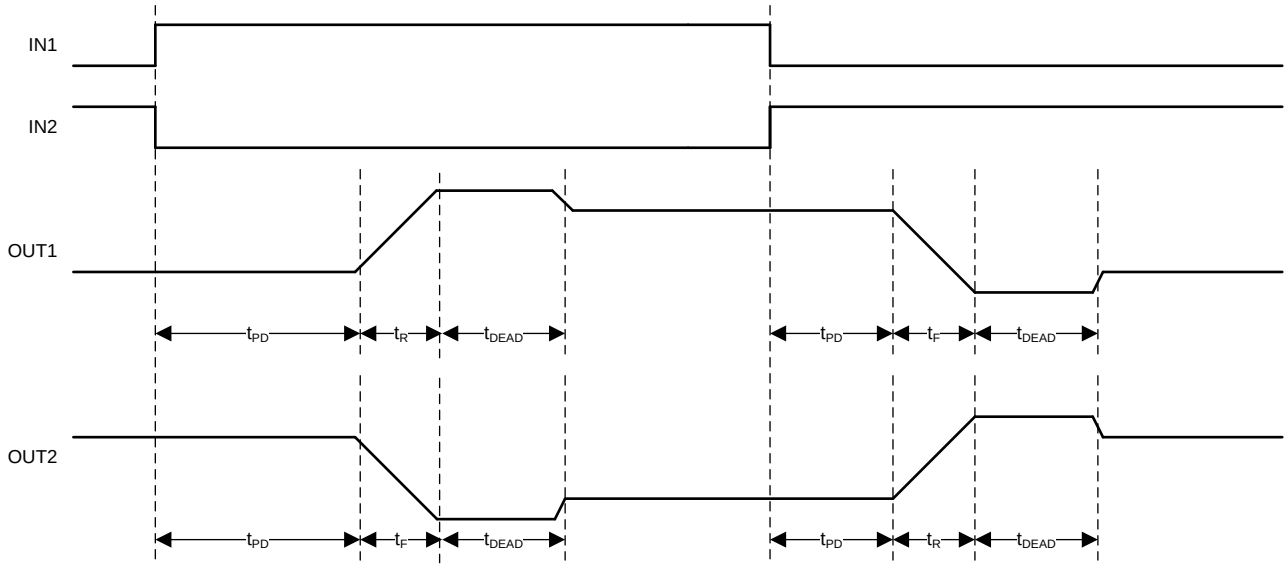


图 6. Propagation Delay Time

7.3.5 Protection Circuits

The DRV8872 device is fully protected against VM undervoltage, overcurrent, and overtemperature events. When the device is in a protected state, nFAULT is driven low. When the fault condition is removed, nFAULT becomes a high-impedance state.

7.3.5.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage-lockout threshold voltage, all FETs in the H-bridge are disabled. Operation resumes when VM rises above the UVLO threshold.

7.3.5.2 Overcurrent Protection (OCP)

If the output current exceeds the OCP threshold I_{OCP} for longer than t_{OCP}, all FETs in the H-bridge are disabled for a duration of t_{RETRY}. After that, the H-bridge re-enables according to the state of the INx pins. If the overcurrent fault is still present, the cycle repeats; otherwise normal device operation resumes.

7.3.5.3 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge is disabled. After the die temperature has fallen to a safe level, operation automatically resumes.

表 2. Protection Functionality

FAULT	CONDITION	H-BRIDGE BECOMES	NFAULT BECOMES	RECOVERY
VM undervoltage lockout (UVLO)	VM < V_{UVLO}	Disabled	Low	VM > V_{UVLO}
Overcurrent (OCP)	I_{OUT} > I_{OCP}	Disabled	Low	t_{RETRY}
Thermal shutdown (TSD)	T_J > 150°C	Disabled	Low	T_J < T_{SD} - T_{HYS}

7.4 Device Functional Modes

The DRV8872 device can be used in multiple ways to drive a brushed DC motor.

7.4.1 PWM With Current Regulation

This scheme uses all of the capabilities of the device. The I_{TRIP} current is set above the normal operating current, and high enough to achieve an adequate spin-up time, but low enough to constrain current to a desired level. Motor speed is controlled by the duty cycle of one of the inputs, while the other input is static. Brake and slow decay is typically used during the off-time.

7.4.2 PWM Without Current Regulation

If current regulation is not needed, the ISEN pin should be directly connected to the PCB ground plane. This mode provides the highest possible peak current: up to 3.6 A for a few hundred milliseconds (depending on PCB characteristics and the ambient temperature). If current exceeds 3.6 A, the device might reach overcurrent protection (OCP) or over-temperature shutdown (TSD). If that occurs, the device disables and protects itself for about 3 ms (t_{RETRY}) and then resumes normal operation.

7.4.3 Static Inputs With Current Regulation

The IN1 and IN2 pins can be set high and low for 100% duty cycle drive, and ITRIP can be used to control the current, speed, and torque capability of the motor.

7.4.4 VM Control

In some systems, varying VM as a means of changing motor speed is desirable. See the *Motor Voltage* section for more information.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8872 device is typically used to drive one brushed DC motor.

8.2 Typical Application

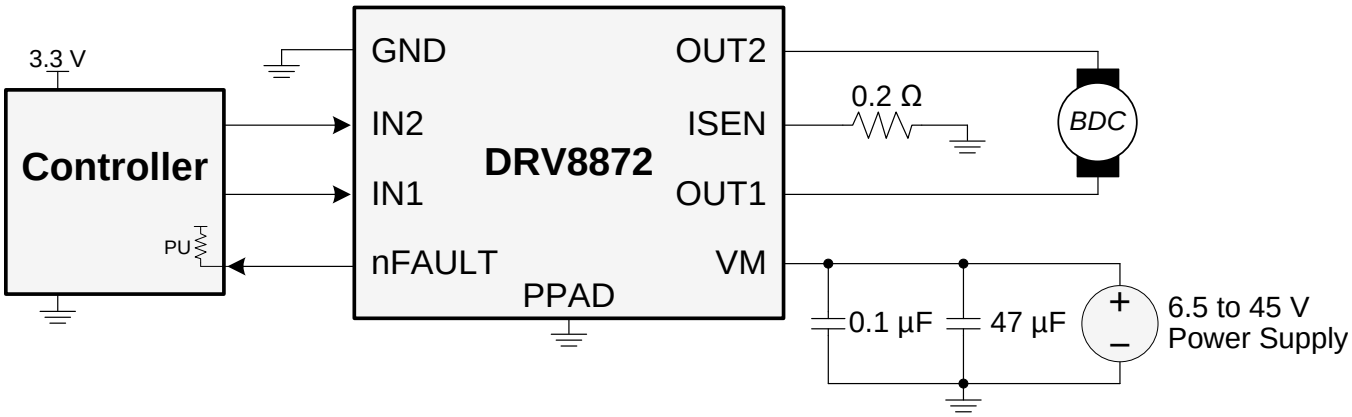


图 7. Typical Connections

8.2.1 Design Requirements

表 3 lists the design parameters.

表 3. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor voltage	V_M	24 V
Motor RMS current	I_{RMS}	0.8 A
Motor startup current	I_{START}	2 A
Motor current trip point	I_{TRIP}	2.2 A
Sense resistance	R_{ISEN}	0.16 Ω
PWM frequency	f_{PWM}	5 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The motor voltage used depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

8.2.2.2 Drive Current

The current path is through the high-side sourcing DMOS power driver, motor winding, and low-side sinking DMOS power driver. Power dissipation losses in one source and sink DMOS power driver are shown in 公式 2.

$$P_D = I^2 \left(R_{DS(on)Source} + R_{DS(on)Sink} \right) \quad (2)$$

The DRV8872 device has been measured to be capable of 2-A RMS current at 25°C on standard FR-4 PCBs. The maximum RMS current varies based on the PCB design, ambient temperature, and PWM frequency. Typically, switching the inputs at 200 kHz compared to 20 kHz causes 20% more power loss in heat.

8.2.2.3 Sense Resistor

For optimal performance, the sense resistor must have the features that follow:

- Surface-mount device
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $I_{RMS}{}^2 \times R$. For example, if peak motor current is 3 A, RMS motor current is 1.5 A, and a 0.2-Ω sense resistor is used, the resistor dissipates $1.5\ A^2 \times 0.2\ \Omega = 0.45$ W. The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, the system designer should add margin. It is always best to measure the actual sense resistor temperature in a final system.

Because power resistors are larger and more expensive than standard resistors, multiple standard resistors can be used in parallel, between the sense node and ground. This configuration distributes the current and heat dissipation.

8.2.3 Application Curves

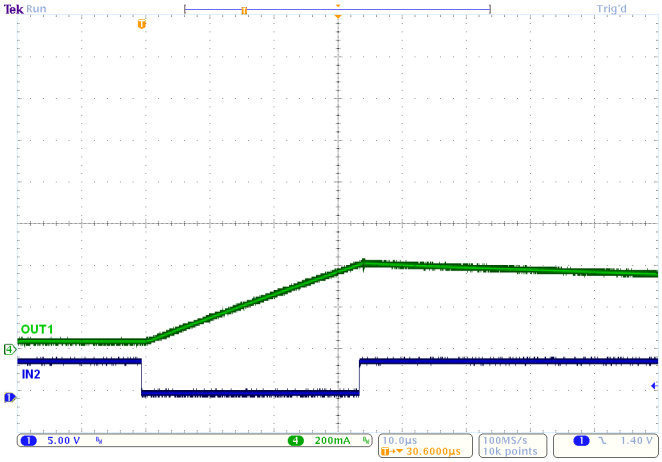


图 8. Current Ramp With a 2-Ω, 1 mH, RL Load and VM = 12 V

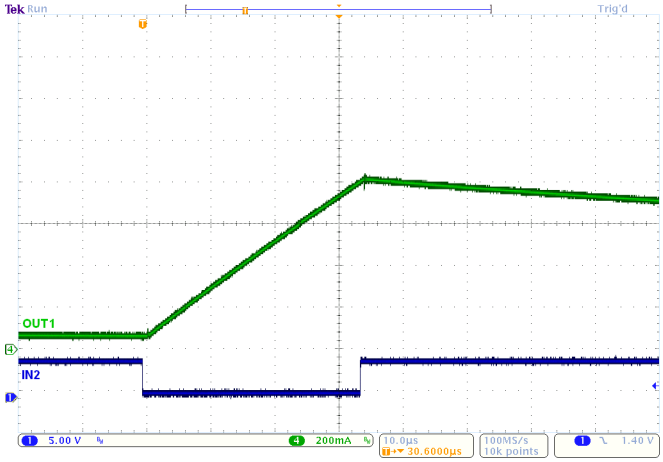


图 9. Current Ramp With a 2-Ω, 1 mH, RL Load and VM = 24 V

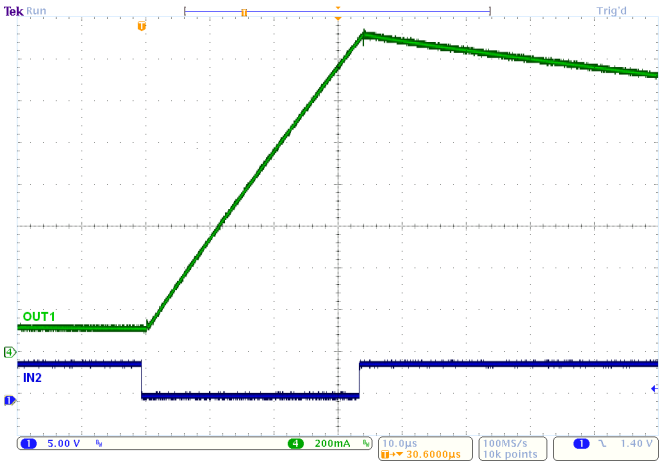


图 10. Current Ramp With a 2-Ω, 1 mH, RL Load and VM = 45 V

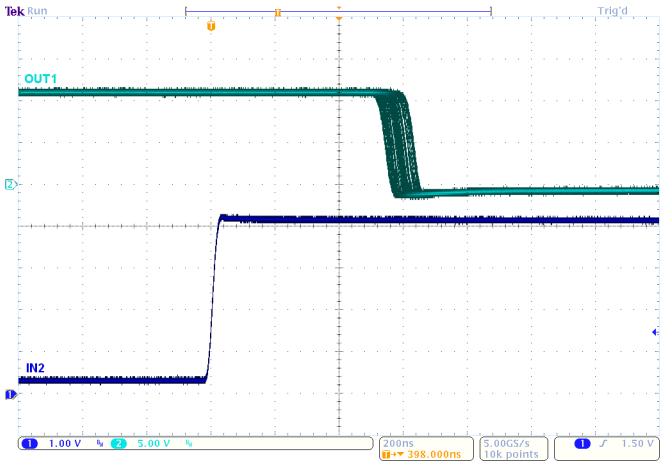


图 11. t_{PD}

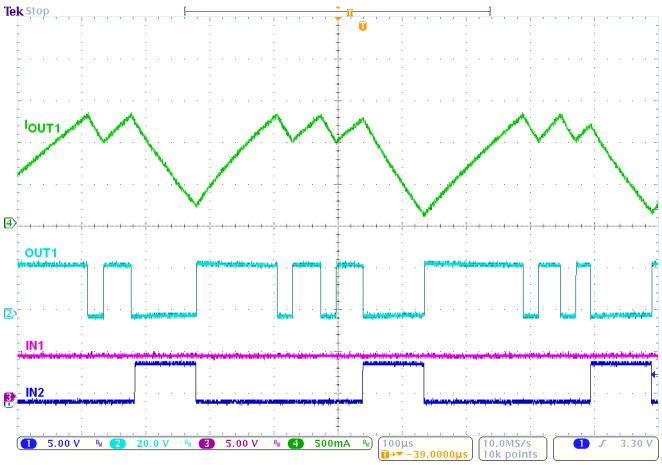


图 12. Current Regulation With R_{SENSE} = 0.26 Ω

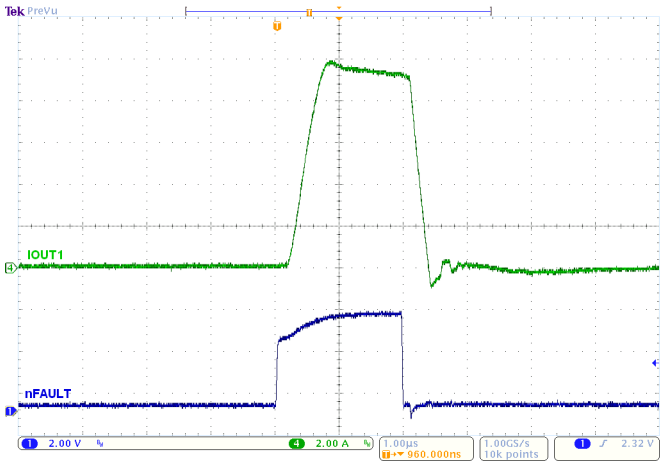


图 13. OCP With 24 V and Outputs Shorted Together

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. More bulk capacitance is generally beneficial but with the disadvantages of increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits the rate that the current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

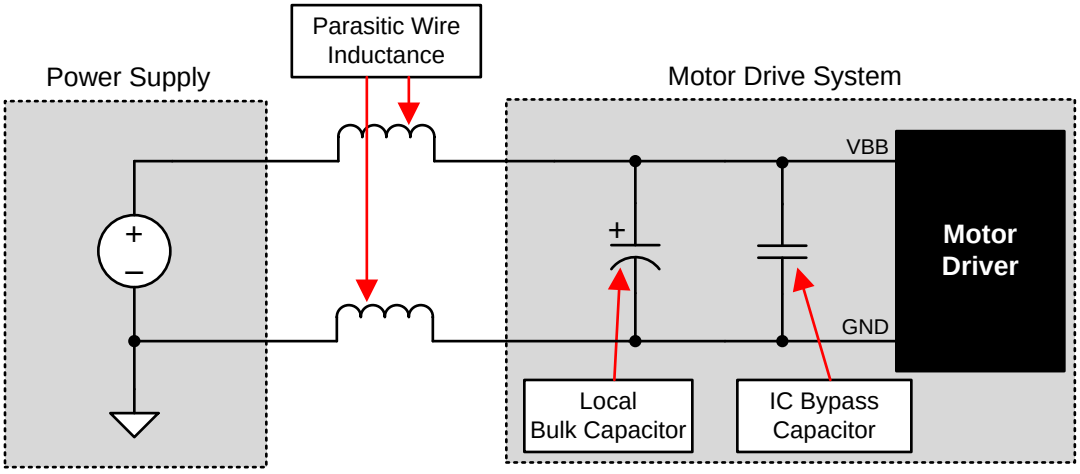


图 14. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

图 15 shows the recommended layout and component placement.

10.2 Layout Example

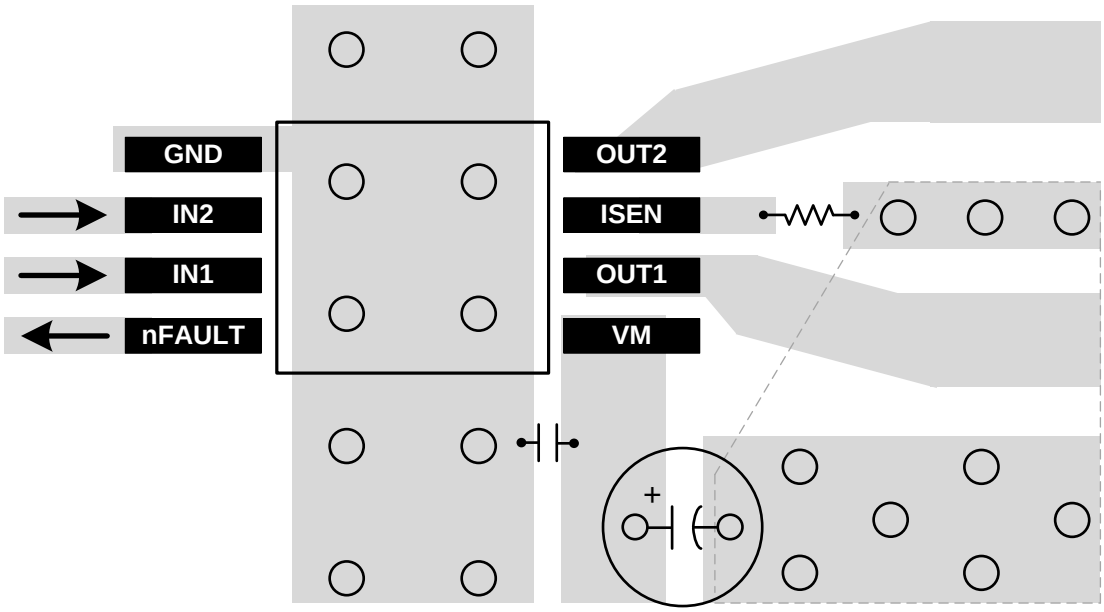


图 15. Layout Recommendation

10.3 Thermal Considerations

The DRV8872 device has thermal shutdown (TSD) as described in the *Thermal Shutdown (TSD)* section. If the die temperature exceeds approximately 175°C, the device is disabled until the temperature drops below the temperature hysteresis level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high of an ambient temperature.

10.4 Power Dissipation

Power dissipation in the DRV8872 device is dominated by the power dissipated in the output FET resistance, $R_{DS(on)}$. Use 公式 2 from the *Drive Current* section to calculate the estimated average power dissipation of when driving a load.

Note that at startup, the output current is much higher than normal running current; this peak current and its duration must be also be considered.

Power Dissipation (接下页)

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

注

$R_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. This fact must be taken into consideration when sizing the heatsink.

The power dissipation of the DRV8872 is a function of RMS motor current and the FET resistance ($R_{DS(ON)}$) of each output.

$$\text{Power} \approx I_{RMS}^2 \times \left(\text{High-side } R_{DS(ON)} + \text{ Low-side } R_{DS(ON)}\right) \quad (3)$$

For this example, the ambient temperature is 58°C, and the junction temperature reaches 80°C. At 58°C, the sum of $R_{DS(ON)}$ is about 0.72 Ω. With an example motor current of 0.8 A, the dissipated power in the form of heat is 0.8 A^2 × 0.72 Ω = 0.46 W.

The temperature that the DRV8872 reaches depends on the thermal resistance to the air and PCB. Soldering the device PowerPAD to the PCB ground plane, with vias to the top and bottom board layers, is important to dissipate heat into the PCB and reduce the device temperature. In the example used here, the DRV8872 had an effective thermal resistance $R_{\theta JA}$ of 48°C/W, and a T_J value as shown in 公式 4.

$$T_J = T_A + (P_D \times R_{\theta JA}) = 58°C + (0.46\ W \times 48°C/W) = 80°C \quad (4)$$

10.4.1 Heatsinking

The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this connection can be accomplished by adding a number of vias to connect the thermal pad to the ground plane.

On PCBs without internal planes, a copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to the TI application report, *PowerPAD™ Thermally Enhanced Package* (SLMA002), and the TI application brief, *PowerPAD Made Easy™* (SLMA004), available at www.ti.com. In general, the more copper area that can be provided, the more power can be dissipated.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

- *《电流再循环和衰减模式》*（文献编号：SLVA321）
- *《计算电机驱动器功耗》*（文献编号：SLVA504）
- *《DRV8872 评估模块》*（文献编号：SLVUAJ5）
- *《PowerPAD™ 耐热增强型封装》*（文献编号：SLMA002）
- *《PowerPAD™ 速成》*（文献编号：SLMA004）
- *《了解电机驱动器电流额定值》*（文献编号：SLVA505）

11.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

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11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8872DDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	8872
DRV8872DDAR.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8872
DRV8872DDAR.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8872

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF DRV8872 :

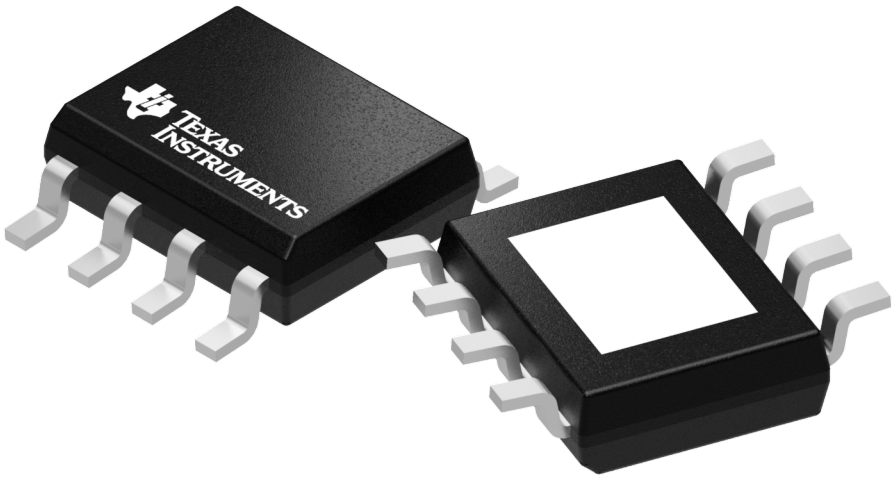
- Automotive : DRV8872-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

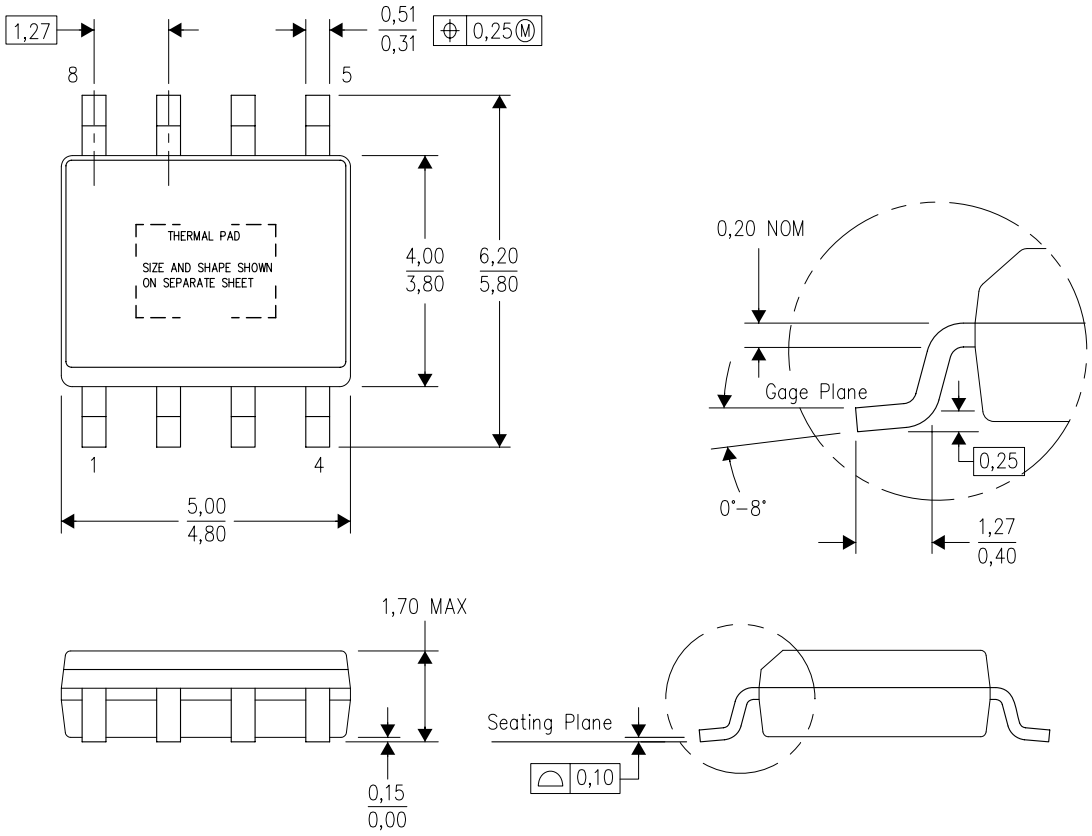
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

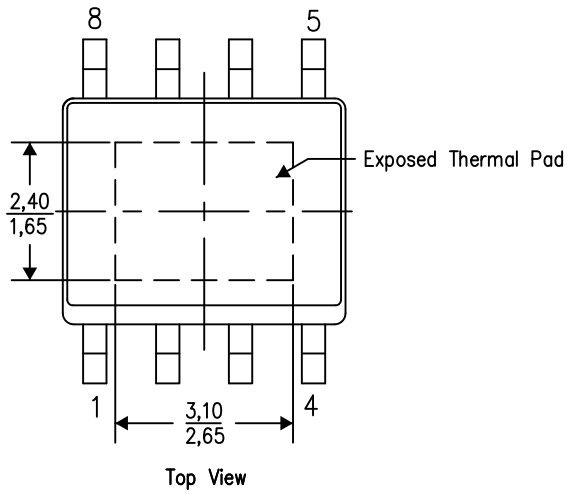
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



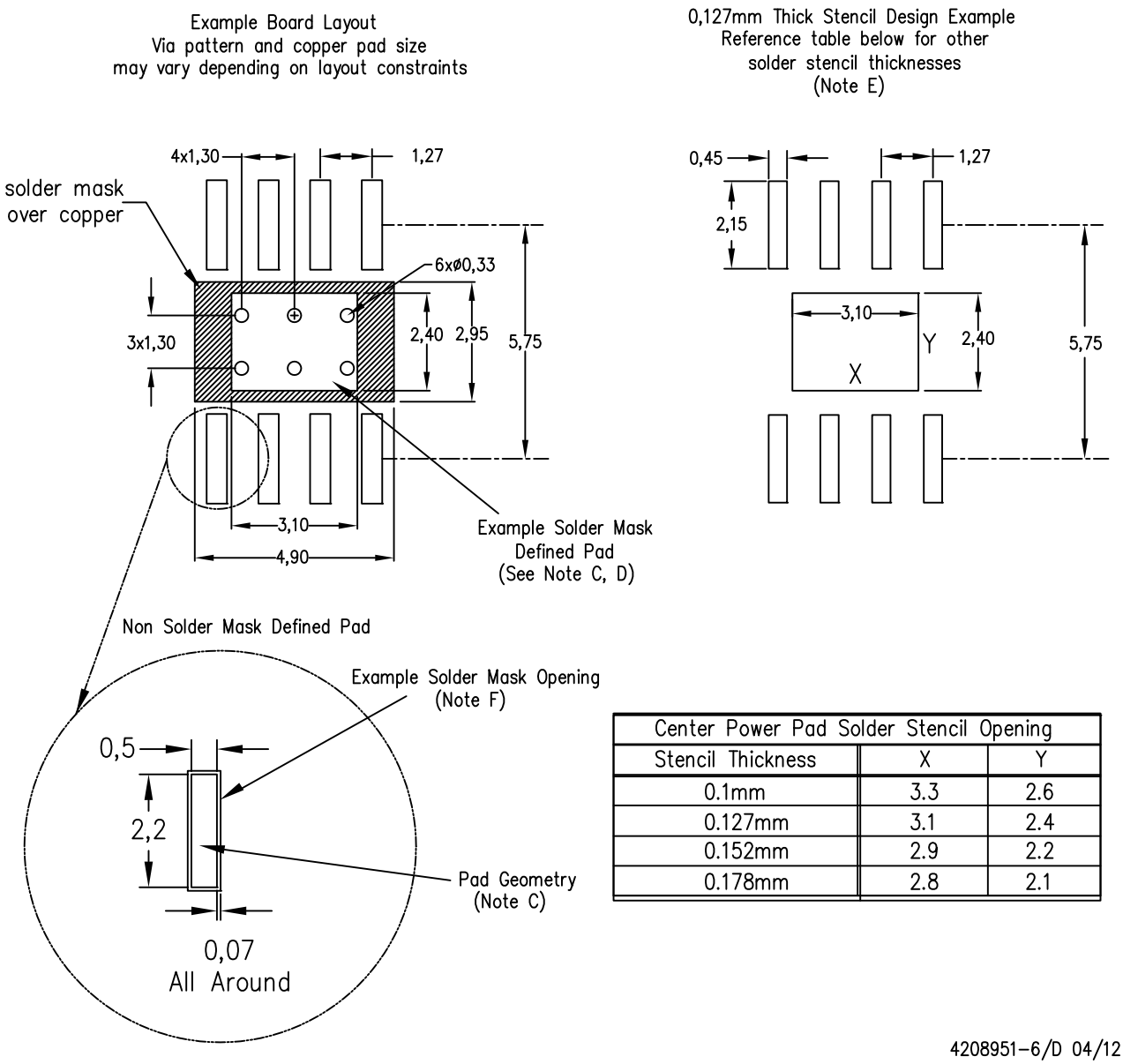
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

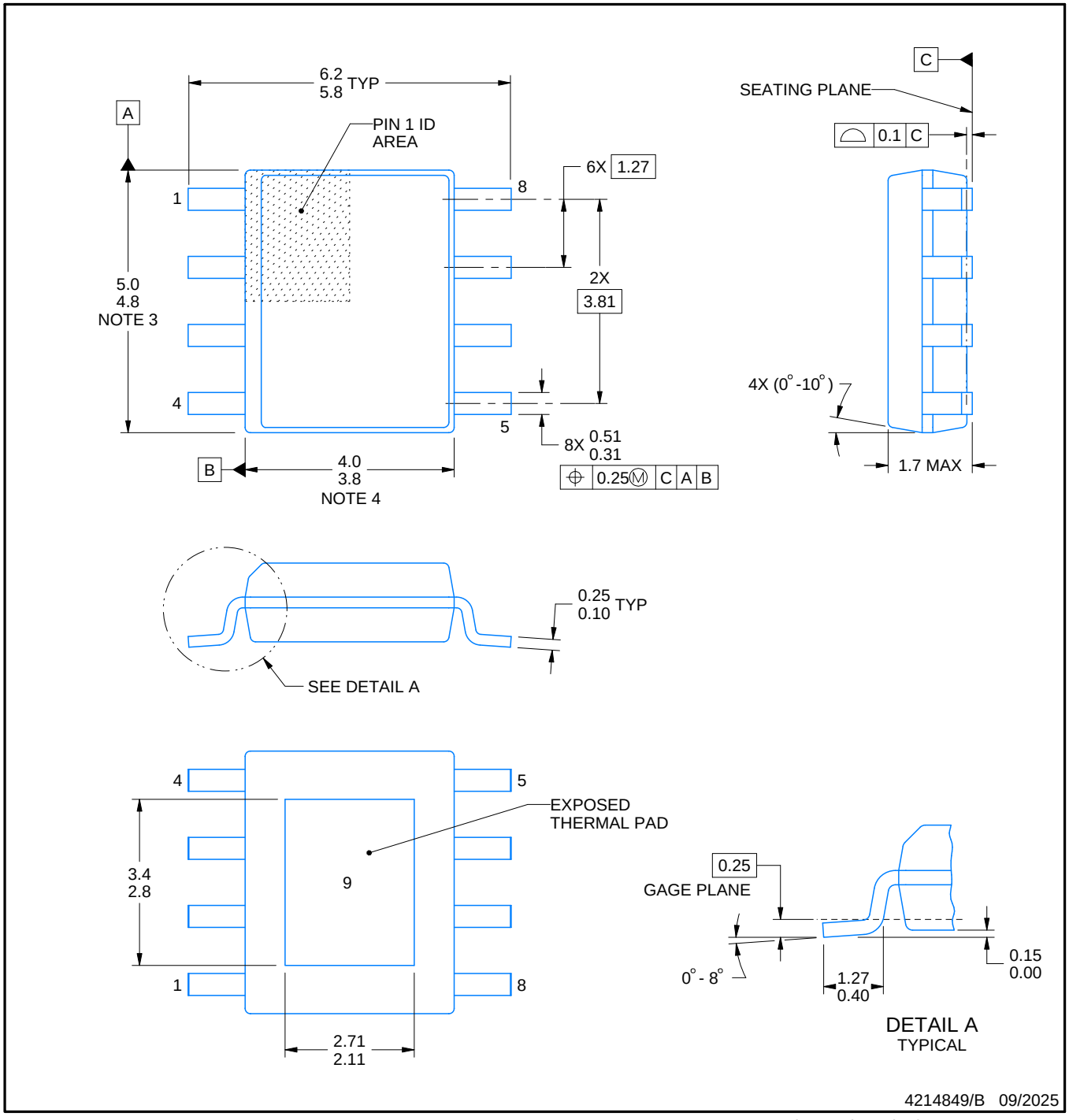
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

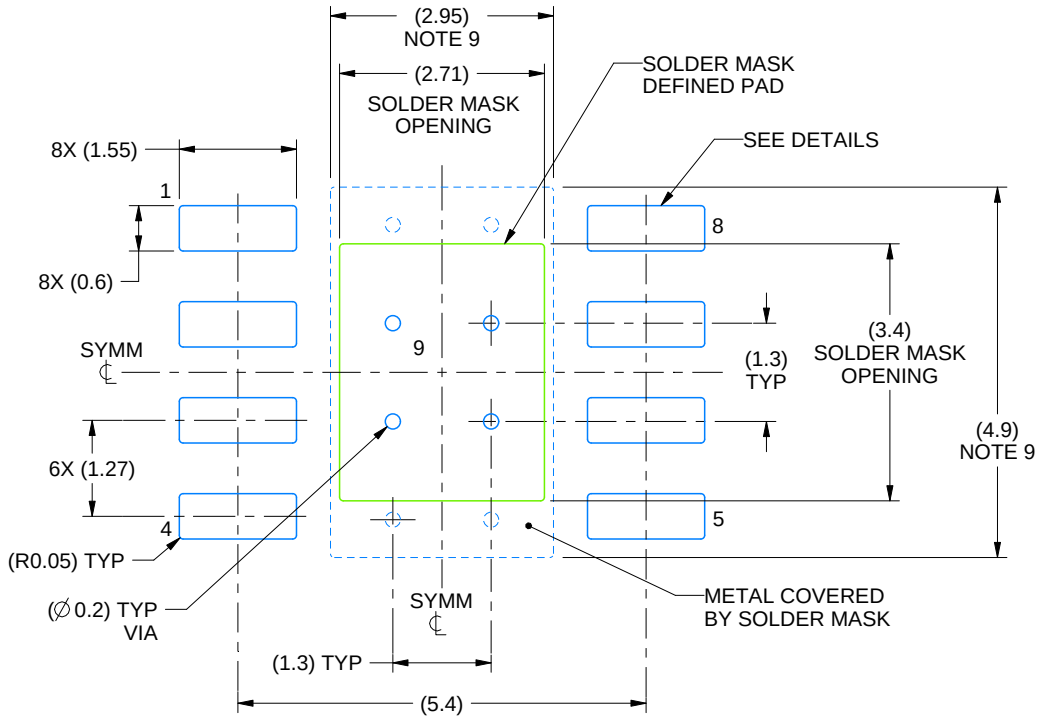
PLASTIC SMALL OUTLINE



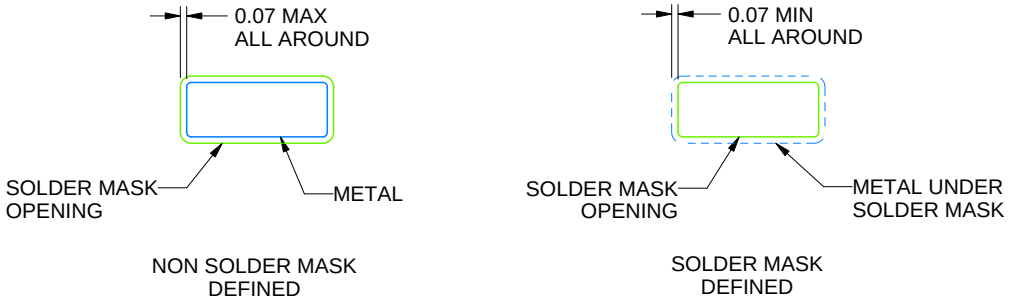
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

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NOTES: (continued)

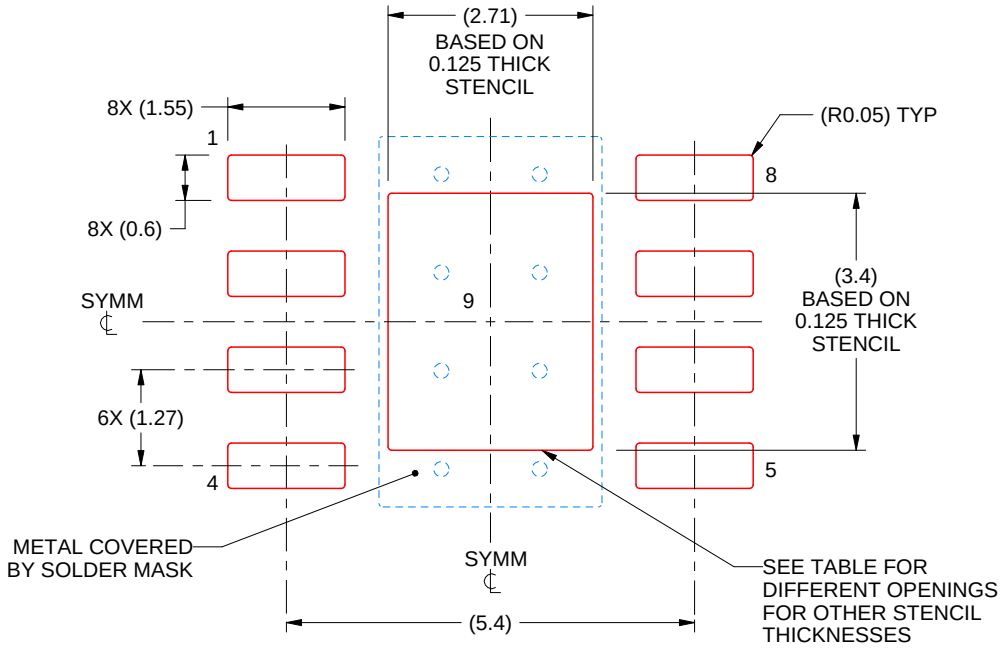
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月