

## DS30EA101 0.15 至 3.125Gbps 自适应电缆均衡器

查询样品: [DS30EA101](#)

### 特性

- 同轴电缆和双绞线电缆的自动均衡
- **150Mbps 至 3.125Gbps** 的数据速率
- 支持标清 (SD) 和高清 (HD) 视频分辨率
- 功耗: 典型值为 **115mW**
- 工业温度范围: **-40°C 至 +85°C**

### 应用范围

- 电缆延长
- 数据恢复均衡
- 安全和监控

### 说明

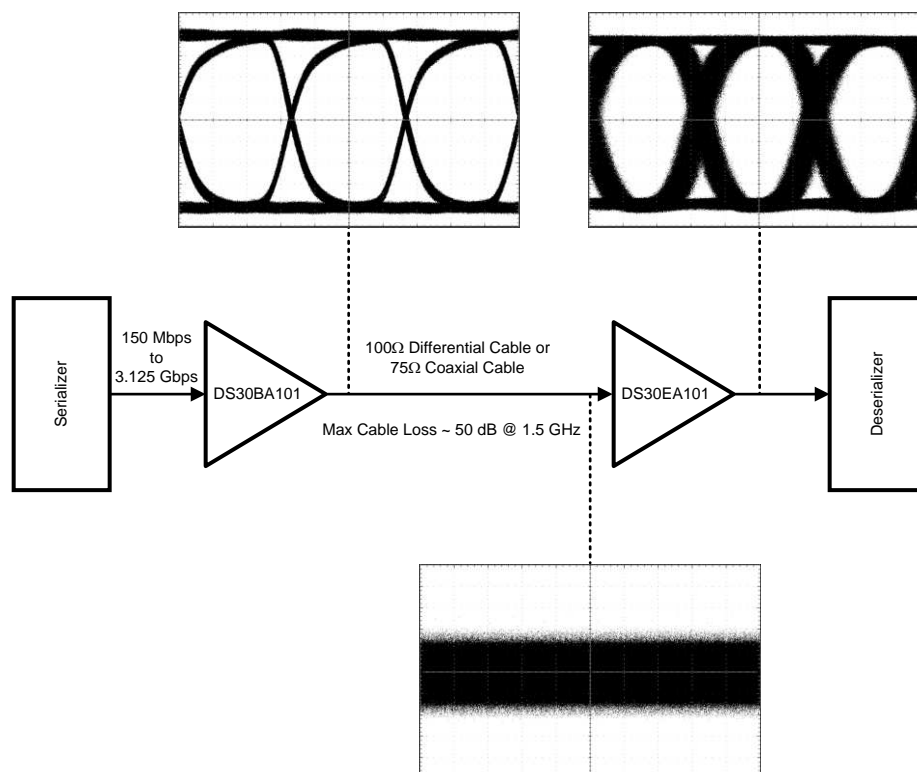
DS30EA101 是一款自适应电缆均衡器, 此均衡器针对铜电缆上的均衡数据传输进行了优化。此均衡器运行在 150Mbps 至 3.125Gbps 的数据速率范围内, 并且自动适应以均衡任一长度电缆上 (从零米至 1.5GHz 时信号衰减为 50dB 的电缆长度) 发送的信号。

DS30EA101 可实现单端或差分输入。这样可实现同轴电缆以及双绞线电缆上的信号均衡。

额外特性包括信号丢失 (LOS) 检测和输出使能, 当二者连接在一起时, 在没有输入信号出现的时候, 禁用输出。

DS30EA101 由一个单个 2.5V 电源供电, 功耗 115mW (典型值)。它运行在 -40°C 至 +85°C 的全工业温度范围内, 并且采用 4mm x 4mm 16 引脚超薄型四方扁平无引线 (WQFN) 封装。

### 典型应用



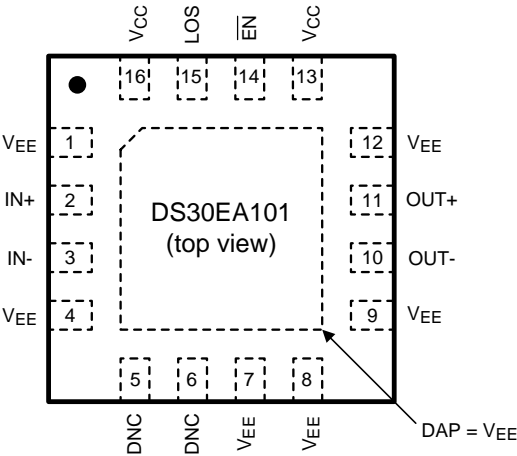
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English Data Sheet: [SNLS404](#)

连接图



外露裸片连接垫是用于这个器件的一个负电端子。它应该被连接至负电源电压。

图 1. 16 引脚 WQFN 封装  
请见封装编号 RUM0016A

引脚说明

引脚	名称	I/O, 类型	说明
1	V <sub>EE</sub>	接地	负电源（接地）。
2	IN+	I, 数据	非反相输入。
3	IN-	I, 数据	反相输入。
4	V <sub>EE</sub>	接地	负电源（接地）。
5	DNC	不可用	不要连接 - 保持打开。
6	DNC	不可用	不要连接 - 保持打开。
7	V <sub>EE</sub>	接地	负电源（接地）。
8	V <sub>EE</sub>	接地	负电源（接地）。
9	V <sub>EE</sub>	接地	负电源（接地）。
10	OUT-	O, 低压差分信号 (LVDS)	反相输出。
11	OUT+	O, LVDS	非反相输出。
12	V <sub>EE</sub>	接地	负电源（接地）。
13	V <sub>CC</sub>	功率	正电源 (+2.5V)。
14	EN	I, LVCMOS	输出使能。LOS 可被接至这个引脚，在没有输入信号出现时禁止输出。这个引脚有一个内部下拉。 H = 输出被禁用。 L = 输出被启用。
15	LOS	O, LVCMOS	信号丢失。 H = 没有检测到输入信号。 L = 检测到输入信号。
16	V <sub>CC</sub>	电源	正电源 (+2.5V)。
DAP	V <sub>EE</sub>	接地	将外露 DAP 连接至负电源（接地）。



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings<sup>(1)</sup>

Supply Voltage	3.1V
Input Voltage (all inputs)	-0.3V to $V_{CC}+0.3V$
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+125°C
Package Thermal Resistance $\theta_{JA}$ 16-pin WQFN $\theta_{JC}$ 16-pin WQFN	+40°C/W +6°C/W
ESD Rating (HBM)	$\geq \pm 6$ kV
ESD Rating (MM)	$\geq \pm 300V$
ESD Rating (CDM)	$\geq \pm 2$ kV

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

## Recommended Operating Conditions<sup>(1)</sup>

Supply Voltage ( $V_{CC}$ )	2.5V $\pm 5\%$
Input Coupling Capacitance	1.0 $\mu F$
Operating Free Air Temperature ( $T_A$ )	-40°C to +85°C

## DC Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified.<sup>(1)(2)</sup>

Parameter		Test Conditions	Reference	Min	Typ	Max	Units
$V_{IN}$	Input Voltage	0m cable length	IN+, IN-	720	800	880	mV <sub>P-P</sub>
$V_{SS}$	Steady State Differential Output Voltage	100 $\Omega$ load, <a href="#">Figure 2</a>	OUT+, OUT-	500	700	900	mV <sub>P-P</sub>
$V_{OD}$	Differential Output Voltage			250	350	450	mV
$\Delta V_{OD}$	Change in Magnitude of $V_{OD}$ for Complimentary Output States					50	mV
$V_{OS}$	Offset Voltage			1.1	1.2	1.35	V
$\Delta V_{OS}$	Change in Magnitude of $V_{OS}$ for Complimentary Output States					50	mV
$I_{OS}$	Output Short Circuit Current					30	mA
$V_{IH}$	Input Voltage High Level		$\overline{EN}$	1.7		$V_{CC}$	V
$V_{IL}$	Input Voltage Low Level			$V_{EE}$		0.7	V
$V_{OH}$	Output Voltage High Level	$I_{OH} = -2$ mA	LOS	2.0			V
$V_{OL}$	Output Voltage Low Level	$I_{OL} = +2$ mA				0.2	V
$I_{CC}$	Supply Current				45	65	mA

- (1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (2) Typical values represent most likely parametric norms at  $V_{CC} = +2.5V$ ,  $T_A = +25^\circ C$ , and at the Recommended Operating Conditions at the time of product characterization and are not ensured.

## AC Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified.<sup>(1)(2)</sup>

Parameter		Test Conditions	Reference	Min	Typ	Max	Units
DR <sub>IN</sub>	Input Data Rate		IN+, IN-	150		3125	Mbps
t <sub>JIT</sub>	Total Jitter at BER 10 <sup>-12</sup> <sup>(3)</sup>	3.125 Gbps, 0-10 meters CAT6			0.35		UI
		2.5 Gbps, 0-25 meters CAT6			0.35		UI
		1.5 Gbps, 0-50 meters CAT6			0.35		UI
		3.125 Gbps, 0-100 meters RG59			0.3		UI
		2.5 Gbps, 0-110 meters RG59			0.35		UI
		1.5 Gbps, 0-120 meters RG59			0.2		UI
t <sub>TLH</sub>	Transition Time Low to High	20% - 80%, 100Ω load, <sup>(4)</sup> , Figure 2	OUT+, OUT-		90	130	ps
t <sub>THL</sub>	Transition Time High to Low				90	130	ps

- (1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (2) Typical values represent most likely parametric norms at V<sub>CC</sub> = +2.5V, T<sub>A</sub> = +25°C, and at the Recommended Operating Conditions at the time of product characterization and are not ensured.
- (3) The total jitter at BER 10<sup>-12</sup> is calculated as DJ + (14 x RJ), where DJ is deterministic jitter and RJ is random jitter. The jitter is expressed as a portion of the unit interval (UI). The UI is the reciprocal of the data rate.
- (4) Specification is ensured by characterization and is not tested in production.

## TIMING DIAGRAMS

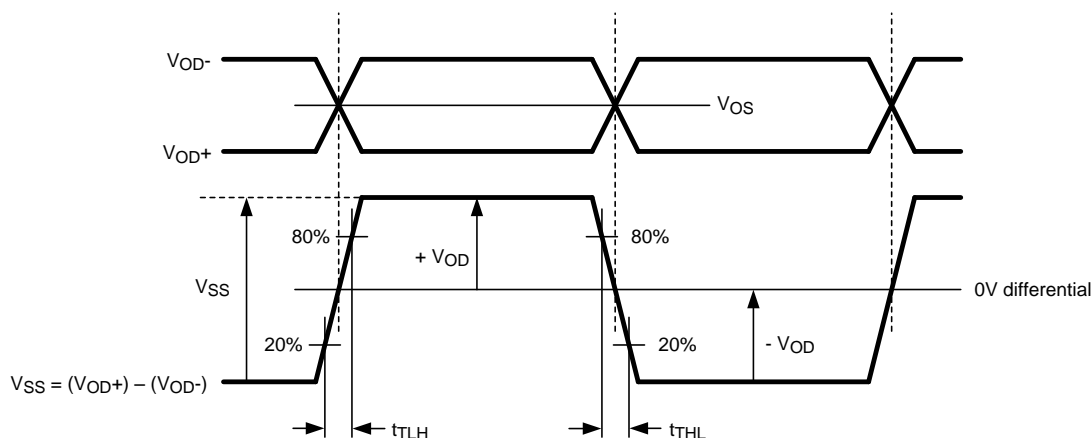


Figure 2. LVDS Output Voltage, Offset, and Timing Parameters

## DEVICE OPERATION

The DS30EA101 equalizes data transmitted over copper cables. It automatically adjusts its gain to reverse the effects of the cable loss and restore the original signal. For proper operation, the launch amplitude of the signal going into the cable (the signal amplitude prior to the cable attenuation) must be set appropriately. If the signal is single-ended, its single-ended amplitude must be 800 mV<sub>P-P</sub> ±10%. If the signal is differential, its differential amplitude must be 800 mV<sub>P-P</sub> ±10% (400 mV<sub>P-P</sub> single-ended).

### INPUT INTERFACING

The DS30EA101 accepts either differential or single-ended input. The input must be AC coupled. Figure 3 and Figure 4 show the typical configurations for differential input and single-ended input, respectively. For single-ended input, the unused input must be properly terminated as shown.

### OUTPUT INTERFACING

The DS30EA101 output signals (OUT+ and OUT-) are internally terminated 100Ω LVDS outputs. These outputs can be DC coupled to most common differential receivers.

### LOS AND $\overline{\text{EN}}$

LOS indicates the loss of signal at the DS30EA101 input. LOS is high when no input signal is present and low when a valid input signal is detected.

$\overline{\text{EN}}$  can be used to manually disable or enable the OUT+ and OUT- output signals. Applying a high input to  $\overline{\text{EN}}$  will disable the DS30EA101 outputs by forcing the output to a logic 1, and applying a low input to  $\overline{\text{EN}}$  will force the outputs to be active.  $\overline{\text{EN}}$  has an internal pulldown to enable the outputs by default.

LOS and  $\overline{\text{EN}}$  may be tied together to automatically disable the DS30EA101 outputs when no input signal is present.

## APPLICATION INFORMATION

### CABLE EXTENDER APPLICATION

The DS30EA101 together with the DS30BA101 form a cable extender chipset optimized for extending serial data streams from serializer/deserializer (SerDes) pairs and FPGAs over 100Ω differential cables and 75Ω coaxial cables. Setting the correct DS30BA101 output amplitude and proper cable termination are essential for optimal operation. Figure 3 shows the recommended chipset configuration for 100Ω differential cable and Figure 4 shows the recommended chipset configuration for 75Ω coaxial cable.

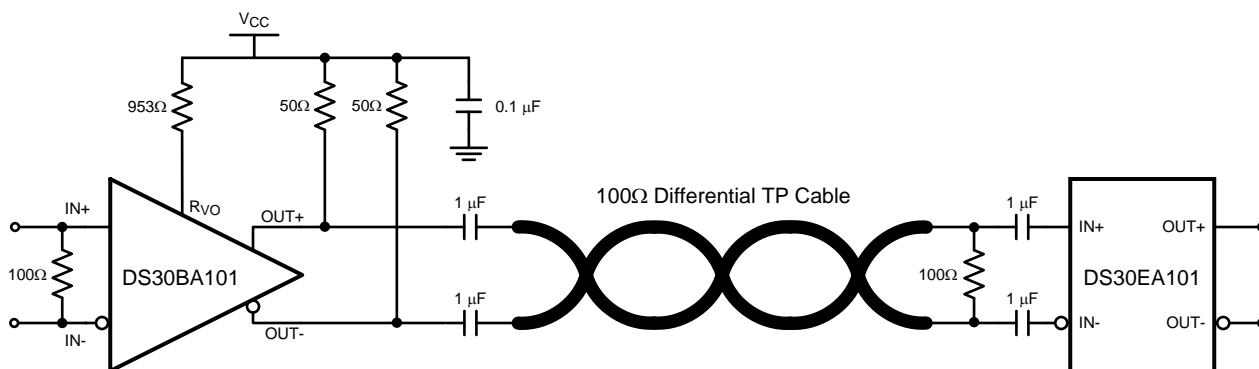
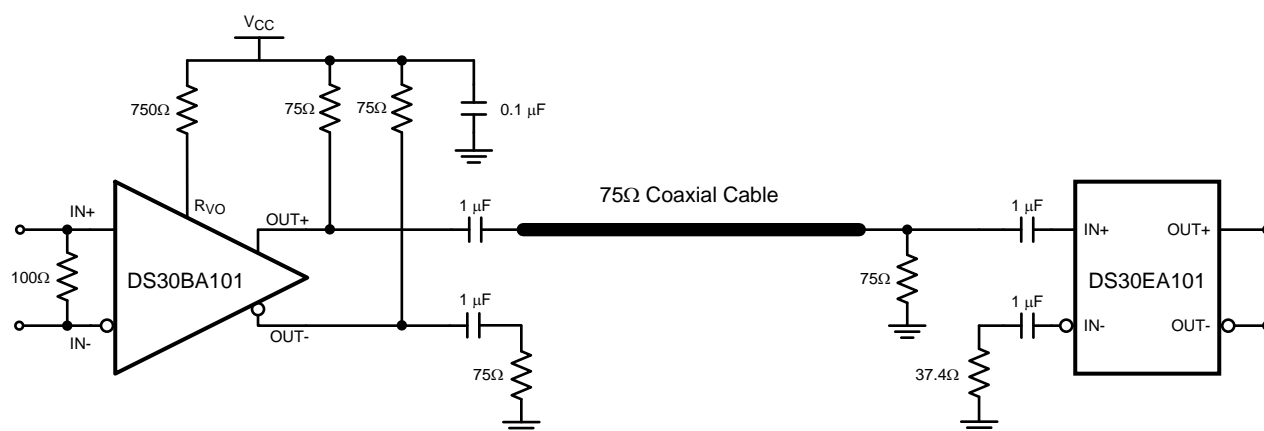


Figure 3. Cable Extender Chipset Application Circuit for 100Ω Differential Cable



**Figure 4. Cable Extender Chipset Application Circuit for 75Ω Coaxial Cable**

## REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format .....	<a href="#">6</a>

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">DS30EA101SQ/NOPB</a>	Active	Production	WQFN (RUM)   16	1000   SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	30EA101
DS30EA101SQ/NOPB.A	Active	Production	WQFN (RUM)   16	1000   SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	30EA101
<a href="#">DS30EA101SQE/NOPB</a>	Active	Production	WQFN (RUM)   16	250   SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	30EA101
DS30EA101SQE/NOPB.A	Active	Production	WQFN (RUM)   16	250   SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	30EA101
<a href="#">DS30EA101SQX/NOPB</a>	Active	Production	WQFN (RUM)   16	4500   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	30EA101
DS30EA101SQX/NOPB.A	Active	Production	WQFN (RUM)   16	4500   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	30EA101
DS30EA101SQX/NOPB.B	Active	Production	WQFN (RUM)   16	4500   LARGE T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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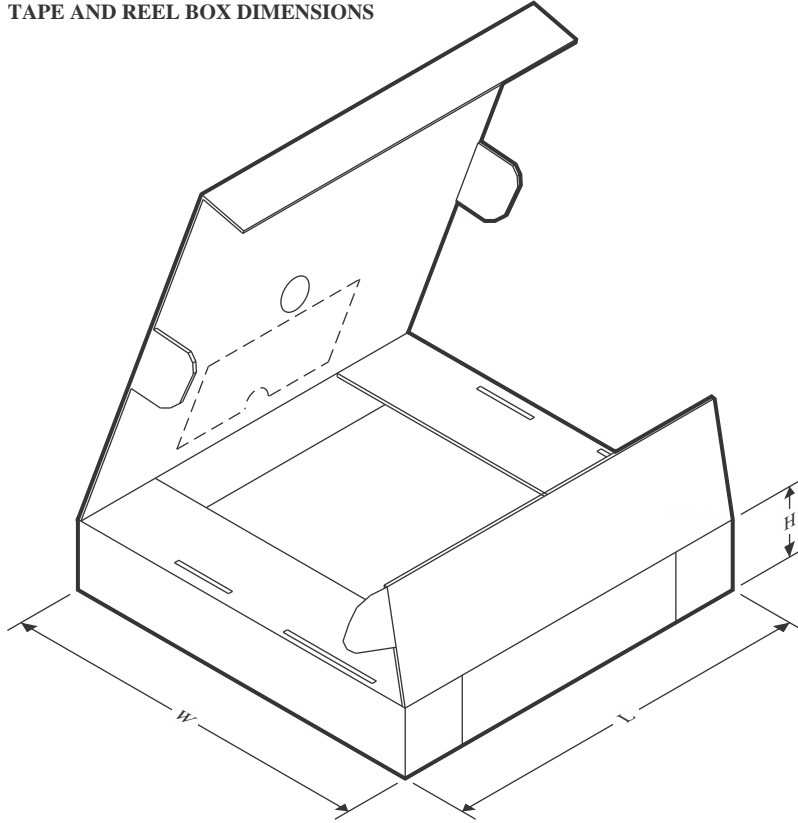
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

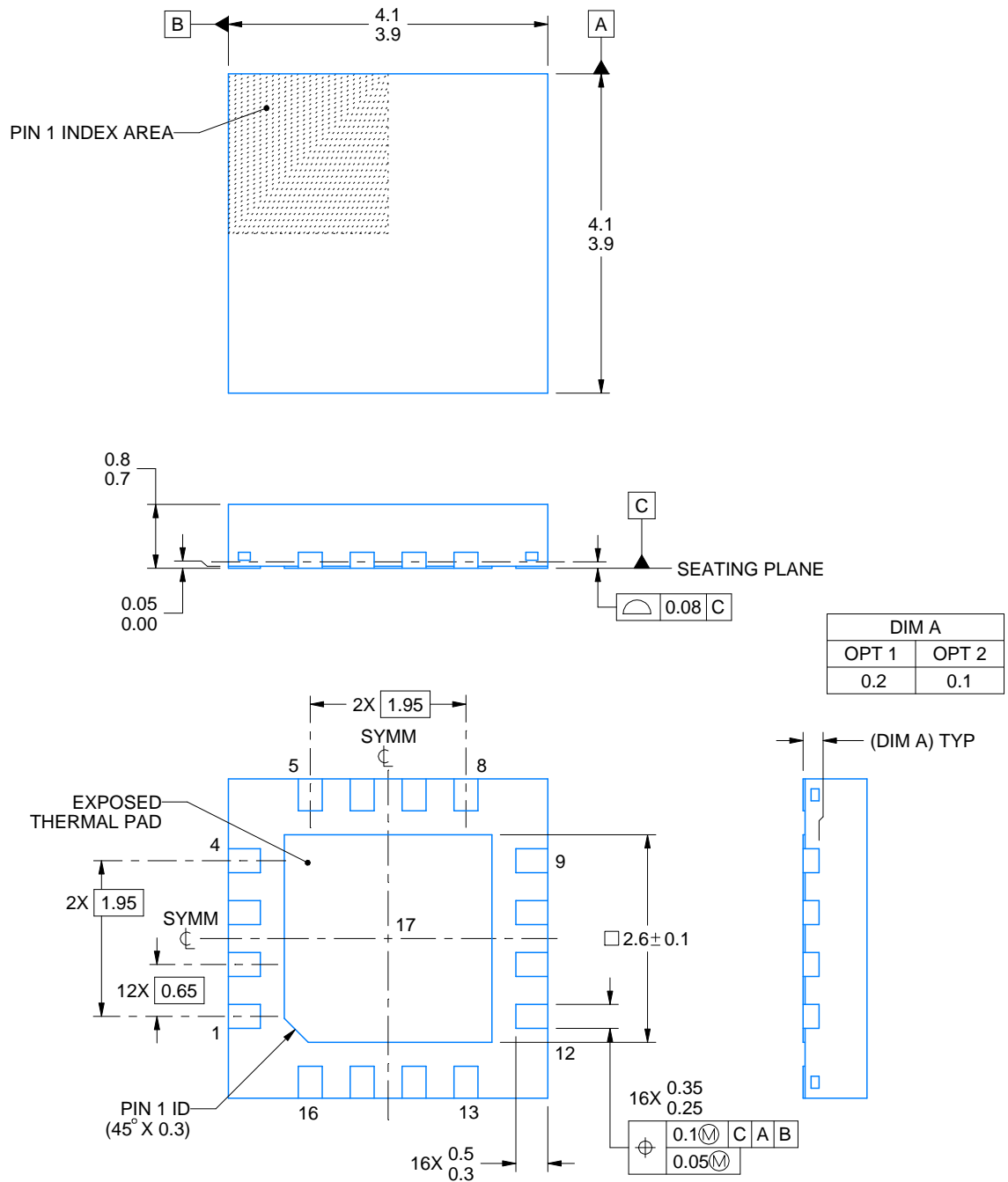
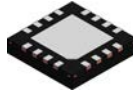
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS30EA101SQ/NOPB	WQFN	RUM	16	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
DS30EA101SQE/NOPB	WQFN	RUM	16	250	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
DS30EA101SQX/NOPB	WQFN	RUM	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS30EA101SQ/NOPB	WQFN	RUM	16	1000	208.0	191.0	35.0
DS30EA101SQE/NOPB	WQFN	RUM	16	250	208.0	191.0	35.0
DS30EA101SQX/NOPB	WQFN	RUM	16	4500	356.0	356.0	36.0



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## NOTES:

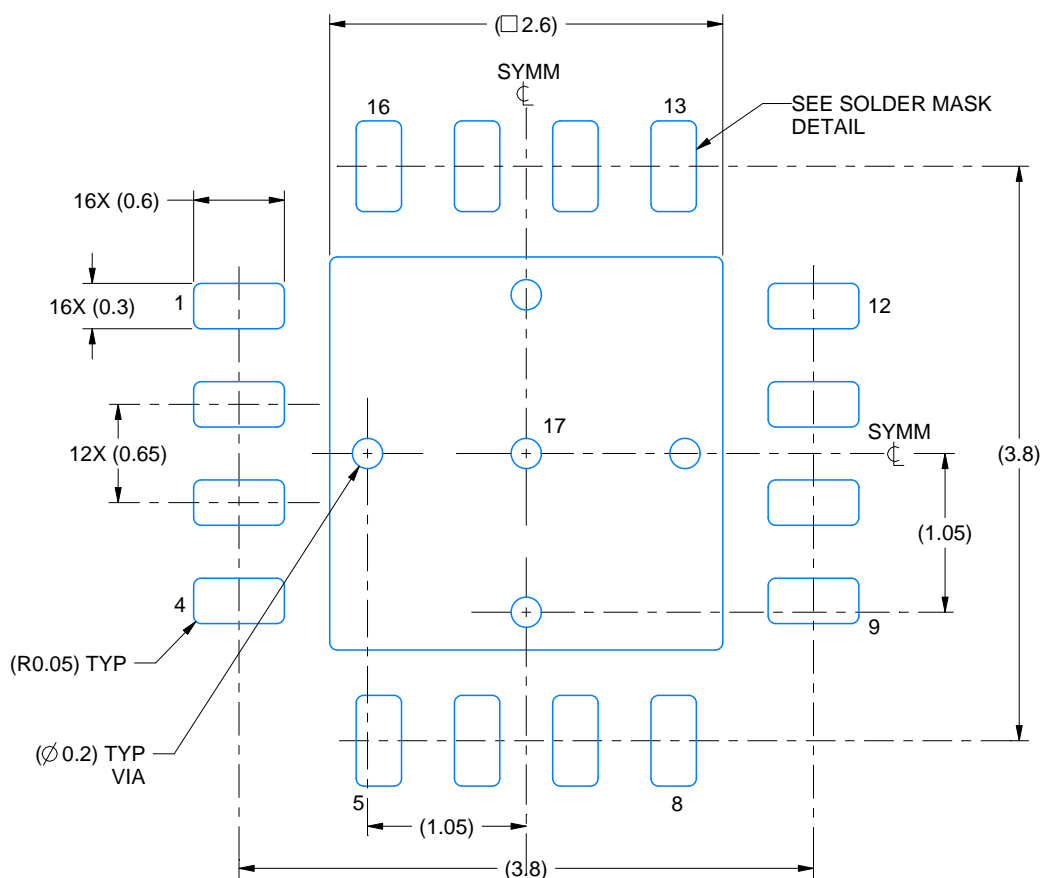
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

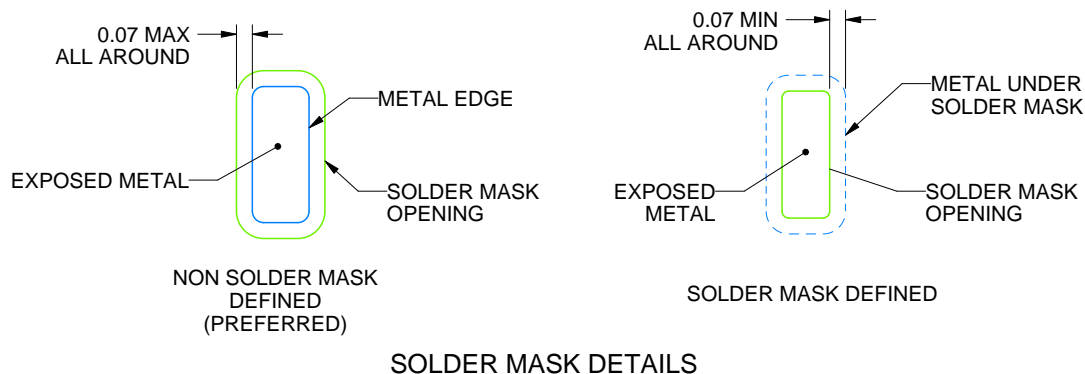
RUM0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



SOLDER MASK DETAILS

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NOTES: (continued)

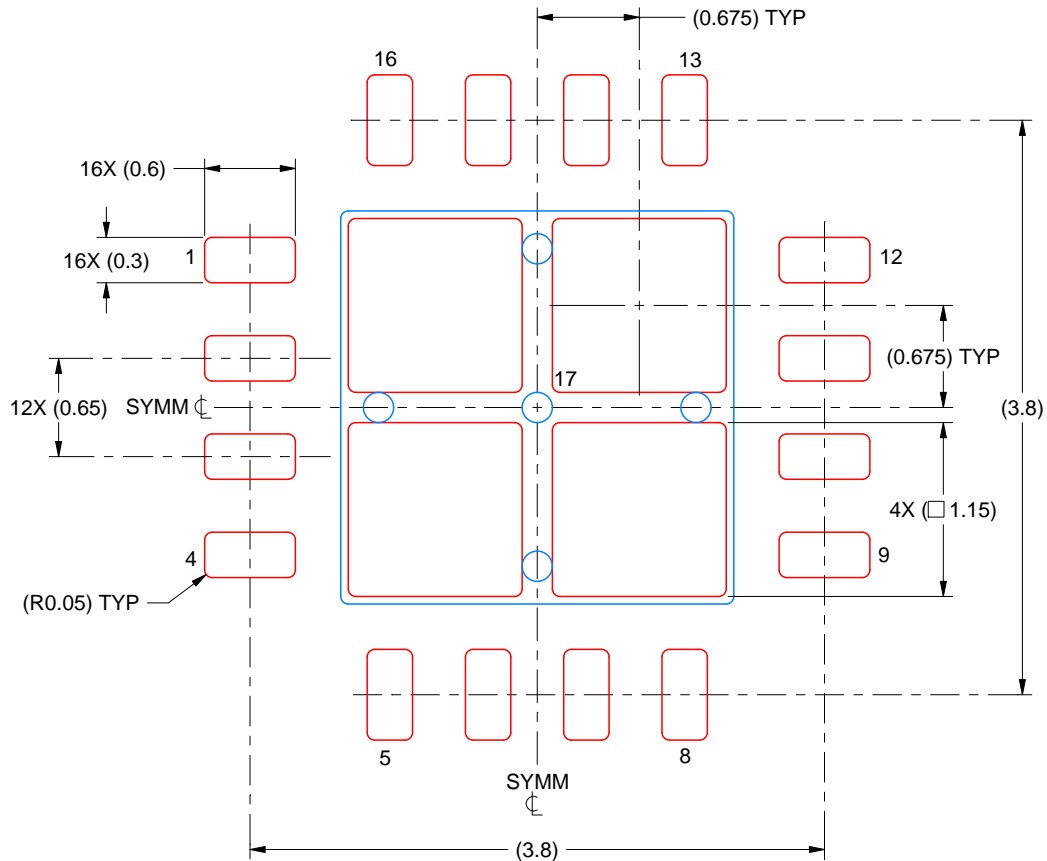
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RUM0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

EXPOSED PAD 17  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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