DS90CF383

DS90CF383 +3.3V LVDS Transmitter 24-Bit Flat Panel Display (FPD) Link-65 MHz

Literature Number: SNLS005

National Semiconductor

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DS90CF383
+3.3V LVDS Transmitter 24-Bit Flat Panel Display (FPD) Link—65 MHz

General Description

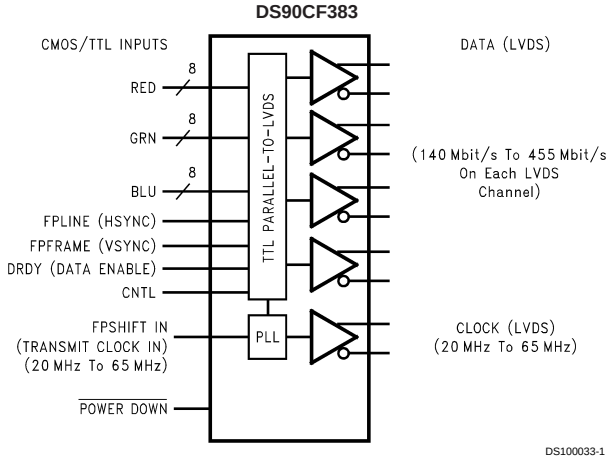
The DS90CF383 transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. At a transmit clock frequency of 65 MHz, 24 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughputs is 227 Mbytes/sec.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

- 20 to 65 MHz shift clock support
- Single 3.3V supply
- Chipset (Tx + Rx) power consumption < 250 mW (typ)
- Power-down mode (< 0.5 mW total)
- Single pixel per clock XGA (1024x768) ready
- Supports VGA, SVGA, XGA and higher addressability.
- Up to 227 Megabytes/sec bandwidth
- Up to 1.8 Gbps throughput
- Narrow bus reduces cable size and cost
- 290 mV swing LVDS devices for low EMI
- PLL requires no external components
- Low profile 56-lead TSSOP package
- Falling edge data strobe Transmitter
- Compatible with TIA/EIA-644 LVDS standard
- ESD rating > 7 kV
- Operating Temperature: −40˚C to +85˚C

Block Diagram



Order Number DS90CF383MTD
See NS Package Number MTD56

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
CMOS/TTL Input Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering, 4 sec)	+260˚C
Maximum Package Power Dissipation Capacity @ 25˚C	
MTD56 (TSSOP) Package: DS90CF383	1.63 W
Package Derating: DS90CF383	12.5 mW/˚C above +25˚C
ESD Rating (HBM, 1.5 kΩ, 100 pF)	> 7 kV

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+85	˚C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV_{PP}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA		2.7	3.3		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.1	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V			±5.1	±10	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V			−60	−120	mA
LVDS DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	345	450	mV
ΔV_{OD}	Change in V_{OD} between complimentary output states					35	mV
V_{OS}	Offset Voltage (Note 4)			1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between complimentary output states					35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−3.5	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	µA
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V				±10	µA
		V_{IN} = 0V, V_{CC} = 3.6V				±10	µA
TRANSMITTER SUPPLY CURRENT							
ICCTW	Transmitter Supply Current Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern *(Figures 1, 3)*	f = 32.5 MHz		31	45	mA
			f = 37.5 MHz		32	50	mA
			f = 65 MHz		42	55	mA
ICCTG	Transmitter Supply Current 16 Grayscale	R_L = 100Ω, C_L = 5 pF, 16 Grayscale Pattern *(Figures 2, 3)*	f = 32.5 MHz		23	35	mA
			f = 37.5 MHz		28	40	mA
			f = 65 MHz		31	45	mA
ICCTZ	Transmitter Supply Current Power Down	$\overline{\text{Power Down}}$ = Low Driver Outputs in TRI-STATE® under Power Down Mode			10	55	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Electrical Characteristics (Continued)

Note 2: Typical values are given for V_{CC} = 3.3V and T_A = +25C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: V_{OS} previously referred as V_{CM}.

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time *(Figure 3)*			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time *(Figure 3)*			0.75	1.5	ns
TCIT	TxCLK IN Transition Time *(Figure 4)*				5	ns
TCCS	TxOUT Channel-to-Channel Skew *(Figure 5)*			250		ps
TPPos0	Transmitter Output Pulse Position for Bit 0 *(Figure 12)*	f = 65 MHz	−0.4	0	0.3	ps
TPPos1	Transmitter Output Pulse Position for Bit 1		1.8	2.2	2.5	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		4.0	4.4	4.7	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		6.2	6.6	6.9	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		8.4	8.8	9.1	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		10.6	11.0	11.3	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		12.8	13.2	13.5	ns
TCIP	TxCLK IN Period *(Figure 6)*		15	T	50	ns
TCIH	TxCLK IN High Time *(Figure 6)*		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time *(Figure 6)*		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN *(Figure 6)*	f = 65 MHz	2.5			ns
THTC	TxIN Hold to TxCLK IN *(Figure 6)*		0			ns
TCCD	TxCLK IN to TxCLK OUT Delay 25˚C, V_{CC} = 3.3V *(Figure 7)*		3		5.5	ns
TPLLS	Transmitter Phase Lock Loop Set *(Figure 8)*				10	ms
TPDD	Transmitter Power Down Delay *(Figure 11)*				100	ns

AC Timing Diagrams

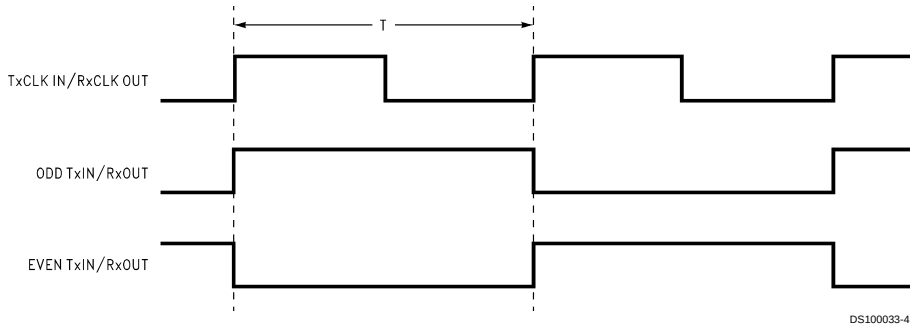


FIGURE 1. “Worst Case” Test Pattern

AC Timing Diagrams (Continued)

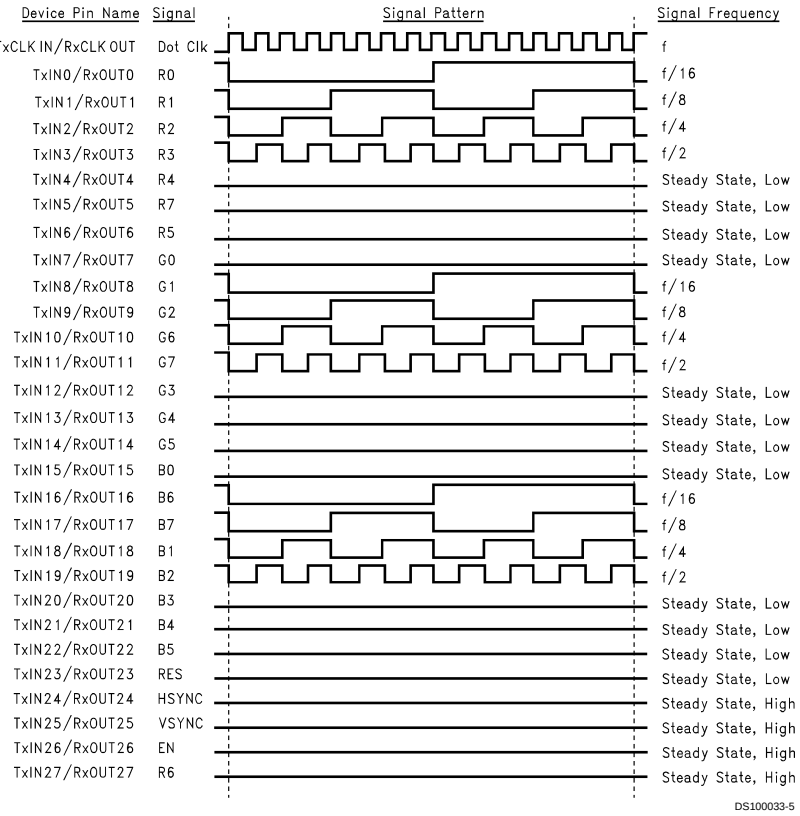


FIGURE 2. "16 Grayscale" Test Pattern (Notes 5, 6, 7, 8)

Note 5: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Note 6: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 7: *Figures 1, 2* show a falling edge data strobe (TxCLK IN/RxCLK OUT).

Note 8: Recommended pin to signal mapping. Customer may choose to define differently.

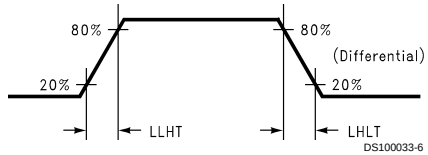


FIGURE 3. DS90CF383 (Transmitter) LVDS Output Load and Transition Times

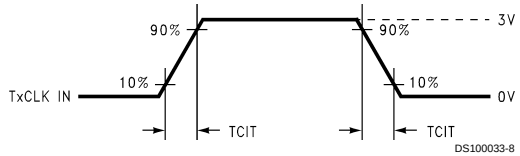
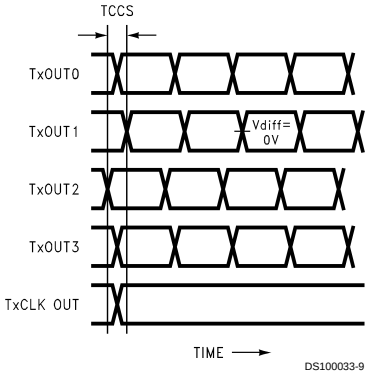


FIGURE 4. DS90CF383 (Transmitter) Input Clock Transition Time

AC Timing Diagrams (Continued)



Measurements at V_{diff} = 0V
TCCS measured between earliest and latest LVDS edges
TxCLK Differential Low → High Edge

FIGURE 5. DS90CF383 (Transmitter) Channel-to-Channel Skew

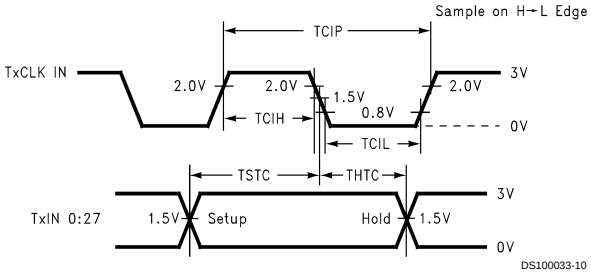


FIGURE 6. DS90CF383 (Transmitter) Setup/Hold and High/Low Times (Falling Edge Strobe)

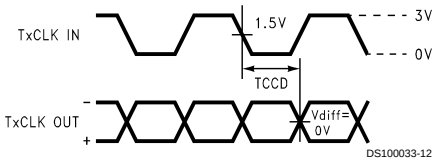


FIGURE 7. DS90CF383 (Transmitter) Clock In to Clock Out Delay

AC Timing Diagrams (Continued)

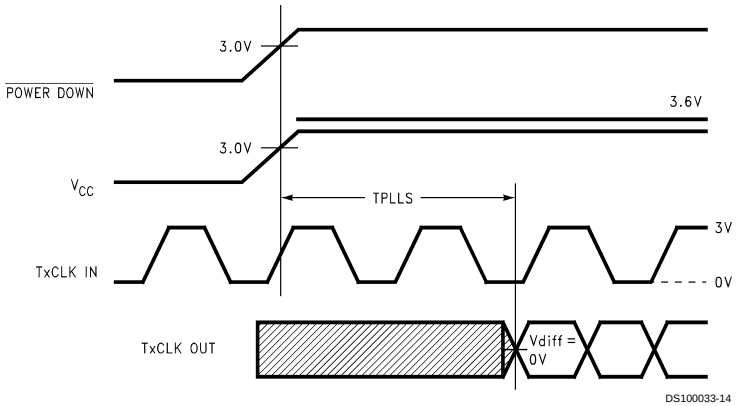


FIGURE 8. DS90CF383 (Transmitter) Phase Lock Loop Set Time

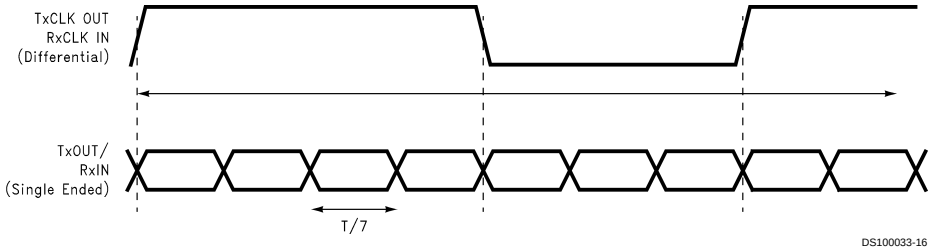


FIGURE 9. Seven Bits of LVDS in Once Clock Cycle

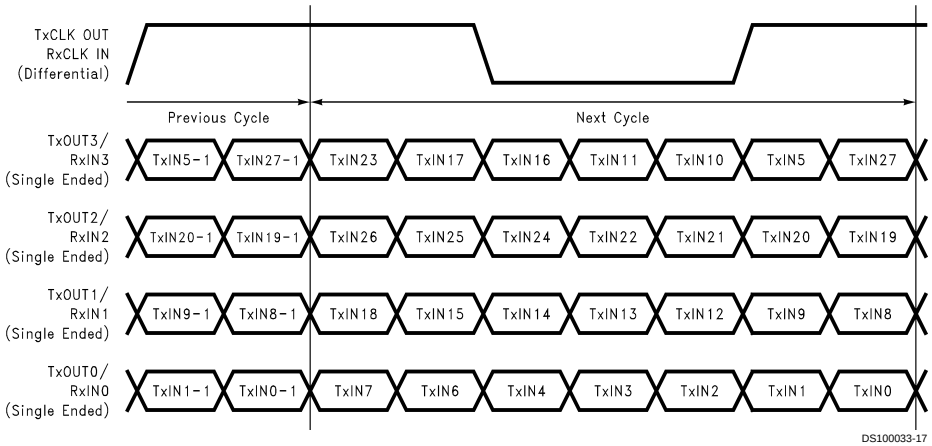


FIGURE 10. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs

AC Timing Diagrams (Continued)

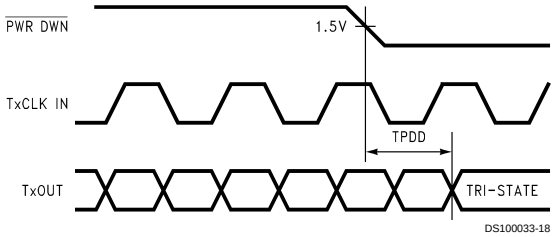


FIGURE 11. Transmitter Power Down Delay

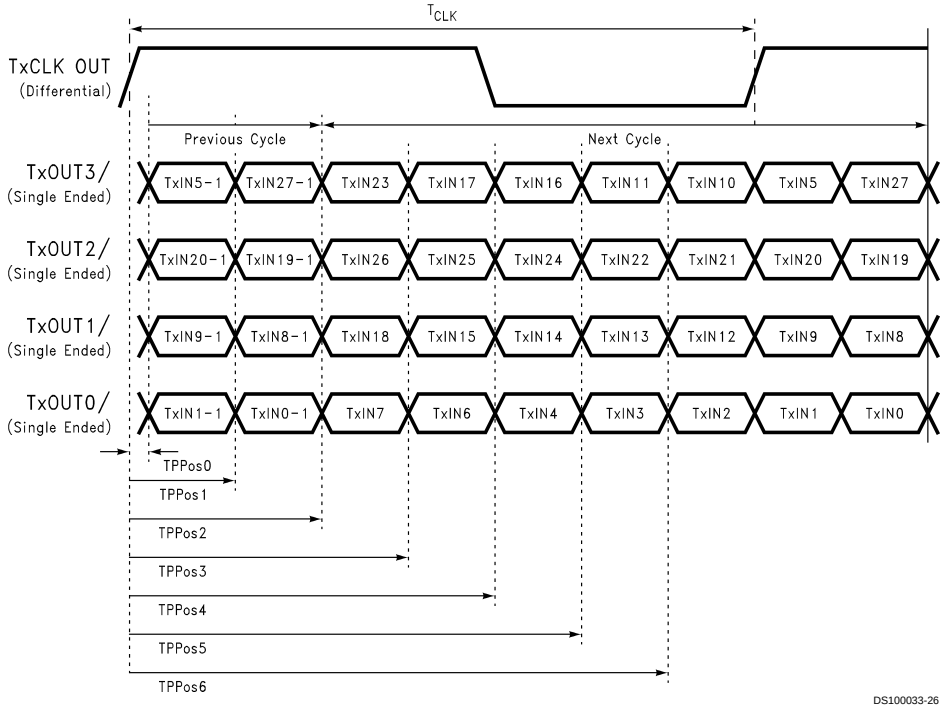


FIGURE 12. Transmitter LVDS Output Pulse Position Measurement

DS90CF383 Pin Description—FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	28	TTL level input. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines—FPLINE, FPFRAME and DRDY (also referred to as HSYNC, VSYNC, Data Enable).
TxOUT+	O	4	Positive LVDS differential data output.
TxOUT−	O	4	Negative LVDS differential data output.
FPSHIFT IN	I	1	TTL level clock input. The falling edge acts as data strobe. Pin name TxCLK IN.
TxCLK OUT+	O	1	Positive LVDS differential clock output.
TxCLK OUT−	O	1	Negative LVDS differential clock output.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. When asserted (low input) TRI-STATES the outputs, ensuring low current at power down.
V_{CC}	I	4	Power supply pins for TTL inputs.

DS90CF383 Pin Description — FPD Link Transmitter (Continued)

Pin Name	I/O	No.	Description
GND	I	4	Ground pins for TTL inputs.
PLL V_{CC}	I	1	Power supply pin for PLL.
PLL GND	I	2	Ground pins for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs.
LVDS GND	I	3	Ground pins for LVDS outputs.

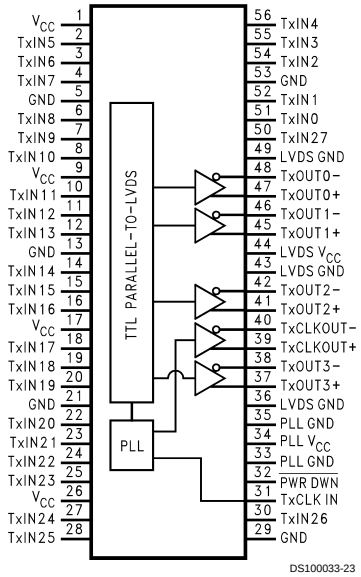
Applications Information

The DS90CF383 and DS90CF384 are backward compatible with the existing 5V FPD Link transmitter/receiver pair (DS90CF583 and DS90CF584). To upgrade from a 5V to a 3.3V system the following must be addressed:

1. Change 5V power supply to 3.3V. Provide this supply to the V_{CC}, LVDS V_{CC} and PLL V_{CC} of both the transmitter and receiver devices. This change may enable the removal of a 5V supply from the system, and power may be supplied from an existing 3V power source.
2. The DS90CF383 transmitter input and control inputs accept 3.3V TTL/CMOS levels. They are not 5V tolerant.

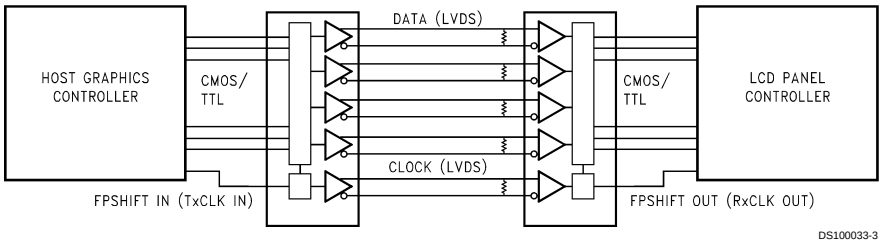
Pin Diagram

DS90CF383



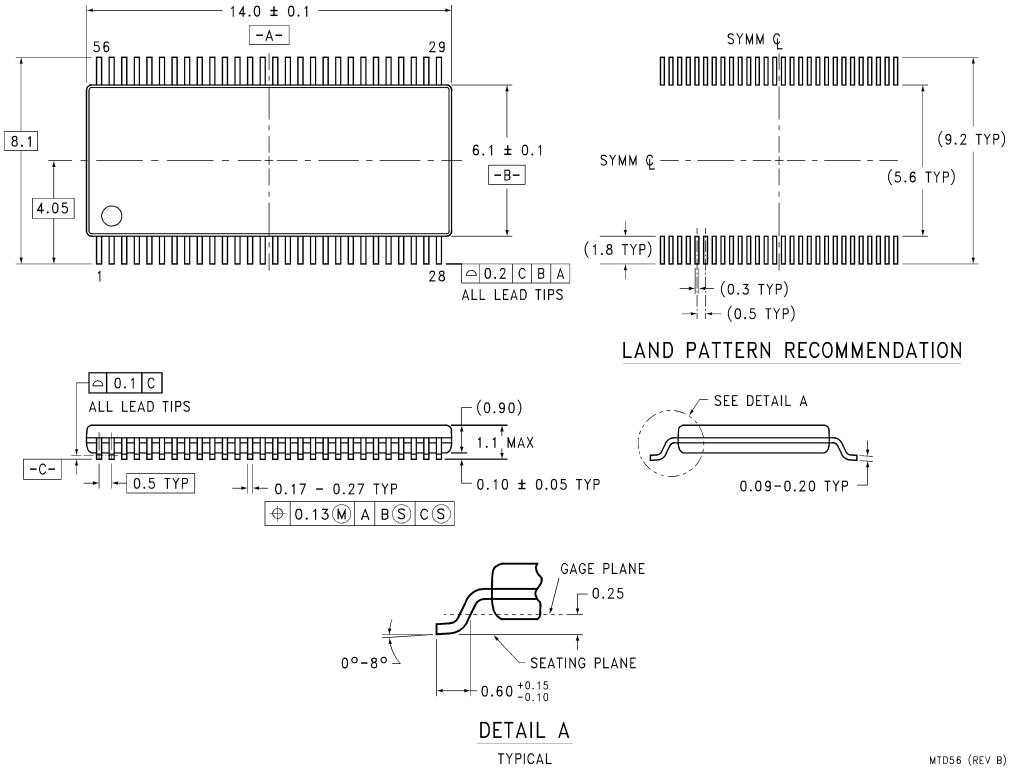
DS100033-23

Application



DS100033-3

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Molded Thin Shrink Small Outline Package, JEDEC
Order Number DS90CF383MTD
NS Package Number MTD56

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90CF383MTD/NOPB	NRND	Production	TSSOP (DGG) | 56	34 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-	DS90CF383MTD >B
DS90CF383MTD/NOPB.B	NRND	Production	TSSOP (DGG) | 56	34 | TUBE	Yes	SN	Level-2-260C-1 YEAR	See DS90CF383MTD/ NOPB	DS90CF383MTD >B
DS90CF383MTDX/NOPB	NRND	Production	TSSOP (DGG) | 56	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-	DS90CF383MTD >B
DS90CF383MTDX/NOPB.B	NRND	Production	TSSOP (DGG) | 56	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	See DS90CF383MTDX/ NOPB	DS90CF383MTD >B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

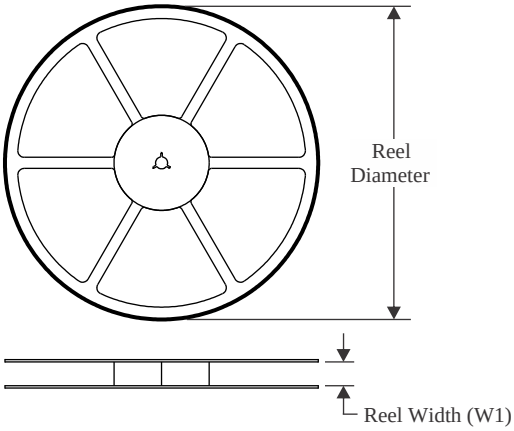
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

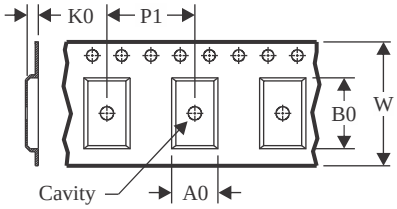
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

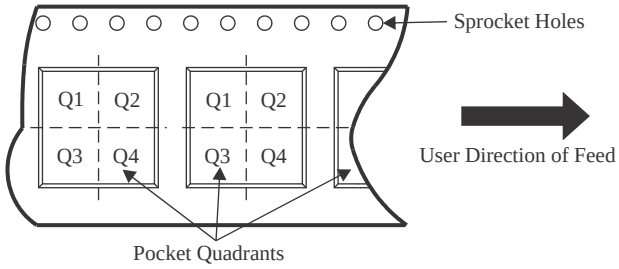


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

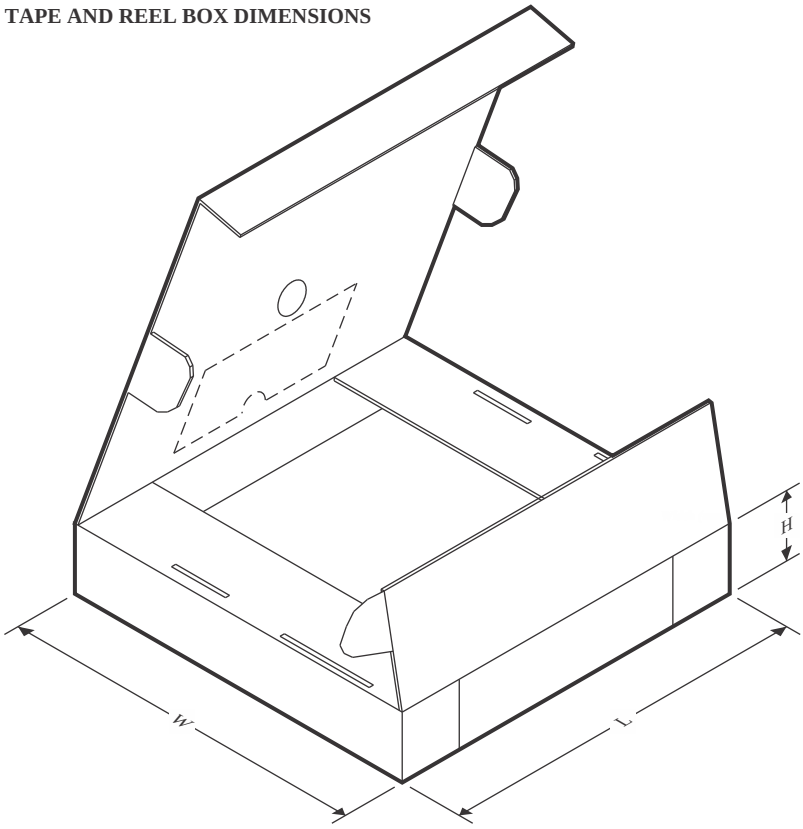
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90CF383MTDX/NOPB	TSSOP	DGG	56	1000	330.0	24.4	8.6	14.5	1.8	12.0	24.0	Q1

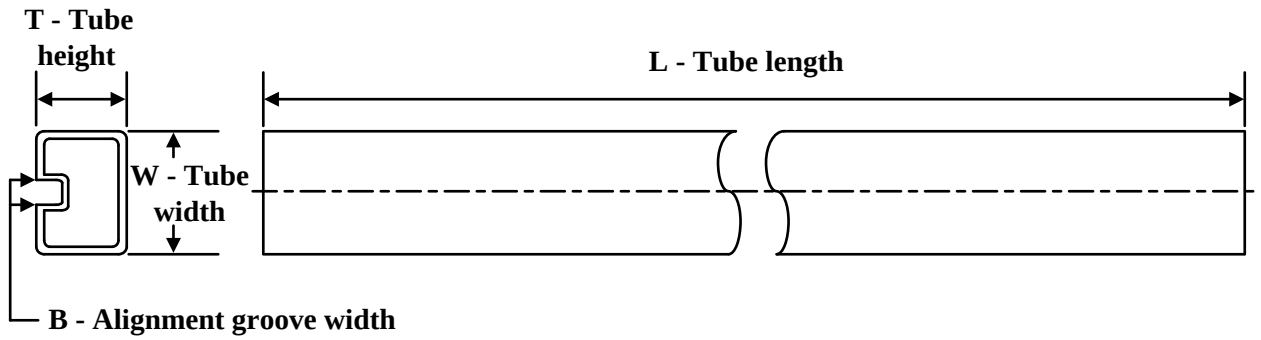
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90CF383MTDX/NOPB	TSSOP	DGG	56	1000	356.0	356.0	45.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS90CF383MTD/NOPB	DGG	TSSOP	56	34	495	10	2540	5.79
DS90CF383MTD/NOPB.B	DGG	TSSOP	56	34	495	10	2540	5.79

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