DS90LV028AH 高温 3V LVDS 双路差动线路接收器

1 特性

- 工作温度范围为 -40°C 至 +125°C
- >400Mbps (200MHz) 转换速率
- 50ps 差动偏斜（典型值）
- 0.1ns 通道到通道偏斜（典型值）
- 2.5ns 最大传播延迟
- 3.3V 电源设计
- 直通引脚
- 在断电模式下，LVDS 输入端具有高阻抗
- 低功耗设计（3.3V 静态条件下为 18mW）
- LVDS 输入可接受 LVDS/CML/LVPECL 信号
- 符合 ANSI/TIA/EIA-644 标准
- 采用 SOIC 封装

2 应用

- 板对板通信
- 测试和测量
- LED 视频墙
- 电机驱动器
- 无线基础设施
- 电信基础设施
- 多功能打印机
- NIC 卡
- 机架式服务器
- 超声波扫描仪

3 说明

DS90LV028AH 器件是一款双路 CMOS 差动线路接收器，专为需要超低功耗、 低噪音和高数据速率的 应用而设计。该器件旨在利用低电压差动信号 (LVDS) 技术支持超过 400Mbps (200MHz) 的数据速率。

DS90LV028AH 接受低电压（350mV 典型值）差动输入信号，并将其转换为 3V CMOS 输出电平。DS90LV028AH 采用了直通式设计，可简化 PCB 布局。

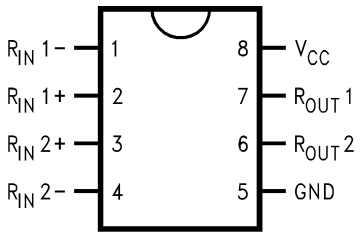
DS90LV028AH 和配套的 LVDS 线路驱动器 DS90LV027AH 为高速点对点接口提供了大功率 PECL/ECL 器件的替代 解决方案。

器件信息(1)

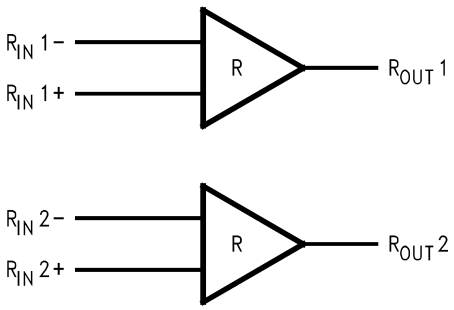
器件型号	封装	封装尺寸（标称值）
DS90LV028AH	SOIC (8)	4.90mm × 3.91mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

连接图



功能图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (April 2013) to Revision B **Page**

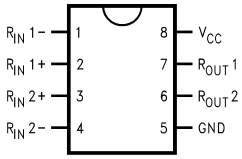
- 添加了*器件信息* 表、*器件比较* 表、*ESD 额定值* 表、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分。 ... 1
- 添加了导航链接，移除了数据表页顶端的 NRND 横幅 ... 1
- Moved the thermal resistance (θ_{JA}) parameter in the *Absolute Maximum Ratings* table to the *Thermal Information* table ... 4

Changes from Original (April 2013) to Revision A **Page**

- Changed layout of National Data Sheet to TI format ... 7

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
R_{IN}–	1, 4	I	Inverting receiver input pin
R_{IN}+	2, 3	I	Noninverting receiver input pin
R_{OUT}	6, 7	O	Receiver output pin
V_{CC}	8	I	Power supply pin, +3.3 V ± 0.3 V
GND	5	I	Ground pin

6 Specifications

6.1 Absolute Maximum Ratings(1)(2)

		MIN	MAX	UNIT
Supply Voltage (V_{CC})		−0.3	4	V
Input Voltage (R_{IN}+, R_{IN}−)		−0.3	3.9	V
Output Voltage (R_{OUT})		−0.3	V_{CC} + 0.3	V
Maximum Package Power Dissipation at +25°C	D Package		1025	mW
	Derate D Package (above +25°C)		8.2	mW/°C
Lead Temperature Range Soldering	(4 sec.)		260	°C
Maximum Junction Temperature			150	°C
Storage Temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2) (1.5 kΩ, 100 pF)	7000	V
		EIAJ (0 Ω, 200 pF)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±7000 V may actually have higher performance.
(2) ESD Rating:
HBM (1.5 kΩ, 100 pF) ≥ 7 kV
EIAJ (0Ω, 200 pF) ≥ 500V

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply Voltage (V_{CC})	+3	+3.3	+3.6	V
Receiver Input Voltage	GND		3	V
Ambient Temperature (T_A)	−40	25	+125	°C
Junction Temperature (T_J)			+130	°C

6.4 Thermal Information

THERMAL METRIC(1)		DS90LV028AH D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(1)(2)

PARAMETER		TEST CONDITIONS		PIN	MIN	TYP	MAX	UNIT
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2 V, 0 V, 3 V(3)		R_{IN}+, R_{IN}−			+100	mV
V_{TL}	Differential Input Low Threshold				−100			mV
I_{IN}	Input Current	V_{IN} = +2.8 V	V_{CC} = 3.6 V or 0 V		−10	±1	+10	µA
		V_{IN} = 0 V			−10	±1	+10	µA
		V_{IN} = +3.6 V	V_{CC} = 0 V		–20		+20	µA
V_{OH}	Output High Voltage	I_{OH} = −0.4 mA, V_{ID} = +200 mV		R_{OUT}	2.7	3.1		V
		I_{OH} = −0.4 mA, Inputs terminated			2.7	3.1		V
		I_{OH} = −0.4 mA, Inputs shorted			2.7	3.1		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = −200 mV				0.3	0.5	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V(4)			−15	−50	−100	mA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−1.5	−0.8		V
I_{CC}	No Load Supply Current	Inputs Open		V_{CC}		5.4	9	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified (such as V_{ID}).
(2) All typicals are given for: V_{CC} = +3.3 V and T_A = +25°C.
(3) V_{CC} is always higher than R_{IN}+ and R_{IN}− voltage. R_{IN}+ and R_{IN}− are allowed to have voltage range –0.05 V to +3.05 V. V_{ID} is not allowed to be greater than 100 mV when V_{CM} = 0 V or 3 V.
(4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

6.6 Switching Characteristics

V_{CC} = +3.3 V ± 10%, T_A = −40°C to +125°C(1)(2)

PARAMETER			MIN	TYP	MAX	UNIT
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 15 pF V_{ID} = 200 mV (Figure 14 and Figure 15)	1	1.6	2.5	ns
t_{PLHD}	Differential Propagation Delay Low to High		1	1.7	2.5	ns
t_{SKD1}	Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$(3)		0	50	650	ps
t_{SKD2}	Differential Channel-to-Channel Skew-same device(4)		0	0.1	0.5	ns
t_{SKD3}	Differential Part to Part Skew(5)		0		1	ns
t_{SKD4}	Differential Part to Part Skew(6)		0		1.5	ns
t_{TLH}	Rise Time			325	800	ps
t_{THL}	Fall Time			225	800	ps
f_{MAX}	Maximum Operating Frequency(7)		200	250		MHz

(1) C_L includes probe and jig capacitance.
(2) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50 Ω, t_r and t_f (0% to 100%) ≤ 3 ns for R_{IN}.
(3) t_{SKD1} is the magnitude difference in differential propagation delay time between the positive-going-edge and the negative-going-edge of the same channel.
(4) t_{SKD2} is the differential channel-to-channel skew of any event on the same device. This specification applies to devices having multiple receivers within the integrated circuit.
(5) t_{SKD3}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(6) t_{SKD4}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over the recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.
(7) f_{MAX} generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, differential (1.05 V to 1.35 V peak-to-peak). Output criteria: 60%/40% duty cycle, V_{OL} (max 0.4 V), V_{OH} (min 2.7 V), load = 15 pF (stray plus probes).

6.7 Typical Characteristics

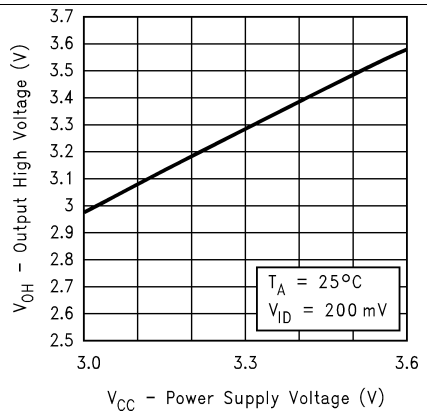


Figure 1. Output High Voltage vs Power Supply Voltage

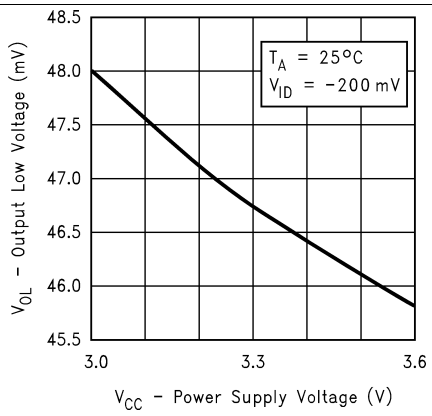


Figure 2. Output Low Voltage vs Power Supply Voltage

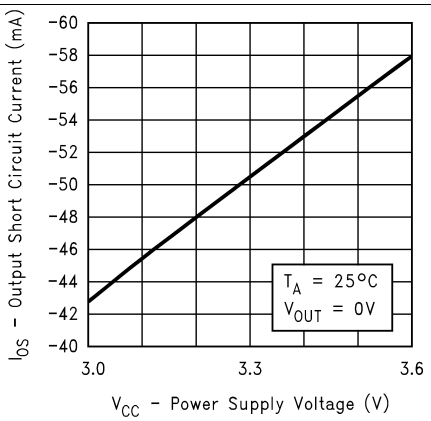


Figure 3. Output Short-Circuit Current vs Power Supply Voltage

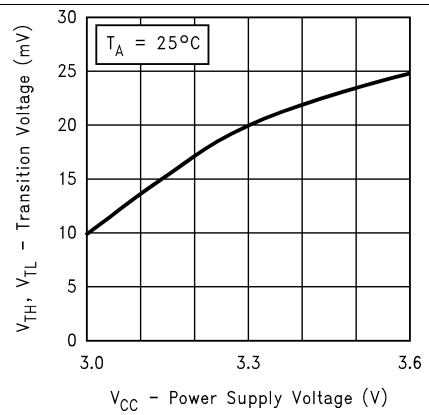


Figure 4. Differential Transition Voltage vs Power Supply Voltage

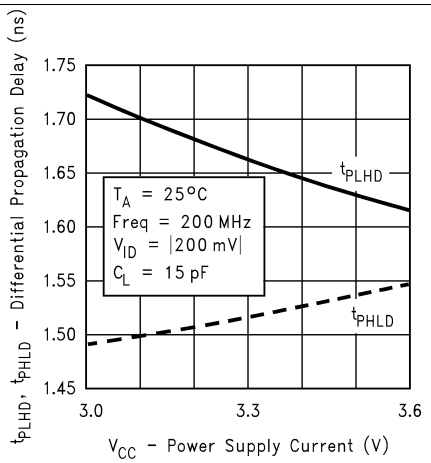


Figure 5. Differential Propagation Delay vs Power Supply Voltage

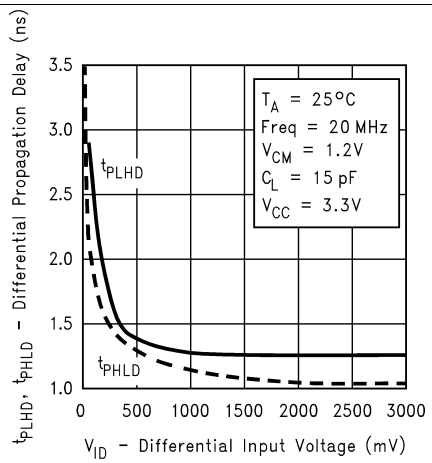


Figure 6. Differential Propagation Delay vs Differential Input Voltage

Typical Characteristics (continued)

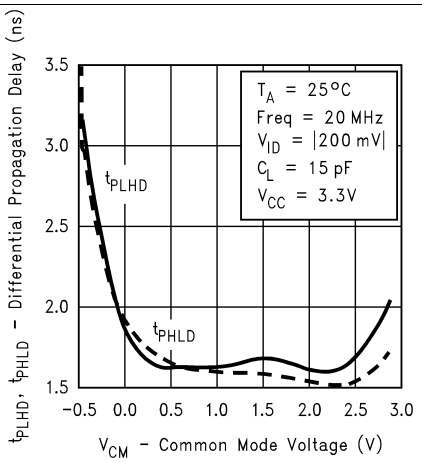


Figure 7. Differential Propagation Delay vs Common-Mode Voltage

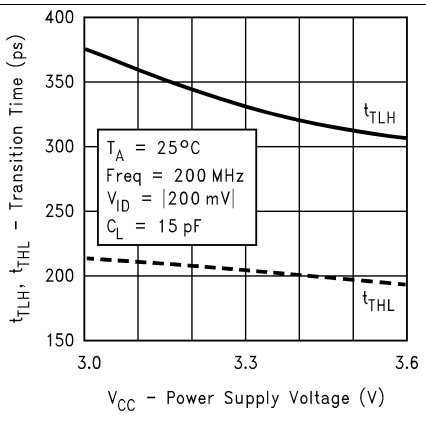


Figure 8. Transition Time vs Power Supply Voltage

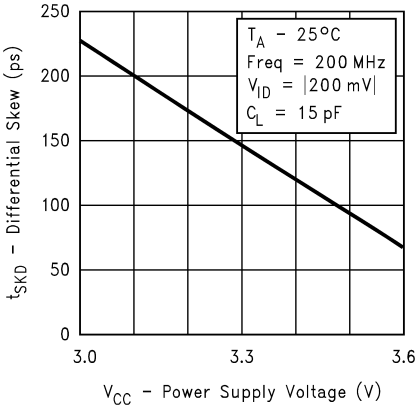


Figure 9. Differential Skew vs Power Supply Voltage

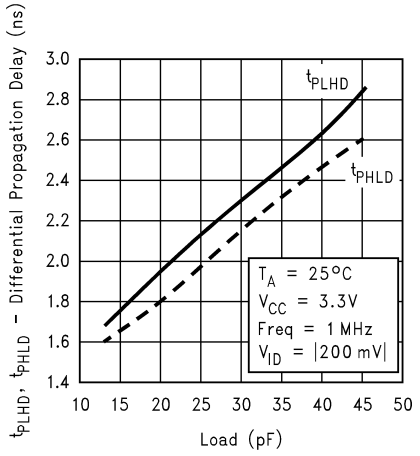


Figure 10. Differential Propagation Delay vs Load

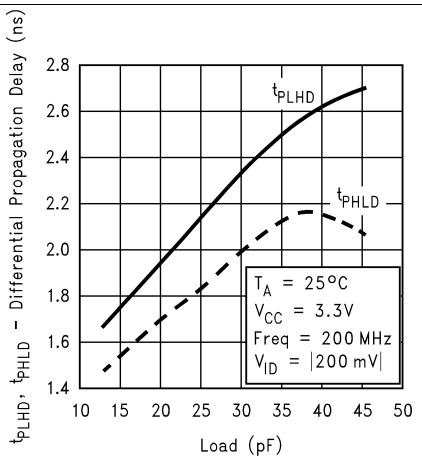


Figure 11. Differential Propagation Delay vs Load

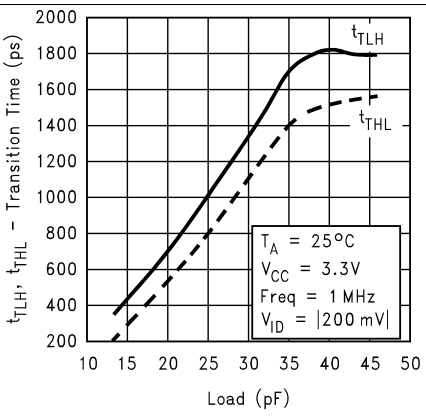


Figure 12. Transition Time vs Load

Typical Characteristics (continued)

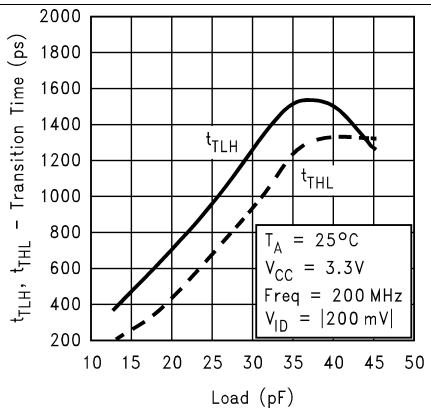


Figure 13. Transition Time vs Load

7 Parameter Measurement Information

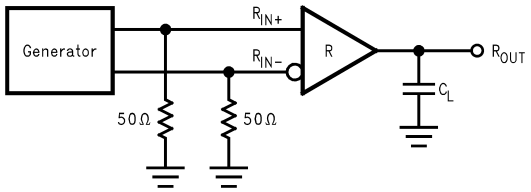


Figure 14. Receiver Propagation Delay and Transition Time Test Circuit

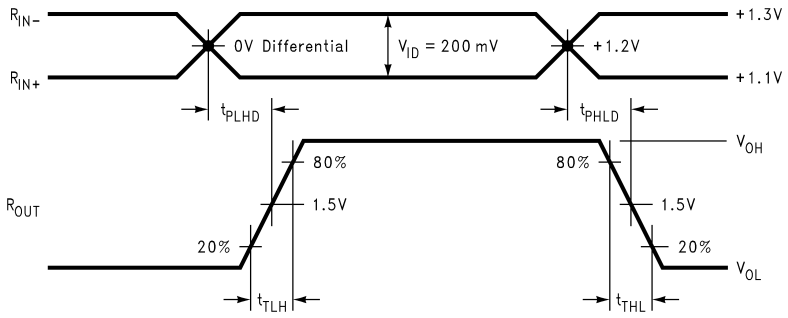


Figure 15. Receiver Propagation Delay and Transition Time Waveforms

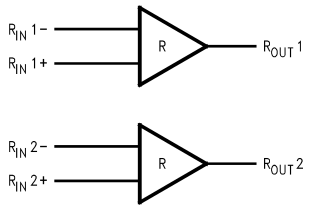
8 Detailed Description

8.1 Overview

The DS90LV028AH is a dual-channel, low-voltage differential signaling (LVDS) line receiver. It operates from a single power supply that is nominally 3.3 V, but the supply can be as low as 3 V and as high as 3.6 V. The input to the DS90LV028AH is a differential signal that complies with the LVDS Standard (TIA/EIA-644), and the output is a 3.3-V LVCMOS/LVTTL signal. The differential input signal operates with a signal level of 350 mV (nominally) at a common-mode voltage of 1.2 V. The differential nature of the inputs provides immunity to common-mode coupled signals that the driven signal may experience. A termination resistor of 100 Ω should be used with DS90LV028AH.

LVDS receivers are intended to be used primarily in point-to-point configurations. This type of configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media that may be a standard twisted-pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100 Ω. The integrated termination resistor converts the driver output (current mode) into a voltage without the need for external termination and is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

8.2 Functional Block Diagram



8.3 Feature Description

The DS90LV028AH is capable of detecting signals as low as 100 mV, over a ±1-V common-mode range centered around 1.2 V. The AC parameters of the input pins are optimized for a recommended operating input voltage range of 0 V to 2.4 V (measured from each pin to ground). The device will operate for receiver input voltages up to V_{DD}, but exceeding V_{DD} will turn on the ESD protection circuitry which will clamp the bus voltages.

Table 1. DS90LV028AH Receiver Function

INPUTS	OUTPUT
$[R_{IN}+] - [R_{IN}-]$	R_{OUT}
$V_{ID} \geq 0.1$ V	H
$V_{ID} \leq -0.1$ V	L

8.3.1 Termination

Use a termination resistor which best matches the differential impedance or your transmission line. The resistor should be between 90 Ω and 130 Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work correctly without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice.

Surface mount 1% to 2% resistors are the best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10 mm (12 mm MAX).

8.3.2 Threshold

The LVDS Standard (ANSI/TIA/EIA-644-A) specifies a maximum threshold of ±100 mV for the LVDS receiver. The DS90LV028AH supports an enhanced threshold region of −100 mV to 0 V. This is useful for fail-safe biasing. The threshold region is shown in the Voltage Transfer Curve (VTC) in Figure 16. The typical DS90LV028AH LVDS receiver switches at about −30 mV. Note that with V_{ID} = 0 V, the output will be in a HIGH state. With an external fail-safe bias of +25 mV applied, the typical differential noise margin is now the difference from the switch point to the bias point. In the example shown in Figure 16, this would be 55 mV of Differential Noise Margin (DNM) (+25 mV − (−30 mV)). With the enhanced threshold region of −100 mV to 0 V, this small external fail-safe biasing of +25 mV (with respect to 0 V) gives a DNM of a comfortable 55 mV. With the standard threshold region of ±100 mV, the external fail-safe biasing must be +25 mV with respect to +100 mV or +125 mV, giving a DNM of 155 mV that is a stronger fail-safe biasing than necessary for the DS90LV028AH. If more DNM is required, then a stronger fail-safe bias point can be set by changing resistor values.

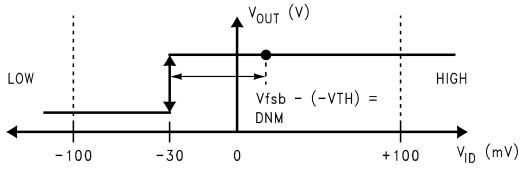


Figure 16. VTC of the DS90LV028AH LVDS Receiver

8.3.3 Fail-Safe Feature

The LVDS receiver is a high-gain, high-speed device that amplifies a small differential signal (20 mV) to LVCMOS/LVTTL logic levels. Due to the high gain and tight threshold of the receiver, take care to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated, or shorted receiver inputs.

1. **Open Input Pins:** It is not required to tie the receiver inputs to ground or any supply voltage. Internal fail-safe circuitry will ensure a HIGH, stable output state for open inputs.
2. **Terminated Input:** If the driver is disconnected (cable unplugged), or if the driver is in a power-off condition, the receiver output will again be in a HIGH state, even with the end cable 100-Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10 mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. A twisted-pair cable will offer better balance than flat ribbon cable.
3. **Shorted Inputs:** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0-V differential input voltage, the receiver output will remain in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4 V). It is only supported with inputs shorted and no external common-mode voltage applied.

External lower value pullup and pulldown resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pullup and pulldown resistors should be in the 5-kΩ to 15-kΩ range to minimize loading and waveform distortion to the receiver. The common-mode bias point should be set to approximately 1.2 V (less than 1.75 V) to be compatible with the internal circuitry.

The DS90LV028AH is compliant to the original ANSI EIA/TIA-644 specification and is also compliant to the new ANSI EIA/TIA-644-A specification with the exception of the newly added ΔI_{IN} specification. Due to the internal fail-safe circuitry, ΔI_{IN} cannot meet the 6-µA maximum specified. This exception will not be relevant unless more than 10 receivers are used.

Additional information on the fail-safe biasing of LVDS devices may be found in *AN-1194 Fail-Safe Biasing of LVDS Interfaces* (SNLA051).

8.4 Device Functional Modes

The device has one mode of operation that applies when operated within the *Recommended Operating Conditions*.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DS90LV028AH device is a dual-channel LVDS receiver. The functionality of this device is simple, yet extremely flexible, leading to its use in designs ranging from wireless base stations to desktop computers. The DS90LV027AH has a flow-through pinout that allows for easy PCB layout. The LVDS signals on one side of the device allow for easy matching of the electrical lengths for the differential pair trace lines between the driver and the receiver, and the signal placement allows the trace lines to be close together to couple noise as common-mode. Noise isolation is achieved with the LVDS signals on one side of the device and the TTL signals on the other side.

9.2 Typical Application

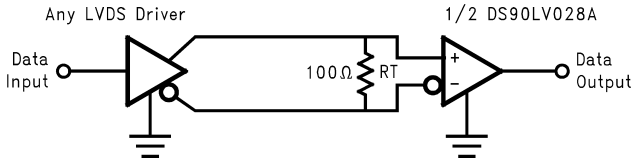


Figure 17. Balanced System Point-to-Point Application

9.2.1 Design Requirements

Table 2 lists the design parameters for this example.

Table 2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Receiver Supply Voltage (V_{CC})	3 to 3.6 V
Receiver Output Voltage	0 to 3.6 V
Signaling Rate	0 to 400 Mbps
Interconnect Characteristic Impedance	100 Ω
Termination Resistance	100 Ω
Number of Driver Nodes	2
Ground shift between driver and receiver	±1 V

9.2.2 Detailed Design Procedure

9.2.2.1 Receiver Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. Specifically, they create low-impedance paths between power and ground. At low frequencies, a good digital power supply offers very low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is quite often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 μF to 1000 μF) at the board-level do a good job up into the kHz range. Due to their size and length of their leads, they tend to have large inductance values at the switching frequencies of modern digital circuitry. To solve this problem, one must resort to the use of smaller capacitors (nF to μF range) installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because their lead inductance is about 1 nH. For comparison purposes, a typical capacitor with leads has a lead inductance around 5 nH.

The value of the bypass capacitors used locally with LVDS chips can be determined by Equation 1 and Equation 2 according to Johnson(1) equations 8.18 to 8.21. A conservative rise time of 200 ps and a worst-case change in supply current of 1 A covers the whole range of LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 200 mV. However, this figure varies depending on the noise budget available in the design. (1)

$$C_{chip} = \left(\frac{\Delta I_{\text{Maximum Step Change Supply Current}}}{\Delta V_{\text{Maximum Power Supply Noise}}} \right) \times T_{\text{Rise Time}} \quad (1)$$

$$C_{LVDS} = \left(\frac{1A}{0.2V} \right) \times 200\ ps = 0.001\ \mu F \quad (2)$$

Figure 18 lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10 µF) and the value of capacitance found above (0.001 µF). TI recommends that the user place the smallest value of capacitance as close to the chip as possible.

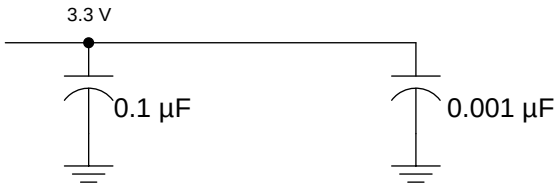


Figure 18. Recommended LVDS Bypass Capacitor Layout

9.2.2.2 Interconnecting Media

The physical communication channel between the driver and the receiver may be any balanced and paired metal conductors meeting the requirements of the LVDS standard, the key points of which are included here. This media may be twisted-pair, twinax cables, flat ribbon cables, or PCB traces.

The nominal characteristic impedance of the interconnect should be between 100 Ω and 120 Ω with a variation of no more than 10% (90 Ω to 132 Ω).

9.2.2.3 PCB Transmission Lines

As per the *LVDS Owner's Manual Design Guide, 4th Edition* (SNLA187), Figure 19 depicts several transmission line structures commonly used in printed-circuit boards (PCBs). Each structure consists of a signal line and return path with a uniform cross section along its length. A microstrip is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The dimensions of the structure along with the dielectric material properties determine the characteristic impedance of the transmission line (also called controlled-impedance transmission line).

When two signal lines are placed close by, they form a pair of coupled transmission lines. Figure 19 shows examples of edge-coupled microstrip lines, and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as a differential pair. The characteristic impedance of each line is called odd-mode impedance. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent (like if S is less than 2 W, for example), the differential pair is called a tightly-coupled differential pair. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.

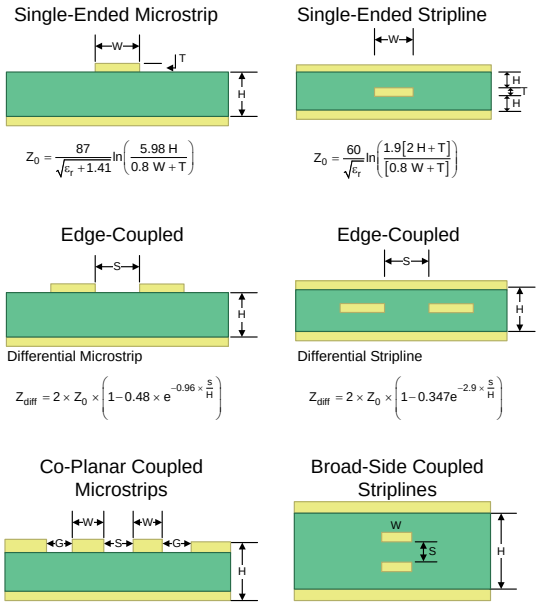


Figure 19. Controlled-Impedance Transmission Lines

9.2.2.4 Input Fail-Safe Biasing

External pullup and pulldown resistors may be used to provide enough of an offset to enable an input fail-safe under open-circuit conditions. This configuration ties the positive LVDS input pin to VDD through a pullup resistor, and the negative LVDS input pin is tied to GND by a pulldown resistor. The pullup and pulldown resistors should be in the 5 kΩ to 15 kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should ideally be set to approximately 1.2 V (less than 1.75 V) to be compatible with the internal circuitry. Refer to application note *AN-1194 Fail-Safe Biasing of LVDS Interfaces* (SNLA051) for more information.

9.2.2.5 Probing LVDS Transmission Lines on PCB

Always use high impedance (> 100 kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will skew results.

9.2.2.6 Cables and Connectors, General Comments

When choosing cable and connectors for LVDS, it is important to use controlled impedance media. The cables and connectors used should have a matched differential impedance of about 100 Ω. They should not introduce major impedance discontinuities.

Balanced cables (like twisted-pair cables, for example) are usually better than unbalanced cables (like ribbon cables, simple coax) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation and common-mode (not differential mode) noise, which the receiver will reject.

For cable distances < 0.5M, most cables can work effectively. For distances 0.5M ≤ d ≤ 10M, TI recommends using CAT 3 (category 3) twisted-pair cables which are readily available and relatively inexpensive.

9.2.3 Application Curve

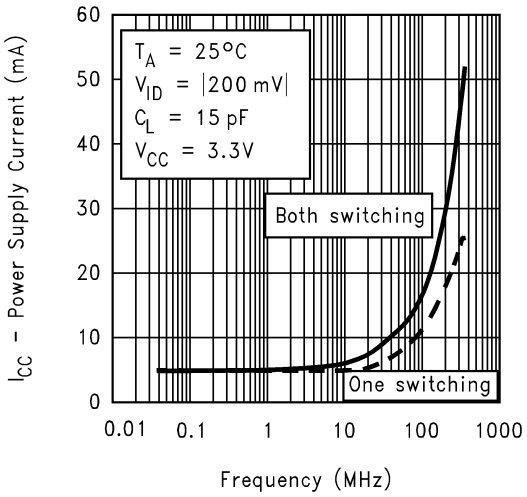


Figure 20. Power Supply Current vs Frequency

10 Power Supply Recommendations

The DS90LV028AH receiver is designed to operate from a single power supply with supply voltage in the range of 3.0 V to 3.6 V. In a typical application, a driver and a receiver may be on separate boards, or even separate equipment. In these cases, separate supplies would be used at each location. The expected ground potential difference between the driver power supply and the receiver power supply would be less than |±1 V|. Board level and local device level bypass capacitance should be used.

11 Layout

11.1 Layout Guidelines

11.1.1 Microstrip vs. Stripline Topologies

As per the *LVDS Application and Data Handbook* (SLLD009), printed-circuit boards usually offer designers two transmission line options: microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in Figure 21.

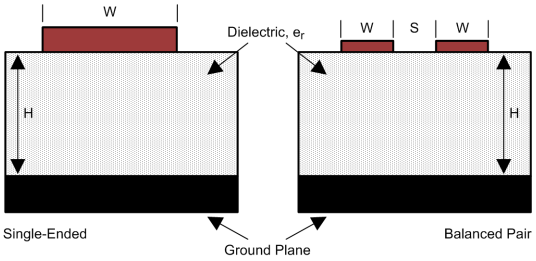


Figure 21. Microstrip Topology

Layout Guidelines (continued)

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines when possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances. Footnotes 1[(2)], 2[(3)], and 3[(4)] provide formulas for Z_O and t_{PD} for differential and single-ended traces. (2) (3) (4)

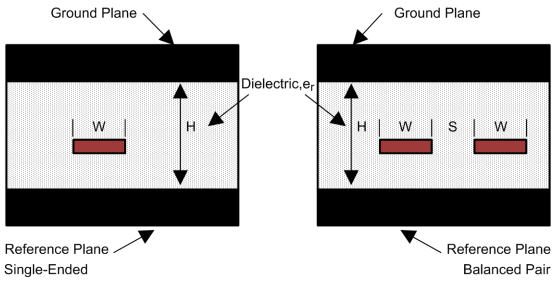


Figure 22. Stripline Topology

11.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or an equivalent, usually provides adequate performance for use with LVDS signals. If rise or fall times of LVCMOS/LVTTL signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 may be desired. When the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry should be solder-plated (60/40) to 7.62 μm or 0.0003 in (minimum).
- Copper plating should be 25.4 μm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

11.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, the designer must decide how many levels to use in the stack. To reduce the LVCMOS/LVTTL to LVDS crosstalk, it is good practice to have at least two separate signal planes as shown in Figure 23.

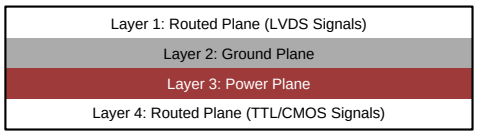


Figure 23. Four-Layer PCB Board

NOTE

The separation between layers 2 and 3 should be 127 μm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

(2) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
(3) Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
(4) Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

Layout Guidelines (continued)

One of the most common stack configurations is the six-layer board, as shown in Figure 24.

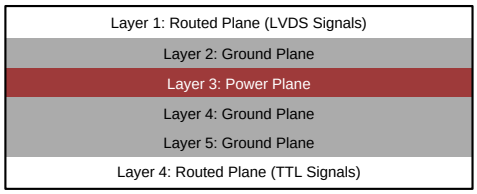


Figure 24. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity, but fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes in addition to ensuring reference to a ground plane for signal layers 1 and 6.

11.1.4 Separation Between Traces

The separation between traces depends on several factors, but the amount of coupling that can be tolerated usually dictates the actual separation. Low-noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

In the case of two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces must be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

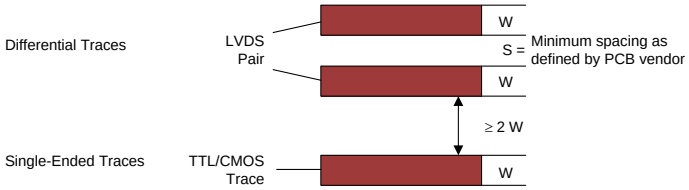


Figure 25. 3-W Rule for Single-Ended and Differential Traces (Top View)

Exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

11.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close to its originating trace as possible. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

11.1.6 Decoupling

Each power or ground lead of a high-speed device should be connected to the PCB through a low inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. TI recommends that the user place a via immediately adjacent to the pin to avoid adding trace inductance. Placing a power plane closer to the top of the board reduces the effective via length and its associated inductance.

Layout Guidelines (continued)

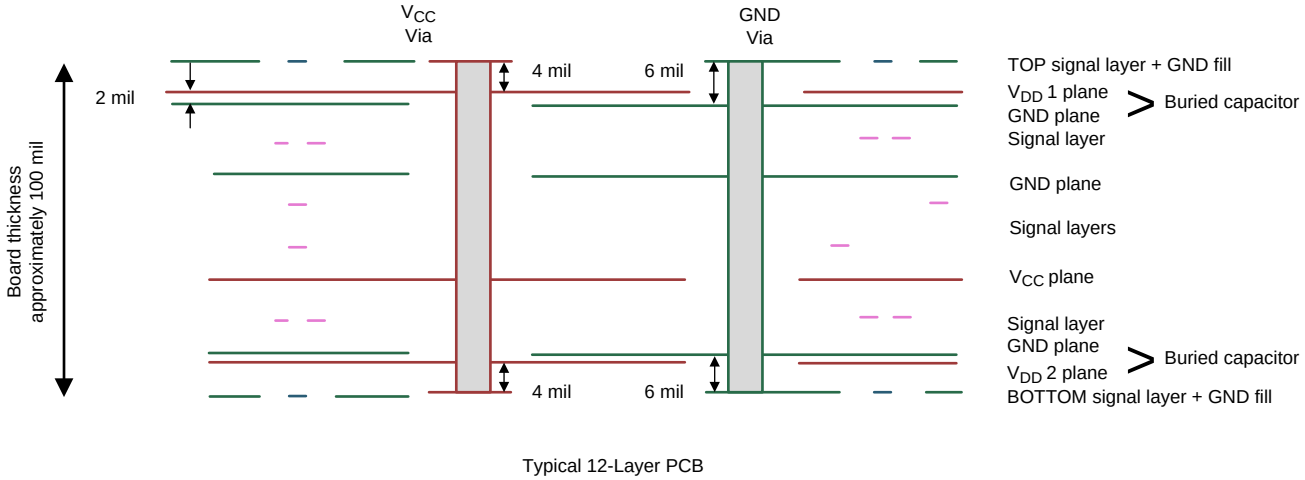


Figure 26. Low Inductance, High-Capacitance Power Connection

Bypass capacitors should be placed close to V_{DD} pins. They can be placed conveniently near the corners or underneath the package to minimize the loop area. This extends the useful frequency range of the added capacitance. Small-physical-size capacitors, such as 0402 or even 0201, or X7R surface-mount capacitors should be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor as shown in Figure 27(a).

An X7R surface-mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low-impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 μF, and 0.1 μF are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2 to 3 mils. With a 2-mil FR4 dielectric, there is approximately 500 pF per square inch of PCB. Refer back to Figure 19 for some examples. Many high-speed devices provide a low-inductance GND connection on the backside of the package. This center dap must be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the small Surface Mount Technology (SMT) package. Placing vias around the perimeter of the dap connection ensures proper heat spreading and the lowest possible die temperature. Placing high-performance devices on opposing sides of the PCB using two GND planes (as shown in Figure 19) creates multiple paths for heat transfer. Often thermal PCB issues are the result of one device adding heat to another, resulting in a very high local temperature. Multiple paths for heat transfer minimize this possibility. In many cases the GND dap that is so important for heat dissipation makes the optimal decoupling layout impossible to achieve due to insufficient pad-to-dap spacing as shown in Figure 27(b). When this occurs, placing the decoupling capacitor on the backside of the board keeps the extra inductance to a minimum. It is important to place the V_{DD} via as close to the device pin as possible while still allowing for sufficient solder mask coverage. If the via is left open, solder may flow from the pad and into the via barrel. This will result in a poor solder connection.

Figure 27. Typical Decoupling Capacitor Layouts

Layout Guidelines (continued)

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in Figure 28.

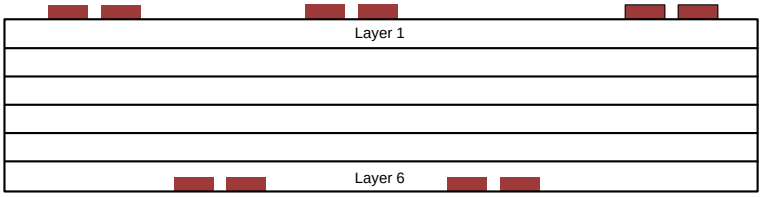


Figure 28. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers. Thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in Figure 29. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

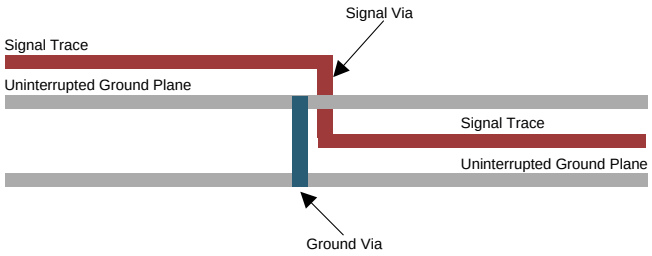


Figure 29. Ground Via Location (Side View)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

11.2 Layout Example

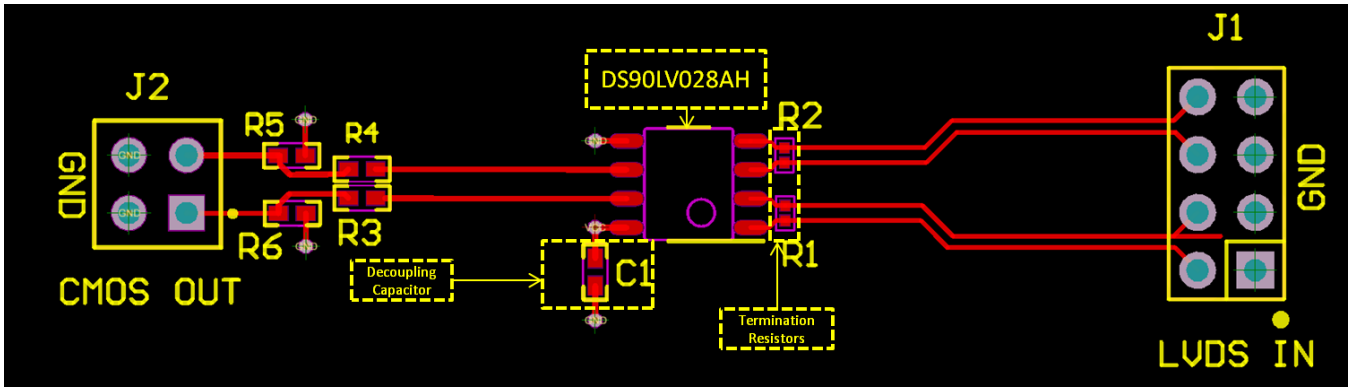


Figure 30. Example DS90LV028AH Layout

12 器件和文档支持

12.1 相关文档

请参阅如下相关文档：

- 《*LVDS 用户手册*》(SNLA187)
- 《*AN-808 长距离传输线路和数据信号质量*》 (SNLA028)
- 《*AN-977 LVDS 信号质量：使用眼图测量抖动测试报告 #1*》 (SNLA166)
- 《*AN-971 LVDS 技术概览*》 (SNLA165)
- 《*AN-916 电缆选择实用指南*》 (SNLA219)
- 《*AN-805 差动线路驱动器功耗计算*》 (SNOA233)
- 《*AN-903 差动终端技巧对比*》 (SNLA034)
- 《*LVDS 接口的 AN-1194 失效防护偏置*》(SNLA051)

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.4 商标

E2E is a trademark of Texas Instruments.
Rogers is a trademark of Rogers Corporation.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90LV028AHM/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	90LV0 28AHM
DS90LV028AHM/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	90LV0 28AHM
DS90LV028AHMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	90LV0 28AHM
DS90LV028AHMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	90LV0 28AHM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

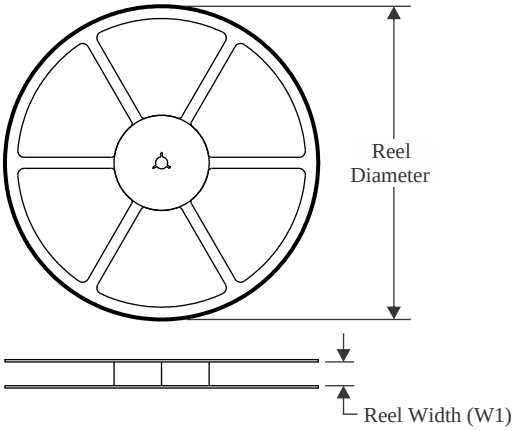
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

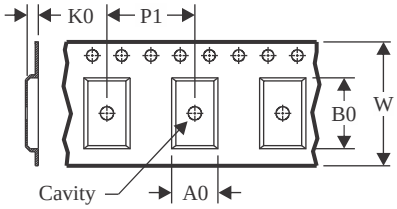
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

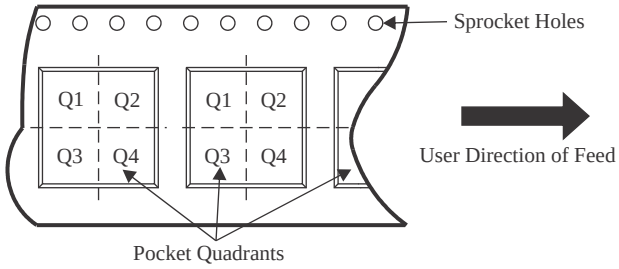


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

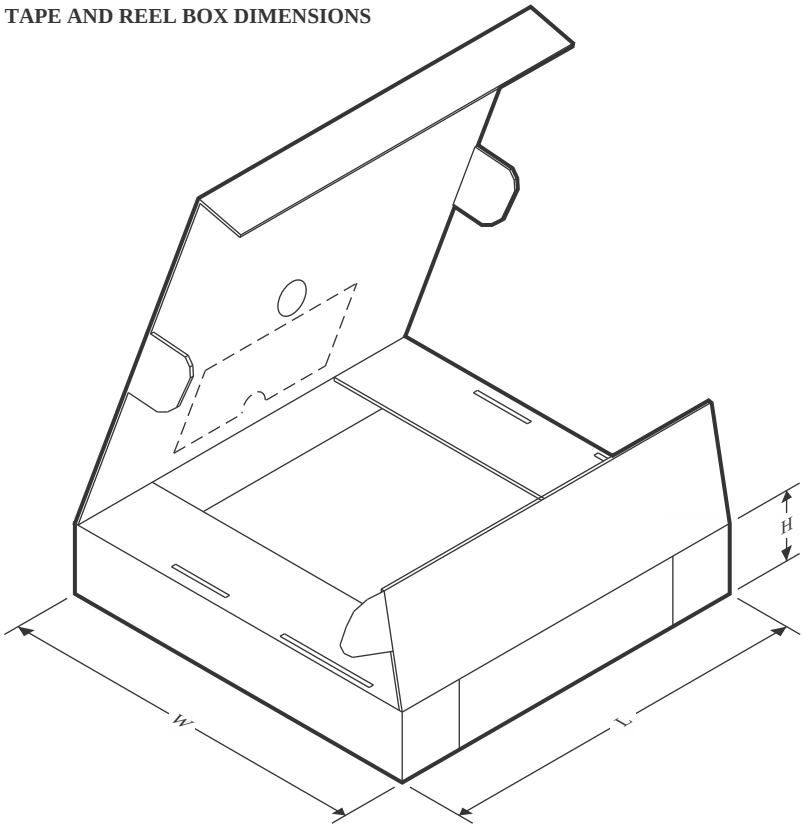
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV028AHMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

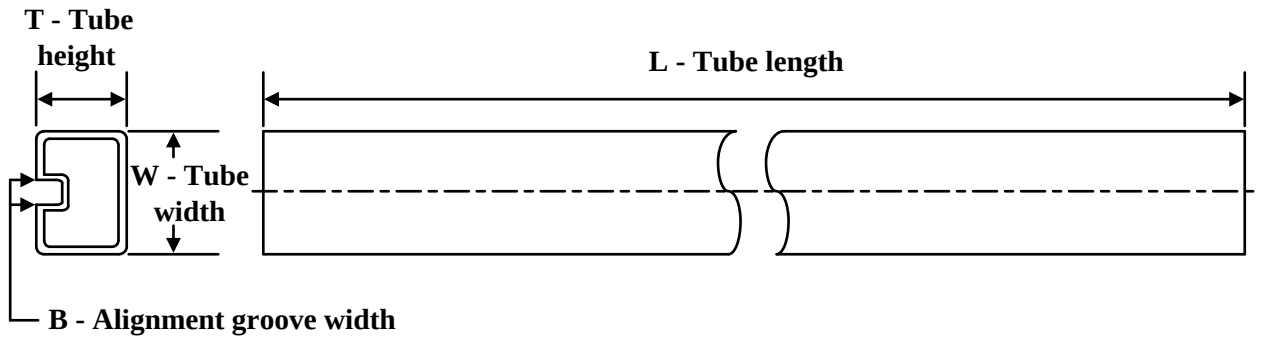
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

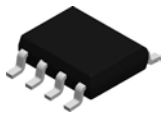
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV028AHMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS90LV028AHM/NOPB	D	SOIC	8	95	495	8	4064	3.05
DS90LV028AHM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05

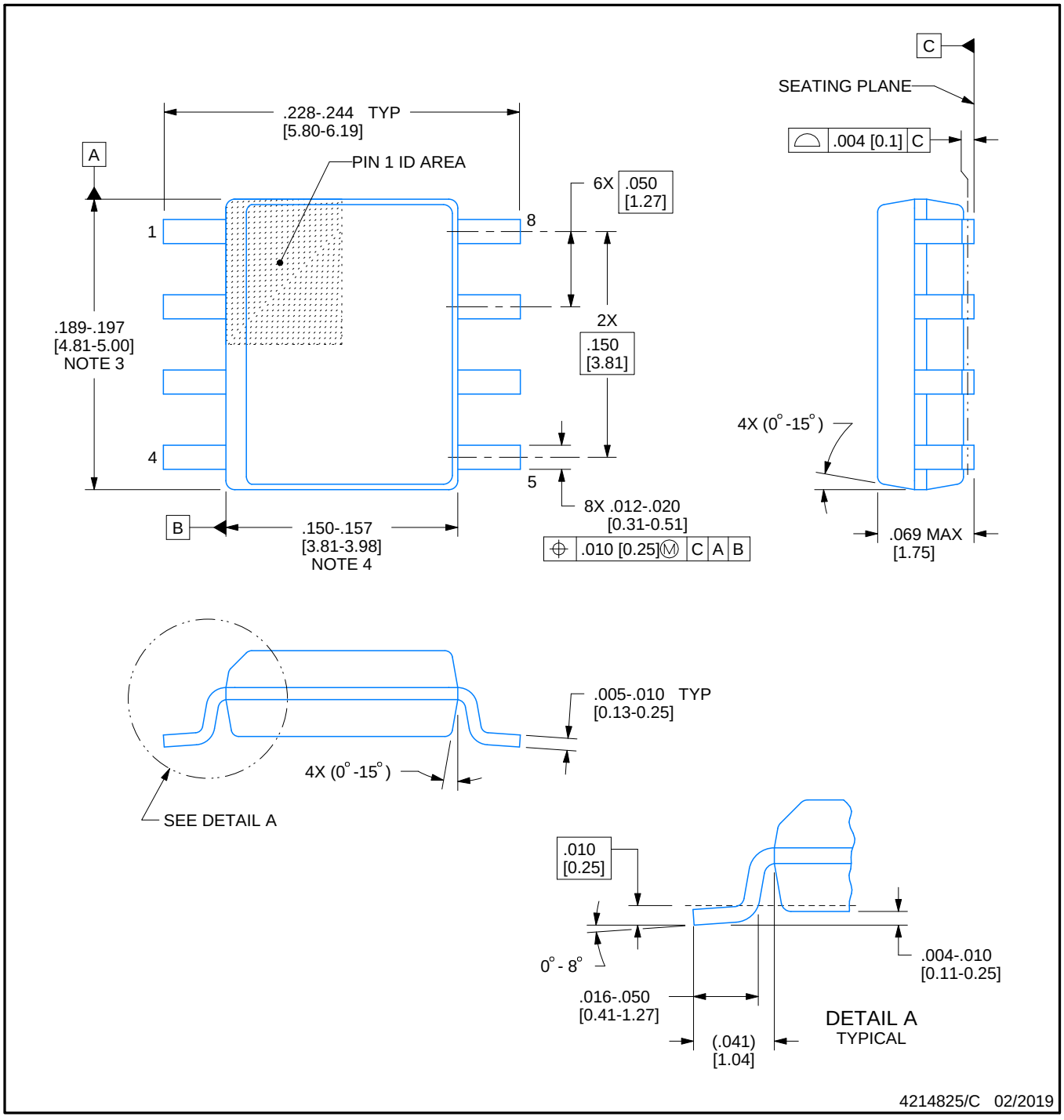


PACKAGE OUTLINE

D0008A

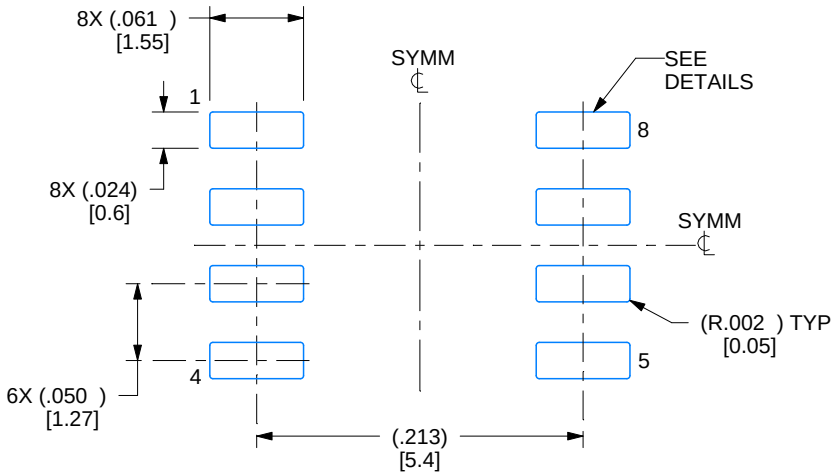
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

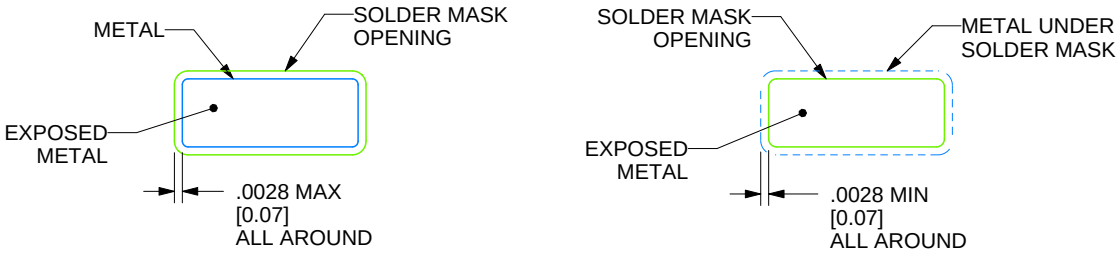


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

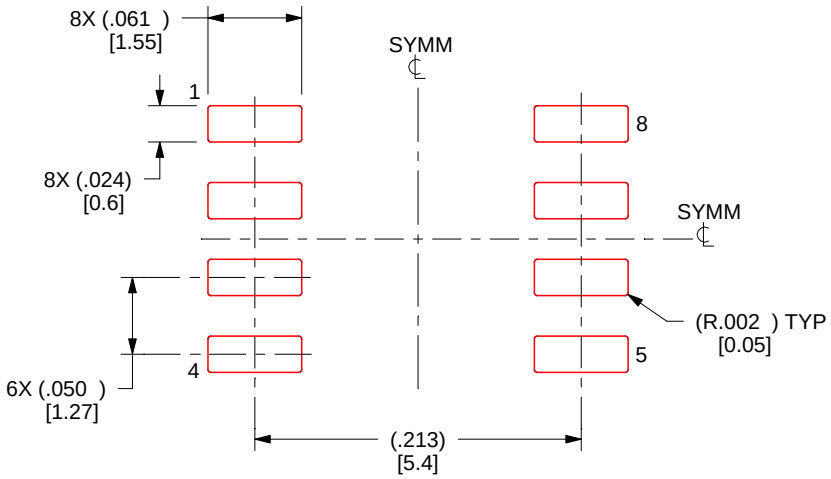
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月