ESD401 具有稳健 IEC ESD 性能的单通道 ESD 保护二极管

1 特性

- 稳健的 IEC 61000-4-2 4 级 ESD 保护：
  - ±24kV 接触放电
  - ±30kV 空气间隙放电
- IEC 61000-4-5 浪涌保护：
  - 4.5A (8/20μs)
  - 1.8A I_{PP} (8/20μs) 时，具有 12V 的低 V_{clamp}
- IEC 61000-4-4 EFT 保护：
  - 80A (5/50ns)
- 具有双向 ESD 二极管，可在高达 ± 5.5V 的电压下保护接口
- IO 电容：0.77pF（典型值）
- 直流击穿电压高：8.3V（典型值）
- 超低漏电流：30pA（典型值）
- 低动态电阻：0.7Ω（典型值）
- 工业级温度范围：-40°C 至 +125°C
- 业界通用 0402 封装

2 应用

- 终端设备：
  - 可穿戴设备
  - 便携式计算机和台式机
  - 手机和平板电脑
  - 机顶盒
  - DVR 和 NVR
  - 电视和监视器
  - EPOS（电子销售点）
- 接口：
  - 1Gbps 以太网
  - USB 2.0/1.1（5.5V 容差）
  - GPIO
  - 按钮/键盘
  - 音频

3 说明

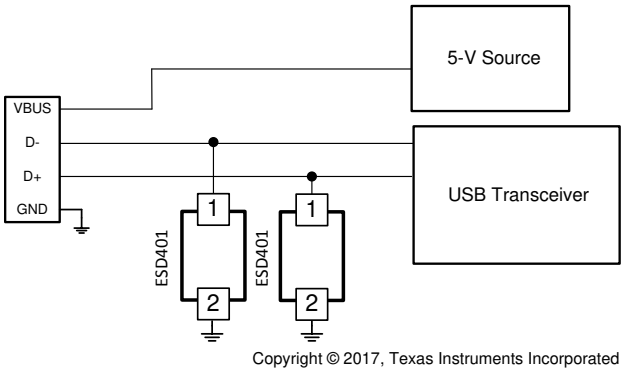
ESD401 是一款双向 TVS ESD 保护二极管，具有低 R_{DYN} 和低钳位电压。ESD401 的额定 ESD 冲击消散值超出了 IEC 61000-4-2 国际标准（4 级）规定的最高水平。低动态电阻 (0.7Ω) 可确保系统级抗瞬变事件保护。该器件具有一个 0.77pF IO 电容，非常适合用于保护 USB 2.0 等接口。该器件可在高达 ±5.5V 的电压运行，具有超低漏电流，并能承受高达 8.3V 的直流故障。

ESD401 采用业界通用的 0402 (DPY) 封装。

封装信息

器件型号	封装(1)	封装尺寸(2)
ESD401	DPY（X1SON，2）	1mm × 0.6mm

(1) 有关更多信息，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



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USB 2.0 典型应用原理图

本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Pin Configuration and Functions

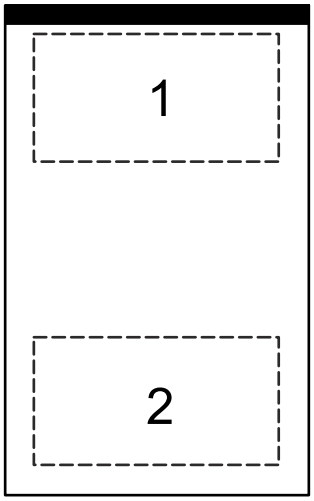


图 4-1. DPY Package, 2-Pin X1SON (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IO	1	I/O	ESD Protected Channel. If used as ESD IO, connect pin 2 to ground
IO	2	I/O	ESD Protected Channel. If used as ESD IO, connect pin 1 to ground

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-4 (5/50 ns) at 25°C		80	A
Peak pulse	IEC 61000-4-5 power (t_p - 8/20 µs) at 25°C		67	W
	IEC 61000-4-5 current (t_p - 8/20 µs) at 25°C		4.5	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings — JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±24000	V
		IEC 61000-4-2 air-gap discharge	±30000	

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	–5.5	5.5	V
T_A	Operating free-air temperature	–40	125	°C

5.5 Thermal Information

THERMAL METRIC(1)		ESD401 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	420	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	169.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	276.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	122.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	157.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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5.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 nA	–5.5		5.5	V
V_{BRF}	Breakdown voltage, Pin 1 to Pin 2 (1)	I_{IO} =1 mA, at T_A = 25°C	7.5		9.1	V
V_{BRR}	Breakdown voltage, Pin 2 to Pin 1 (1)	I_{IO} =1 mA, at T_A = 25°C	7.5		9.1	V
V_{HOLD}	Holding voltage (2)	I_{IO} =1 mA		8.3		V
V_{CLAMP}	Clamping voltage	I_{PP} = 1 A, TLP, from Pin 1 to Pin 2 and Pin 2 to Pin 1, T_A = 25°C		11		V
		I_{PP} = 5 A, TLP, from Pin 1 to Pin 2 and Pin 2 to Pin 1, T_A = 25°C		16		
		I_{PP} = 16 A, TLP, from Pin 1 to Pin 2 and Pin 2 to Pin 1, T_A = 25°C		24		
		I_{PP} = 1.8 A, IEC-61000-4-5 (t_p - 8/20 µs) from Pin 1 to Pin 2 and Pin 2 to Pin 1, T_A = 25°C		12		
		I_{PP} = 4.5 A, IEC-61000-4-5 (t_p - 8/20 µs) from Pin 1 to Pin 2 and Pin 2 to Pin 1, T_A = 25°C		15		
I_{LEAK}	Leakage current, Pin 1 to Pin2 and PIn2 to Pin 1	V_{IO} = ±2.5 V		0.03	10	nA
R_{DYN}	Dynamic resistance	Measured between TLP I_{PP} of 10 A and 20 A, Pin 2 to Pin 1 and Pin 1 to Pin2, T_A = 25°C		0.7		Ω
C_L	Line capacitance	V_{IO} = 0 V, f = 1 MHz, Pin 1 to Pin 2 and Pin2 to Pin1, T_A = 25°C		0.77	0.95	pF

(1) V_{BRF} and V_{BRR} are defined as the voltage obtained at 1 mA when sweeping the voltage up, before the device latches into the snapback state.
(2) V_{HOLD} is defined as the voltage when 1 mA is applied, after the device has successfully latched into the snapback state.

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5.7 Typical Characteristics

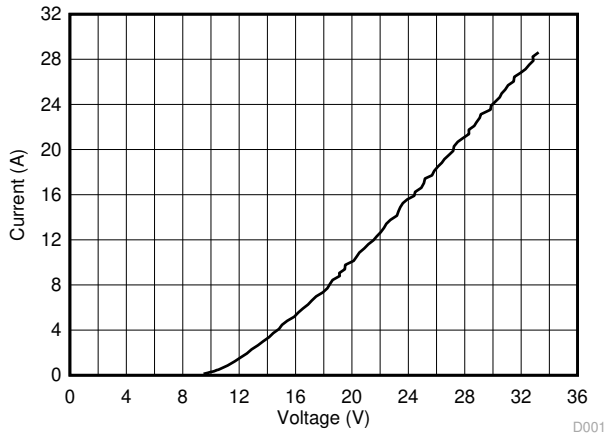


图 5-1. Positive TLP Curve, Pin 1 to Pin 2

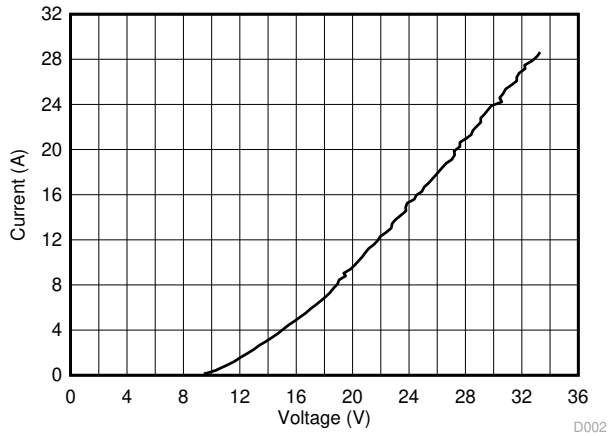


图 5-2. Negative TLP Curve, Pin 1 to Pin 2 (Plotted as Positive TLP Curve Pin 2 to Pin 1

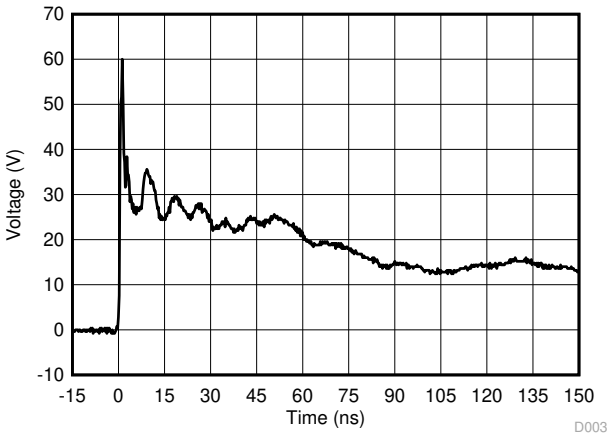


图 5-3. 8-kV IEC 61000-4-2 Waveform, Pin1 to Pin 2

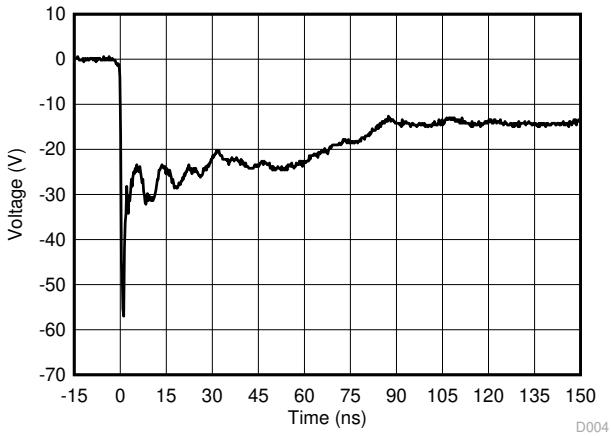


图 5-4. – 8-kV IEC 61000-4-2 Waveform, Pin 1 to Pin 2

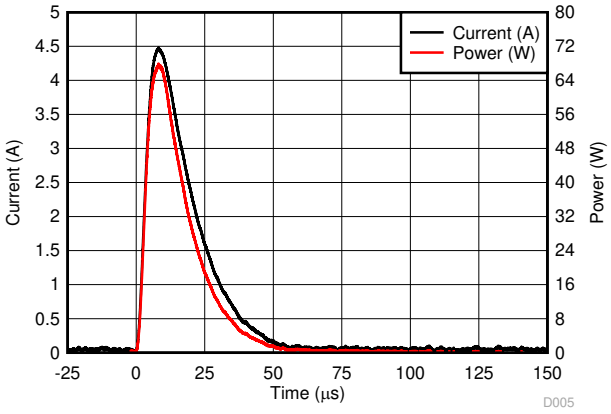


图 5-5. Surge (IEC 61000-4-5) Curve (tp = 8/20 µs), Pin 1 to Pin 2

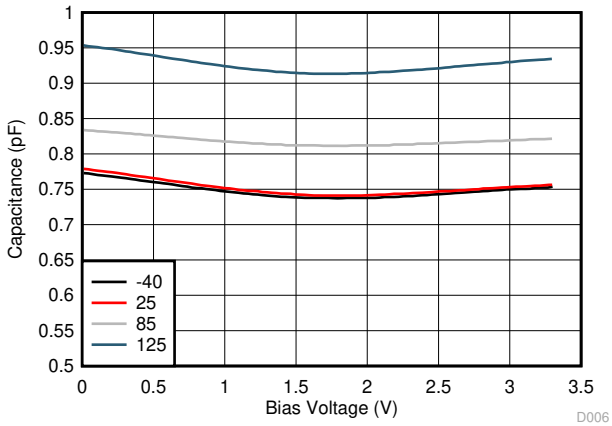


图 5-6. Capacitance vs Bias Voltage, Pin 1 to Pin 2

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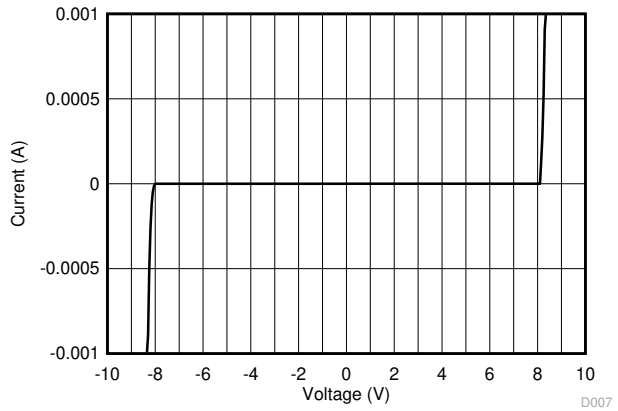


图 5-7. DC Voltage Sweep I-V Curve, Pin 1 to Pin 2

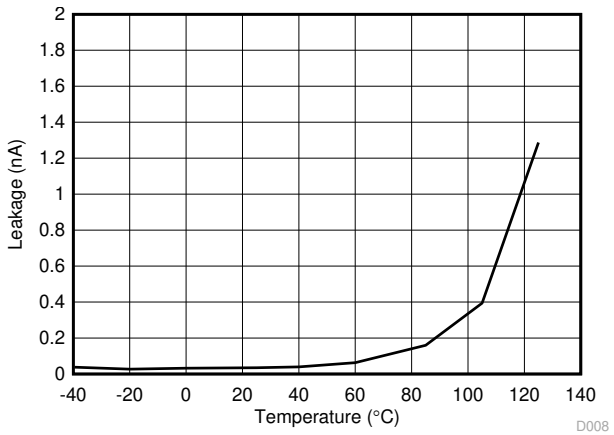


图 5-8. Leakage Current vs. Temperature, Pin 1 to Pin 2

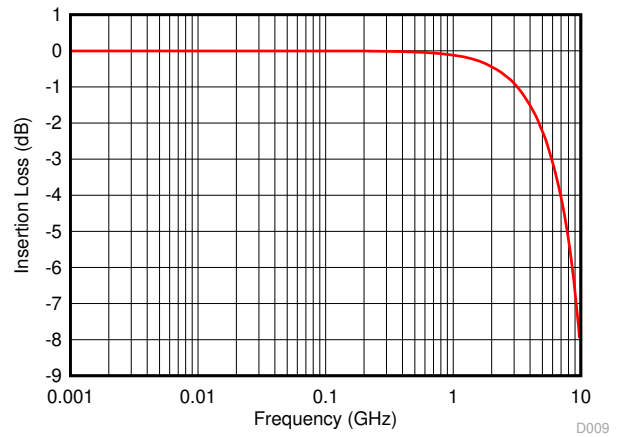


图 5-9. Insertion Loss

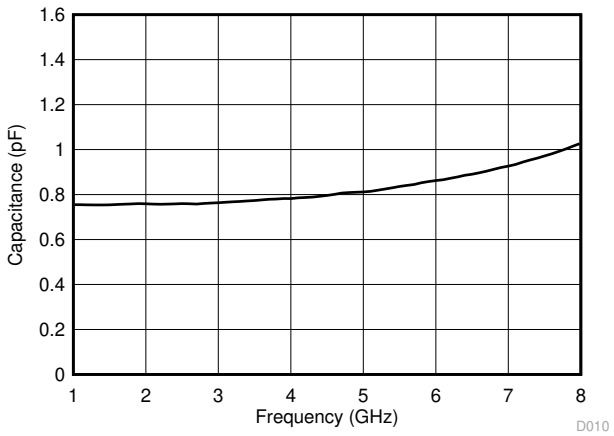


图 5-10. Capacitance vs. Frequency, Pin 1 to Pin 2

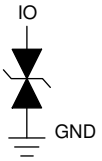
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6 Detailed Description

6.1 Overview

The ESD401 is a bidirectional ESD Protection Diode with ultra-low clamping voltage. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low clamping makes this device ideal for protecting any sensitive signal pins.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ±24-kV contact and ±30-kV air gap. An ESD-surge clamp diverts the current to ground.

6.3.2 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

6.3.3 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 4.5 A and 67W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

6.3.4 IO Capacitance

The capacitance between each I/O pin to ground is 0.77 pF (typical) and 0.95 pF (maximum).

6.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is ±8.3 V typical. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ±5.5 V.

6.3.6 Low Leakage Current

The I/O pins feature an low leakage current of 10 nA (maximum) with a bias of ±2.5 V.

6.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 24 V (TLP I_{PP} = 16 A).

6.3.8 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

6.3.9 Industry Standard Footprint

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

6.4 Device Functional Modes

The ESD401 is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{BRR}. During ESD events, voltages as high as ±24 kV (contact) or ±30 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of ESD401 (usually within 10s of nano-seconds) the device reverts to passive.

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图 6-1 shows typical TLP behavior of bi-directional ESD device that does not exhibit snapback.

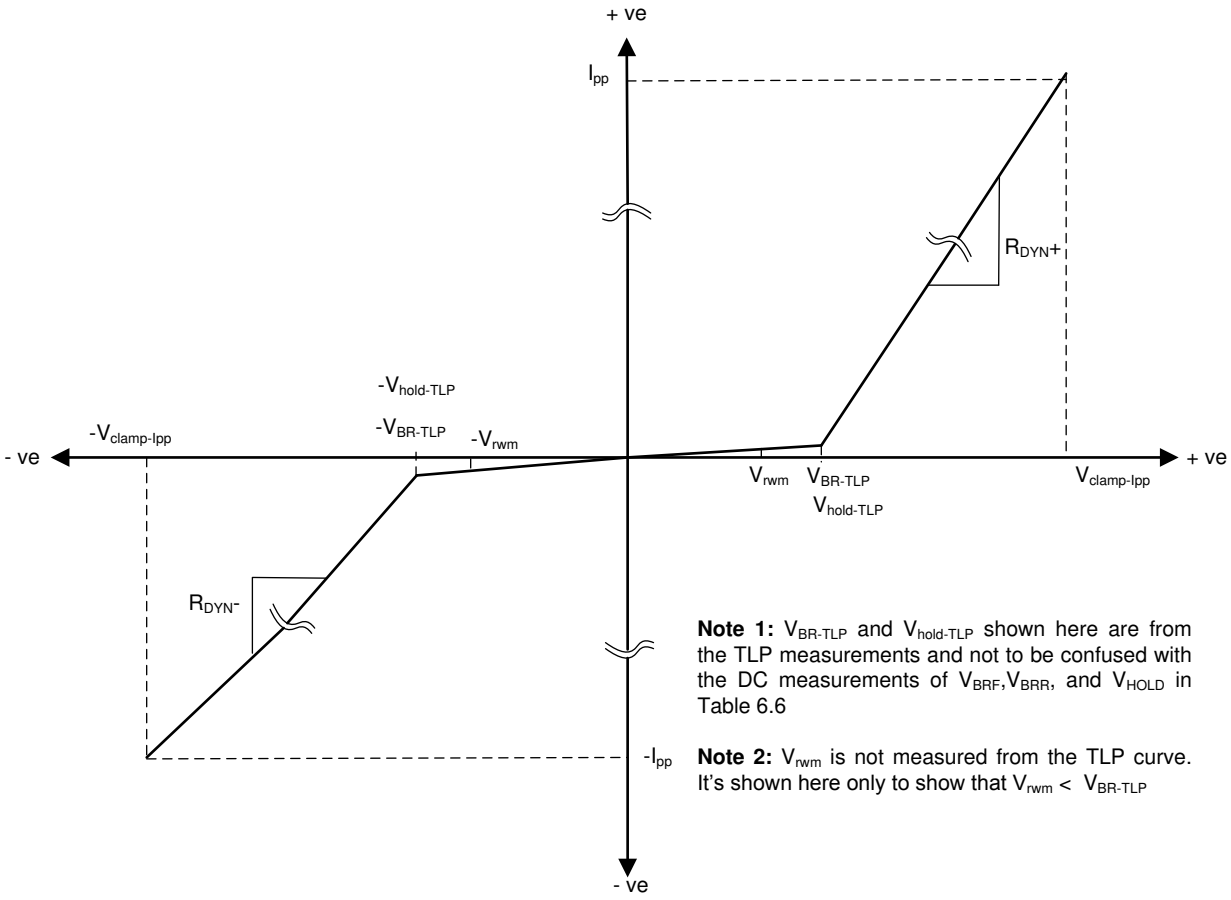


图 6-1. Typical TlpLP Behavior Of Bi-directional ESD Device that Does Not Exhibit Snapback

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7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户负责确定元件是否适合其用途，以及验证和测试其设计实现以确认系统功能。

7.1 Application Information

The ESD401 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

7.2 Typical Application

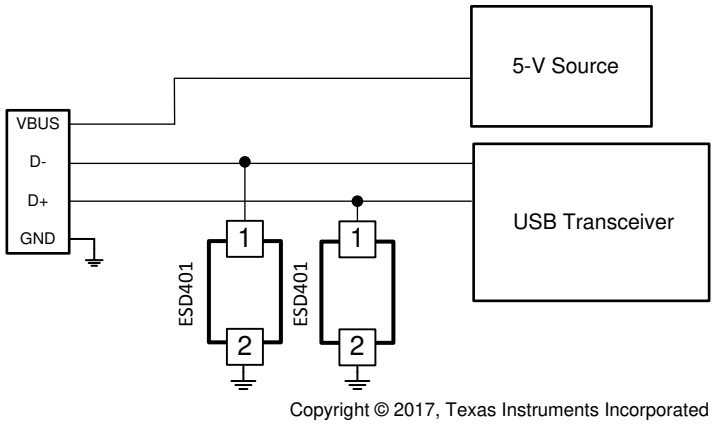


图 7-1. USB 2.0 ESD Schematic

7.2.1 Design Requirements

For this design example, two ESD401 devices are being used in a USB 2.0 application. This provides a complete ESD protection scheme.

Given the USB 2.0 application, the parameters listed in 表 7-1 are known.

表 7-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on DP-DM lines	0 V to 3.6 V
Operating frequency on DP-DM lines	up to 240 MHz or 480 Mbps

7.2.2 Detailed Design Procedure

7.2.2.1 Signal Range

The ESD401 supports signal ranges between –5.5 V and 5.5 V, which supports the USB 2.0 signal range of 0 to 3.6 V on the DM/DP lines..

7.2.2.2 Operating Frequency

The ESD401 has a 0.85 pF (typical) capacitance, which supports the USB 2.0 data rates of 480 Mbps.

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7.2.3 Application Curves

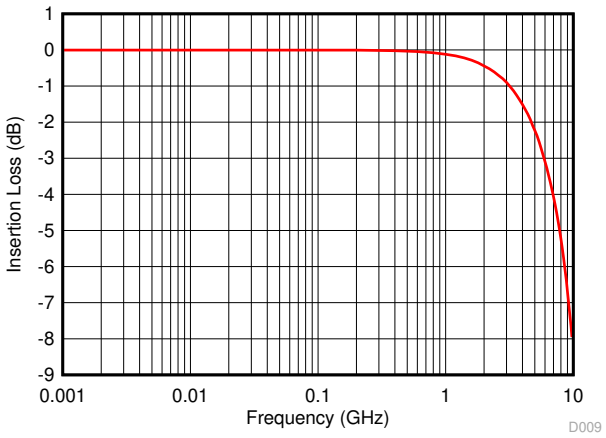


图 7-2. Insertion Loss

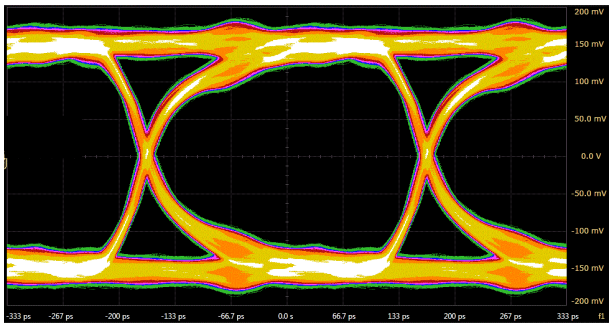


图 7-3. Eye Diagram - 3-Gbps Signal No Device

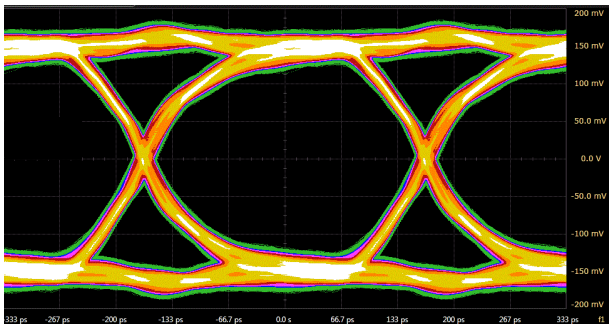


图 7-4. Eye Diagram - 3-Gbps Signal With ESD401

7.3 Power Supply Recommendations

The ESD401 is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (– 5.5 V to 5.5 V) to ensure the device functions properly.

7.4 Layout

7.4.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

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7.4.2 Layout Example

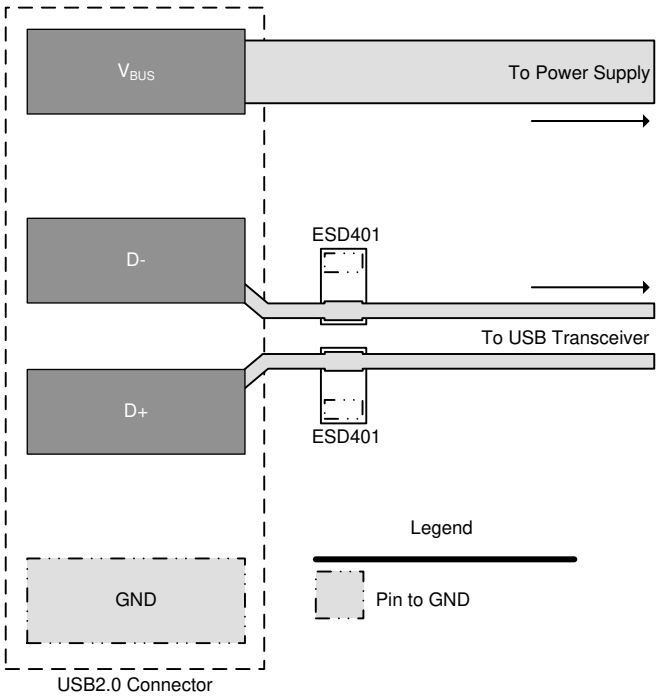


图 7-5. USB 2.0 ESD Layout

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8 Device and Documentation Support

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.3 Trademarks

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所有商标均为其各自所有者的财产。

8.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (July 2017) to Revision B (August 2024)	Page
• Updated Tape and Reel Information	14

Changes from Revision * (July 2017) to Revision A (July 2017)	Page
• Updated 图 5-9 and 图 7-2	6

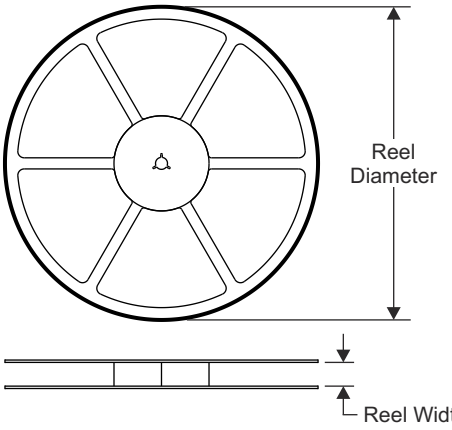
10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

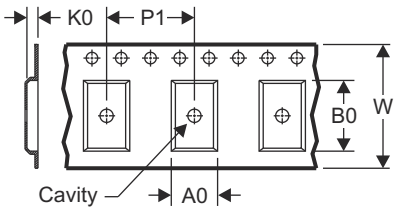
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10.1 Tape and Reel Information

REEL DIMENSIONS

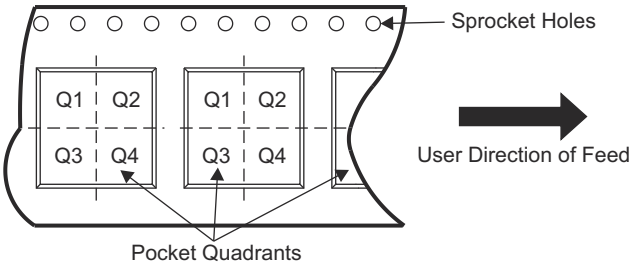


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

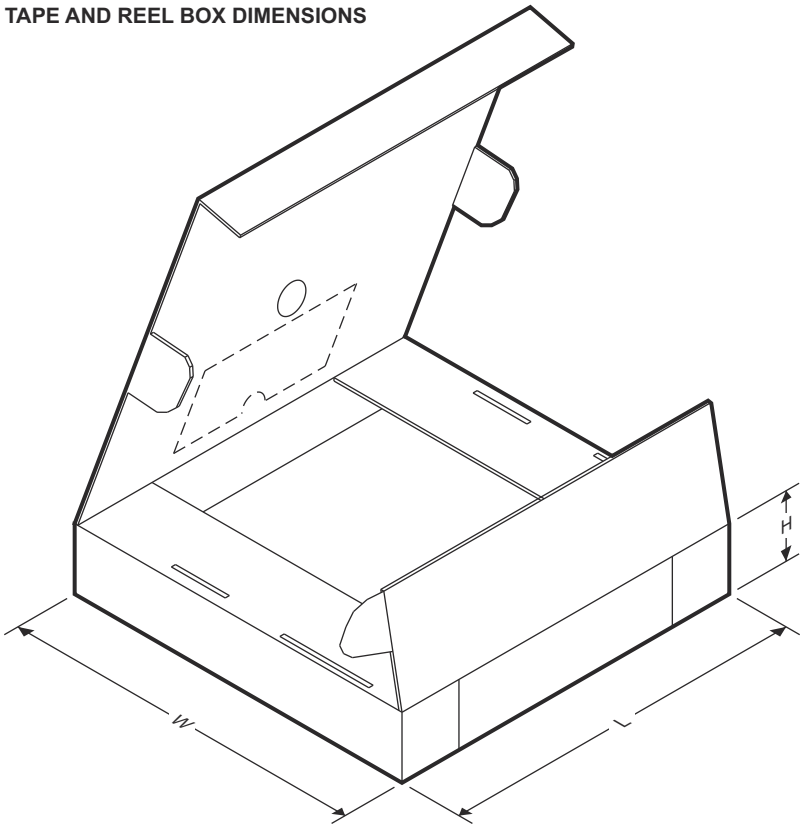
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD401DPYR	X1SON	DPY	2	10,000	180.00	8.400	0.67	1.15	0.46	2.0	8.000	Q2

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TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD401DPYR	X1SON	DPY	2	10,000	185.000	210.000	35.000

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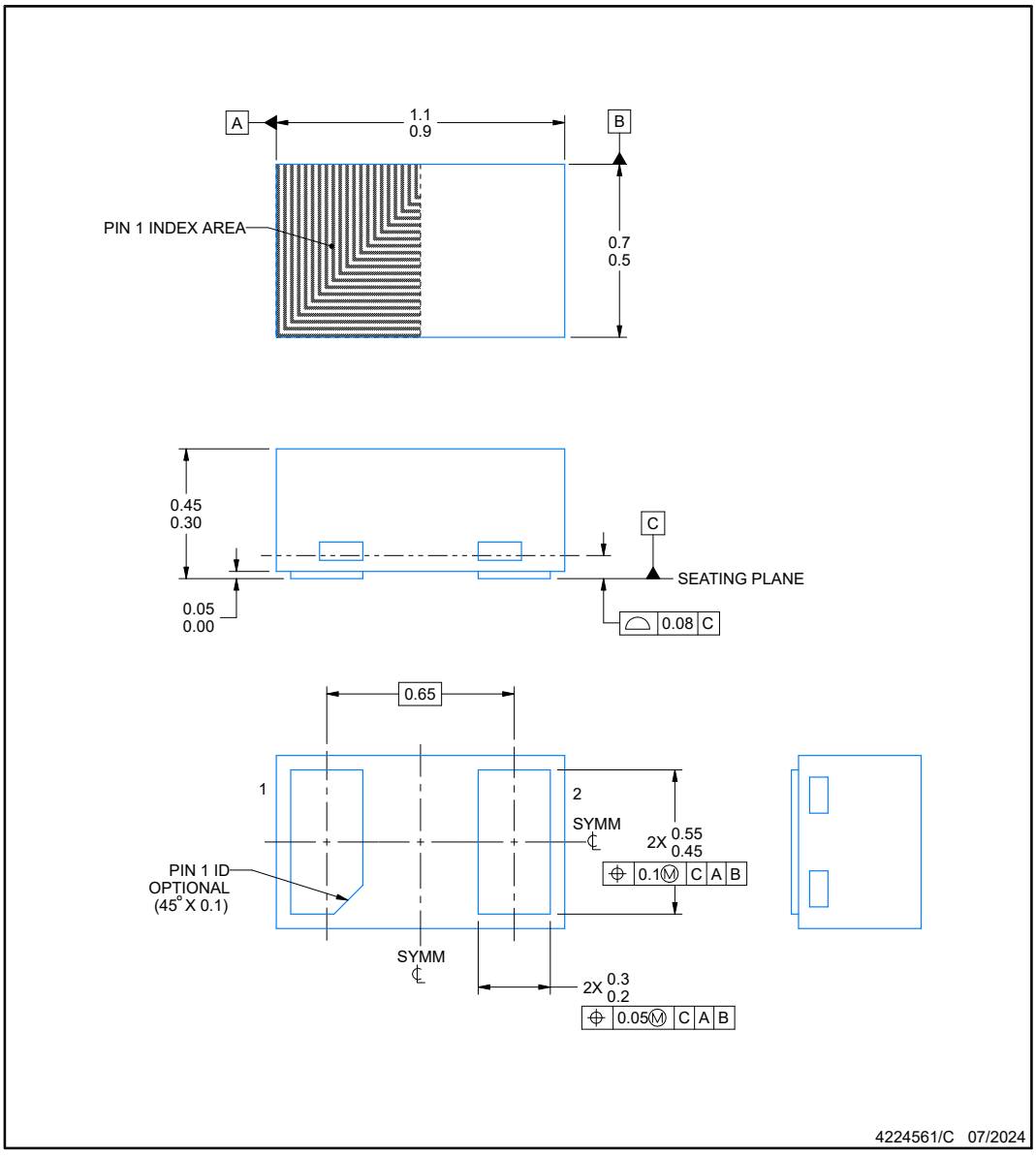
11 Mechanical Data



PACKAGE OUTLINE

DPY0002A — **X1SON - 0.45 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.

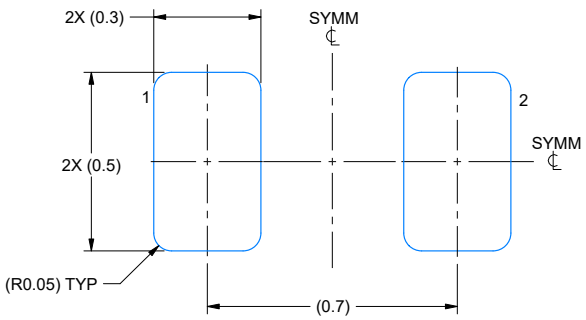
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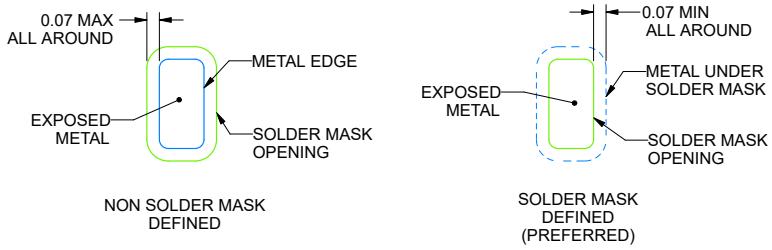
EXAMPLE BOARD LAYOUT

DPY0002A — **X1SON - 0.45 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS

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NOTES: (continued)

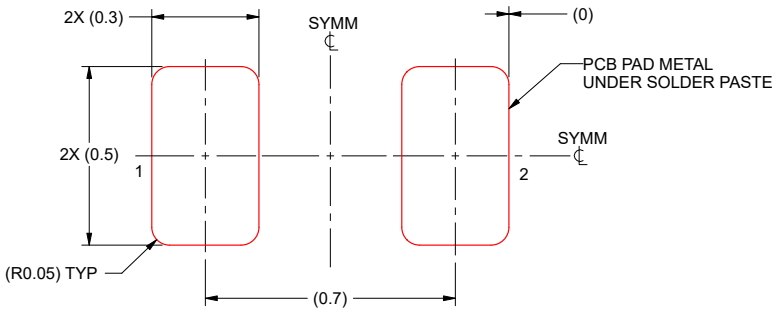
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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EXAMPLE STENCIL DESIGN

DPY0002A — **X1SON - 0.45 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD401DPYR	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	8I
ESD401DPYR.B	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	8I
ESD401DPYRG4	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8I
ESD401DPYRG4.B	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

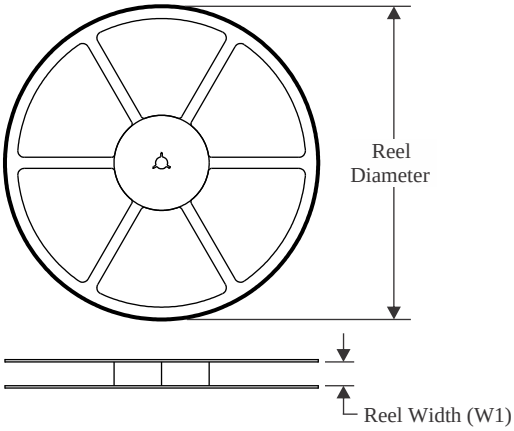
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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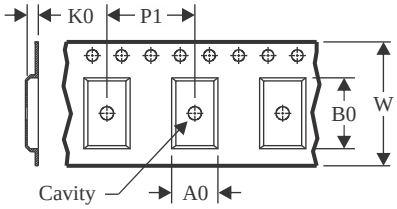
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

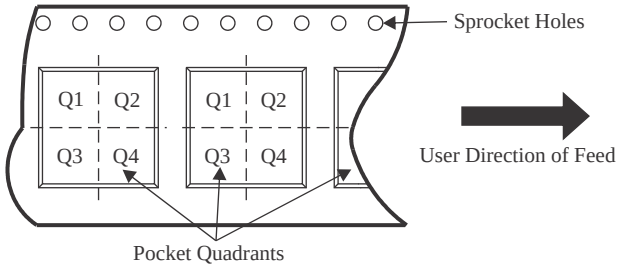


TAPE DIMENSIONS



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B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

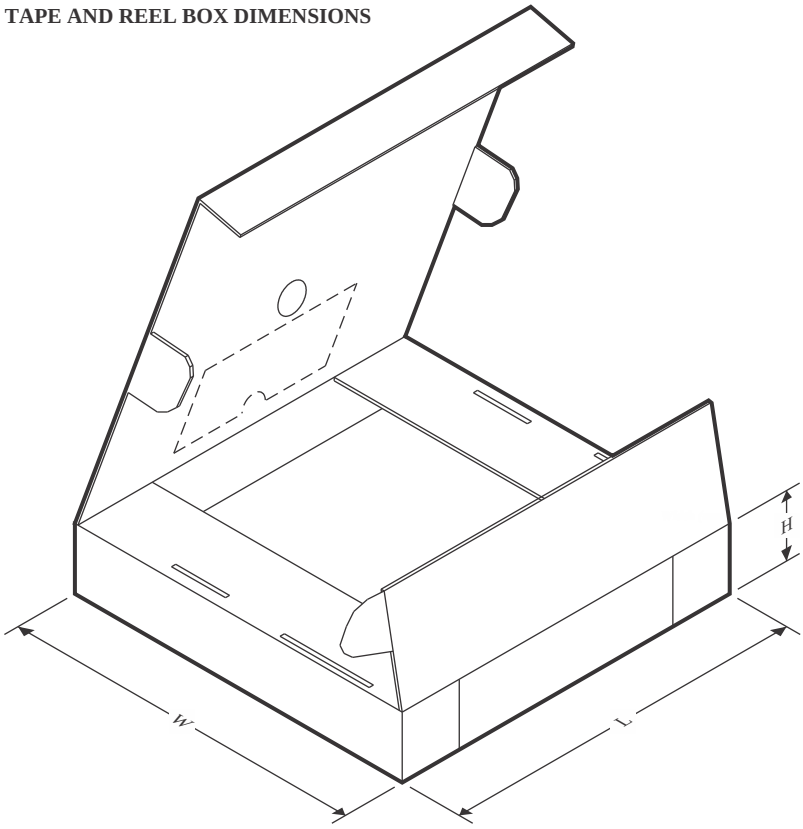
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD401DPYR	X1SON	DPY	2	10000	178.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2
ESD401DPYR	X1SON	DPY	2	10000	180.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2
ESD401DPYRG4	X1SON	DPY	2	10000	180.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD401DPYR	X1SON	DPY	2	10000	208.0	191.0	35.0
ESD401DPYR	X1SON	DPY	2	10000	210.0	185.0	35.0
ESD401DPYRG4	X1SON	DPY	2	10000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DPY 2

X1SON - 0.45 mm max height

1 x 0.6 mm

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



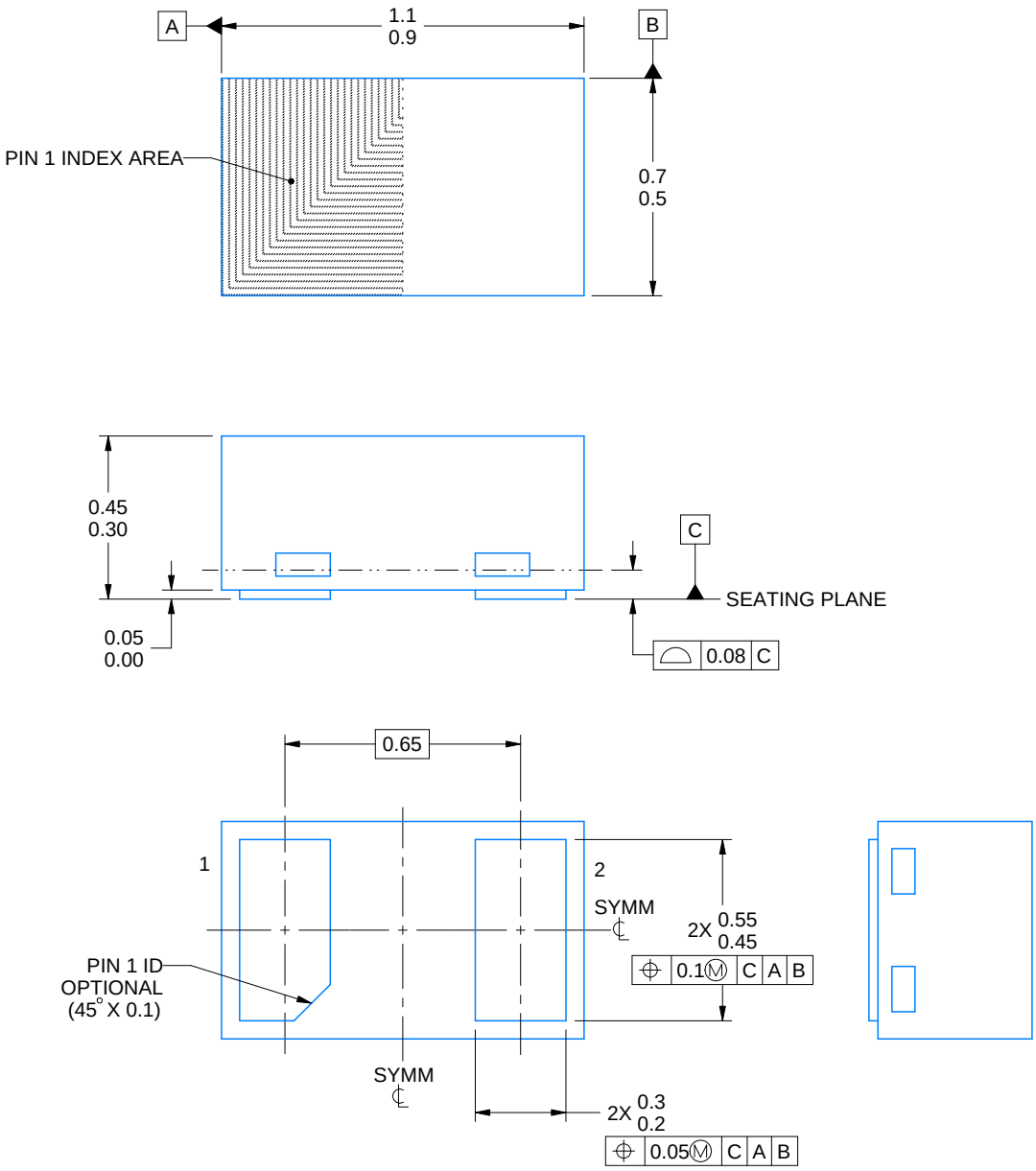
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PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

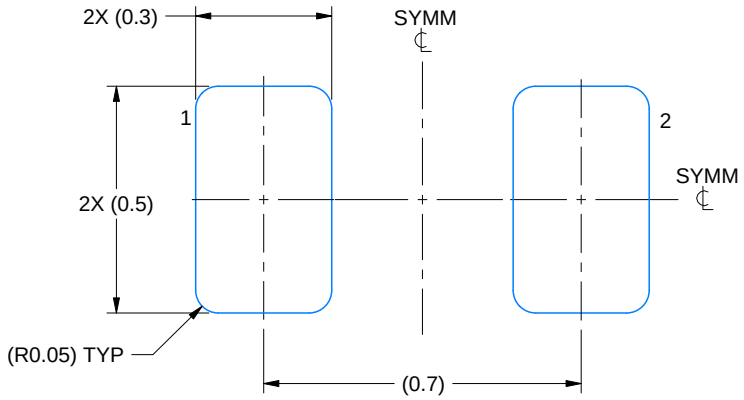
PLASTIC SMALL OUTLINE - NO LEAD



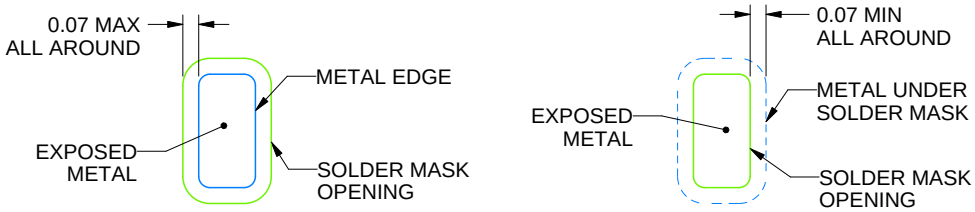
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

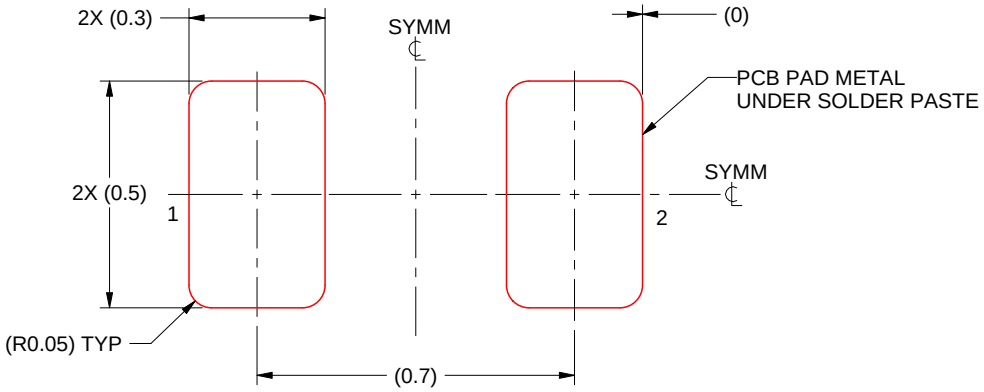


SOLDER MASK DETAILS

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NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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