双通道数字隔离器

查询样品: ISO7221C-HT

特性

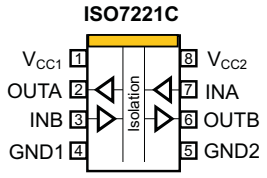
- **1-, 5-** 和 **25-Mbps** 信号传输速度选项
  - 低通道到通道输出偏移; **1 ns** 最大
  - 低脉宽失真 **(PWD); 1 ns** 最大
  - 低抖动（在速率为 **150Mbps** 时为 **1ns**）（典型值）
- **4000-$V_{峰值}$**隔离, **560 $V_{峰值}$ V_{IORM}**
  - **UL 1577** 经过检验
  - **50-kV/μs** 典型瞬变抗扰性
- **3.3-V** 或 **5-V** 电源供电下运行
- **4-kV ESD** 保护
- 高电磁抗扰度

应用

- 潜孔钻进
- 高温环境

支持极端温度应用

- 受控基线
- **One Assembly and Test Site**
- 一个制造场所
- 可在极端温度范围 **(–55°C/175°C)** 下工作 (1) (2)
- 产品生命周期有所延长
- 拓展的产品变更通知
- 产品可追溯性
- 德州仪器的高温产品运用了高度优化的硅片（芯片）解决方案，此类解决方案在设计与工艺方面均有所强化，以在扩展的温度范围内实现性能的最大化。



(1) 可定制温度范围。
(2) 在最大额定温度，设备能可靠运行1000小时。 这包括, 但并不限于温度烘烤, 温度循环, 电迁移, 内部粘合金属寿命, 和模具混合寿命。 不应该观看这样资格测试作为辩解对在指定的表现和环境极限之外的这个组分的用途。

说明

ISO7221是一个双通道数字隔离器。 为了使PCB布局更加便利, 通道都是面向相反的方向、 这个设备有一个由TI的二氧化硅(SiO_2)隔离栏栅分开的逻辑输入和输出缓冲器, 提供高达4000V的电流隔离. 与隔离电源联合使用, 这个设备能阻止高电压, 隔离接地, 并且在数据总线上防止噪声电流或者其它电路进入本地接地和干扰或者损坏敏感电路。

一个二进制输入信号经调节, 翻译成平衡信号,然后由电容隔离栏栅进行区分。 通过隔离栏栅后, 一个差动比较器接收到逻辑信息, 然后相应地设定或重置一个触发器和输出电路。 周期性更新脉冲也会通过栏栅发送，以确保设置正确的 DC 级别。 如果在每4μs内没有接收到这个DC刷新脉冲,则这个输入就被假定为没被供电或者没有被正常驱动, 并且这个故障自动保险电路将输出驱动至一个逻辑高能状态。

这个小电容和结果时间持续提供信号速率在
0 Mbps (dc) 到150 Mbps间的快速运行. (3) A-, B- and C-选项设备有TTL输入阀值和一个输入端噪音过滤器，这能够防止瞬时脉冲通过设备的输出端。 M选项设备具有CMOS V_{CC}/2个输入阀值并且没有输入噪音过滤和额外的传播延迟。

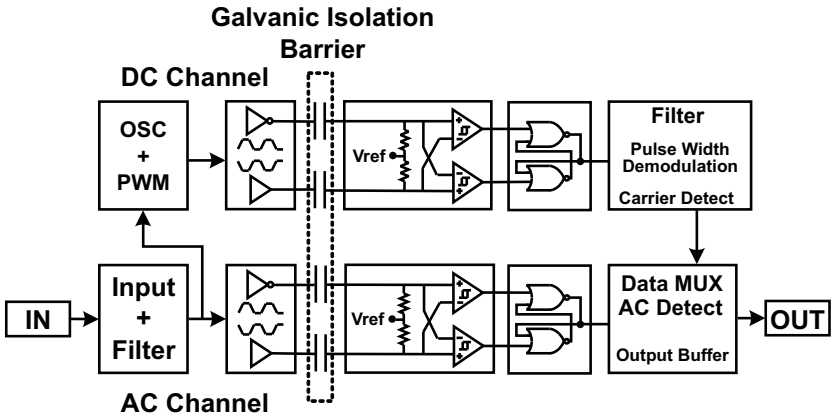
这个设备要求3.3 V, 5 V两个供电电压,或者任一组合。 当采用一个 3.3V 电源来供电并且所有的输出都是4-mA CMOS时，所有的输入均可容许 5V 电压。

ISO7221针对环境温度在–55°C 到 175°C间的操作。

(3) 一条线路的信号传输速率就是电压瞬变的次数，即每秒钟单位 bps（每秒比特数）。

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SINGLE-CHANNEL FUNCTION DIAGRAM



AVAILABLE OPTIONS(1)

PRODUCT	MAX SIGNALING RATE	PACKAGE(2)	INPUT THRESHOLD	MARKED AS	ORDERING NUMBER
ISO7221C	25 Mbps	SOIC-8	≠ 1.5 V (TTL) (CMOS compatible)	I7221H	ISO7221CHD

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

REGULATORY INFORMATION

UL
Recognized under 1577 Component Recognition Program(1)
File Number: E181974

(1) Production tested ≥3000 VRMS for 1 second in accordance with UL 1577.

ABSOLUTE MAXIMUM RATINGS(1)

					VALUE	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}				–0.5 to 6	V
V_I	Voltage at IN, OUT				–0.5 to 6	V
I_O	Output current				±15	mA
ESD	Electrostatic discharge	Human Body Model	Electrostatic discharge JEDEC Standard 22, Test Method A114-C.01	All pins	±4	kV
		Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101		±1	
		Machine Model	ANSI/ESDS5.2-1996		±200	V
T_J	Maximum junction temperature				180	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage(1), V_{CC1}, V_{CC2}	3		5.5	V
I_{OH}	High-level output current			4	mA
I_{OL}	Low-level output current	–4			mA
t_{ui}	Input pulse width(2)	40	33		ns
$1/t_{ui}$	Signaling rate(2)	0	30	25	Mbps
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	0		0.8	V
T_A	Operating temperature	–55		175	°C

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.
(2) Typical signaling rate and Input pulse width are measured at ideal conditions at 25°C.

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{CC1}	25 Mbps	V_I = V_{CC} or 0 V, no load		12	22	mA
I_{CC2}	25 Mbps	V_I = V_{CC} or 0 V, no load		12	22	
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.8	4.6		V
		I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 1		0.2	0.4	V
		I_{OL} = 20 µA, See Figure 1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	IN from 0 V to V_{CC}			11	µA
I_{IL}	Low-level input current	IN from 0 V to V_{CC}	–11			µA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 3	25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay	See Figure 1	21	32	43	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$(1)	See Figure 1		1	2	ns
$t_{sk(pp)}$	Part-to-part skew (2)				10	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)			0.2	5	ns
t_r	Output signal rise time	See Figure 1		1		ns
t_f	Output signal fall time	See Figure 1		1		ns
t_{fs}	Failsafe output delay time from input power loss	See Figure 2		3		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 5 V, V_{CC2} at 3.3 V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	25 Mbps		V_I = V_{CC} or 0 V, no load		12	22	mA
I_{CC2}	25 Mbps		V_I = V_{CC} or 0 V, no load		6	12	mA
V_{OH}	High-level output voltage	(5-V side)	I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.8			V
			I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.4	V
			I_{OL} = 20 µA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}			11	µA
I_{IL}	Low-level input current		IN from 0 V to V_{CC}	–11			µA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 3	15	40		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 5 V, V_{CC2} at 3.3 V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay		24	36	49	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$ (1)			1	2	ns
$t_{sk(pp)}$	Part-to-part skew (2)				10	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)			0.2	10	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time	See Figure 1		2		ns
t_{fs}	Failsafe output delay time from input power loss	See Figure 2		3		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 3.3 V, V_{CC2} at 5 V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	25 Mbps		V_I = V_{CC} or 0 V, no load		6	12	mA
I_{CC2}	25 Mbps		V_I = V_{CC} or 0 V, no load		12	22	mA
V_{OH}	High-level output voltage	(3.3-V side)	I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.4			V
			I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		IOL = 4 mA, See Figure 1			0.4	
			IOL = 20 µA, See Figure 1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V or V_{CC}			11	µA
I_{IL}	Low-level input current		IN from 0 V or V_{CC}	–11			µA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 3	15	40		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 3.3 V, V_{CC2} at 5 V OPERTAION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay		24	36	49	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$ (1)			1	3	ns
$t_{sk(pp)}$	Part-to-part skew (2)				10	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)			0.2	10	ns
t_r	Output signal rise time	See Figure 1		1		
t_f	Output signal fall time			1		
t_{fs}	Failsafe output delay time from input power loss	See Figure 2		3		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{CC1}	25 Mbps	$V_I = V_{CC}$ or 0 V, no load		6	12	mA
I_{CC2}	25 Mbps	$V_I = V_{CC}$ or 0 V, no load		6	12	mA
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.4	3		V
		I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 1		0.2	0.4	V
		I_{OL} = 20 µA, See Figure 1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}			11	µA
I_{IL}	Low-level input current	IN from 0 V or V_{CC}	–11			
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See Figure 3	15	40		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

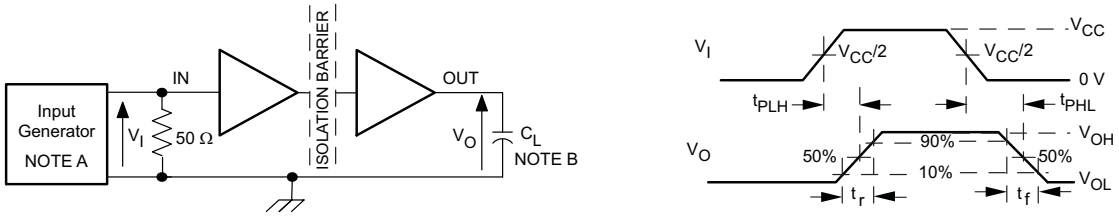
SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 V

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay		25	40	53	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$ (1)			1	3	ns
$t_{sk(pp)}$	Part-to-part skew (2)				10	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)			0.2	5	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time	See Figure 1		2		ns
t_{fs}	Failsafe output delay time from input power loss	See Figure 2		3		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

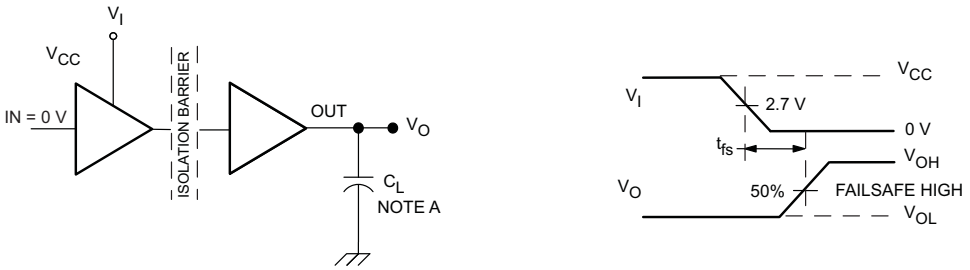
PARAMETER MEASUREMENT INFORMATION



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

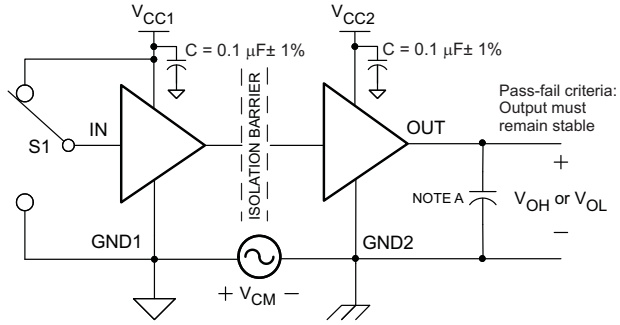
B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



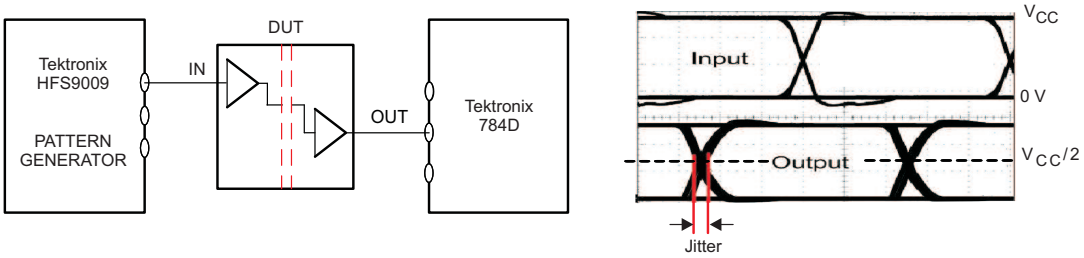
A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 2. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 3. Common-Mode Transient Immunity Test Circuit

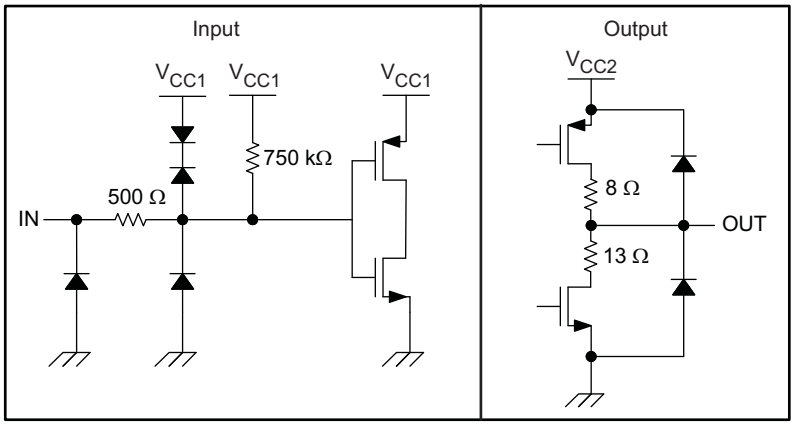


NOTE: PRBS bit pattern run length is 2^{16} – 1. Transition time is 800 ps.

Figure 4. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

DEVICE INFORMATION

DEVICE I/O SCHEMATICS



SOIC-8 PACKAGE THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air	Low-K Thermal Resistance(1)		212		°C/W
		High-K Thermal Resistance		122		
θ_{JB}	Junction-to-Board Thermal Resistance			37		
θ_{JC}	Junction-to-Case Thermal Resistance			69.1		

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

DEVICE FUNCTION TABLE

Table 1. Function Table(1)

INPUT SIDE V_{CC}	OUTPUT SIDE V_{CC}	INPUT IN	OUTPUT OUT
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H

(1) PU = Powered Up(Vcc ≥ 3.0V); PD = Powered Down (Vcc ≤ 2.5V); X = Irrelevant; H = High Level; L = Low Level

TYPICAL CHARACTERISTIC CURVES

3.3-V RMS SUPPLY CURRENT vs SIGNALING RATE (Mbps)

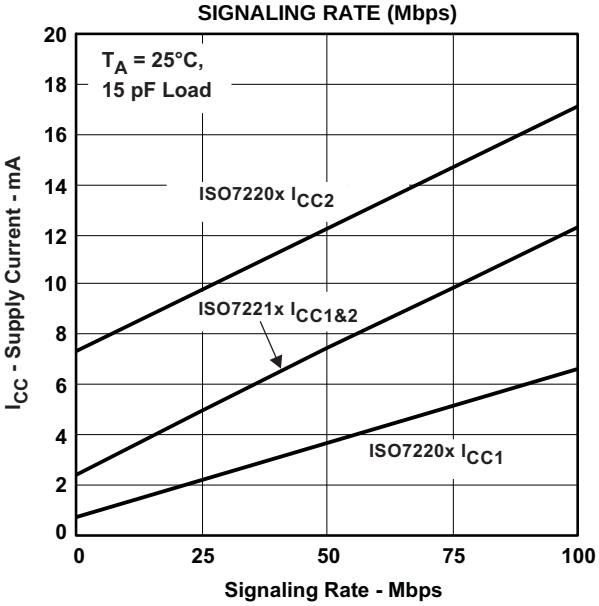


Figure 5.

5-V RMS SUPPLY CURRENT vs SIGNALING RATE (Mbps)

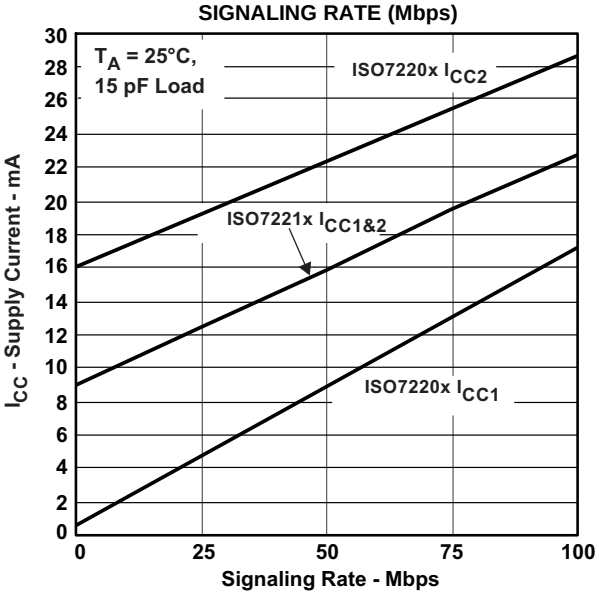


Figure 6.

PROPAGATION DELAY vs FREE-AIR TEMPERATURE

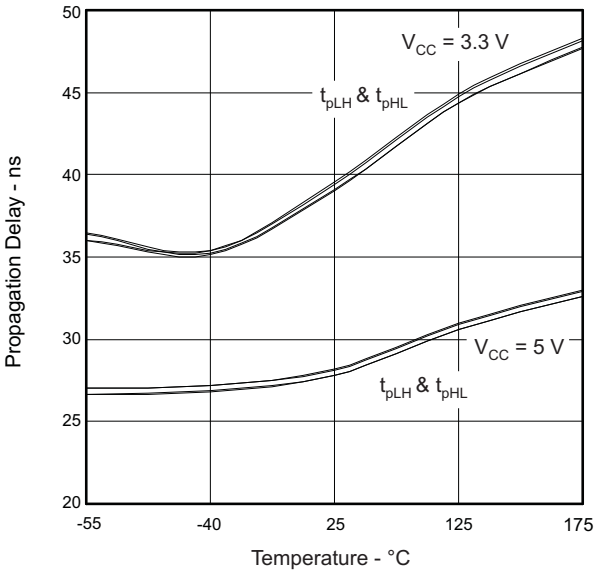


Figure 7.

INPUT VOLTAGE LOW-TO-HIGH SWITCHING THRESHOLD vs FREE-AIR TEMPERATURE

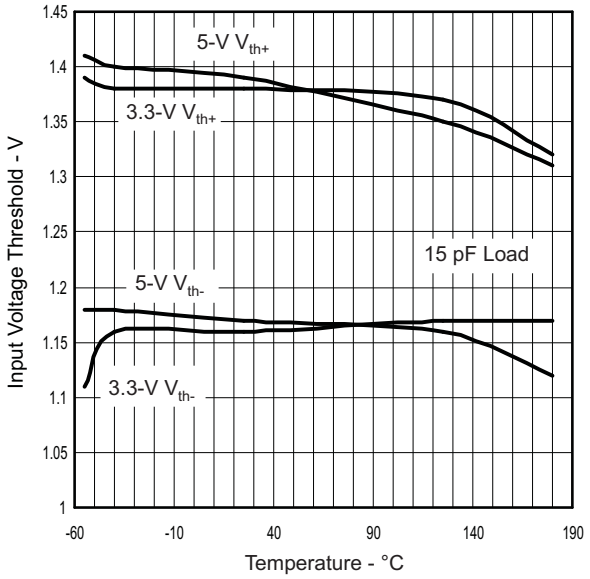


Figure 8.

TYPICAL CHARACTERISTIC CURVES (continued)

V_{CC} FAILSAFE THRESHOLD vs FREE-AIR TEMPERATURE

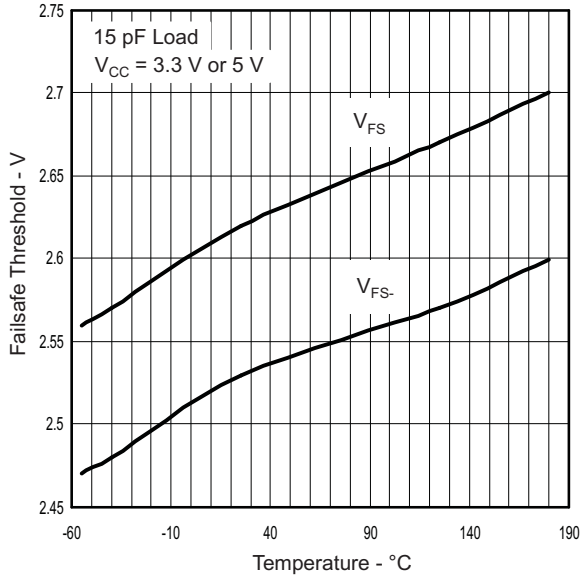


Figure 9.

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

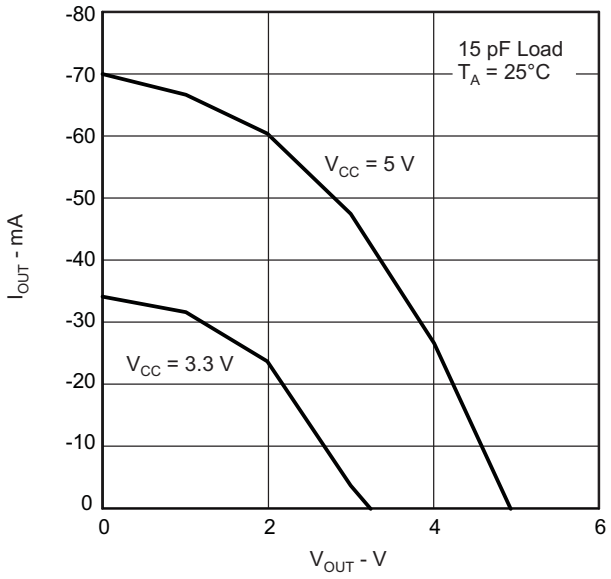


Figure 10.

LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

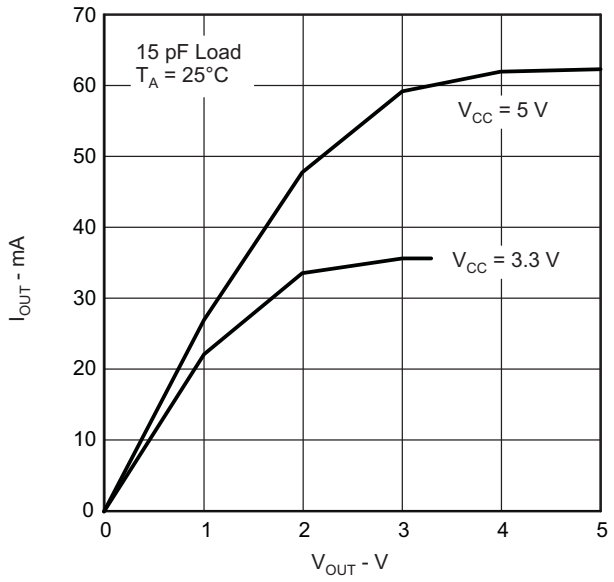


Figure 11.

APPLICATION INFORMATION

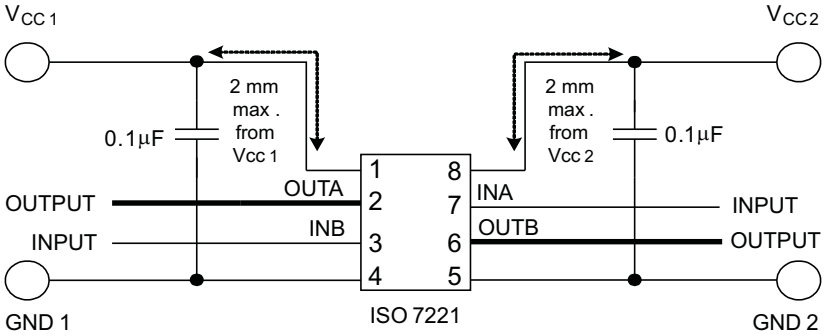
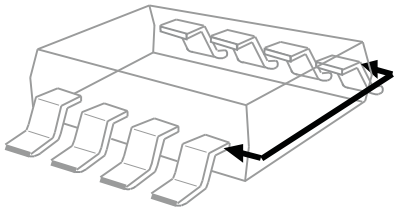


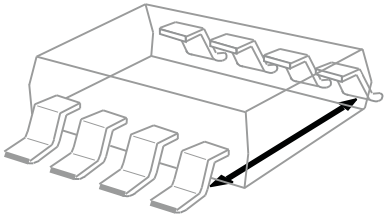
Figure 12. Typical ISO7221 Application Circuit

ISOLATION GLOSSARY

Creepage Distance — The shortest path between two conductive input to output leads measured along the surface of the insulation. The shortest distance path is found around the end of the package body.



Clearance — The shortest distance between two conductive input to output leads measured through air (line of sight).



Input-to Output Barrier Capacitance — The total capacitance between all input terminals connected together, and all output terminals connected together.

Input-to Output Barrier Resistance — The total resistance between all input terminals connected together, and all output terminals connected together.

Primary Circuit — An internal circuit directly connected to an external supply mains or other equivalent source which supplies the primary circuit electric power.

Secondary Circuit — A circuit with no direct connection to primary power, and derives its power from a separate isolated source.

Comparative Tracking Index (CTI) — CTI is an index used for electrical insulating materials which is defined as the numerical value of the voltage which causes failure by tracking during standard testing. Tracking is the process that produces a partially conducting path of localized deterioration on or through the surface of an insulating material as a result of the action of electric discharges on or close to an insulation surface -- the higher CTI value of the insulating material, the smaller the minimum creepage distance.

Generally, insulation breakdown occurs either through the material, over its surface, or both. Surface failure may arise from flashover or from the progressive degradation of the insulation surface by small localized sparks. Such sparks are the result of the breaking of a surface film of conducting contaminant on the insulation. The resulting break in the leakage current produces an overvoltage at the site of the discontinuity, and an electric spark is generated. These sparks often cause carbonization on insulation material and lead to a carbon track between points of different potential. This process is known as *tracking*.

Insulation:

Operational insulation — Insulation needed for the correct operation of the equipment.

Basic insulation — Insulation to provide basic protection against electric shock.

Supplementary insulation — Independent insulation applied in addition to basic insulation in order to ensure protection against electric shock in the event of a failure of the basic insulation.

Double insulation — Insulation comprising both basic and supplementary insulation.

Reinforced insulation — A single insulation system which provides a degree of protection against electric shock equivalent to double insulation.

Pollution Degree:

Pollution Degree 1 — No pollution, or only dry, nonconductive pollution occurs. The pollution has no influence.

Pollution Degree 2 — Normally, only nonconductive pollution occurs. However, a temporary conductivity caused by condensation must be expected.

Pollution Degree 3 — Conductive pollution occurs or dry nonconductive pollution occurs which becomes conductive due to condensation which is to be expected.

Pollution Degree 4 – Continuous conductivity occurs due to conductive dust, rain, or other wet conditions.

Installation Category:

Overvoltage Category — This section is directed at insulation co-ordination by identifying the transient overvoltages which may occur, and by assigning 4 different levels as indicated in IEC 60664.

I: Signal Level — Special equipment or parts of equipment.

II: Local Level — Portable equipment etc.

III: Distribution Level — Fixed installation

IV: Primary Supply Level — Overhead lines, cable systems

Each category should be subject to smaller transients than the category above.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7221CHD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 175	I7221H
ISO7221CHD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 175	I7221H

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF ISO7221C-HT :

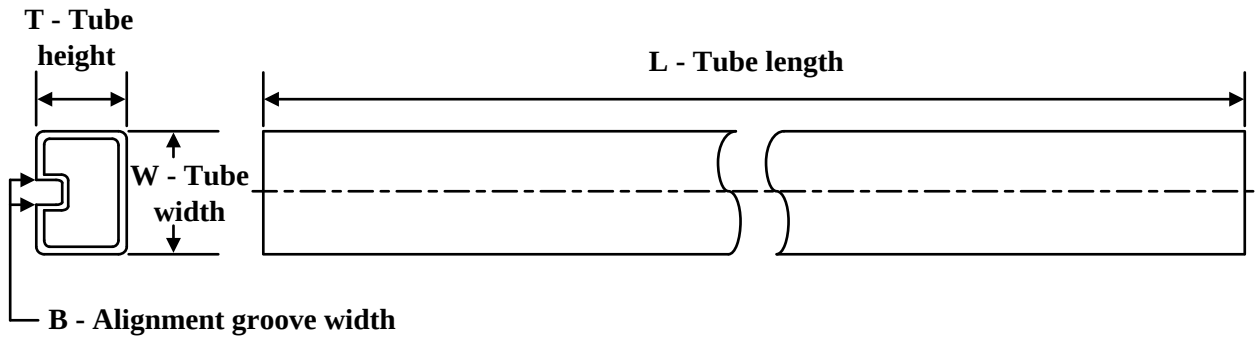
- Catalog : ISO7221C

- Automotive : ISO7221C-Q1

NOTE: Qualified Version Definitions:

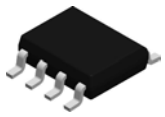
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7221CHD	D	SOIC	8	75	505.46	6.76	3810	4
ISO7221CHD.A	D	SOIC	8	75	505.46	6.76	3810	4

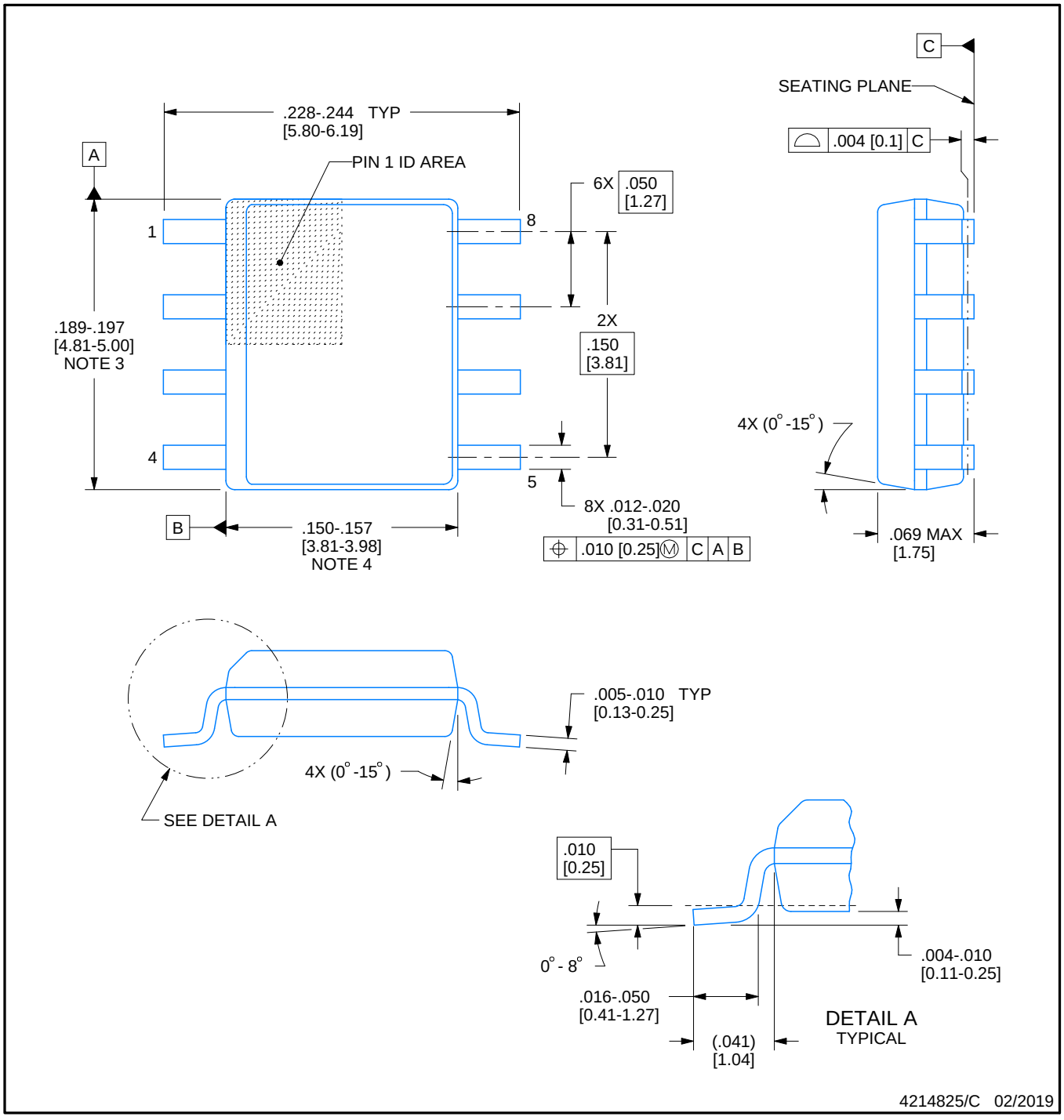


PACKAGE OUTLINE

D0008A

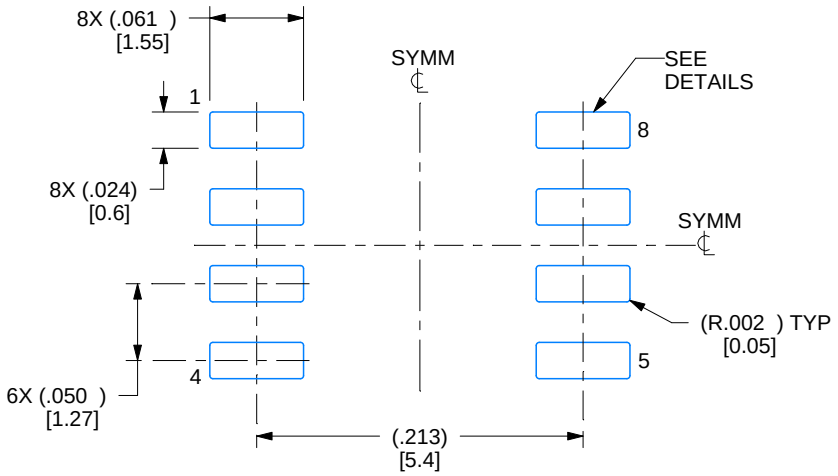
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

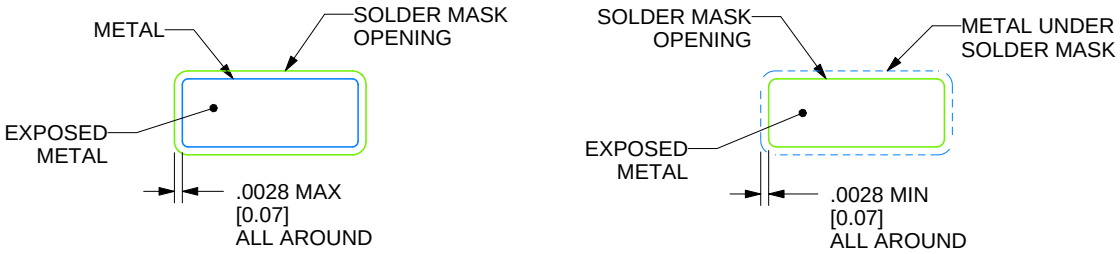


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

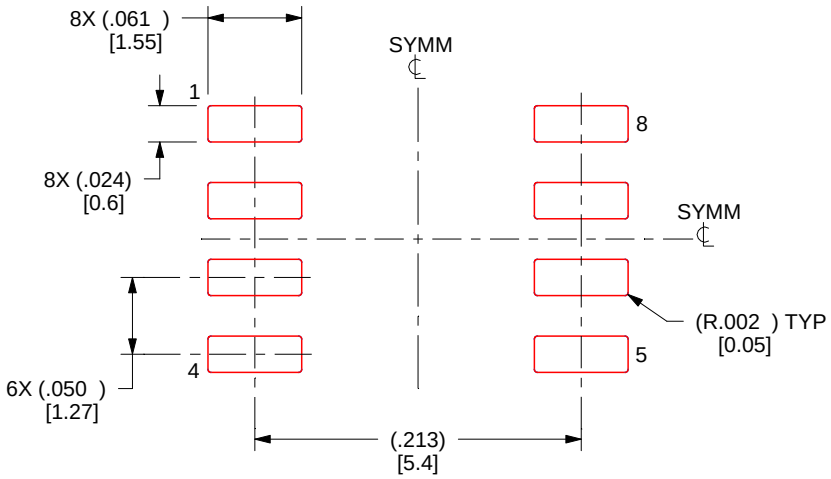
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月