# JFE150 超低噪音、低栅极电流、音频、N 通道 JFET

Texas Instruments
Burr-Brown Audio

## 1 特性

- 超低噪声：
  - 电压噪声：
    - 1kHz 时为 0.8nV/√Hz，$I_{DS}$ = 5mA
    - 1kHz 时为 0.9nV/√Hz，$I_{DS}$ = 2mA
  - 电流噪声：1 kHz 时为 1.8fA/√Hz
- 低栅极电流：10 pA（最大值）
- 低输入电容：$V_{DS}$ = 5V 时为 24pF
- 高栅漏电压和栅源击穿电压：-40 V
- 高跨导：68mS
- 封装：小型 SC70 和 SOT-23

## 2 应用

- 麦克风输入
- 水听器和船用设备
- DJ 控制器、混频器和其他 DJ 设备
- 专业音频混合器或控制平面
- 吉他放大器和其他乐器放大器
- 状态监控传感器

## 3 说明

JFE150 是使用德州仪器 (TI) 的现代高性能模拟双极工艺构建的 Burr-Brown™ 分立式 JFET。JFE150 具有以前较旧的分立式 JFET 技术所不具备的性能。JFE150 提供出色的噪声功率效率和灵活性，静态电流可由用户设置，并为 50 µA 至 20mA 的电流提供出色的噪声性能。当偏置电流为 5mA 时，该器件会产生 0.8nV/√Hz 的输入参考噪声，从而以极高的输入阻抗 (> 1TΩ) 提供超低噪声性能。JFE150 还具有连接到独立钳位节点的集成二极管，无需添加高泄漏、非线性外部二极管即可提供保护。

JFE150 可承受 40V 的高漏源电压，以及低至 –40V 的栅源电压和栅漏电压。该器件额定工作温度范围为 –40°C 至 + 125°C，并采用 5 引脚 SOT-23 和 SC70 封装。

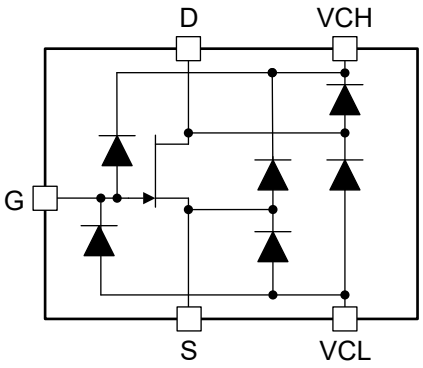
**封装信息**

| 器件型号 | 封装(1) | 封装尺寸（标称值） |
|---|---|---|
| JFE150 | DBV（SOT-23，5） | 2.90mm × 1.60mm |
| | DCK（SC70，5） | 2.00mm × 1.25mm |

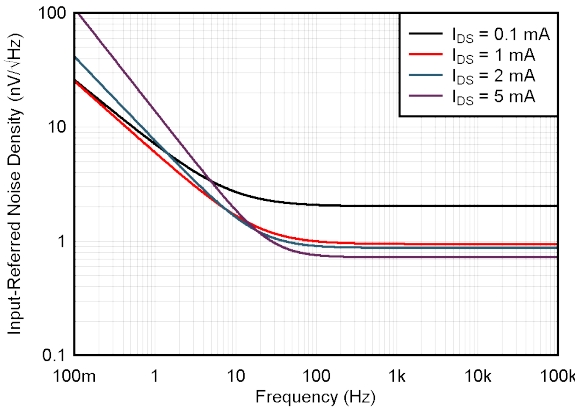
(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

**器件概要**

| 参数 | | 值 |
|---|---|---|
| $V_{GSS}$ | 栅源击穿电压 | -40 V |
| $V_{DSS}$ | 漏源击穿电压 | ±40V |
| $C_{ISS}$ | 输入电容 | 24pF |
| $T_J$ | 结温 | –40°C 至 +125°C |
| $I_{DSS}$ | 漏源饱和电流 | 35mA |




功能方框图




超低输入电压噪声

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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

**Changes from Revision A (November 2021) to Revision B (April 2023)** **Page**

- 将 DBV 封装（SOT-23，5）从预发布更改为量产数据（正在供货）并添加了相关内容 ..... 1
- 将*器件概要*表中的参数说明从“栅源电压”更改为“栅源击穿电压”，并从“漏源电压”更改为“漏源击穿电压”，以便与*电气特性*保持一致 ..... 1
- 将*器件概要*表中的“漏源饱和电流”值从 36mA 更改为 35mA，以便与*电气特性*保持一致 ..... 1
- Changed VCH and VCL pin type and description in *Pin Functions* to reflect optional nature of diode clamps ..... 3
- Changed Figure 6-2, *Drain-to-Source Current vs Drain-to-Source Voltage,* to show correct $V_{GS}$ values ..... 6
- Changed Figure 8-1, $V_{DS}$ *vs* $I_{DS}$, to show correct $V_{GS}$ values and improve image resolution ..... 10
- Added JFE150EVM user's guide and JFE150 Ultra-Low-Noise Pre-Amp application note to *Related Documentation* ..... 19

**Changes from Revision * (June 2021) to Revision A (November 2021)** **Page**

- Changed $V_{GS}$ minimum from –1.1 V to –1.3 V (100 µA), –0.9 V to –1.1 V (2 mA) ..... 5
- Changed Figure 6-3, *Drain-to-Source Current vs Drain-to-Source Voltage,* to show correct $V_{GS}$ values ..... 6

# 5 Pin Configuration and Functions

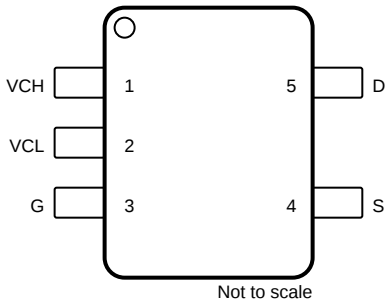



**图 5-1. DBV, 5-Pin SOT-23 and DCK, 5-Pin SC70 Packages (Top View)**

**表 5-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| D | 5 | Output | Drain |
| G | 3 | Input | Gate |
| S | 4 | Output | Source |
| VCH | 1 | — | Positive diode clamp voltage. Float this pin if clamp diodes are not used. |
| VCL | 2 | — | Negative diode clamp voltage. Float this pin if clamp diodes are not used. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain-to-source voltage | | –40 | 40 | V |
| $V_{GS}$, $V_{GD}$ | Gate-to-source, gate-to-drain voltage | | –40 | 0.9 | V |
| $V_{VCH}$ | Voltage between VCH to D, G, or S | | | 40 | V |
| $V_{VCL}$ | Voltage between VCL to D, G, or S | | –40 | | |
| $I_{VCL}$, $I_{VCH}$ | Clamp diode current | DC | | 20 | mA |
| | | 50-ms pulse(2) | | 200 | |
| $I_{DS}$ | Drain-to-source current | | –50 | 50 | mA |
| $I_{GS}$, $I_{GD}$ | Gate-to-source, gate-to-drain current | | –20 | 20 | mA |
| $T_A$ | Ambient temperature | | –55 | 150 | °C |
| $T_J$ | Junction temperature | | –55 | 150 | °C |
| $T_{stg}$ | Storage temperature | | –55 | 175 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Maximum diode current pulse specified for 50 ms at 1% duty cycle.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2500 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $I_{DS}$ | Drain-to-source current | 0.02 | | $I_{DSS}$ | mA |
| $V_{GS}$ | Gate-to-source voltage | 0 | | –1.2 | V |
| $T_A$ | Specified temperature | –40 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | JFE150 | | UNIT |
|---|---|---|---|---|
| | | DCK (SC70) | DBV (SOT-23) | |
| | | 5 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 197.1 | 183.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 93.7 | 83.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 44.8 | 51.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 16.7 | 24.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 44.6 | 51.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

at $T_A$ = 25°C, $I_{DS}$ = 2 mA, and $V_{DS}$ = 10 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **NOISE** | | | | | | | |
| $e_n$ | Input-referred voltage noise density | $I_{DS}$ = 100 µA , $V_{DS}$ = 5 V | f = 10 Hz | | 3 | | nV/ √Hz |
| | | | f = 1 kHz | | 2 | | |
| | | $I_{DS}$ = 2 mA, $V_{DS}$ = 5 V | f = 10 Hz | | 1.6 | | |
| | | | f = 1 kHz | | 0.9 | | |
| | | $I_{DS}$ = 5 mA, $V_{DS}$ = 5 V | f = 10 Hz | | 1.8 | | |
| | | | f = 1 kHz | | 0.8 | | |
| | Input-referred voltage noise | f = 0.1 Hz to 10 Hz, $V_{DS}$ = 5 V | $I_{DS}$ = 100 µA | | 0.19 | | $µV_{PP}$ |
| | | | $I_{DS}$ = 2 mA | | 0.09 | | |
| | | | $I_{DS}$ = 5 mA | | 0.13 | | |
| $e_i$ | Input current noise | f = 1 kHz, $V_{DS}$ = 5 V | | | 1.8 | | fA/ √Hz |
| **INPUT CURRENT** | | | | | | | |
| $I_G$ | Input gate current | $V_{DS}$ = 2 V, $V_{GS}$ = – 0.7 V, $V_{VCH}$ = 5 V, $V_{VCL}$ = – 5 V | | | 0.2 | ±10 | pA |
| | | $V_{DS}$ = 0 V, $V_{GS}$ = – 30 V | | | 0.2 | | |
| | | | $T_A$ = – 40°C to +85°C | | | ±2000 | |
| | | | $T_A$ = – 40°C to +125°C | | | ±10000 | |
| **INPUT VOLTAGE** | | | | | | | |
| $V_{GSS}$ | Gate-to-source breakdown voltage | $V_{DS}$ = 0 V, $\|I_G\|$ < 100 µA | | | | −40 | V |
| $V_{GSC}$ | Gate-to-source cutoff voltage | $V_{DS}$ = 10 V, $I_{DS}$ = 0.1 µA | | −1.5 | −1.2 | −0.9 | V |
| $V_{GS}$ | Gate-to-source voltage | $I_{DS}$ = 100 µA | | – 1.3 | | – 0.7 | V |
| | | $I_{DS}$ = 2 mA | | – 1.1 | | – 0.5 | |
| **INPUT IMPEDANCE** | | | | | | | |
| $R_{IN}$ | Gate input resistance | $V_{GS}$ = – 5 V to 0 V, $V_{DS}$ = 0 V | | | 1 | | TΩ |
| $C_{ISS}$ | Input capacitance | $V_{DS}$ = 0 V | | | 30 | | pF |
| | | $V_{DS}$ = 5 V | | | 24 | | |
| $C_{RSS}$ | Reverse transfer capacitance | $V_{DS}$ = 0 V | | | 7 | | |
| **OUTPUT** | | | | | | | |
| $I_{DSS}$ | Drain-to-source saturation current | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V | | 24 | 35 | 46 | mA |
| | | | $T_A$ = – 40°C to +125°C | 22 | | 57 | |
| gm | Transconductance | $I_{DS}$ = 100 µA | | | 3 | | mS |
| | | $I_{DS}$ = 2 mA | | | 18 | | |
| $G_{FS}$ | Full conduction transconductance | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V | | 55 | 68 | 80 | mS |
| $V_{DSS}$ | Drain-to-source breakdown voltage | $\|I_{DS}\|$ < 100 µA, $V_{GS}$ = – 2 V | | 40 | | | V |
| $C_{OSS}$ | Output capacitance | $V_{DS}$ = 5 V | | | 8 | | pF |

## 6.6 Typical Characteristics

at $T_A$ = 25°C, $I_{DS}$ = 2 mA, common-source configuration, and $V_{DS}$ = 5 V (unless otherwise noted)

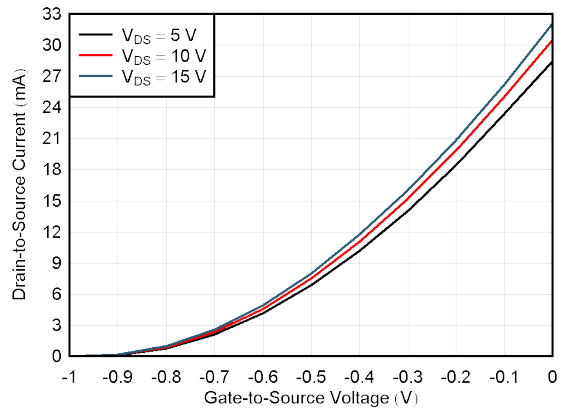



图 6-1. Drain-to-Source Current vs Gate-to-Source Voltage

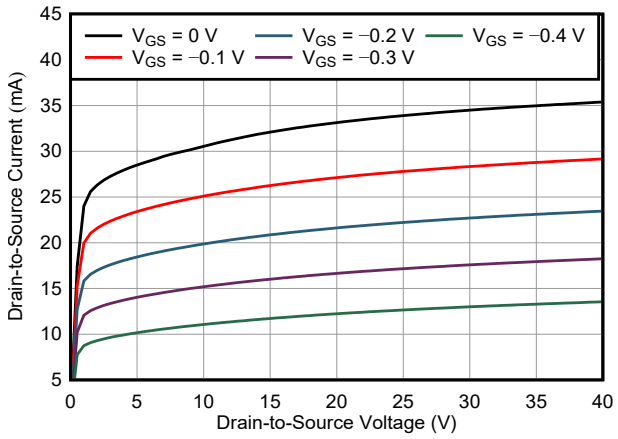



图 6-2. Drain-to-Source Current vs Drain-to-Source Voltage

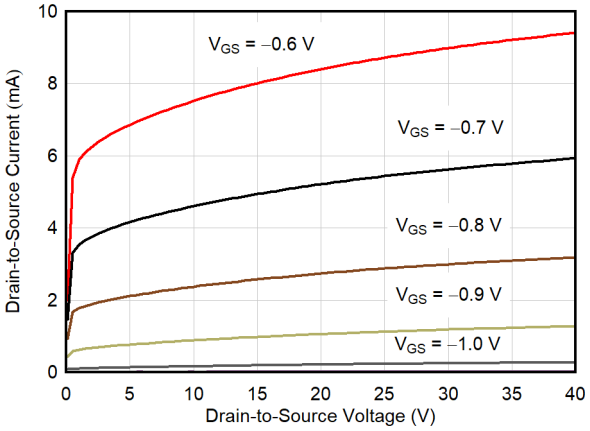



图 6-3. Drain-to-Source Current vs Drain-to-Source Voltage

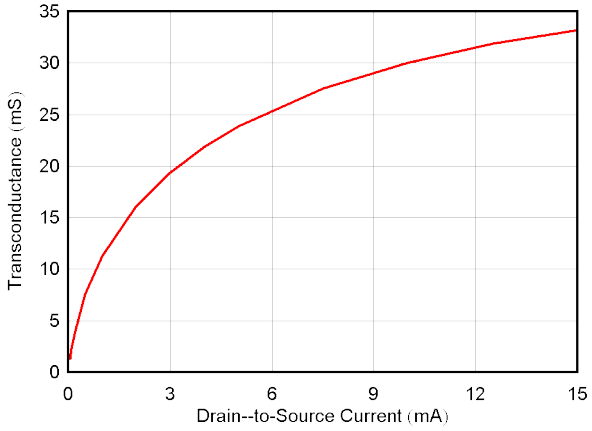



图 6-4. Common Source Transconductance vs Drain-to-Source Current

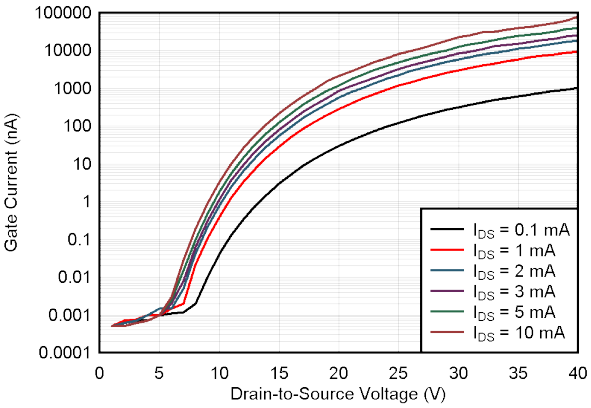



图 6-5. Gate Current vs Drain-to-Source Voltage

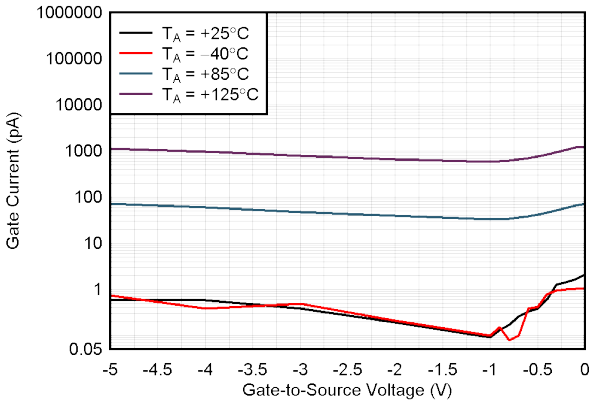
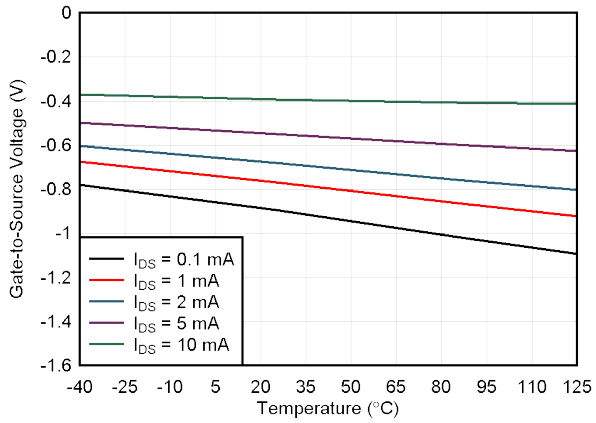



图 6-6. Gate Current vs Gate-to-Source Voltage

## 6.6 Typical Characteristics (continued)

at $T_A$ = 25°C, $I_{DS}$ = 2 mA, common-source configuration, and $V_{DS}$ = 5 V (unless otherwise noted)




$V_{DS}$ = 5 V

**图 6-7. Gate-to-Source Voltage vs Temperature**

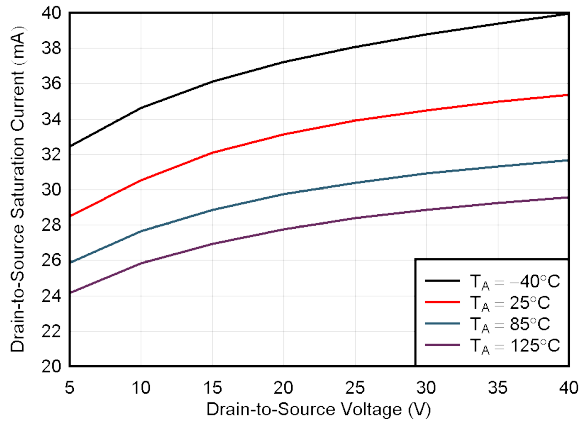



**图 6-8. $I_{DSS}$ vs Drain-to-Source Voltage**

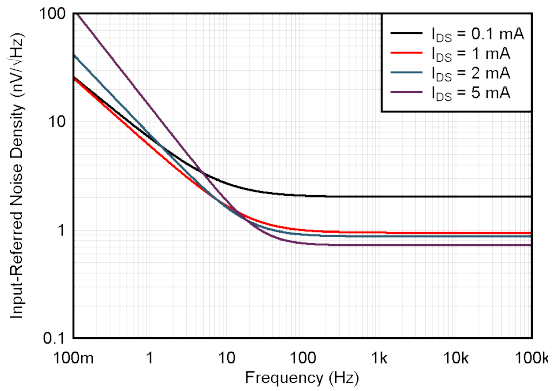
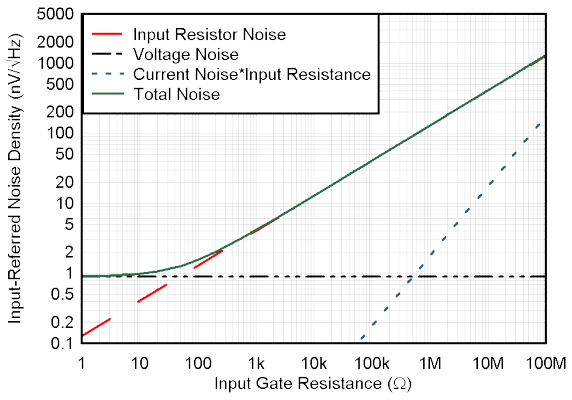
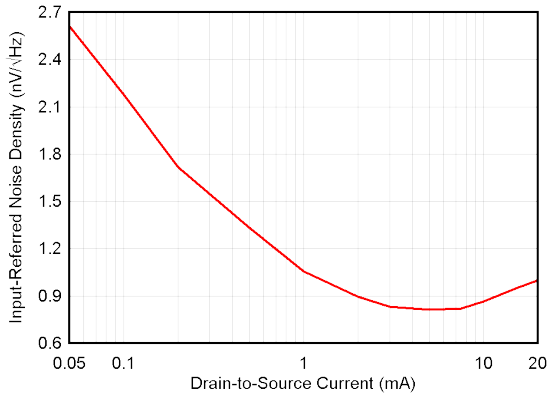



**图 6-9. Input-Referred Noise Density vs Frequency**




f = 1 kHz

**图 6-10. Noise Density Contributors vs Input Gate Resistance**




f = 1 kHz

**图 6-11. Input-Referred Noise Spectral Density vs Drain-to-Source Current**

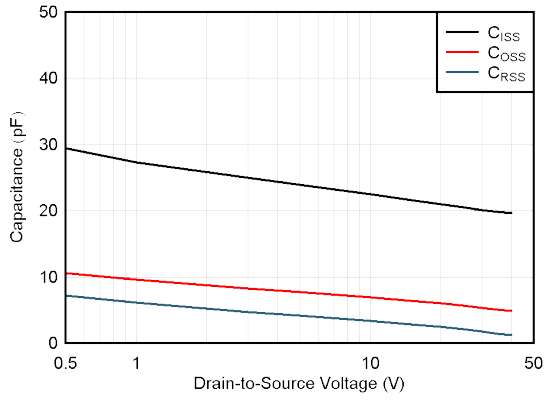



**图 6-12. Input, Output, and Reverse Transfer Capacitance vs Drain-to-Source Voltage**

# 7 Parameter Measurement Information

## 7.1 AC Measurement Configurations

The circuit configuration used for noise measurements is seen in 图 7-1. The nominal $I_{DS}$ current is configured in the schematic by calibrating V – . After $I_{DS}$ is fixed, the $V_{DS}$ voltage is set by calibrating V+. For input-referred noise data, the gain of the circuit is calibrated from $V_{IN}$ to $V_{OUT}$ and used for the input-referred gain calculation.

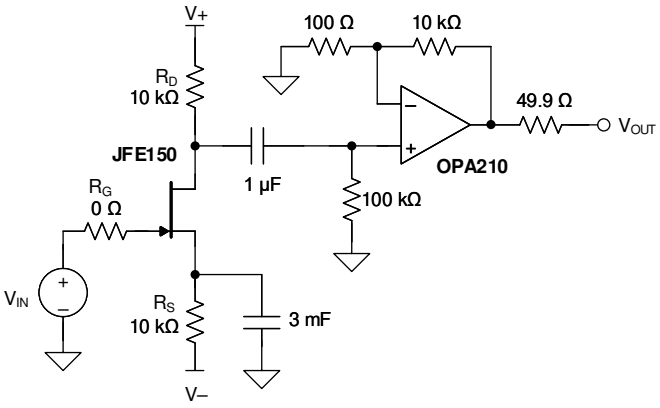


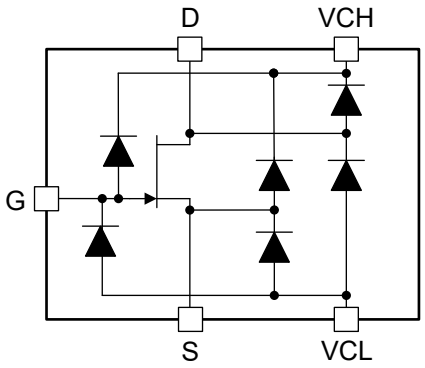

图 7-1. AC Measurement Reference Schematic

# 8 Detailed Description

## 8.1 Overview

The JFE150 is an ultra-low noise JFET designed to create low-noise gain stages for very high output impedance sensors or microphones. Advanced processing technology gives the JFE150 extremely low-noise performance, a high gm/$C_{ISS}$ ratio, and ultra-low gate-current performance. Input protection diodes are integrated to clamp high-voltage spurious input signals without the need for additional input diodes that can add leakage current or distortion-creating non-linear capacitance. The JFE150 provides a next-generation device to implement low-noise amplifiers for piezoelectric sensors, transducers, large-area condenser microphones, and hydrophones in small-package options.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Ultra-Low Noise

Junction-gate field-effect transistors (JFETs) are commonly used as an input stage in high-input-impedance, low-noise designs in audio, SONAR, vibration analysis, and other technologies. The JFE150 is a new generation JFET device that offers very low noise performance at the lowest possible current consumption in high-input-impedance amplifier designs. The JFE150 is manufactured on a high-performance analog process technology, giving tighter process parameter control than a standard JFET.

Designs that feature operational amplifiers (op amps) as the primary gain stage are common, but these designs are not able to achieve the lowest possible noise as a result of the inherent challenges and tradeoffs required from a full operational amplifier design. Noise in JFET designs can be evaluated in two separate regions: low-frequency flicker noise and wideband thermal noise. Flicker, or 1/f noise, is extremely important for systems that require signal gain at frequencies less that 100 Hz. The JFE150 achieves extremely low 1/f noise in this range. Thermal noise is noise in the region greater than 1 kHz and depends on the gain, or gm, of the circuit. The gm is a function of the drain-to-source bias current; therefore, thermal noise is also a function of drain-to-source bias current. 图 6-9 shows both 1/f and thermal noise with multiple bias conditions measured using the circuit shown in 图 7-1.

Noise is typically modeled as a voltage source (voltage noise) and current source (current noise) on the input. The 1/f and thermal noise can be represented as voltage noise. Current noise is dominated by current flow into the gate, and is called *shot noise*. The JFE150 features extremely low gate current, and therefore, extremely low current noise. 图 6-10 shows how source impedance on the input is the dominant noise source. In nearly all cases, noise created as a result of current noise is negligible.

### 8.3.2 Low Gate Current

The JFE150 features a maximum gate current of 10 pA at room temperature, making the device an excellent choice for maximizing the gain and dynamic range from extremely high impedance sensors. Additionally, any noise contributions as a result of gate current are minimized because of the negligible shot noise at low current levels. As with all JFET devices, when the drain-to-source voltage increases, the gate current also increases. Keep the drain-to-source voltage to less than 5 V for the lowest gate input current operation.

### 8.3.3 Input Protection

The JFE150 features input protection diodes that are used for surge clamping and ESD events. The diodes are rated to withstand high current surges for short times, steering current from the gate (G) pin to the VCH and VCL pins. The diodes also feature very low leakage, removing the need for external protection devices that can have high leakage currents or nonlinear capacitance that degrade the distortion performance.

## 8.4 Device Functional Modes

The JFE150 functionality is identical to standard N-channel depletion JFET devices. The gate-to-source ($V_{GS}$) voltage, drain-to-source voltage ($V_{DS}$) and drain-to-source current ($I_{DS}$) determine the region of operation.

- For $V_{GS} < V_{GSC}$: JFE150 conduction channel is closed; $I_{DS}$ is only determined by junction leakage current.
- For $V_{GS} > V_{GSC}$: Two modes of operation can exist depending on $V_{DS}$. When $V_{DS}$ is less than the linear (saturation) region threshold (see 图 8-1), the device operates in the linear region, meaning that the device behaves as a resistor connected from drain-to-source with minimal variation from any changes in $V_{GS}$. When $V_{DS}$ is greater than the linear (saturation) region threshold, $I_{DS}$ has a strong dependance on $V_{GS}$, where the relationship is described by the parameter gm.

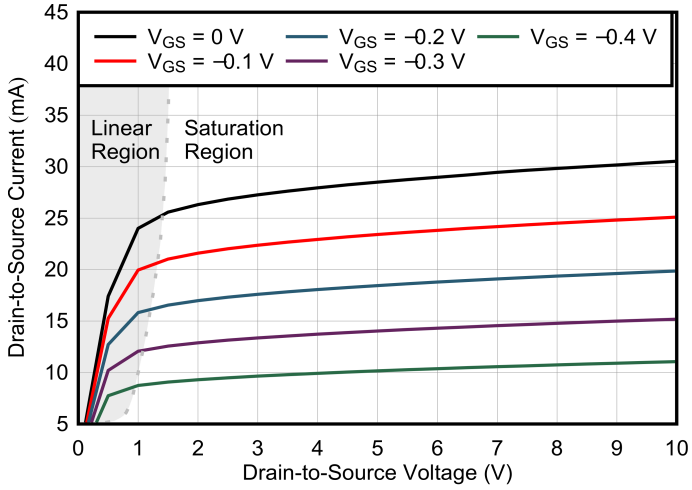



**图 8-1. $V_{DS}$ vs $I_{DS}$**

# 9 Application and Implementation

**备注**

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

## 9.1 Application Information

### 9.1.1 Input Protection Diodes

The JFE150 features diodes that are used to help clamp voltage surges that can occur on the input sensor to the gate. The diodes are connected between the gate and two separate pins, VCL and VCH. The clamping mechanism works by *steering* current from the gate into the VCL or VCH nodes when the voltage at the gate is less than VCL or greater than VCH. 图 9-1 shows an example of a microphone input circuit where a dc blocking capacitor operates with a large dc voltage. When the microphone input is dropped or shorted, the dc blocking capacitor discharges into the VCL or VCH nodes, thus helping eliminate large signal transient voltages on the gate. There are also clamping diodes from the drain and source to VCL and VCH, respectively. The clamping diodes can withstand high surge currents up to 200 mA for 50 ms; however, limit dc current to less than 20 mA.

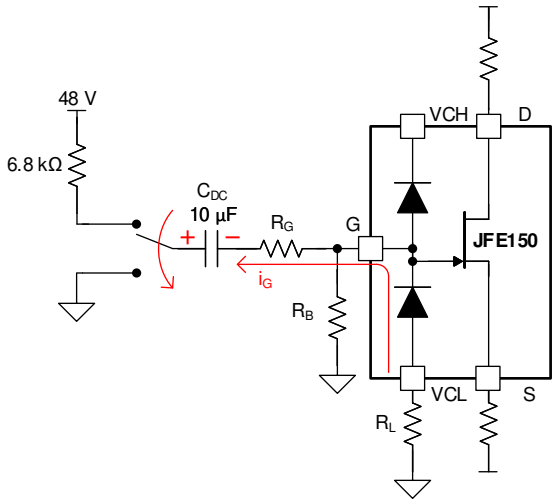



**图 9-1. JFE150 Clamping Diode Example**

图 9-1 shows an example of configuring the diode clamp to protect the JFET against overvoltage in a phantom-powered microphone circuit. Phantom power typically delivers 48 V through a 6.8-kΩ pullup resistor to a microphone or dynamic load. If the microphone is disconnected, dc blocking capacitor $C_{DC}$ can be biased up to 48 V. If the input to the capacitor is then shorted to ground (shown by the switch in 图 9-1), the gate voltage can exceed the absolute maximum rating for $V_{GS}$. In this case, the blocking diode is used, along with current limiting resistors $R_G$ and $R_L$, to clamp the gate voltage to a safe level. Be aware that the thermal noise of $R_G$ couples directly into the gate input; therefore, make sure to minimize the resistance of $R_G$.

The clamping diodes are not required for operation. The $V_{GS}$ voltage can withstand –40 V, so clamping is not required if the $V_{GS}$ voltage is kept greater than this limit. If the diodes are not needed, leave the VCL and VCH nodes floating.

Most previous-generation JFET devices featured only three pins (gate, source, and drain). For these devices, the gate pin is in the same physical location as the VCL pin on the JFE150. To test the JFE150 in a three-pin socket, short pin 2 of the JFE150 (VCL) to pin 3 (G). When the devices are connected with pin 2 shorted to pin 3, the diode from VCL is shorted out and cannot provide any clamping protection. The input capacitance ($C_{ISS}$) also increases by 1 pF; see 图 6-12.

### 9.1.2 Capacitive Transducer Input Stage

Piezoelectric transducers are used for many different applications that require low-noise, high-gain performance. These transducers exhibit high output impedance (> 10 MΩ), and therefore require very high impedance loading for subsequent input stages. The JFE150 has ultra-low input gate current (maximum $I_G$ = ±10 pA) and low input capacitance ($C_{ISS}$ = 24 pF), which makes the device an excellent choice for transducers with an effective capacitance of greater than 240 pF. For smaller, lower-capacitance transducers, the $C_{ISS}$ can impact the gain of the front end by attenuating the input signal, thereby reducing the noise performance.

### 9.1.3 Common-Source Amplifier

The common-source amplifier is a commonly used open-loop gain stage for JFET amplifiers. 图 9-2 shows the basic circuit.

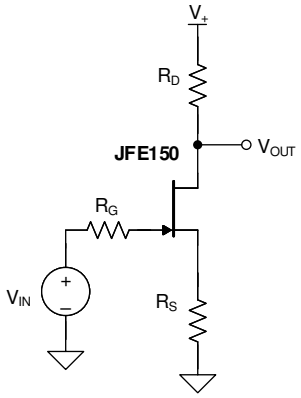



**图 9-2. Common-Source Amplifier**

方程式 1 shows the equation for gain of the circuit in 图 9-2.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{gm^*R_D}{1+gm^*R_S} \quad (1)$$

Generally, higher gain results in improved noise performance. Gain increases as the bias current is increased as a result of increasing gm (see 图 6-4). As a result, the input-referred noise decreases as bias current is increased (see 图 6-9). Any JFET design must make a tradeoff between current consumption and noise performance. The JFE150, however, delivers significantly lower noise performance than most operational amplifiers at the same current consumption. The bias current ($I_{DS}$) is set by the value of the source resistor, $R_S$, and the threshold voltage, $V_T$, of the JFE150. 图 9-3 is a graph showing nominal $I_{DS}$ vs $R_S$.

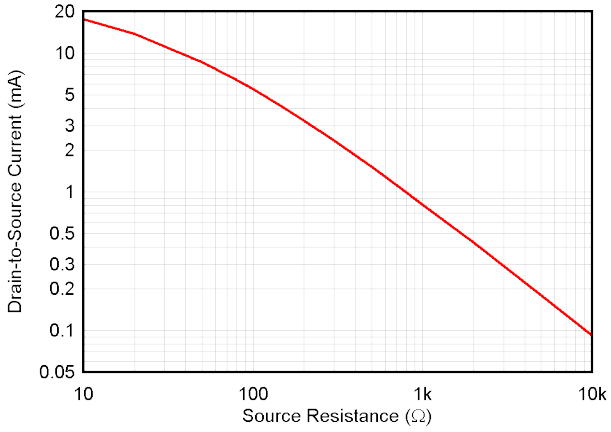



**图 9-3. Drain-to-Source Current vs $R_S$, $V_{DS}$ = 5 V**

The bias current varies according to the resistor and threshold voltage tolerances. Additionally, thermal noise associated with $R_S$ couples directly into the gain of the circuit, degrading the overall noise performance. To improve the circuit in 图 9-4, use a current-source biasing scheme. Current-source biasing removes the JFET threshold variation from the biasing scheme, and allows for lower-value filtering capacitance ($C_S$) for equivalent filtering due to the high output impedance of current sources.

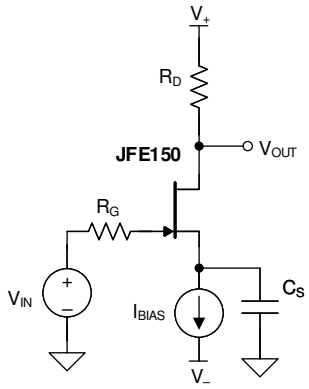



**图 9-4. Common-Source Amplifier With Current-Source Biasing**

### 9.1.4 Composite Amplifiers

The JFE150 can be configured to provide a low-noise, high-input impedance front-end stage for a typical op amp. Open-loop transistor gain stages shown previously suffer from wide gain variations that are dependent on the forward transcondutance of the JFE150. When precision gain is required, the composite amplifier (JFET front-end + operational amplifier) achieves excellent results by allowing for a fixed gain determined by external resistors, and improving the noise and bandwidth of the operational amplifier. The JFE150 gain stage provides a boost to the open-loop performance of the system, extending the bandwidth beyond what the operational amplifier alone can provide, and gives a high-input impedance, ultra-low noise input stage to interface with high source impedance microphones.

图 9-5 shows a generic schematic representation of a current-feedback composite amplifier. The component requirements and tradeoffs are listed in 表 9-1.

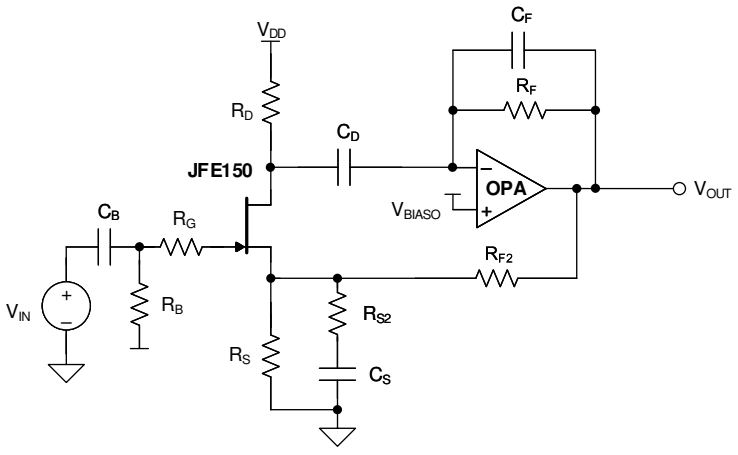



**图 9-5. Low Noise, High Input Impedance Composite Amplifier**

表 9-1. Composite Amplifier Component List and Function

| COMPONENT | DESCRIPTION | RELATED EQUATION |
|---|---|---|
| $C_B$ | DC blocking capacitor for input source. Use a dc blocking capacitor if the dc voltage of the input source is not the same as the gate bias voltage. | $f_{-3dBDC} = \frac{1}{2*\pi*R_{B1}\|\|R_{B2}*C_{B1}}$ (2) |
| $R_B$ | Bias resistor. Use biasing resistors to set the dc voltage at the gate. High-value resistors can be used without an impact to noise if the source impedance and bypass capacitor have sufficiently low impedance. | See 方程式 2 |
| $R_G$ | Gate resistor. Can be used to help limit current flow into gate in overvoltage cases. | |
| $R_D$ | Drain resistor. Sets gain of JFET stage in common source biasing, along with gm and $R_S$. | |
| $R_S$ | Source resistor. Used to set bias of JFET; see 图 9-3. Resistor thermal noise directly impacts noise performance. | |
| $C_D$ | DC blocking capacitor. Blocks nominal drain voltage so the amplifier operates at a midsupply bias point. | |
| $C_F$ | Feedback capacitor. Along with $R_F$, this capacitor sets the –3-dB high-pass cutoff frequency when the amplifier gain-bandwidth product (GBW) is sufficiently high enough to support the –3-dB frequency. If the GBW is not high enough, then the GBW sets the –3-dB frequency. | $f_{-3dBHP} = \frac{1}{2*\pi*R_F*C_F}$ (3) |
| $R_F$ | Feedback resistor. Along with $C_F$, this resistor sets the –3-dB high-pass cutoff frequency when the amplifier gain-bandwidth product (GBW) is sufficiently high enough to support the –3-dB frequency. If the GBW is not high enough, then the GBW sets the –3-dB frequency. | See 方程式 3 |
| $R_{F2}$ | Current feedback gain-setting resistor 1. Along with $R_{S2}$, sets gain closed-loop. | $\frac{V_{OUT}}{V_{IN}} = \frac{R_{F2}}{R_{S2}}$ (4) |
| $R_{S2}$ | Current feedback gain-setting resistor 2. Along with $R_{S2}$, sets gain closed-loop. Resistor thermal noise directly impacts noise performance. | See 方程式 4 |
| $C_S$ | Current feedback ac-coupling capacitor. This capacitor, along with $R_2$, sets the low-pass –3-dB frequency. | $f_{-3dBLP} = \frac{1}{2*\pi*R_{S2}*C_S}$ (5) |

## 9.2 Typical Application

The JFE150 can be configured to provide a low-noise, high-input-impedance front-end stage for a typical op amp. Single-transistor gain stages shown previously suffer from wide gain variations dependent on the forward transcondutance of the JFE150. When precision gain is required, the composite amplifier (JFET front-end + operational amplifier) achieves excellent results.

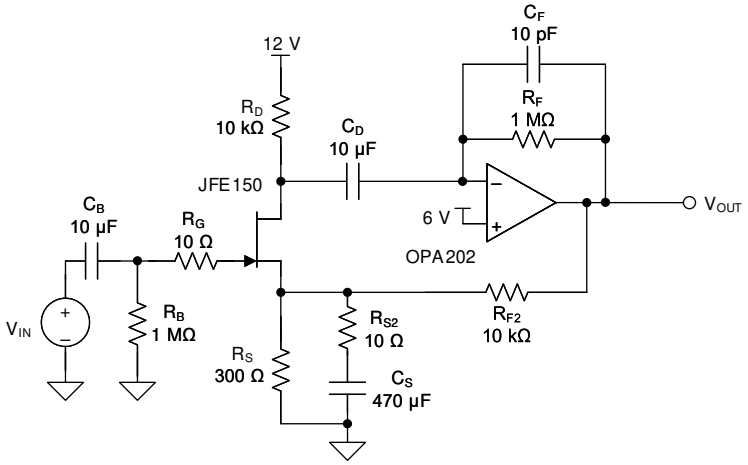



**图 9-6. Low-Noise, High-Input-Impedance Composite Amplifier**

### 9.2.1 Design Requirements

| PARAMETER | DESIGN GOAL |
|---|---|
| Gain | 60 dB |
| Frequency response | 60 Hz to 20 kHz |
| Noise | < 1.5 nV/ $\sqrt{\text{Hz}}$ |
| Input current | < 100 pA |
| Output swing | ±5 V |

### 9.2.2 Detailed Design Procedure

This design provides 60 dB of gain with extremely high input impedance at a very low frequency response. The order of design priorities are as follows:

- The JFE150 bias current is set by selecting the desired bias current and noise tradeoff (see 图 6-11). The input-referred noise is dominated by the JFE150 bias current and gain. To set the bias current point, adjust the source resistance according to 图 9-3.
- After the bias current is selected, set the JFET stage gain as high as possible without pushing the device into the linear region of operation. This is achieved by using the largest drain resistor ($R_D$) possible while maintaining a minimum of 2 V across the drain to source nodes. Be aware that the amplifier forces the drain node to match the noninverting amplifier input in normal closed-loop operation. Both ac and dc voltages must be considered, but generally, only the dc operating point on the drain is considered because the ac voltage swing is minimal.
- Set the closed gain according to $R_{F2}$ and $R_{S2}$, as seen in 方程式 4. Thermal noise from $R_{S2}$ directly couples into the circuit; therefore, small values for this resistor are required.
- $C_S$ is required to block dc voltages from altering the bias point set by source resistor $R_S$. $C_S$ also forms the low-frequency response as described in 方程式 5.

### 9.2.3 Application Curves

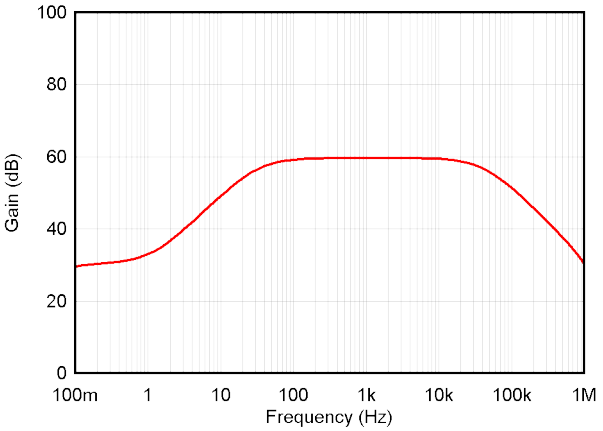



图 9-7. Voltage Gain

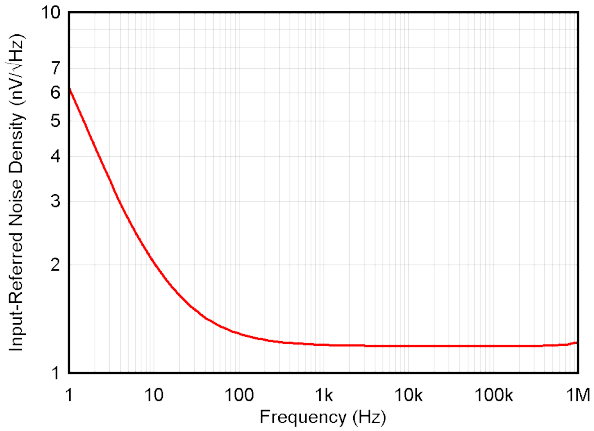



图 9-8. Input-Referred Noise Density

## 9.3 Power Supply Recommendations

The JFE150 is a JFET transistor with clamping diodes. There are no specific power-supply connections; however, take care not to exceed any absolute maximum voltages on any of the pins if system supply voltages greater than or equal to 40 V are used.

## 9.4 Layout

### 9.4.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Reduce parasitic coupling by running the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Keep high impedance input signals away from noisy traces.
- Make sure supply voltages are adequately filtered.
- Minimize distance between source-connected and drain-connected components to the JFE150.
- Consider a driven, low-impedance guard ring around the critical gate traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

### 9.4.2 Layout Example

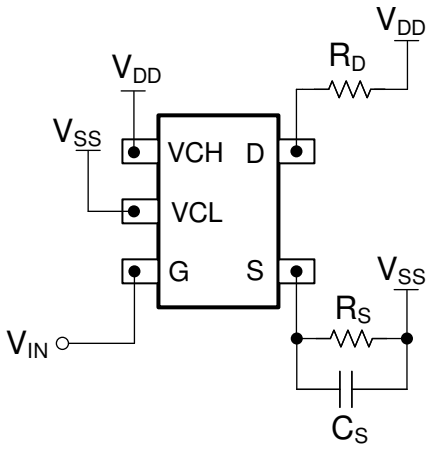



**图 9-9. JFE150 Layout Example, Common Source Configuration**

# 10 Device and Documentation Support

## 10.1 Device Support

### 10.1.1 Development Support

#### *10.1.1.1 PSpice® for TI*

PSpice® for TI 是可帮助评估模拟电路性能的设计和仿真环境。在进行布局和制造之前创建子系统设计和原型解决方案，可降低开发成本并缩短上市时间。

#### *10.1.1.2 TINA-TI™ 仿真软件（免费下载）*

TINA-TI™ 仿真软件是一款简单易用、功能强大且基于 SPICE 引擎的电路仿真程序。TINA-TI 仿真软件是 TINA™ 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 仿真软件提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 仿真软件提供全面的后处理能力，便于用户以多种方式获得结果，用户可从设计工具和仿真网页免费下载。虚拟仪器提供选择输入波形和探测电路节点、电压以及波形的能力，从而构建一个动态的快速启动工具。

**备注**

必须安装 TINA 软件或者 TINA-TI 软件后才能使用这些文件。请从 TINA-TI™ 软件文件夹中下载免费的 TINA-TI 仿真软件。

#### *10.1.1.3 TI 参考设计*

TI 参考设计是由 TI 的精密模拟应用专家创建的模拟解决方案。TI 参考设计提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。TI 参考设计可在线获取，网址为 https://www.ti.com/reference-designs。

#### *10.1.1.4 滤波器设计工具*

滤波器设计工具是一款简单、功能强大且便于使用的有源滤波器设计程序。利用滤波设计器，用户可使用精选 TI 运算放大器和 TI 供应商合作伙伴提供的无源器件来打造理想滤波器设计方案。

设计工具和仿真网页以基于网络的工具形式提供滤波设计工具。用户通过该工具可在短时间内完成多级有源滤波器解决方案的设计、优化和仿真。

## 10.2 Documentation Support

### 10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *JFE150 Ultra-Low-Noise Pre-Amp* application note
- Texas Instruments, *JFE150 Evaluation Module* user's guide
- Texas Instruments, *OPAx202 Precision, Low-Noise, Heavy Capacitive Drive, 36-V Operational Amplifiers* data sheet
- Texas Instruments, *OPAx210 2.2-nV/ √Hz Precision, Low-Power, 36-V Operational Amplifiers* data sheet

## 10.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 10.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## 10.5 Trademarks

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TINA™ is a trademark of DesignSoft, Inc.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
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## 10.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 10.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| JFE150DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2GLW |
| JFE150DBVR.B | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2GLW |
| JFE150DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2GLW |
| JFE150DBVT.B | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2GLW |
| JFE150DCKR | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1IF |
| JFE150DCKR.B | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1IF |
| JFE150DCKT | Active | Production | SC70 (DCK) \| 5 | 250 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1IF |
| JFE150DCKT.B | Active | Production | SC70 (DCK) \| 5 | 250 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1IF |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

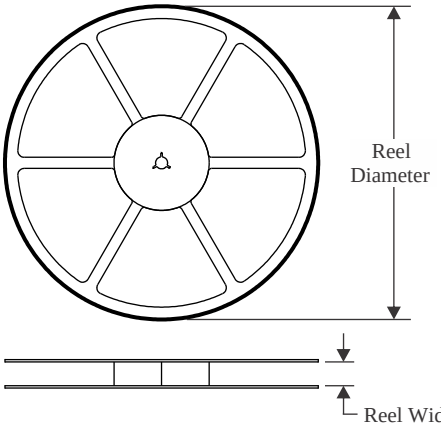
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

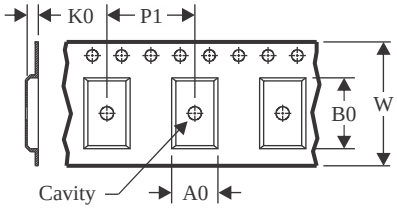
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

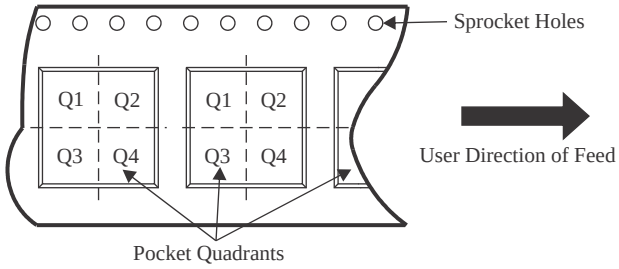



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

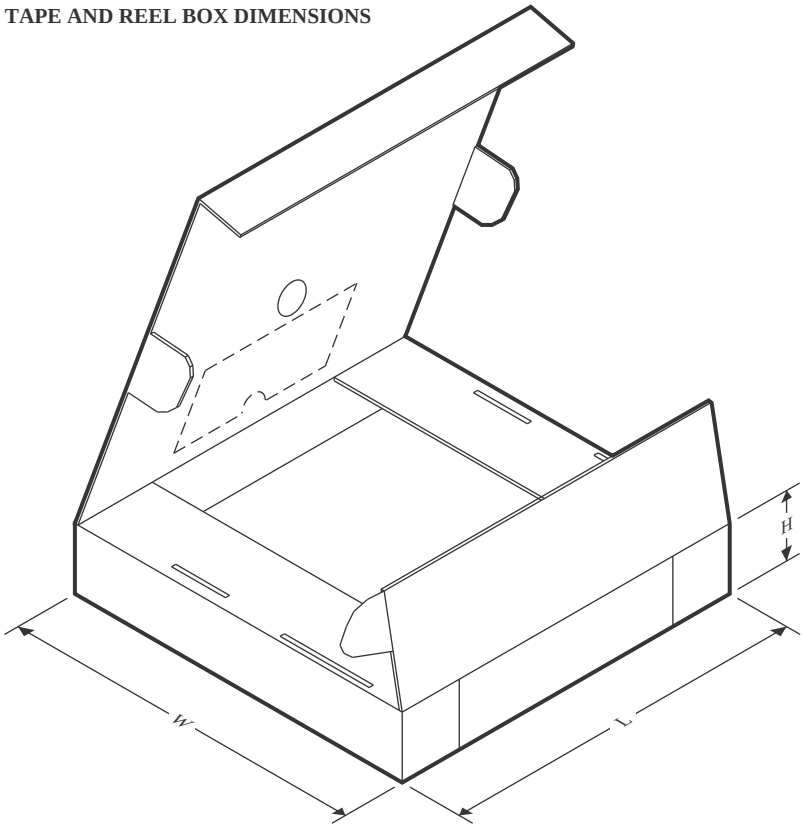
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| JFE150DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| JFE150DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| JFE150DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.3 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| JFE150DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| JFE150DCKT | SC70 | DCK | 5 | 250 | 180.0 | 8.4 | 2.3 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

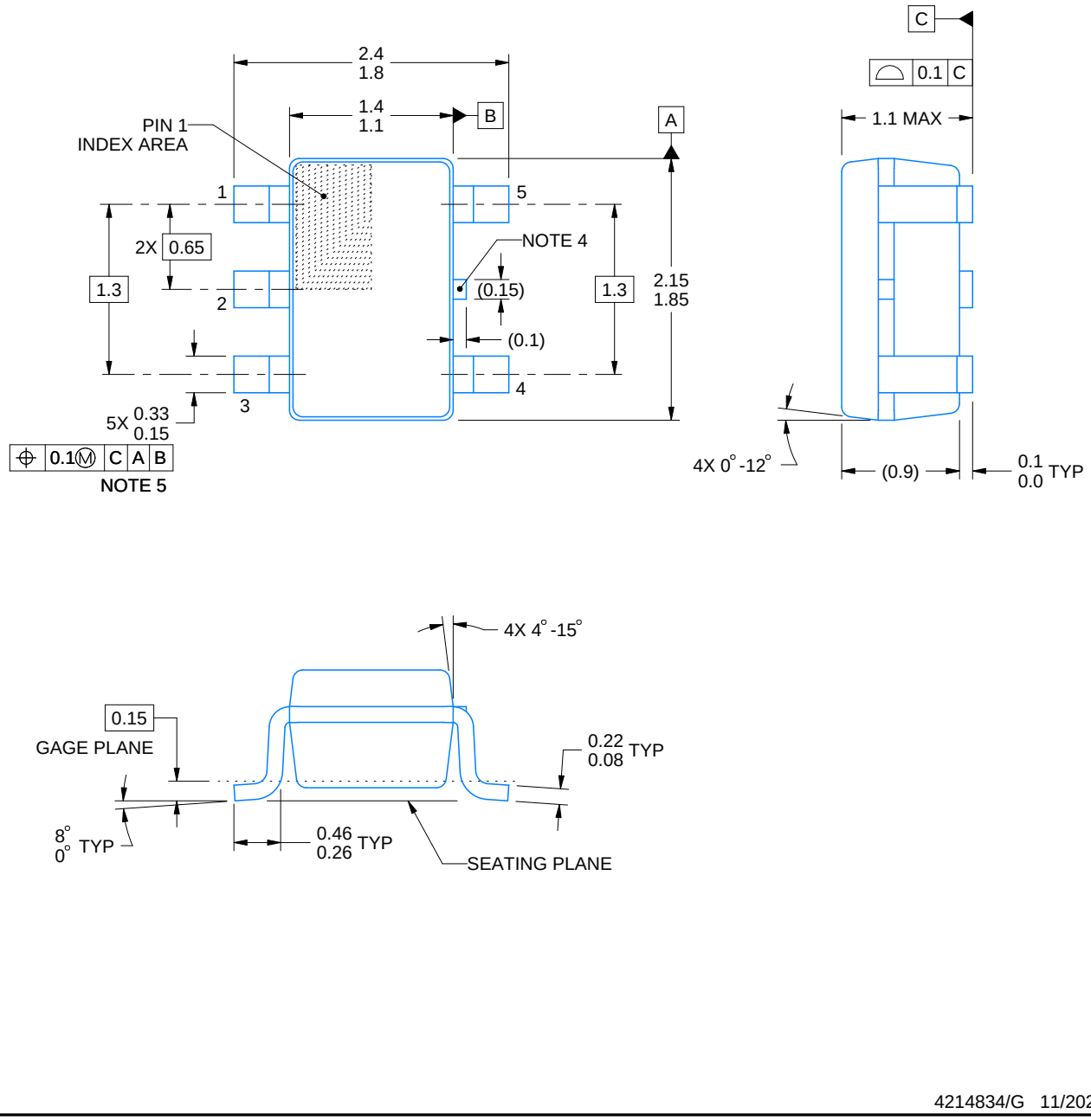
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| JFE150DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| JFE150DBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| JFE150DCKR | SC70 | DCK | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| JFE150DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| JFE150DCKT | SC70 | DCK | 5 | 250 | 210.0 | 185.0 | 35.0 |

# PACKAGE OUTLINE

## DCK0005A

## SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR

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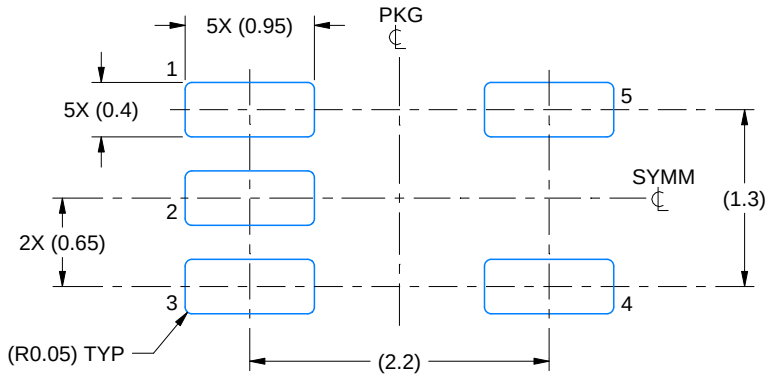
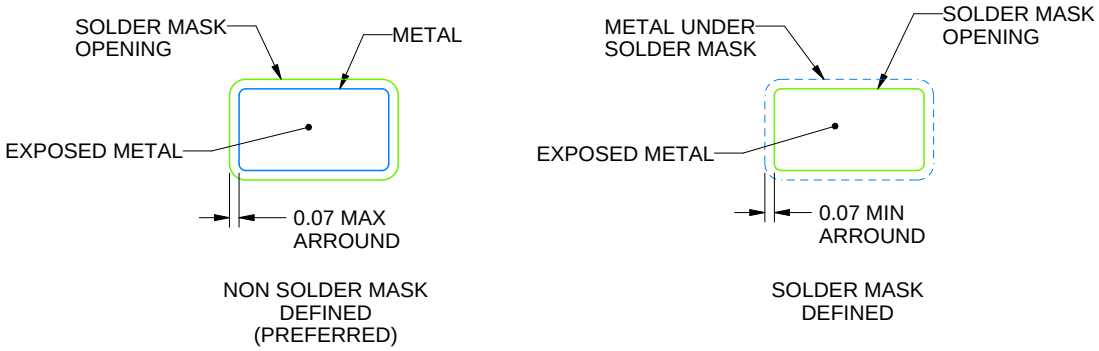
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X




SOLDER MASK DETAILS

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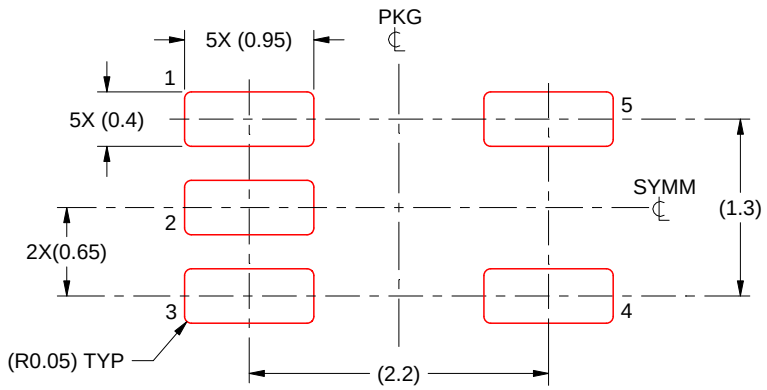
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

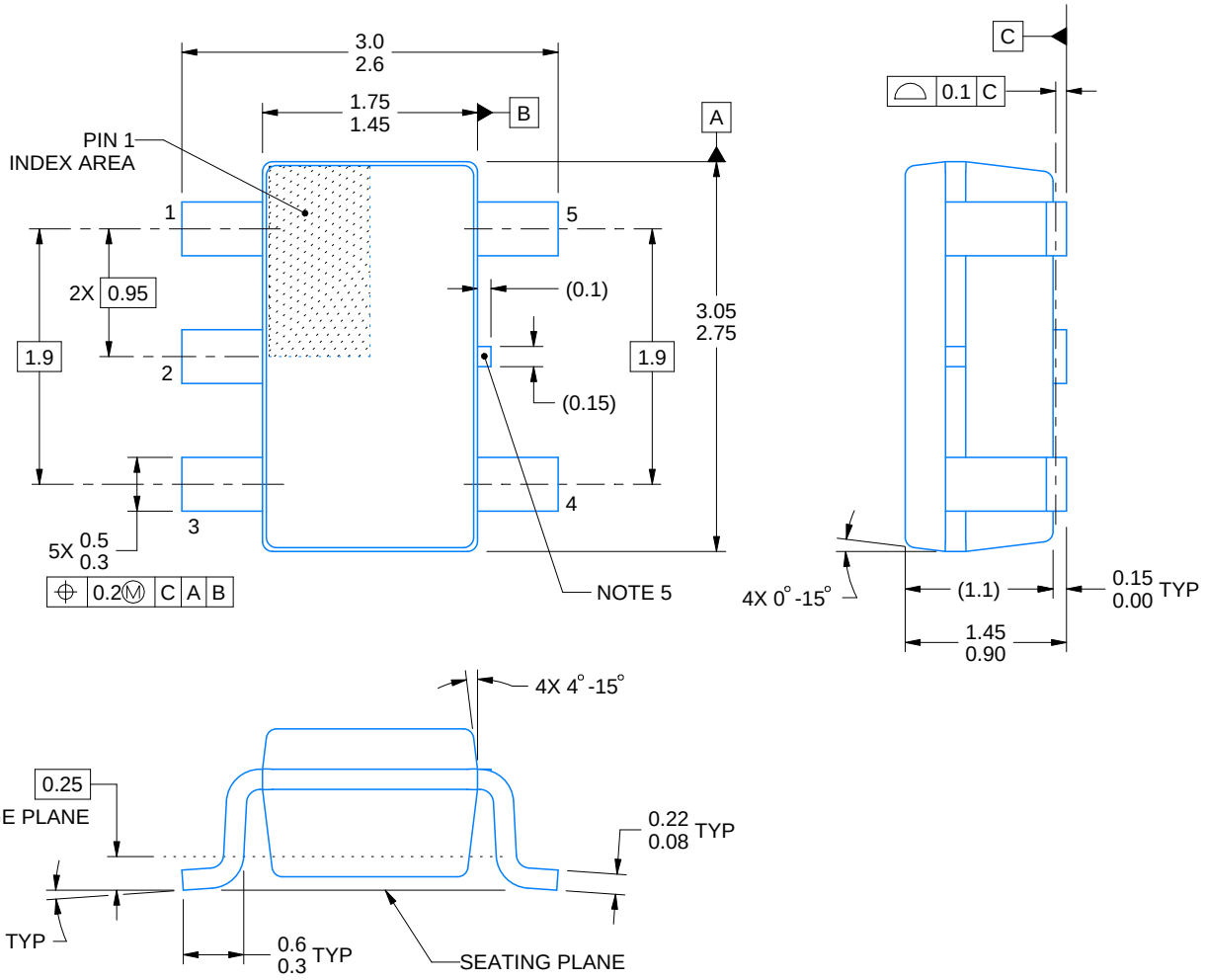
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

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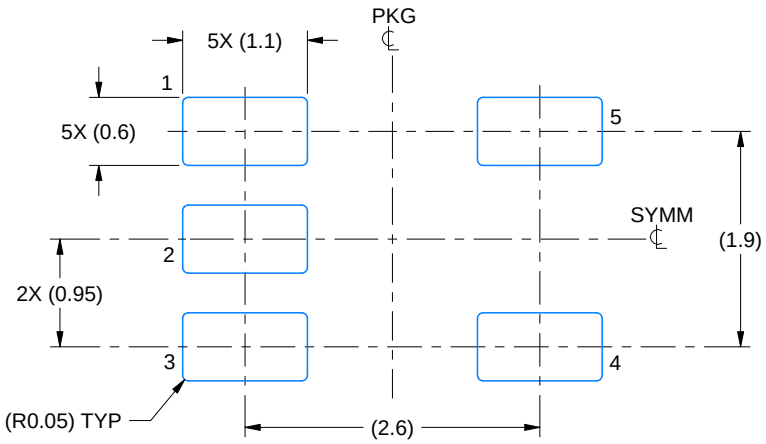
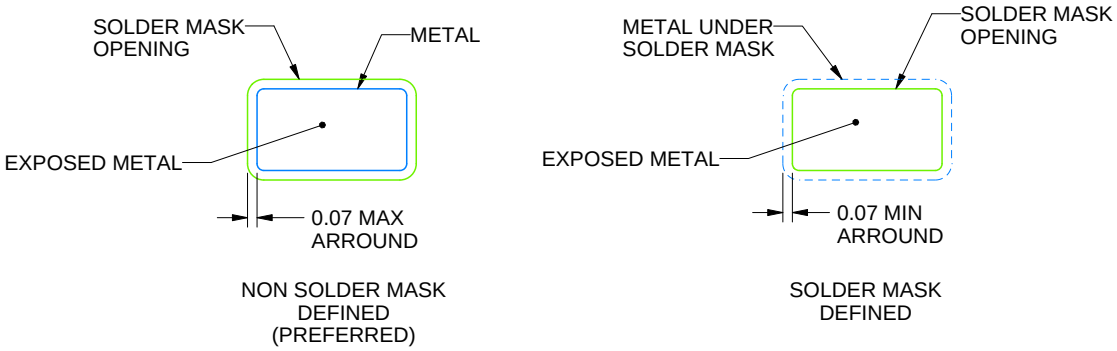
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

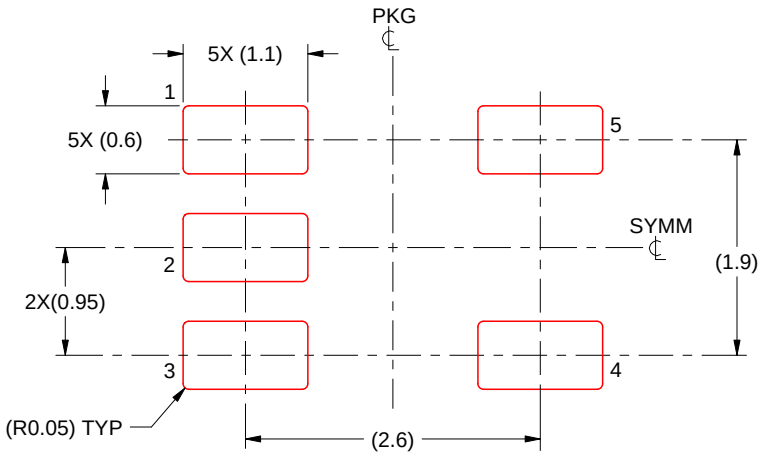



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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