LM25019 48V、100mA 恒定导通时间同步降压/Fly-Buck™ 稳压器

1 特性

- 7.5V 至 48V 宽输入范围
- 集成了 100mA 高侧和低侧开关
- 无需肖特基二极管
- 恒定导通时间控制
- 无需环路补偿
- 超快瞬态响应
- 接近恒定的运行频率
- 智能峰值电流限制
- 可调节输出电压（以 1.225V 为基准电压）
- 精度为 2% 的反馈基准电压
- 频率可调至 1MHz
- 可调节的欠压锁定
- 远程关断
- 热关断
- 封装：
  - 8 引脚 WSON
  - 8 引脚 SO PowerPAD™

2 应用

- 工业设备
- 智能电表
- 电信系统
- 隔离式偏置电源 (Fly-Buck™)

3 说明

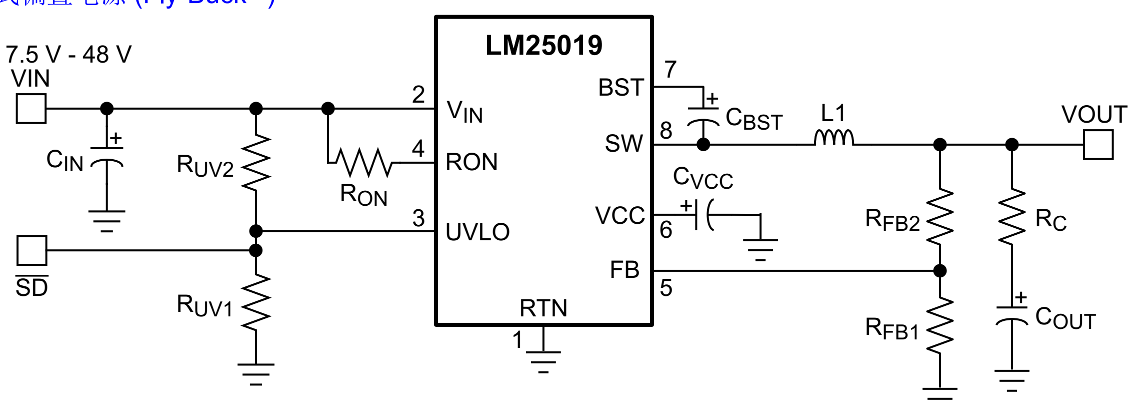
LM25019 是一款集成了高侧和低侧 MOSFET 的 48V、100mA 同步降压稳压器。LM25019 所采用的恒定导通时间 (COT) 控制方案无需环路补偿，可提供出色的瞬态响应，并且可实现超高降压比。导通时间与输入电压成反比，这使得整个输入电压范围内的频率几乎保持恒定。高压启动稳压器为 IC 的内部运行以及集成栅极驱动器提供了偏置电源。

峰值电流限制电路可防止出现过载情况。欠压锁定 (UVLO) 电路支持对输入欠压阈值和迟滞进行单独编程。其他保护特性包括：热关断和偏置电源欠压锁定。

LM25019 采用 8 引脚 WSON 和 8 引脚 SO PowerPAD 塑料封装。

器件信息

器件型号	封装	封装尺寸（标称值）
LM25019	SO PowerPAD (8)	4.89mm x 3.90mm
	WSON (8)	4.00mm × 4.00mm



典型应用

English Data Sheet: SNVS952

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4 Revision History

Changes from Revision E (April 2015) to Revision F (May 2021) **Page**

- 在标题中添加了“同步 Fly-Buck” 1
- 更新了整个文档中的表格、图和交叉参考的编号格式........ 1

Changes from Revision D (December 2014) to Revision E (November 2015) **Page**

- Changed 14 V to 13 V in V_{CC} *Regulator* section........ 10
- Changed 8 to 4 on equation in *Input Capacitor* section........ 18
- Changed 0.06 µF to 0.12 µF in *Input Capacitor* section........ 18

Changes from Revision C (December 2013) to Revision D (November 2014) **Page**

- 添加了 *引脚配置和功能* 部分、*ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分........ 1
- Changed *Soft-Start Circuit* graphic........ 14
- Changed *Frequency Selection* section, *Inductor Selection* section, *Output Capacitor* section, *Input Capacitor* section, and *UVLO Resistors* section........ 17
- Changed *Series Ripple Resistor* R_C section to *Type III Ripple Circuit* 18

Changes from Revision B (December 2013) to Revision C (December 2013) **Page**

- Added Thermal Parameters 4

Changes from Revision A (September 2013) to Revision B (December 2013) **Page**

- 将文档中的格式更改为符合 TI 标准的格式........ 1
- 将 *特性* 中的最低工作输入电压从 9V 更改为 7.5V........ 1
- 将 *典型应用* 中的最低工作输入电压从 9V 更改为 7.5V........ 1
- Added Absolute Maximum Junction Temperature........ 4
- Changed minimum operating input voltage from 9 V to 7.5 V in *Recommended Operating Conditions* 4

Changes from Revision * (December 2012) to Revision A (September 2013) **Page**

- Added SW to RTN (100 ns transient) in *Absolute Maximum Ratings* table........ 4

5 Pin Configuration and Functions

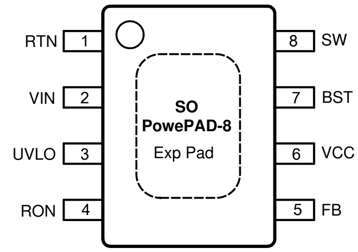


图 5-1. 8-Pin SO PowerPAD DDA Package Top View

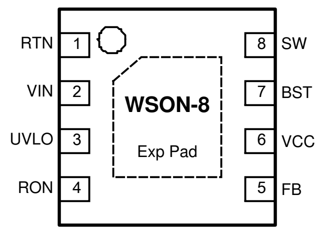


图 5-2. 8-Pin WSON NGU Package Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	RTN	—	Ground	Ground connection of the integrated circuit
2	VIN	I	Input Voltage	Operating input range is 7.5 V to 48 V.
3	UVLO	I	Input Pin of Undervoltage Comparator	Resistor divider from V_{IN} to UVLO to GND programs the undervoltage detection threshold. An internal current source is enabled when UVLO is above 1.225 V to provide hysteresis. When UVLO pin is pulled below 0.66 V externally, the regulator is in shutdown mode.
4	RON	I	On-Time Control	A resistor between this pin and V_{IN} sets the buck switch on-time as a function of V_{IN}. Minimum recommended on-time is 100 ns at max input voltage.
5	FB	I	Feedback	This pin is connected to the inverting input of the internal regulation comparator. The regulation level is 1.225 V.
6	VCC	O	Output from the Internal High Voltage Series Pass Regulator. Regulated at 7.6 V	The internal V_{CC} regulator provides bias supply for the gate drivers and other internal circuitry. A 1.0-µF decoupling capacitor is recommended.
7	BST	I	Bootstrap Capacitor	An external capacitor is required between the BST and SW pins (0.01-µF ceramic). The BST pin capacitor is charged by the V_{CC} regulator through an internal diode when the SW pin is low.
8	SW	O	Switching Node	Power switching node. Connect to the output inductor and bootstrap capacitor.
—	EP	—	Exposed Pad	Exposed pad must be connected to the RTN pin. Solder to the system ground plane on application board for reduced thermal resistance.

6 Specifications

6.1 Absolute Maximum Ratings

	MIN(1)	MAX	UNIT
V_{IN}, UVLO to RTN	– 0.3	53	V
SW to RTN	– 1.5	V_{IN} + 0.3	V
SW to RTN (100 ns transient)	– 5	V_{IN} + 0.3	V
BST to VCC		53	V
BST to SW		13	V
RON to RTN	– 0.3	53	V
VCC to RTN	– 0.3	13	V
FB to RTN	– 0.3	5	V
Lead Temperature(2)		200	°C
Maximum Junction Temperature(3)		150	°C
Storage temperature, T_{stg}	– 55	150	°C

(1) *Absolute Maximum Ratings* are limits beyond which damage to the device may occur. 节 *6.3* are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see 节 *6.5* . The RTN pin is the GND reference electrically connected to the substrate.
(2) For detailed information on soldering plastic SO Power PAD-8 package, refer to the Packaging Data Book available from Texas Instruments. Max solder time not to exceed 4 seconds.
(3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{IN} Voltage	7.5	48	V
Operating Junction Temperature(2)	−40	125	°C

(1) *Recommended Operating Conditions* are conditions under the device is intended to be functional. For specifications and test conditions, see 节 *6.5*.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRICS(1)		LM25019		UNIT
		WSON NGU	SO PowerPAD DDA	
		8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.3	41.1	°C/W
$R_{\theta JC}$(bot)	Junction-to-case (bottom) thermal resistance	3.2	2.4	°C/W
Ψ_{JB}	Junction-to-board thermal characteristic parameter	19.2	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.1	30.6	°C/W
$R_{\theta JC}$(top)	Junction-to-case (top) thermal resistance	34.7	37.3	°C/W

THERMAL METRICS[1]		LM25019		UNIT
		WSON NGU	SO PowerPAD DDA	
		8 PINS		
Ψ_{JT}	Junction-to-top thermal characteristic parameter	0.3	6.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated. V_{IN} = 48V unless stated otherwise. See[1].

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} SUPPLY						
V_{CC} Reg	V_{CC} Regulator Output	V_{IN} = 48 V, I_{CC} = 20 mA	6.25	7.6	8.55	V
	V_{CC} Current Limit	V_{IN} = 48 V[2]	26			mA
	V_{CC} Undervoltage Lockout Voltage (V_{CC} Increasing)		4.15	4.5	4.9	V
	V_{CC} Undervoltage Hysteresis			300		mV
	V_{CC} Drop Out Voltage	V_{IN} = 9 V, I_{CC} = 20 mA		2.3		V
	I_{IN} Operating Current	Nonswitching, FB = 3 V		1.75		mA
	I_{IN} Shutdown Current	UVLO = 0 V		50	225	µA
SWITCH CHARACTERISTICS						
	Buck Switch $R_{DS(ON)}$	I_{TEST} = 100 mA, BST-SW = 7 V		0.8	1.8	Ω
	Synchronous $R_{DS(ON)}$	I_{TEST} = 200 mA		0.45	1	Ω
	Gate Drive UVLO	$V_{BST} - V_{SW}$ Rising	2.4	3	3.6	V
	Gate Drive UVLO Hysteresis			260		mV
CURRENT LIMIT						
	Current Limit Threshold		150	270	370	mA
	Current Limit Response Time	Time to Switch Off		150		ns
	Off-Time Generator (Test 1)	FB = 0.1 V, V_{IN} = 48 V		12		µs
	Off-Time Generator (Test 2)	FB = 1 V, V_{IN} = 48 V		2.5		µs
REGULATION AND OVERVOLTAGE COMPARATORS						
	FB Regulation Level	Internal Reference Trip Point for Switch ON	1.2	1.225	1.25	V
	FB Overvoltage Threshold	Trip Point for Switch OFF		1.62		V
	FB Bias Current			60		nA
UNDERVOLTAGE SENSING FUNCTION						
	UV Threshold	UV Rising	1.19	1.225	1.26	V
	UV Hysteresis Input Current	UV = 2.5 V	–10	–20	–29	µA
	Remote Shutdown Threshold	Voltage at UVLO Falling	0.32	0.66		V
	Remote Shutdown Hysteresis			110		mV
THERMAL SHUTDOWN						
T_{sd}	Thermal Shutdown Temperature			165		°C
	Thermal Shutdown Hysteresis			20		°C

(1) All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) V_{CC} provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

6.6 Switching Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated. V_{IN} = 48 V unless otherwise stated.

		MIN	TYP	MAX	UNIT
ON-TIME GENERATOR					
T_{ON} Test 1	V_{IN} = 32 V, R_{ON} = 100 kΩ	270	350	460	ns
T_{ON} Test 2	V_{IN} = 48 V, R_{ON} = 100 kΩ	188	250	336	ns
T_{ON} Test 4	V_{IN} = 10 V, R_{ON} = 250 kΩ	1880	3200	4425	ns

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated. V_{IN} = 48 V unless otherwise stated.

		MIN	TYP	MAX	UNIT
MINIMUM OFF-TIME					
Minimum Off-Timer	FB = 0 V		144		ns

6.7 Typical Characteristics

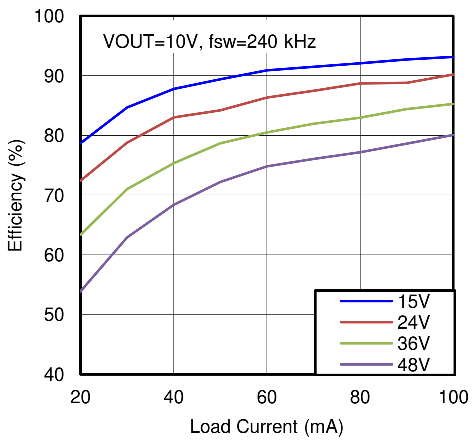


图 6-1. Efficiency at 240 kHz, 10 V

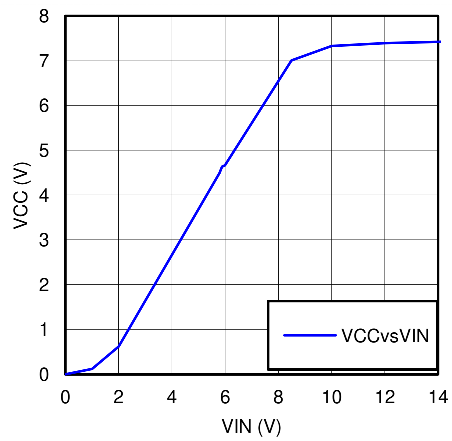


图 6-2. V_{CC} versus V_{IN}

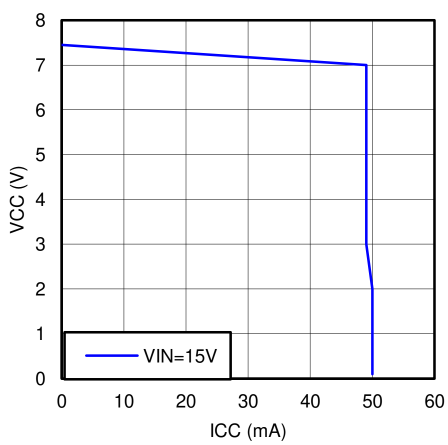


图 6-3. V_{CC} versus I_{CC}

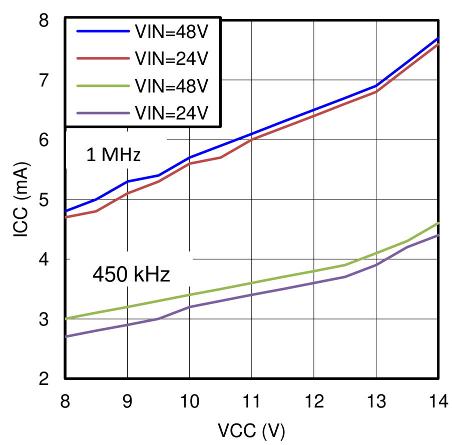


图 6-4. I_{CC} vs External V_{CC}

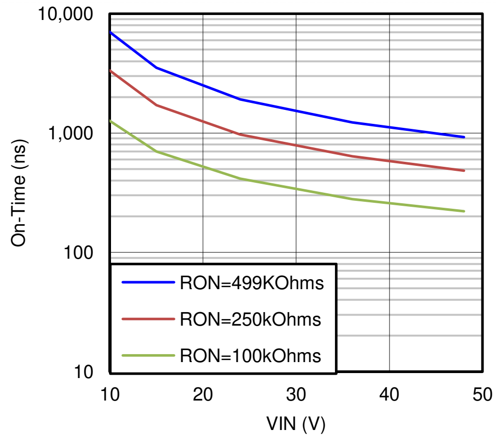


图 6-5. T_{ON} versus V_{IN} and R_{ON}

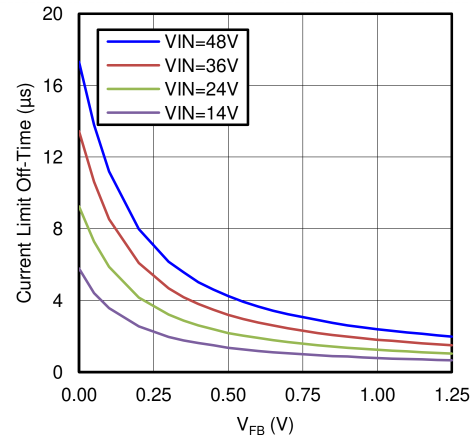


图 6-6. T_{OFF} (I_{LIM}) versus V_{FB} and V_{IN}

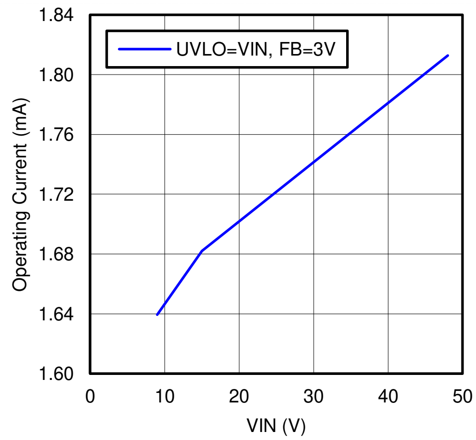


图 6-7. I_{IN} versus V_{IN} (Operating, Nonswitching)

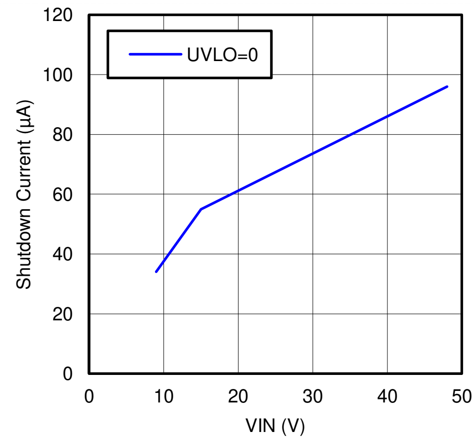


图 6-8. I_{IN} versus V_{IN} (Shutdown)

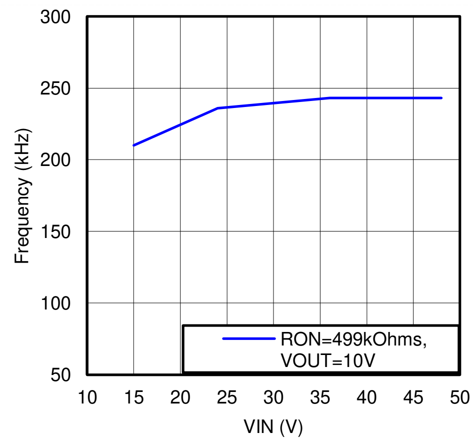


图 6-9. Switching Frequency versus V_{IN}

7 Detailed Description

7.1 Overview

The LM25019 step-down switching regulator features all the functions needed to implement a low-cost, efficient, buck converter that can supply up to 100 mA to the load. This high-voltage regulator contains 48-V, N-channel buck and synchronous switches, is easy to implement, and is provided in thermally-enhanced SO PowerPAD-8 and WSON-8 packages. The regulator operation is based on a constant on-time control scheme using an on-time inversely proportional to V_{IN}. This control scheme does not require loop compensation. The current limit is implemented with a forced off-time inversely proportional to V_{OUT}. This scheme ensures short circuit protection while providing minimum foldback. The simplified block diagram of the LM25019 device is shown in the 图 7-1.

The LM25019 device can be applied in numerous applications to efficiently regulate down higher voltages. This regulator is well suited for 12-V and 24-V rails. Protection features include: thermal shutdown, undervoltage lockout, minimum forced off-time, and an intelligent current limit.

7.2 Functional Block Diagram

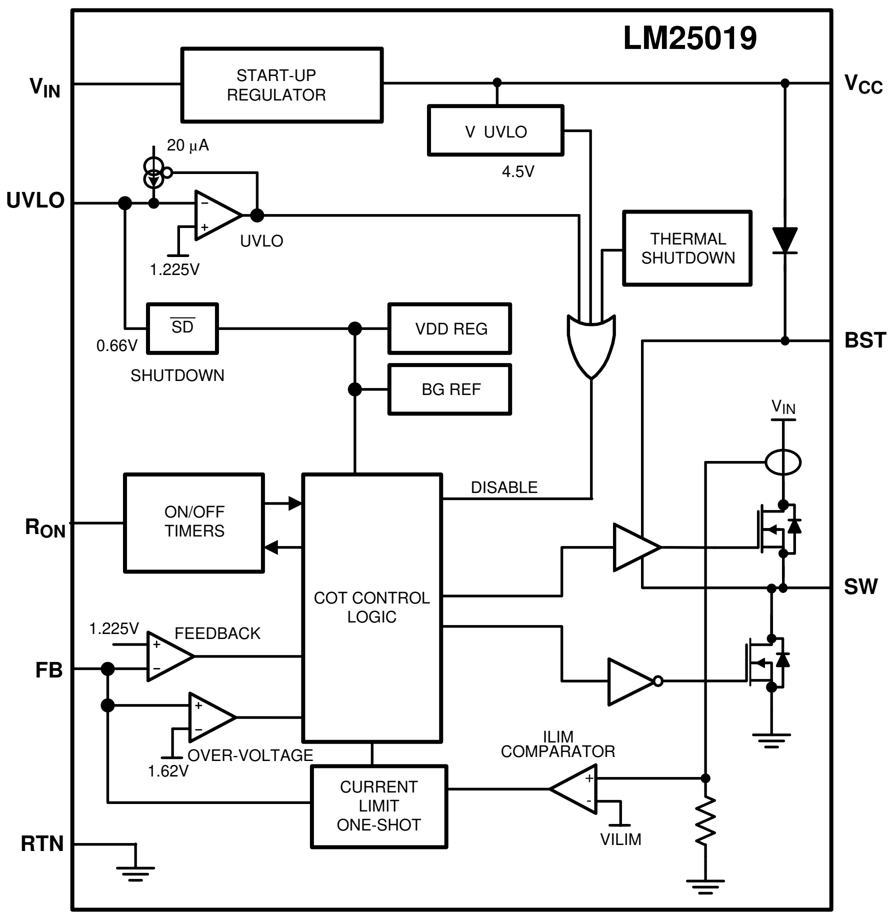


图 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Control Overview

The LM25019 buck regulator employs a control principle based on a comparator and a one-shot on-timer, with the output voltage feedback (FB) compared to an internal reference (1.225 V). If the FB voltage is below the reference, the internal buck switch is turned on for the one-shot timer period, which is a function of the input voltage and the programming resistor (R_{ON}). Following the on-time, the switch remains off until the FB voltage falls below the reference, but never before the minimum off-time forced by the minimum off-time one-shot timer.

When the FB pin voltage falls below the reference and the minimum off-time one-shot period expires, the buck switch is turned on for another on-time one-shot period. This continues until regulation is achieved and the FB voltage is approximately equal to 1.225 V (typ).

In a synchronous buck converter, the low-side (sync) FET is on when the high-side (buck) FET is off. The inductor current ramps up when the high-side switch is on and ramps down when the high-side switch is off. There is no diode emulation feature in this IC, and therefore, the inductor current can ramp in the negative direction at light load. This causes the converter to operate in continuous conduction mode (CCM) regardless of the output loading. The operating frequency remains relatively constant with load and line variations. The operating frequency can be calculated as shown in 方程式 1.

$$f_{SW} = \frac{V_{OUT}}{9 \times 10^{-11} \times R_{ON}} \tag{1}$$

The output voltage (V_{OUT}) is set by two external resistors (R_{FB1}, R_{FB2}). The regulated output voltage is calculated as shown in 方程式 2.

$$V_{OUT} = 1.225\text{V} \times \frac{R_{FB2} + R_{FB1}}{R_{FB1}} \tag{2}$$

This regulator regulates the output voltage based on ripple voltage at the feedback input, requiring a minimum amount of ESR for the output capacitor (C_{OUT}). A minimum of 25 mV of ripple voltage at the feedback pin (FB) is required for the LM25019. In cases where the capacitor ESR is too small, additional series resistance can be required (R_C in 图 7-2).

For applications where lower output voltage ripple is required the output can be taken directly from a low ESR output capacitor, as shown in 图 7-2. However, R_C slightly degrades the load regulation.

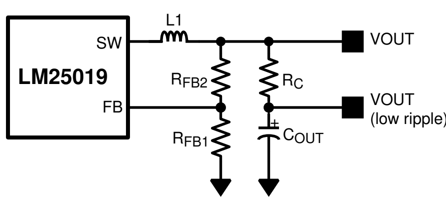


图 7-2. Low Ripple Output Configuration

7.3.2 V_{CC} Regulator

The LM25019 device contains an internal high-voltage linear regulator with a nominal output of 7.6 V. The input pin (V_{IN}) can be connected directly to the line voltages up to 48 V. The V_{CC} regulator is internally current limited to 30 mA. The regulator sources current into the external capacitor at V_{CC}. This regulator supplies current to internal circuit blocks including the synchronous MOSFET driver and the logic circuits. When the voltage on the V_{CC} pin reaches the UVLO threshold of 4.5 V, the IC is enabled.

The V_{CC} regulator contains an internal diode connection to the BST pin to replenish the charge in the gate drive boot capacitor when SW pin is low.

At high input voltages, the power dissipated in the high-voltage regulator is significant and can limit the overall achievable output power. As an example, with the input at 48 V and switching at high frequency, the V_{CC} regulator can supply up to 7 mA of current resulting in 48 V × 7 mA = 336 mW of power dissipation. If the V_{CC} voltage is driven externally by an alternate voltage source, between 8.55 V and 13 V, the internal regulator is disabled. This reduces the power dissipation in the IC.

7.3.3 Regulation Comparator

The feedback voltage at FB is compared to an internal 1.225 V reference. In normal operation, when the output voltage is in regulation, an on-time period is initiated when the voltage at FB falls below 1.225 V. The high-side switch stays on for the on-time, causing the FB voltage to rise above 1.225 V. After the on-time period, the high-side switch stays off until the FB voltage again falls below 1.225 V. During start-up, the FB voltage is below 1.225

V at the end of each on-time, causing the high-side switch to turn on immediately after the minimum forced off-time of 144 ns. The high-side switch can be turned off before the on-time is over if the peak current in the inductor reaches the current limit threshold.

7.3.4 Overvoltage Comparator

The feedback voltage at FB is compared to an internal 1.62-V reference. If the voltage at FB rises above 1.62 V, the on-time pulse is immediately terminated. This condition can occur if the input voltage, the output load, or both, changes suddenly. The high-side switch does not turn on again until the voltage at FB falls below 1.225 V.

7.3.5 On-Time Generator

The on-time for the LM25019 device is determined by the R_{ON} resistor, and is inversely proportional to the input voltage (V_{IN}), resulting in a nearly constant frequency as V_{IN} is varied over its range. The on-time equation for the LM25019 device is shown in 方程式 3.

$$T_{ON} = \frac{10^{-10} \times R_{ON}}{V_{IN}} \quad (3)$$

See 图 6-5. R_{ON} must be selected for a minimum on-time (at maximum V_{IN}) greater than 100 ns, for proper operation. This requirement limits the maximum switching frequency for high V_{IN}.

7.3.6 Current Limit

The LM25019 device contains an intelligent current limit off-timer. If the current in the buck switch exceeds 240 mA, the present cycle is immediately terminated, and a nonresetable off-timer is initiated. The length of off-time is controlled by the FB voltage and the input voltage V_{IN}. As an example, when FB = 0 V and V_{IN} = 48 V, the maximum off-time is set to 16 μs. This condition occurs when the output is shorted, and during the initial part of start-up. This amount of time ensures safe short circuit operation up to the maximum input voltage of 48 V.

In cases of overload where the FB voltage is above zero volts (not a short circuit), the current limit off-time is reduced. Reducing the off-time during less severe overloads reduces the amount of foldback, recovery time, and start-up time. The off-time is calculated from 方程式 4.

$$T_{OFF(ILIM)} = \frac{0.07 \text{ x } V_{IN}}{V_{FB} + 0.2V}\ \mu s \quad (4)$$

The current limit protection feature is peak limited. The maximum average output is less than the peak.

7.3.7 N-Channel Buck Switch and Driver

The LM25019 device integrates an N-Channel Buck switch and associated floating high-voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high-voltage diode. A 0.01-uF ceramic capacitor connected between the BST pin and the SW pin provides the voltage to the driver during the on-time. During each off-time, the SW pin is at approximately 0 V, and the bootstrap capacitor charges from V_{CC} through the internal diode. The minimum off-timer, set to 144 ns, ensures a minimum time each cycle to recharge the bootstrap capacitor.

7.3.8 Synchronous Rectifier

The LM25019 device provides an internal synchronous N-channel MOSFET rectifier. This MOSFET provides a path for the inductor current to flow when the high-side MOSFET is turned off.

The synchronous rectifier has no diode emulation mode, and is designed to keep the regulator in continuous conduction mode even during light loads which would otherwise result in discontinuous operation.

7.3.9 Undervoltage Detector

The LM25019 device contains a dual-level UVLO circuit. A summary of threshold voltages and operational states is provided in the *节 7.4*. When the UVLO pin voltage is below 0.66 V, the controller is in a low-current shutdown mode. When the UVLO pin voltage is greater than 0.66 V but less than 1.225 V, the controller is in standby mode. In standby mode, the V_{CC} bias regulator is active while the regulator output is disabled. When the V_{CC} pin exceeds the V_{CC} undervoltage threshold and the UVLO pin voltage is greater than 1.225 V, normal operation begins. An external set-point voltage divider from V_{IN} to GND can be used to set the minimum operating voltage of the regulator.

UVLO hysteresis is accomplished with an internal 20-µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to quickly raise the voltage at the UVLO pin. The hysteresis is equal to the value of this current times the resistance R_{UV2}.

If the UVLO pin is wired directly to the V_{IN} pin, the regulator begins operation once the V_{CC} undervoltage is satisfied.

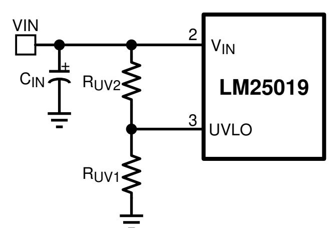


图 7-3. UVLO Resistor Setting

7.3.10 Thermal Protection

The LM25019 device must be operated so the junction temperature does not exceed 150°C during normal operation. An internal Thermal Shutdown circuit is provided to protect the LM25019 in the event of a higher than normal junction temperature. When activated, typically at 165°C, the controller is forced into a low-power reset state, disabling the buck switch and the V_{CC} regulator. This feature prevents catastrophic failures from accidental device overheating. When the junction temperature reduces below 145°C (typical hysteresis = 20°C), the V_{CC} regulator is enabled, and normal operation is resumed.

7.3.11 Ripple Configuration

The LM25019 uses Constant-On-Time (COT) control scheme where the on-time is terminated by an on-timer, and the off-time is terminated by the feedback voltage (V_{FB}) falling below the reference voltage (V_{REF}). Therefore, for stable operation, the feedback voltage must decrease monotonically, in phase with the inductor current during the off-time. Furthermore, this change in feedback voltage (V_{FB}) during off-time must be large enough to suppress any noise component present at the feedback node.

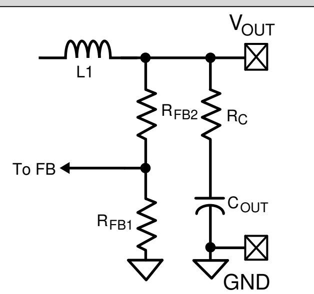
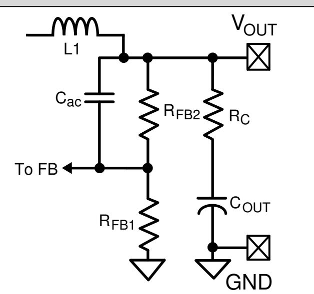
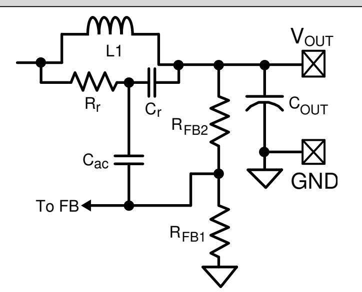
表 7-1 shows three different methods for generating appropriate voltage ripple at the feedback node. Type 1 and Type 2 ripple circuits couple the ripple at the output of the converter to the feedback node (FB). The output voltage ripple has two components:

1. Capacitive ripple caused by the inductor current ripple charging/discharging the output capacitor.
2. Resistive ripple caused by the inductor current ripple flowing through the ESR of the output capacitor.

The capacitive ripple is not in phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the off-time. The resistive ripple is in phase with the inductor current and decreases monotonically during the off-time. The resistive ripple must exceed the capacitive ripple at the output node (V_{OUT}) for stable operation. If this condition is not satisfied, unstable switching behavior is observed in COT converters, with multiple on-time bursts in close succession followed by a long off-time.

Type 3 ripple method uses R_r and C_r and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is ac coupled using C_{ac} to the feedback node (FB). Because this circuit does not use the output voltage ripple, it is ideally suited for applications where low output voltage ripple is required. See the *AN-1481 Controlling Output Ripple and Achieving ESR Independence in Constant On-Time (COT) Regulator Designs Application Report* for more details for each ripple generation method.

表 7-1. Ripple Configurations

<table>
<tr><th>TYPE 1
LOWEST COST CONFIGURATION</th><th>TYPE 2
REDUCED RIPPLE CONFIGURATION</th><th>TYPE 3
MINIMUM RIPPLE CONFIGURATION</th></tr>
<tr><td>
</td><td>
</td><td>
</td></tr>
<tr><td>$$R_C \ge \frac{25\text{ mV}}{\Delta I_{L(MIN)}} \times \frac{V_{OUT}}{V_{REF}} \quad (5)$$</td><td>$$C \ge \frac{5}{f_{sw}(R_{FB2}||R_{FB1})}$$ $$R_C \ge \frac{25\text{ mV}}{\Delta I_{L(MIN)}} \quad (6)$$</td><td>$$C_r = 3300\text{ pF}$$ $$C_{ac} = 100\text{ nF}$$ $$R_rC_r \le \frac{(V_{IN(MIN)} - V_{OUT}) \times T_{ON}}{25\text{ mV}} \quad (7)$$</td></tr>
</table>

7.3.12 Soft Start

A soft-start feature can be implemented with the LM25019 device using an external circuit. As shown in 图 7-4, the soft-start circuit consists of one capacitor C_1, two resistors, R_1 and R_2, and a diode, D. During the initial start-up, the VCC voltage is established before the V_{OUT} voltage. Capacitor C_1 is discharged and D is thereby forward biased. The FB voltage is pulled up above the reference voltage (1.225 V) and switching is thereby disabled. As capacitor C_1 charges, the voltage at node B gradually decreases and switching commences. V_{OUT} gradually rises to maintain the FB voltage at the reference voltage. Once the voltage at node B is less than a diode drop above the FB voltage, the soft-start sequence is finished and D is reverse-biased.

During the initial part of the start-up, the FB voltage can be approximated as shown in 方程式 8.

$$V_{FB} = (VCC - V_D) \times \frac{R_{FB1} \times R_{FB2}}{R_2 \times (R_{FB1} + R_{FB2}) + R_{FB1} \times R_{FB2}} \tag{8}$$

C1 is charged after the first start-up. Diode D1 is optional and can be added to discharge C1 and initialize the soft-start sequence when the input voltage experiences a momentary drop.

To achieve the desired soft start, the following design guidance is recommended:

1. R_2 is selected so that V_{FB} is higher than 1.225 V for a V_{CC} of 4.5 V, but is lower than 5 V when V_{CC} is 8.55 V. If an external V_{CC} is used, V_{FB} must not exceed 5 V at maximum V_{CC}.
2. C_1 is selected to achieve the desired start-up time that can be determined from 方程式 9.

$$t_S = C_1 \times (R_2 + \frac{R_{FB1} \times R_{FB2}}{R_{FB1} + R_{FB2}}) \tag{9}$$

3. R_1 is used to maintain the node B voltage at zero after the soft start is finished. A value larger than the feedback resistor divider is preferred. The effect of resistor R1 is ignored in 方程式 9.

With component values from the applications schematic shown in 图 8-1, selecting C_1 = 1 μF, R_2 = 1 kΩ, and R_1 = 30 kΩ results in a soft-start time of about 2 ms.

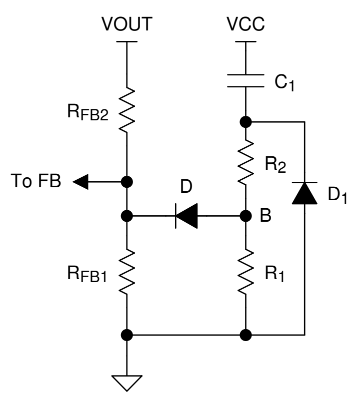


图 7-4. Soft-Start Circuit

7.4 Device Functional Modes

The UVLO pin controls the operating mode of the LM25019 device (see 表 7-2 for the detailed functional states).

表 7-2. UVLO Mode

UVLO	V_{CC}	MODE	DESCRIPTION
< 0.66 V	Disabled	Shutdown	V_{CC} regulator disabled. Switching disabled
0.66 V – 1.225 V	Enabled	Standby	V_{CC} regulator enabled Switching disabled
> 1.225 V	V_{CC} < 4.5 V	Standby	V_{CC} regulator enabled. Switching disabled
	V_{CC} > 4.5 V	Operating	V_{CC} enabled. Switching enabled

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LM25019 device is step-down DC-DC converter. The device is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 650 mA. Use the following design procedure to select component values for the LM25019 device. Alternately, use the WEBENCH® software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The application schematic of a buck supply is shown in 图 8-1. For output voltage (V_{OUT}) more than one diode drop higher than the maximum regulation voltage of V_{CC} (8.55 V, see the *节 6.5*), the V_{CC} pin can be connected to V_{OUT} through a diode (D2), as shown in 图 8-1, to improve efficiency and reduce power dissipation in the IC.

The design example shown in 图 8-1 uses equations from the *节 7.3* with component names provided in the *图 3-1* schematic. Corresponding component designators from 图 8-1 are also provided for each selected value.

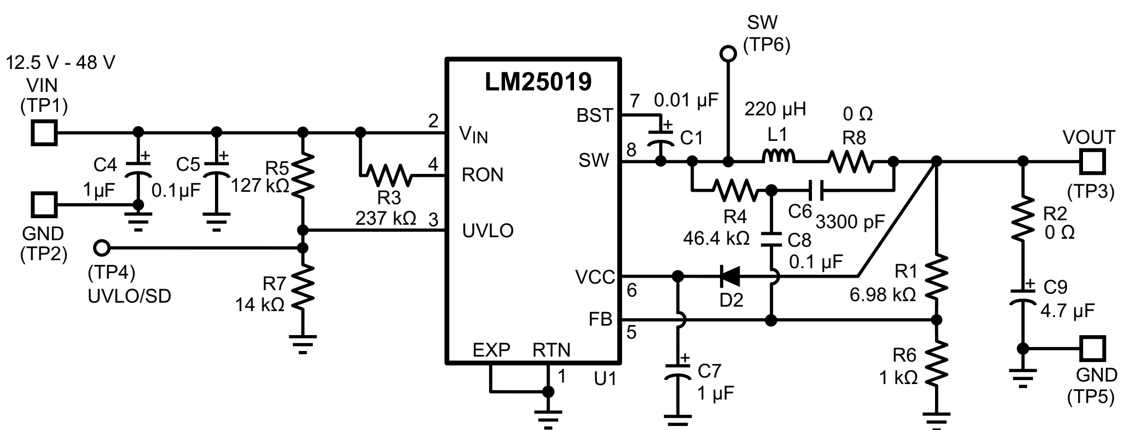


图 8-1. Final Schematic for 12.5-V to 48-V Input, and 10-V, 100-mA Output Buck Converter

8.2.1 Design Requirements

DESIGN PARAMETERS	VALUE
Input Range	12.5 V to 48 V
Output Voltage	10 V
Maximum Output Current	100 mA
Nominal Switching Frequency	≈ 440 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 RFB1, RFB2

$V_{OUT} = V_{FB} \times (R_{FB2} / R_{FB1} + 1)$, and because V_{FB} = 1.225 V, the ratio of R_{FB2} to R_{FB1} calculates as 7:1. Standard values are chosen with R_{FB2} = R1 = 6.98 kΩ and R_{FB1} = R6 = 1.00 kΩ. Other values can be used as long as the 7:1 ratio is maintained.

8.2.2.2 Frequency Selection

At the minimum input voltage, the maximum switching frequency of the LM25019 is restricted by the forced minimum off-time ($T_{OFF(MIN)}$) as shown in 方程式 10.

$$f_{SW(MAX)} = \frac{1 - D_{MAX}}{T_{OFF(MIN)}} = \frac{1 - 10/12.5}{200\ \text{ns}} = 1\ \text{MHz} \tag{10}$$

Similarly, at maximum input voltage, the maximum switching frequency of the LM25019 is restricted by the minimum T_{ON} as shown in 方程式 11.

$$f_{SW(MAX)} = \frac{D_{MIN}}{T_{ON(MIN)}} = \frac{10/48}{100\ \text{ns}} = 2.1\ \text{MHz} \tag{11}$$

Resistor R_{ON} sets the nominal switching frequency based on 方程式 12.

$$f_{SW} = \frac{V_{OUT}}{K \times R_{ON}} \tag{12}$$

where

- $K = 9 \times 10^{-11}$

Operation at high switching frequency results in lower efficiency while providing the smallest solution. Using 440 kHz as the target swtiching frequency, the calculated valued of R_{ON} is 253 kΩ. The standard value for R_{ON} = R3 = 237 kΩ is selected.

8.2.2.3 Inductor Selection

The inductance selection is a compromise between solution size, output ripple, and efficiency. The peak inductor current at maximum load current must be smaller than the minimum current limit of 150 mA. The maximum permissible peak to peak inductor ripple is determined by 方程式 13.

$$\Delta IL = 2 \times (I_{LIM(min)} - I_{OUT(max)}) = 2 \times 50 = 100\ \text{mA} \tag{13}$$

The minimum inductance is determined by 方程式 14.

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L1 \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \tag{14}$$

Using the maximum V_{IN} of 48 V, the calculation from 方程式 14 results in L = 179 μH. A standard value of 220 μH is selected. For proper operation, the inductor saturation current must be higher than the peak current encountered in the application. For robust short circuit protection, the inductor saturation current must be higher than the maximum current limit of 300 mA.

8.2.2.4 Output Capacitor

The output capacitor is selected to minimize the capacitive ripple across it. The maximum ripple is observed at maximum input voltage and is shown in 方程式 15.

$$C_{OUT} = \frac{\Delta I_L}{8 \times f_{sw} \times \Delta V_{ripple}} \tag{15}$$

where

- ΔV_{ripple} is the voltage ripple across the capacitor
- ΔI_L is calculated using 方程式 14

Substituting ΔV_{ripple} = 5 mV gives C_{OUT} = 4.65 µF. A 4.7-µF standard value is selected for C_{OUT} =C9. An X5R or X7R type capacitor with a voltage rating 16 V or higher must be selected.

8.2.2.5 Type III Ripple Circuit

Type III ripple circuit as described in the *节 7.3.11* section is chosen for this example. For a constant on-time converter to be stable, the injected in-phase ripple must be larger than the capacitive ripple on C_{OUT}.

Using type III ripple circuit equations, the target ripple must be greater than the capacitive ripple generated at the primary output.

C_r = C6 = 3300 pF

C_{ac} = C8 = 100 nF

$$R_r \le \frac{(V_{IN(MIN)} - V_{OUT}) \times T_{ON(VINMIN)}}{(25\,mV \times C_r)} \quad (16)$$

For T_{ON}, refer to 方程式 3.

Ripple resistor R_r is calculated to be 57.6 kΩ. This value provides the minimum ripple for stable operation. A smaller resistance should be selected to allow for variations in T_{ON}, C_{OUT}, and other components. R_r = R4 = 46.4 kΩ is selected for this example application.

8.2.2.6 V_{CC} and Bootstrap Capacitor

The V_{CC} capacitor provides charge to bootstrap capacitor as well as internal circuitry and low-side gate driver. The bootstrap capacitor provides charge to high-side gate driver. The recommended value for C_{VCC} = C7 is 1-µF. A good value for C_{BST} = C1 is 0.01 µF.

8.2.2.7 Input Capacitor

The input capacitor should be large enough to limit the input voltage ripple and can be calculated using 方程式 17.

$$C_{IN} \ge \frac{I_{OUT(MAX)}}{4 \times f_{SW} \times \Delta V_{IN}} \quad (17)$$

Choosing a ΔV_{IN} = 0.5 V gives a minimum C_{IN} = 0.12 µF. A standard value of 1 µF is selected for C_{IN} = C4. The input capacitor should be rated for the maximum input voltage under all conditions. A 50-V, X7R dielectric should be selected for this design.

The input capacitor should be placed directly across V_{IN} and RTN (pin 2 and 1) of the IC. If it is not possible to place all of the input capacitor close to the IC, a 0.1-µF capacitor should be placed near the IC to provide a bypass path for the high-frequency component of the switching current. This helps limit the switching noise.

8.2.2.8 UVLO Resistors

The UVLO resistors R_{UV1} and R_{UV2} set the UVLO threshold and hysteresis according to 方程式 18 and 方程式 19.

$$V_{IN}(HYS) = I_{HYS} \times R_{UV2} \quad (18)$$

$$V_{IN}\,(UVLO,rising) = 1.225V \times \left(\frac{R_{UV2}}{R_{UV1}} + 1\right) \quad (19)$$

where

- I_{HYS} = 20 µA

Selecting UVLO hysteresis of 2.5 V and UVLO rising threshold of 12 V results in R_{UV1} = 14.53 kΩ and R_{UV2} = 125 kΩ. Selecting a standard value of R_{UV1} = R7 = 14 kΩ and R_{UV2} = R5 = 127 kΩ results in UVLO thresholds and hysteresis of 12.5 V to 2.5 V, respectively.

8.2.3 Application Curves

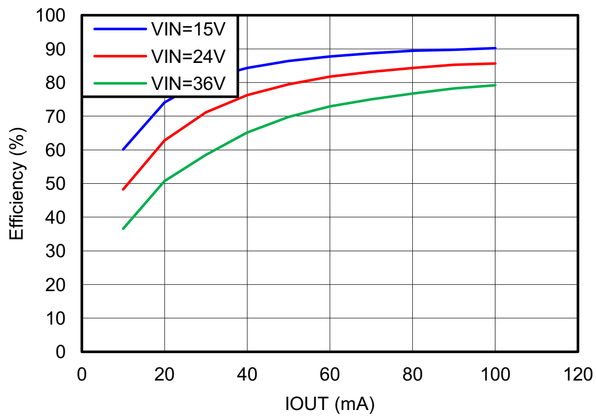


图 8-2. Efficiency versus Load Current

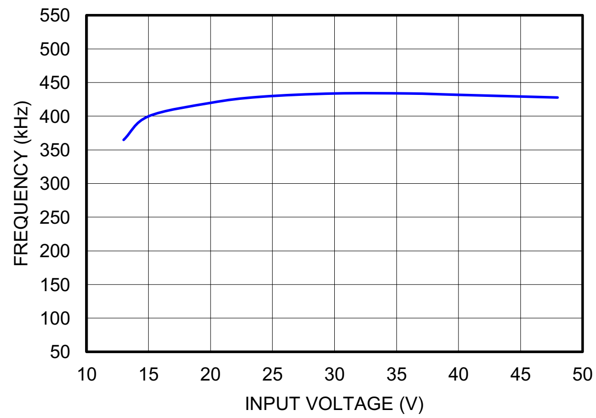


图 8-3. Frequency versus Input Voltage (I_{OUT} = 100 mA)

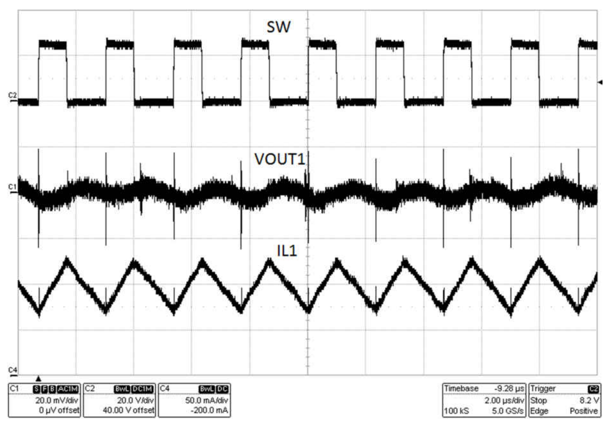


图 8-4. Typical Switching Waveform (V_{IN} = 24 V, I_{OUT} = 100 mA)

9 Power Supply Recommendations

The LM25019 is a power-management device. The power supply for the device is any DC voltage source within the specified input range.

10 Layout

10.1 Layout Guidelines

A proper layout is essential for optimum performance of the circuit. In particular, the following guidelines should be observed:

1. C_{IN}: The loop consisting of input capacitor (C_{IN}), V_{IN} pin, and RTN pin carries switching currents. Therefore, the input capacitor must be placed close to the IC, directly across V_{IN} and RTN pins and the connections to these two pins should be direct to minimize the loop area. In general it is not possible to accommodate all of input capacitance near the IC. A good practice is to use a 0.1-µF or 0.47-µF capacitor directly across the V_{IN} and RTN pins close to the IC, and the remaining bulk capacitor as close as possible (see 图 10-1).
2. C_{VCC} and C_{BST}: The V_{CC} and bootstrap (BST) bypass capacitors supply switching currents to the high-side and low-side gate drivers. These two capacitors must also be placed as close to the IC as possible, and the connecting trace length and loop area should be minimized (see 图 10-1).
3. The feedback trace carries the output voltage information and a small ripple component that is necessary for proper operation of the LM25019. Therefore, take care while routing the feedback trace to avoid coupling any noise to this pin. In particular, feedback trace must not run close to magnetic components, or parallel to any other switching trace.
4. SW trace: The SW node switches rapidly between V_{IN} and GND every cycle is therefore a possible source of noise. The SW node area should be minimized. In particular, the SW node must not be inadvertently connected to a copper plane or pour.

10.2 Layout Example

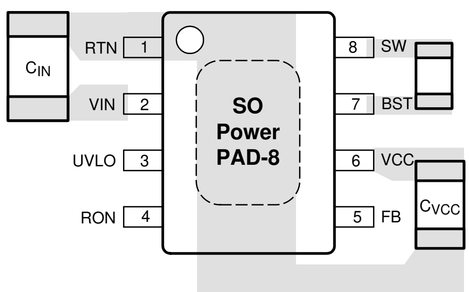


图 10-1. Placement of Bypass Capacitors

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- Texas Instruments, *AN-1481 Controlling Output Ripple and Achieving ESR Independence in Constant On-Time (COT) Regulator Designs*
- Texas Instruments, *AN-2292 Designing an Isolated Buck (Flybuck) Converter*
- Texas Instruments, *LM25019 Isolated Evaluation Board*

11.2 接收文档更新通知

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要声明和免责声明

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM25019MR/NOPB	Active	Production	SO PowerPAD (DDA) | 8	95 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 125	L25019 MR
LM25019MR/NOPB.A	Active	Production	SO PowerPAD (DDA) | 8	95 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 125	L25019 MR
LM25019MRE/NOPB	Active	Production	SO PowerPAD (DDA) | 8	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L25019 MR
LM25019MRE/NOPB.A	Active	Production	SO PowerPAD (DDA) | 8	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L25019 MR
LM25019MRX/NOPB	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L25019 MR
LM25019MRX/NOPB.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L25019 MR
LM25019SD/NOPB	Active	Production	WSON (NGU) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25019
LM25019SD/NOPB.A	Active	Production	WSON (NGU) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25019
LM25019SDE/NOPB	Active	Production	WSON (NGU) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25019
LM25019SDE/NOPB.A	Active	Production	WSON (NGU) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25019
LM25019SDX/NOPB	Active	Production	WSON (NGU) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25019
LM25019SDX/NOPB.A	Active	Production	WSON (NGU) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25019

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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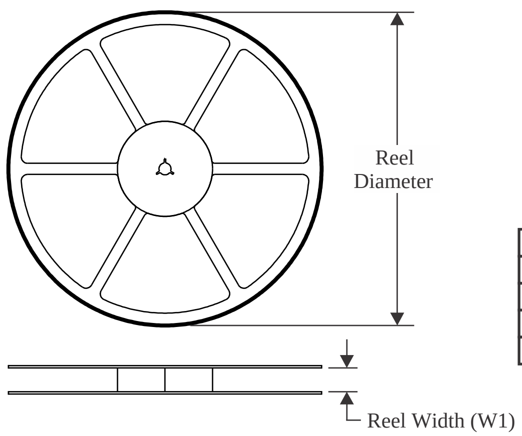
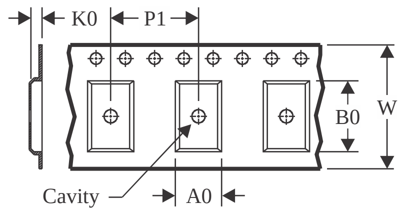
TAPE AND REEL INFORMATION

REEL DIMENSIONS

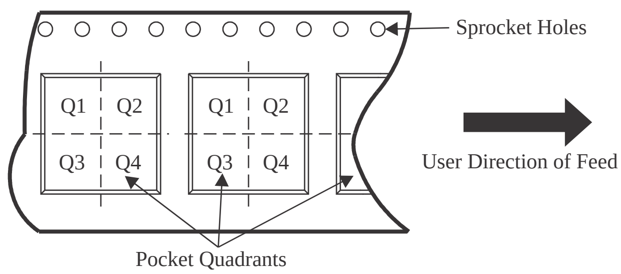


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

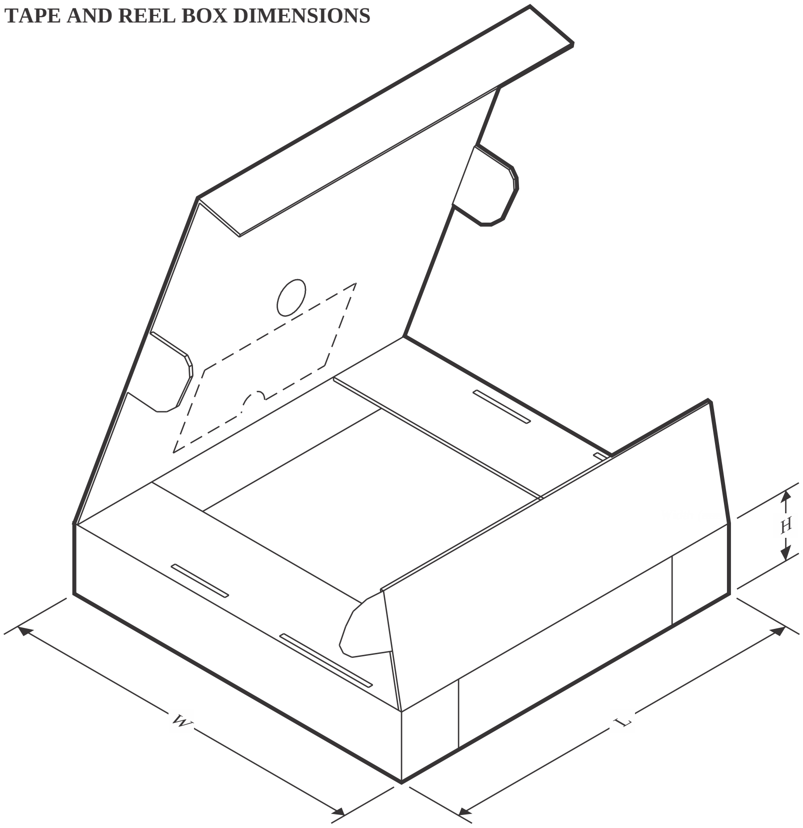
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25019MRE/NOPB	SO PowerPAD	DDA	8	250	177.8	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM25019MRX/NOPB	SO PowerPAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM25019SD/NOPB	WSON	NGU	8	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25019SDE/NOPB	WSON	NGU	8	250	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25019SDX/NOPB	WSON	NGU	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

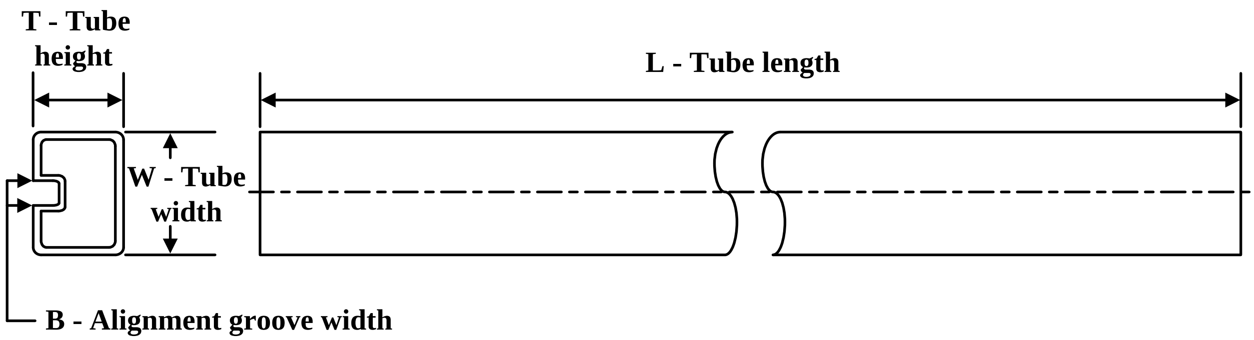
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

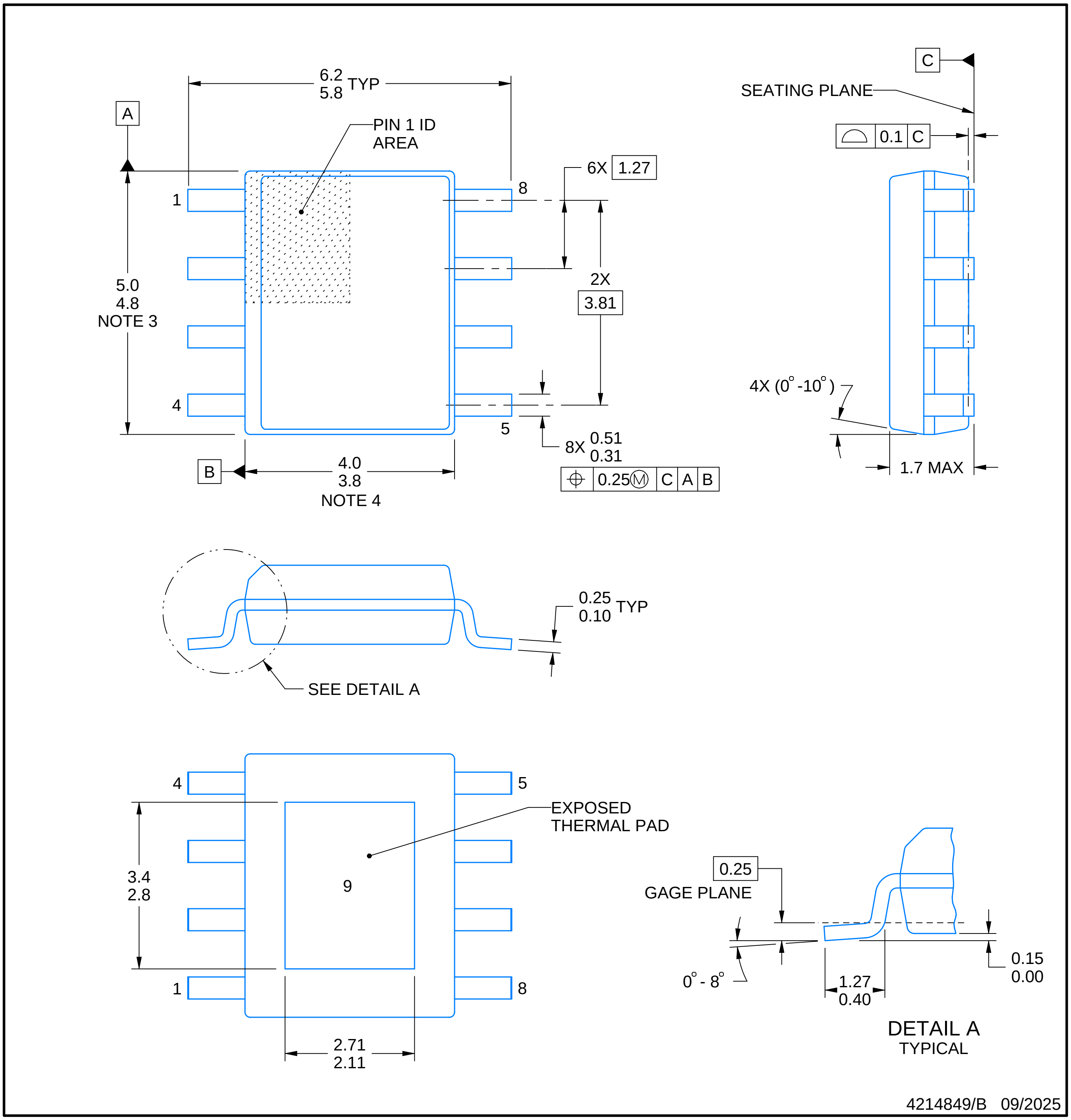
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25019MRE/NOPB	SO PowerPAD	DDA	8	250	208.0	191.0	35.0
LM25019MRX/NOPB	SO PowerPAD	DDA	8	2500	356.0	356.0	36.0
LM25019SD/NOPB	WSON	NGU	8	1000	210.0	185.0	35.0
LM25019SDE/NOPB	WSON	NGU	8	250	210.0	185.0	35.0
LM25019SDX/NOPB	WSON	NGU	8	4500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

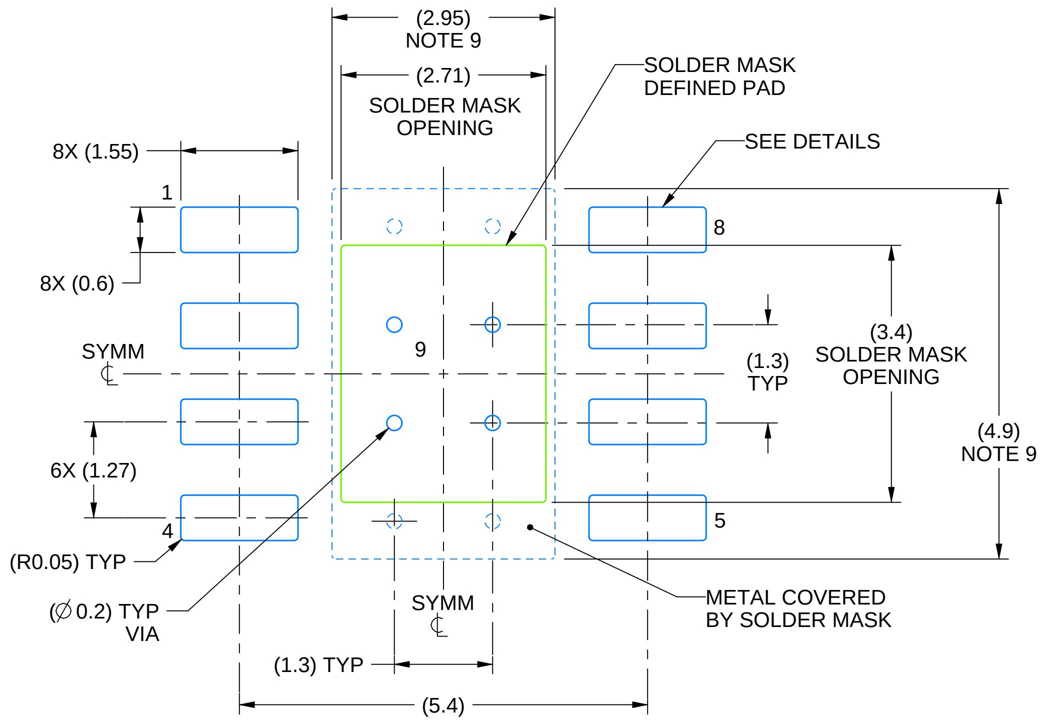
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM25019MR/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05
LM25019MR/NOPB.A	DDA	HSOIC	8	95	495	8	4064	3.05



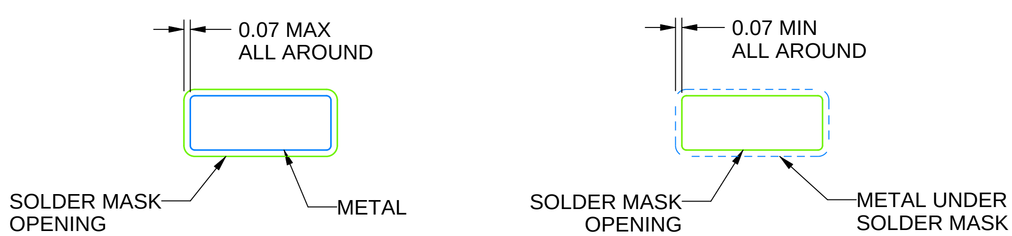
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS
PADS 1-8

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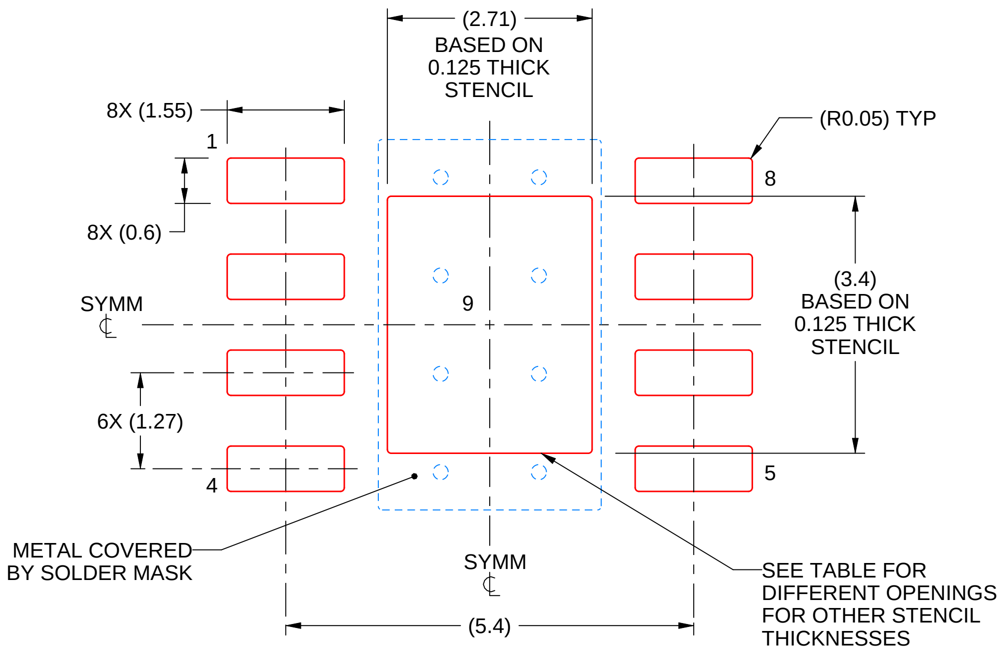
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

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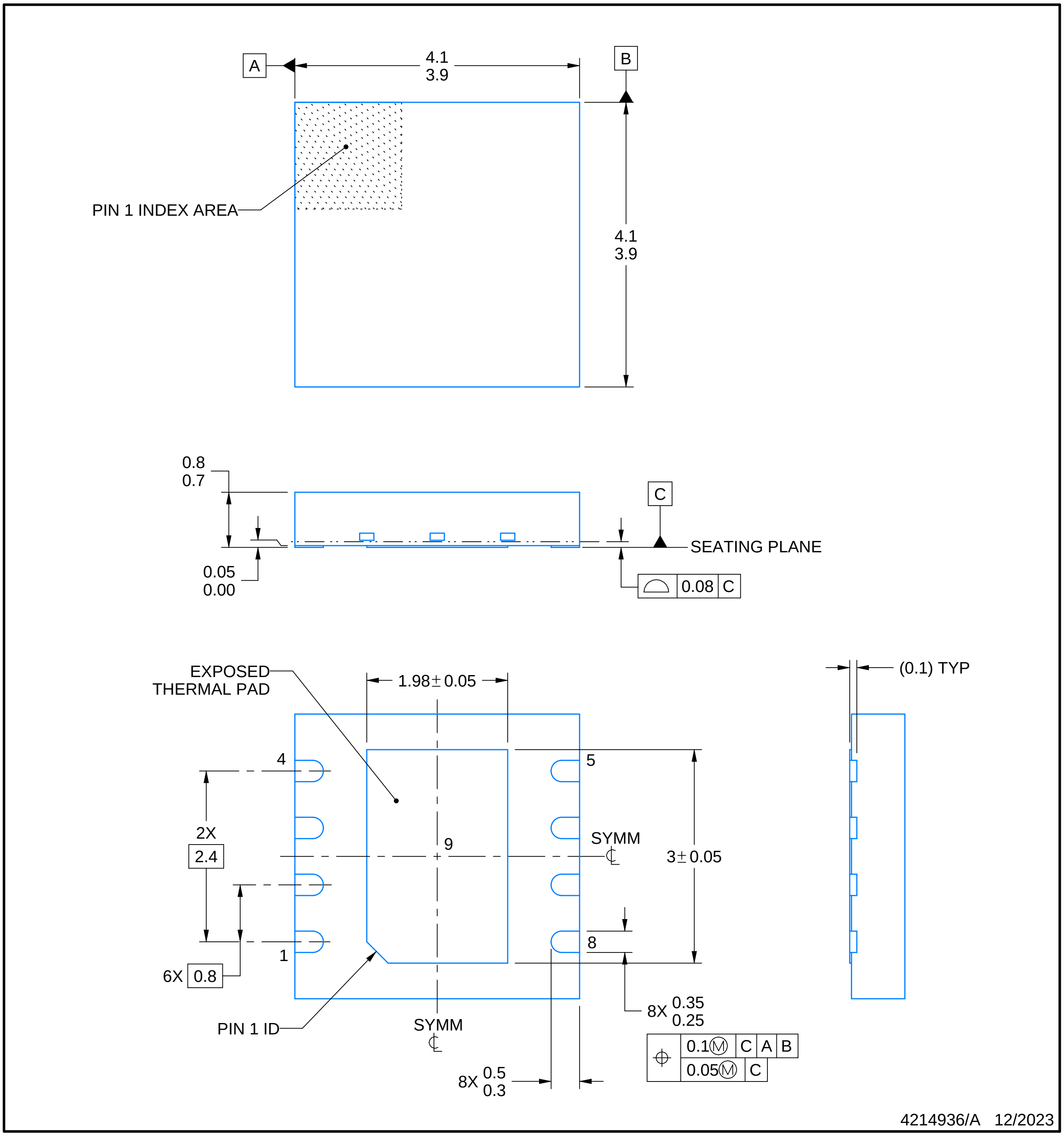
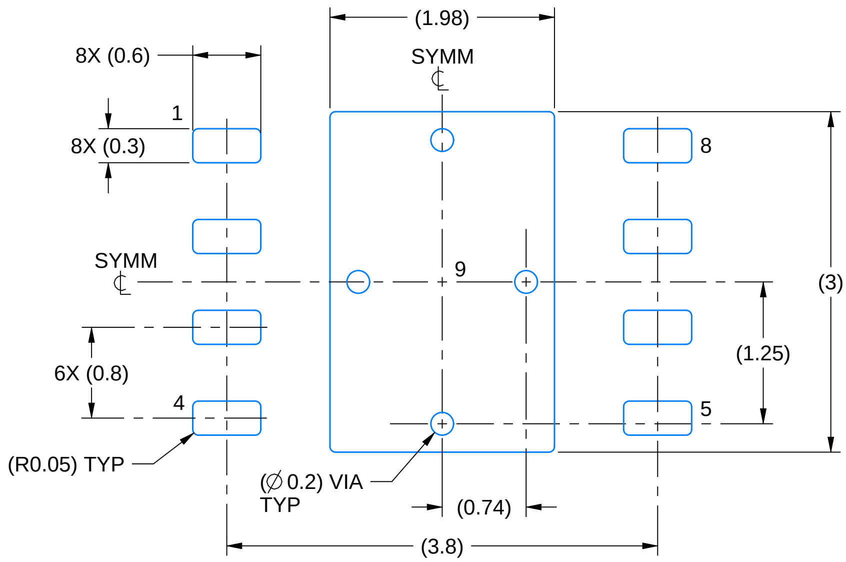
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

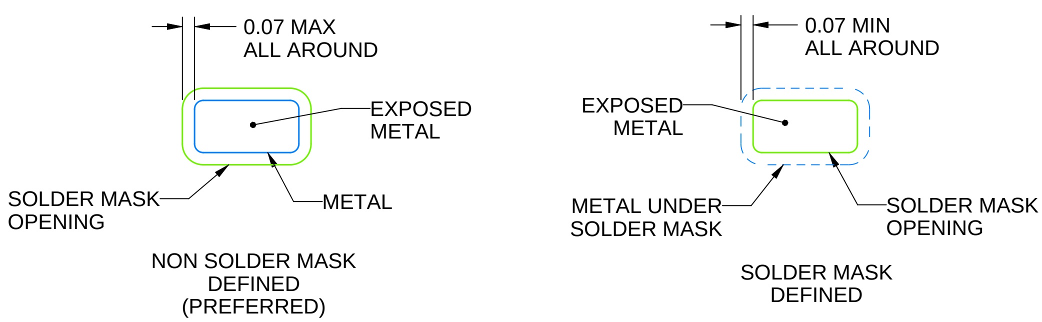


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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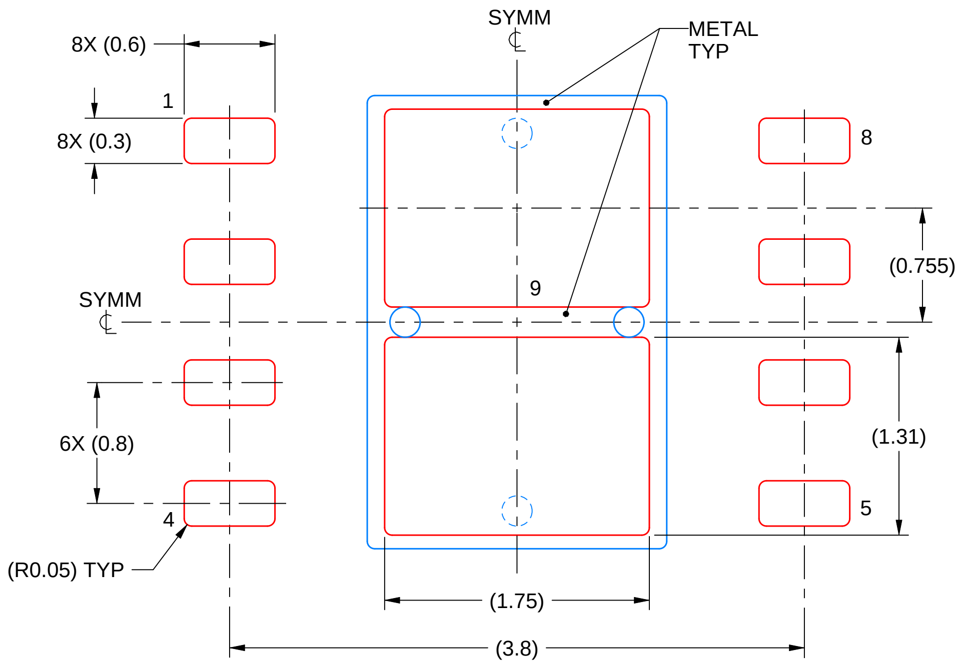
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月