LM266x Switched Capacitor Voltage Converter

1 Features

- Inverts or Doubles Input Supply Voltage
- 3.5-Ω Typical Output Resistance
- 86% Typical Conversion Efficiency at 200 mA
- (LM2662) Selectable Oscillator Frequency: 20 kHz/150 kHz
- (LM2663) Low Current Shutdown Mode

2 Applications

- Laptop Computers
- Cellular Phones
- Medical Instruments
- Operational Amplifier Power Supplies
- Interface Power Supplies
- Handheld Instruments

3 Description

The LM2662/LM2663 CMOS charge-pump voltage converter inverts a positive voltage in the range of 1.5 V to 5.5 V to the corresponding negative voltage. The LM2662/LM2663 uses two low cost capacitors to provide 200 mA of output current without the cost, size, and EMI related to inductor based converters. With an operating current of only 300 µA and operating efficiency greater than 90% at most loads, the LM2662/LM2663 provides ideal performance for battery powered systems. The LM2662/LM2663 may also be used as a positive voltage doubler.

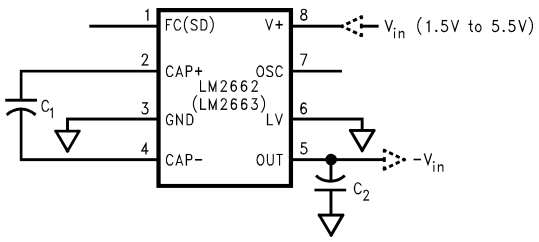
The oscillator frequency can be lowered by adding an external capacitor to the OSC pin. Also, the OSC pin may be used to drive the LM2662/LM2663 with an external clock. For LM2662, a frequency control (FC) pin selects the oscillator frequency of 20 kHz or 150 kHz. For LM2663, an external shutdown (SD) pin replaces the FC pin. The SD pin can be used to disable the device and reduce the quiescent current to 10 µA. The oscillator frequency for LM2663 is 150 kHz.

Device Information(1)

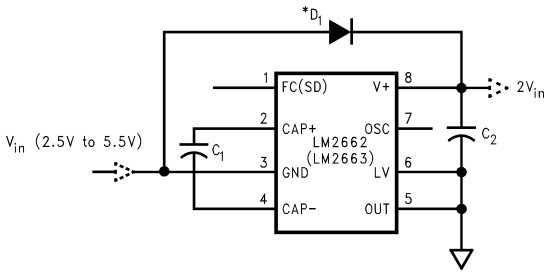
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2662	SOIC (8)	4.90 mm x 3.91 mm
LM2663		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Voltage Inverter

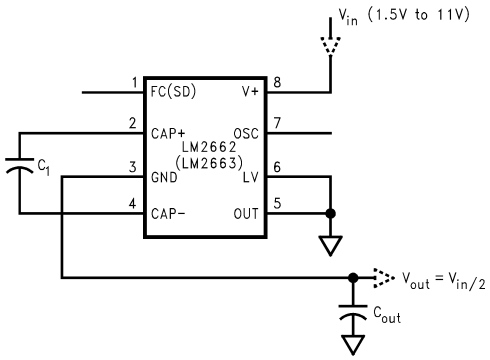


Positive Voltage Doubler



* Please see *Positive Voltage Doubler* section regarding choice of D1.

Splitting V_{IN} in Half



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2013) to Revision E — **Page**

- Added *Device Information* and *Handling Rating* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; moved some curves to *Application Curves* section ... 1

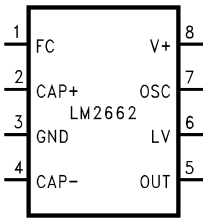
Changes from Revision C (May 2013) to Revision D — **Page**

- Changed layout of National Data Sheet to TI format ... 15

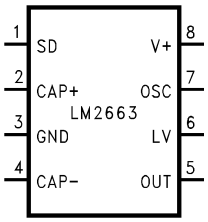
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5 Pin Configuration and Functions

8 Pins
LM2662 SOIC (D)
Top View



8 Pins
LM2663 SOIC (D)
Top View



Pin Functions

PIN		TYPE	DESCRIPTION	
NUMBER	NAME		VOLTAGE INVERTER	VOLTAGE DOUBLER
1	FC (LM2662)	Input	Frequency control for internal oscillator: FC = open, f_{OSC} = 20 kHz (typ); FC = V+, f_{OSC} = 150 kHz (typ); FC has no effect when OSC pin is driven externally.	Same as inverter.
1	SD (LM2663)	Input	Shutdown control pin, tie this pin to the ground in normal operation.	Same as inverter.
2	CAP+	Power	Connect this pin to the positive terminal of charge-pump capacitor.	Same as inverter.
3	GND	Ground	Power supply ground input.	Power supply positive voltage input.
4	CAP−	Power	Connect this pin to the negative terminal of charge-pump capacitor.	Same as inverter.
5	OUT	Power	Negative voltage output.	Power supply ground input.
6	LV	Input	Low-voltage operation input. Tie LV to GND when input voltage is less than 3.5 V. Above 3.5 V, LV can be connected to GND or left open. When driving OSC with an external clock, LV must be connected to GND.	LV must be tied to OUT.
7	OSC	Input	Oscillator control input. OSC is connected to an internal 15-pF capacitor. An external capacitor can be connected to slow the oscillator. Also, an external clock can be used to drive OSC.	Same as inverter except that OSC cannot be driven by an external clock.
8	V+	Power Input	Power supply positive voltage input.	Positive voltage output.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Supply voltage (V+ to GND, or GND to OUT)		6	V
LV	(OUT − 0.3 V)	(GND + 3 V)	
FC, OSC, SD	The least negative of (OUT − 0.3 V) or (V+ − 6 V) to (V+ + 0.3 V)		
V+ and OUT continuous output current		250	
Output short-circuit duration to GND(3)		1	sec.
Power dissipation (T_A = 25°C)(4)		735	mW
T_J max(4)		150	°C
Operating ambient temperature	−40	85	
Operating junction temperature	−40	105	
Lead temperature (soldering, 10 seconds)		300	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) OUT may be shorted to GND for one second without damage. However, shorting OUT to V+ may damage the device and should be avoided. Also, for temperatures above 85°C, OUT must not be shorted to GND or V+, or device may be damaged.
(4) The maximum allowable power dissipation is calculated by using $P_{DMax} = (T_{JMax} - T_A)/R_{\theta JA}$, where T_{JMax} is the maximum junction temperature, T_A is the ambient temperature, and $R_{\theta JA}$ is the junction-to-ambient thermal resistance of the specified package.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V+ (supply voltage)	2.5		5.5	V
Junction temperature (T_J)	–40		105	°C
Ambient temperature (T_J)	–40		85	

6.4 Thermal Information

THERMAL METRIC(1)		LM2662	LM2663	UNIT
		SOIC (D)		
		8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	170	170	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Unless otherwise specified: V+ = 5 V, FC = Open, $C_1 = C_2 = 47$ µF.(1)

PARAMETER		TEST CONDITION		MIN(2)	TYP(3)	MAX(2)	UNIT
V+	Supply Voltage	R_L = 1k	Inverter, LV = Open	3.5		5.5	V
			Inverter, LV = GND	1.5		5.5	
			Doubler, LV = OUT	2.5		5.5	
I_Q	Supply Current	No Load LV = Open	FC = V+ (LM2662)		1.3	4	mA
			SD = Ground (LM2663)				
			FC = Open		0.3	0.8	
I_{SD}	Shutdown Supply Current (LM2663)				10		µA
V_{SD}	Shutdown Pin Input Voltage (LM2663)	Shutdown Mode		2	(4)		V
		Normal Operation				0.3	
I_L	Output Current			200			mA
R_{OUT}	Output Resistance(5)	I_L = 200 mA			3.5	7	Ω
f_{OSC}	Oscillator Frequency(6)	OSC = Open	FC = Open	7	20		kHz
			FC = V+	55	150		
f_{SW}	Switching Frequency(7)	OSC = Open	FC = Open	3.5	10		kHz
			FC = V+	27.5	75		
I_{OSC}	OSC Input Current	FC = Open			±2		µA
		FC = V+			±10		
P_{EFF}	Power Efficiency	R_L (500) between V^+ and OUT		90%	96%		
		I_L = 200 mA to GND			86%		
V_{OEFF}	Voltage Conversion Efficiency	No Load		99%	99.96%		

(1) In the test circuit, capacitors C_1 and C_2 are 47-µF, 0.2-Ω maximum ESR capacitors. Capacitors with higher ESR will increase output resistance, reduce output voltage and efficiency.
(2) –40°C to 105°C
(3) T_J = 25°C
(4) In doubling mode, when $V_{out} > 5$ V, minimum input high for shutdown equals $V_{out} - 3$ V.
(5) Specified output resistance includes internal switch resistance and capacitor ESR.
(6) For LM2663, the oscillator frequency is 150 kHz.
(7) The output switches operate at one half of the oscillator frequency, $f_{OSC} = 2f_{SW}$.

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6.6 Typical Performance Characteristics

(Circuit of Figure 14 and Figure 15)

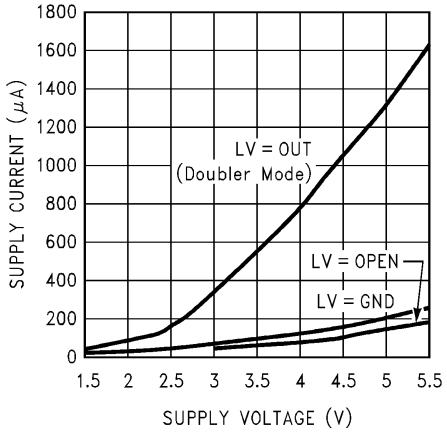


Figure 1. Supply Current vs Supply Voltage

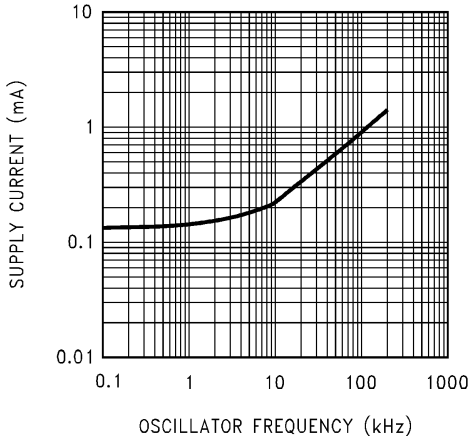


Figure 2. Supply Current vs Oscillator Frequency

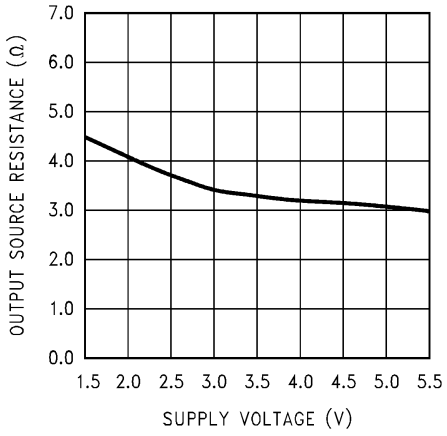


Figure 3. Output Source Resistance vs Supply Voltage

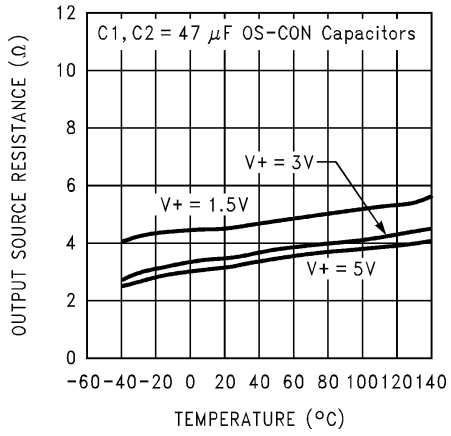


Figure 4. Output Source Resistance vs Temperature

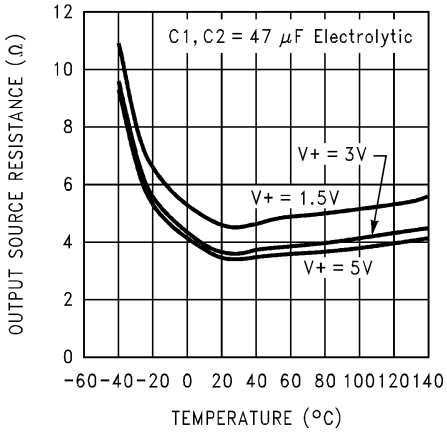


Figure 5. Output Source Resistance vs Temperature

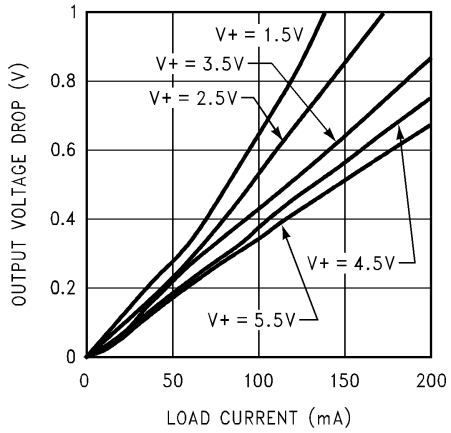


Figure 6. Output Voltage Drop vs Load Current

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Typical Performance Characteristics (continued)

(Circuit of Figure 14 and Figure 15)

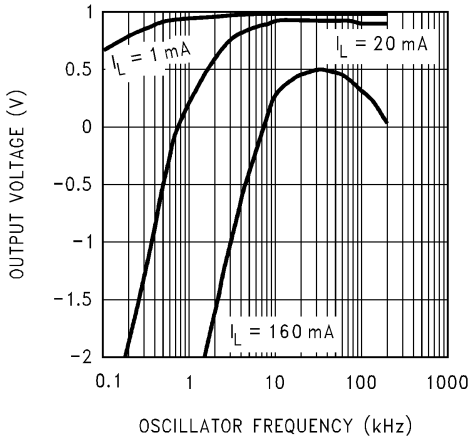


Figure 7. Output Voltage vs Oscillator Frequency

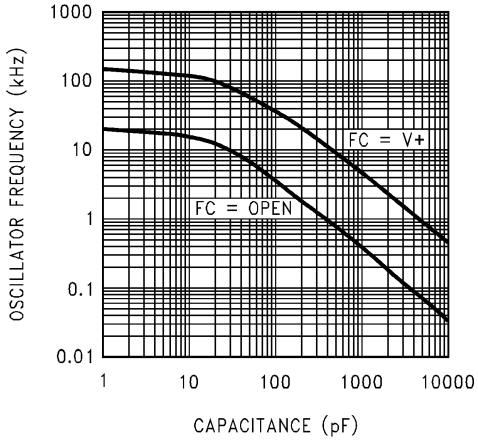


Figure 8. Oscillator Frequency vs External Capacitance

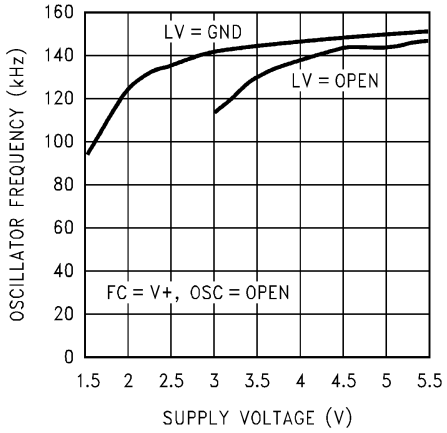


Figure 9. Oscillator Frequency vs Supply Voltage

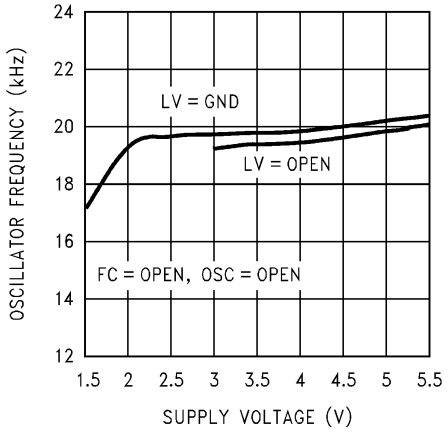


Figure 10. Oscillator Frequency vs Supply Voltage

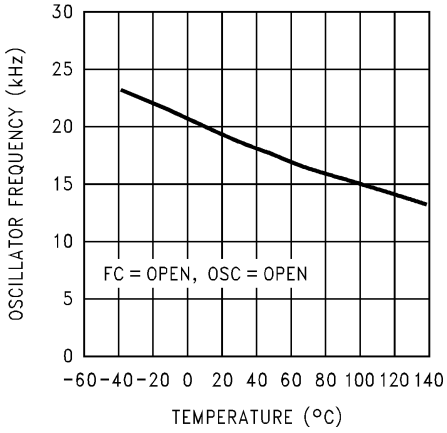


Figure 11. Oscillator Frequency vs Temperatur

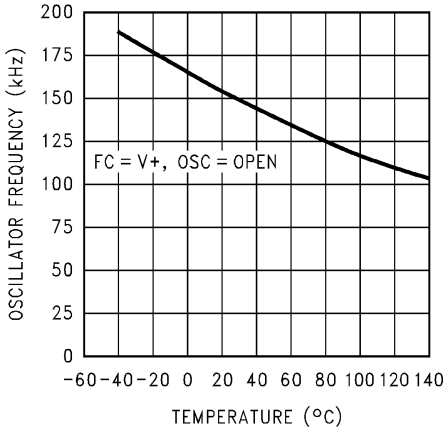


Figure 12. Oscillator Frequency vs Temperature

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Typical Performance Characteristics (continued)

(Circuit of Figure 14 and Figure 15)

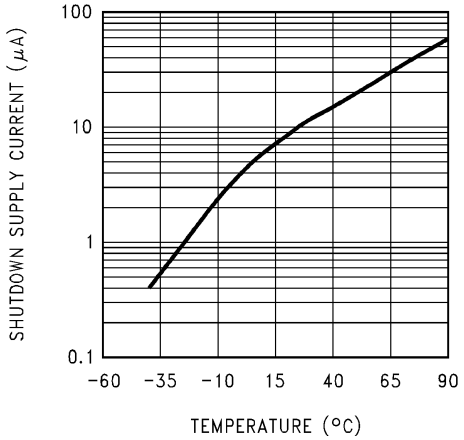


Figure 13. Shutdown Supply Current vs Temperature (LM2663 Only)

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7 Parameter Measurement Information

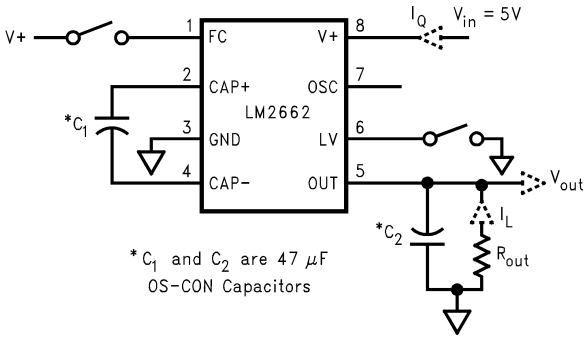


Figure 14. LM2662 Test Circuit

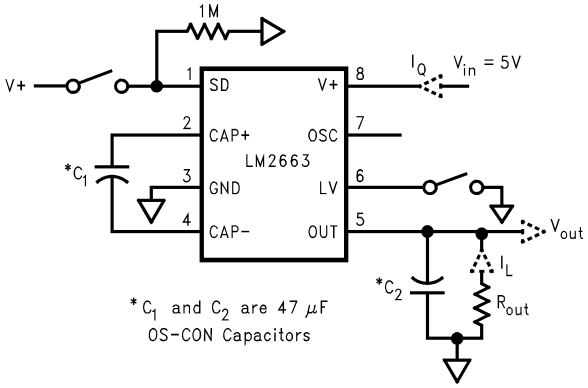


Figure 15. LM2663 Test Circuit

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8 Detailed Description

8.1 Overview

The LM2662/LM2663 contains four large CMOS switches which are switched in a sequence to invert the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 16 illustrates the voltage conversion scheme. When S_1 and S_3 are closed, C_1 charges to the supply voltage V+. During this time interval switches S_2 and S_4 are open. In the second time interval, S_1 and S_3 are open and S_2 and S_4 are closed, C_1 is charging C_2. After a number of cycles, the voltage across C_2 will be pumped to V+. Since the anode of C_2 is connected to ground, the output at the cathode of C_2 equals −(V+) assuming no load on C_2, no loss in the switches, and no ESR in the capacitors. In reality, the charge transfer efficiency depends on the switching frequency, the on-resistance of the switches, and the ESR of the capacitors.

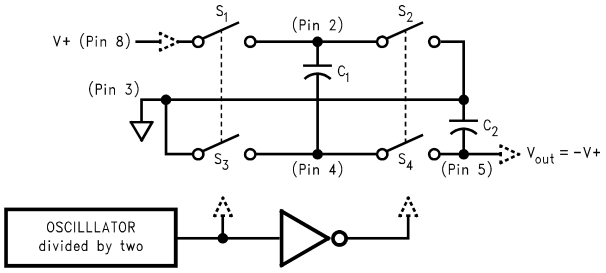
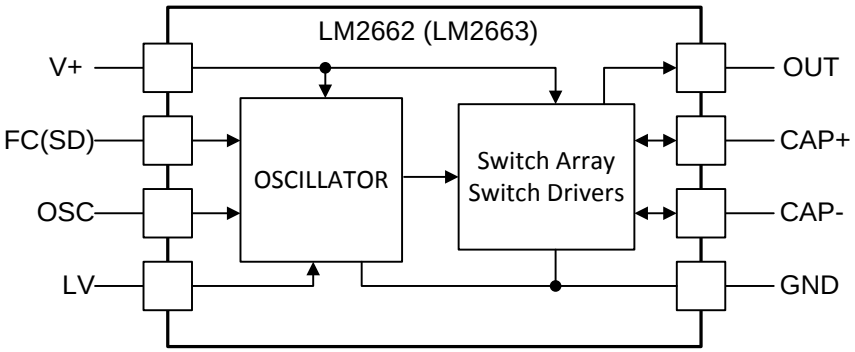


Figure 16. Voltage Inverting Principle

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Changing Oscillator Frequency

For the LM2662, the internal oscillator frequency can be selected using the Frequency Control (FC) pin. When FC is open, the oscillator frequency is 20 kHz; when FC is connected to V+, the frequency increases to 150 kHz. A higher oscillator frequency allows smaller capacitors to be used for equivalent output resistance and ripple, but increases the typical supply current from 0.3 mA to 1.3 mA.

The oscillator frequency can be lowered by adding an external capacitor between OSC and GND (See typical performance characteristics). Also, in the inverter mode, an external clock that swings within 100 mV of V+ and GND can be used to drive OSC. Any CMOS logic gate is suitable for driving OSC. LV must be grounded when driving OSC. The maximum external clock frequency is limited to 150 kHz.

The switching frequency of the converter (also called the charge pump frequency) is half of the oscillator frequency.

NOTE

OSC cannot be driven by an external clock in the voltage-doubling mode.

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Feature Description (continued)

Table 1. LM2662 Oscillator Frequency Selection

FC	OSC	OSCILLATOR
Open	Open	20 kHz
V+	Open	150 kHz
Open or V+	External Capacitor	See Typical Performance Characteristics
N/A	External Clock **(inverter mode only)**	External Clock Frequency

Table 2. LM2663 Oscillator Frequency Selection

OSC	OSCILLATOR
Open	150 kHz
External Capacitor	See Typical Performance Characteristics
External Clock **(inverter mode only)**	External Clock Frequency

8.4 Device Functional Modes

8.4.1 Shutdown Mode

For the LM2663, a shutdown (SD) pin is available to disable the device and reduce the quiescent current to 10 µA. Applying a voltage greater than 2 V to the SD pin will bring the device into shutdown mode. While in normal operating mode, the SD pin is connected to ground.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM2662/LM2663 CMOS charge-pump voltage converter inverts a positive voltage in the range of 1.5 V to 5.5 V to the corresponding negative voltage. The LM2662/LM2663 uses two low cost capacitors to provide 200 mA of output current without the cost, size, and EMI related to inductor based converters. With an operating current of only 300 µA and operating efficiency greater than 90% at most loads, the LM2662/LM2663 provides ideal performance for battery powered systems. The LM2662/LM2663 may also be used as a positive voltage doubler.

9.2 Typical Applications

9.2.1 Simple Negative Voltage Converter

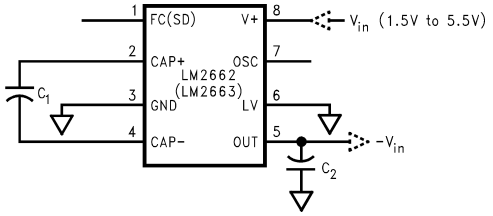


Figure 17. Simple Negative Voltage Converter

9.2.1.1 Design Requirements

The main application of LM2662/LM2663 is to generate a negative supply voltage. The voltage inverter circuit uses only two external capacitors as shown in Figure 17. The range of the input supply voltage is 1.5 V to 5.5 V. For a supply voltage less than 3.5 V, the LV pin must be connected to ground to bypass the internal regulator circuitry. This gives the best performance in low voltage applications. If the supply voltage is greater than 3.5 V, LV may be connected to ground or left open. The choice of leaving LV open simplifies the direct substitution of the LM2662/LM2663 for the LMC7660 Switched Capacitor Voltage Converter.

9.2.1.2 Detailed Design Procedure

The output characteristics of this circuit can be approximated by an ideal voltage source in series with a resistor. The voltage source equals −(V+). The output resistance R_{out} is a function of the ON resistance of the internal MOS switches, the oscillator frequency, and the capacitance and ESR of C_1 and C_2. Since the switching current charging and discharging C_1 is approximately twice as the output current, the effect of the ESR of the pumping capacitor C_1 is multiplied by four in the output resistance. The output capacitor C_2 is charging and discharging at a current approximately equal to the output current, therefore, its ESR only counts once in the output resistance. A good approximation is:

$$R_{out} \cong 2R_{SW} + \frac{2}{f_{osc} \times C_1} + 4\,ESR_{C1} + ESR_{C2} \quad (1)$$

where R_{SW} is the sum of the ON resistance of the internal MOS switches shown in the Voltage Inverting Principle.

High value, low ESR capacitors will reduce the output resistance. Instead of increasing the capacitance, the oscillator frequency can be increased to reduce the $2/(f_{osc} \times C_1)$ term. Once this term is trivial compared with R_{SW} and ESRs, further increasing in oscillator frequency and capacitance will become ineffective.

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Typical Applications (continued)

The peak-to-peak output voltage ripple is determined by the oscillator frequency, and the capacitance and ESR of the output capacitor C_2:

$$V_{ripple} = \frac{I_L}{f_{osc} \times C_2} + 2 \times I_L \times ESR_{C2} \quad (2)$$

Again, using a low ESR capacitor will result in lower ripple.

9.2.1.2.1 Paralleling Devices

Any number of LM2662 devicess (or LM2663 devices) can be paralleled to reduce the output resistance. Each device must have its own pumping capacitor C_1, while only one output capacitor C_{out} is needed as shown in Figure 18. The composite output resistance is:

$$R_{out} = \frac{R_{out} \text{ of each LM2662 (or LM2663)}}{\text{Number of Devices}} \quad (3)$$

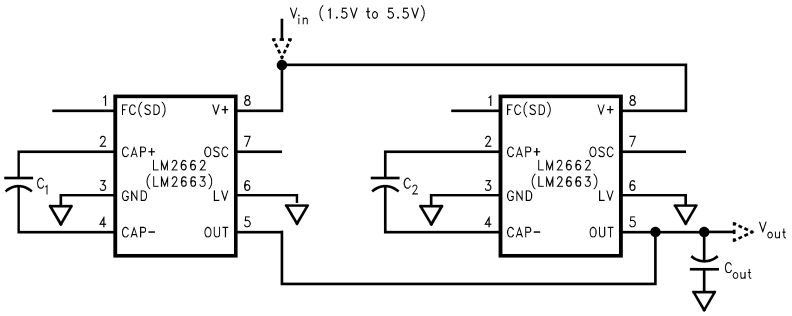


Figure 18. Lowering Output Resistance by Paralleling Devices

9.2.1.2.2 Cascading Devices

Cascading the LM2662 devices (or LM2663 devices) is an easy way to produce a greater negative voltage (as shown in Figure 19). If *n* is the integer representing the number of devices cascaded, the unloaded output voltage V_{out} is ($-nV_{in}$). The effective output resistance is equal to the weighted sum of each individual device:

$$R_{out} = nR_{out_1} + \frac{n}{2}R_{out_2} + \ldots + R_{out_n} \quad (4)$$

A three-stage cascade circuit shown in Figure 20 generates −3 V_{in}, from V_{in}.

Cascading is also possible when devices are operating in doubling mode. In Figure 21, two devices are cascaded to generate 3 V_{in}.

An example of using the circuit in Figure 20 or Figure 21 is generating +15 V or −15 V from a +5-V input.

Note that, the number of *n* is practically limited since the increasing of n significantly reduces the efficiency and increases the output resistance and output voltage ripple.

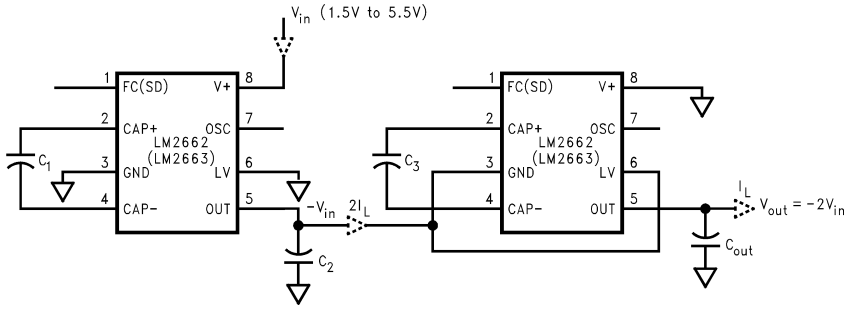


Figure 19. Increasing Output Voltage by Cascading Devices

Typical Applications (continued)

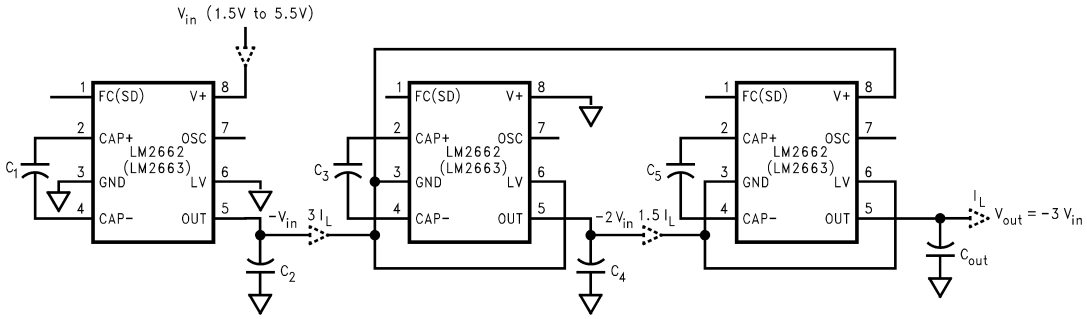


Figure 20. Generating −3 V_{IN} From +V_{IN}

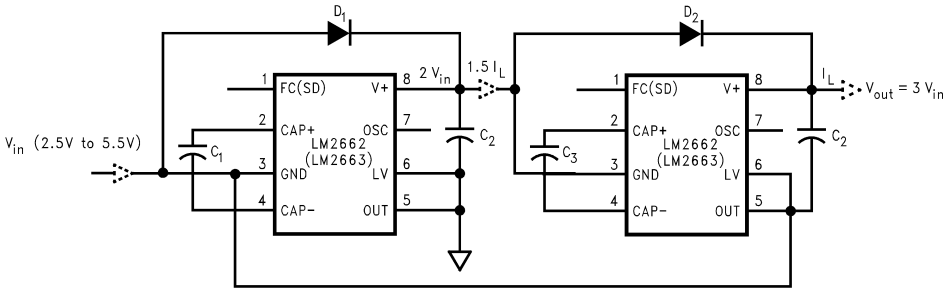


Figure 21. Generating +3 V_{IN} From +V_{IN}

9.2.1.2.3 Regulating V_{OUT}

It is possible to regulate the output of the LM2662/LM2663 by use of a low dropout regulator (such as LP2986). The whole converter is depicted in Figure 22. This converter can give a regulated output from −1.5 V to −5.5 V by choosing the proper resistor ratio:

$$V_{out} = V_{ref}\left(1 + \frac{R_1}{100k}\right)$$

where

- $V_{ref} = 1.23V$ (5)

The error flag on pin 7 of the LP2986 goes low when the regulated output at pin 5 drops by about 5% below nominal. The LP2986 can be shutdown by taking pin 8 low. The less than 1 µA quiescent current in the shutdown mode is favorable for battery powered applications.

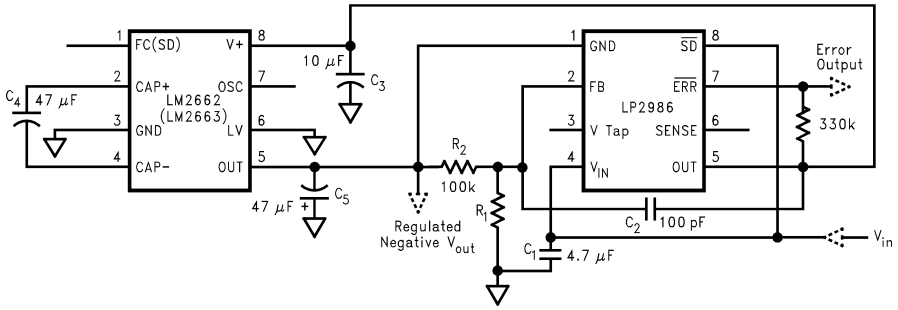


Figure 22. Combining LM2662/LM2663 With LP2986 to Make a Negative Adjustable Regulator

Also, as shown in Figure 23 by operating the LM2662/LM2663 in voltage doubling mode and adding a low dropout regulator (such as LP2986) at the output, we can get +5 V output from an input as low as +3.3 V.

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Typical Applications (continued)

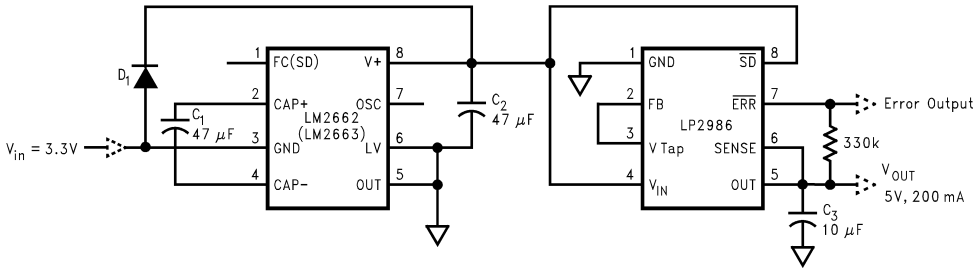


Figure 23. Generating +5 V From +3.3 V Input Voltage

9.2.1.3 Application Curves

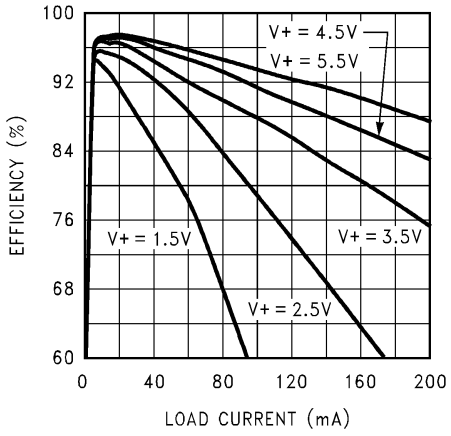


Figure 24. Efficiency vs Load Current

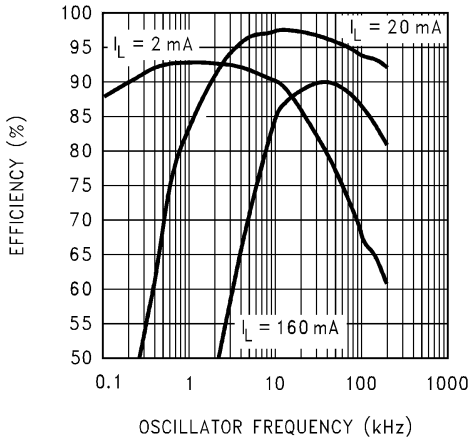


Figure 25. Efficiency vs Oscillator Frequency

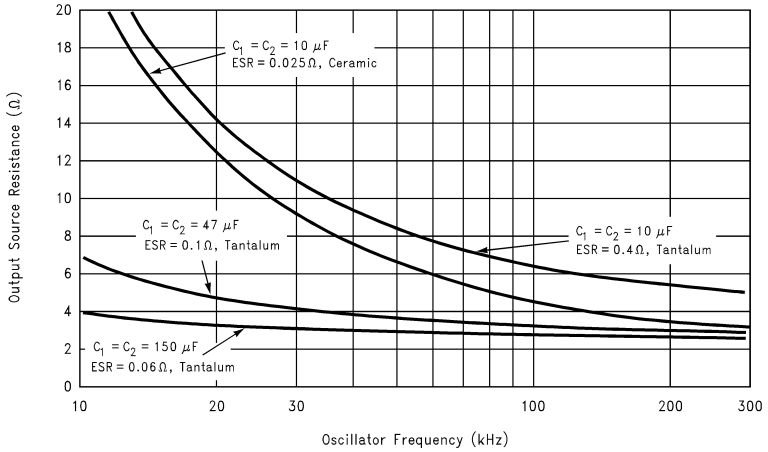


Figure 26. Output Source Resistance vs Oscillator Frequency

Typical Applications (continued)

9.2.2 Positive Voltage Doubler

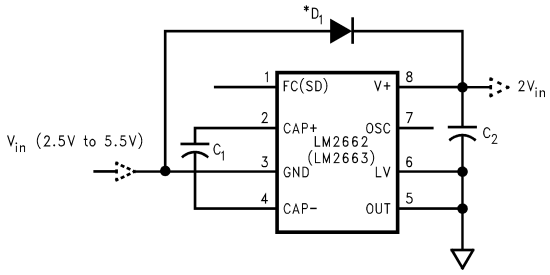


Figure 27. Positive Voltage Doubler

9.2.2.1 Design Requirements

The LM2662/LM2663 can operate as a positive voltage doubler (as shown in Figure 27). The doubling function is achieved by reversing some of the connections to the device.

9.2.2.2 Detailed Design Procedure

The input voltage is applied to the GND pin with an allowable voltage from 2.5 V to 5.5 V. The V+ pin is used as the output. The LV pin and OUT pin must be connected to ground. The OSC pin can not be driven by an external clock in this operation mode. The unloaded output voltage is twice of the input voltage and is not reduced by the diode D_1's forward drop.

The Schottky diode D_1 is only needed for start-up. The internal oscillator circuit uses the V+ pin and the LV pin (connected to ground in the voltage doubler circuit) as its power rails. Voltage across V+ and LV must be larger than 1.5 V to insure the operation of the oscillator. During start-up, D_1 is used to charge up the voltage at V+ pin to start the oscillator; also, it protects the device from turning-on its own parasitic diode and potentially latching-up. Therefore, the Schottky diode D_1 should have enough current carrying capability to charge the output capacitor at start-up, as well as a low forward voltage to prevent the internal parasitic diode from turning-on. A Schottky diode like 1N5817 can be used for most applications. If the input voltage ramp is less than 10 V/ms, a smaller Schottky diode like MBR0520LT1 can be used to reduce the circuit size.

9.2.2.3 Application Curves

See *Application Curves* section.

9.2.3 Splitting V_{IN} in Half

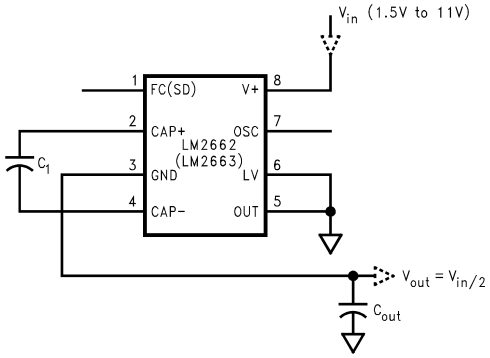


Figure 28. Splitting V_{IN} in Half

9.2.3.1 Design Requirements

Another interesting application shown in Figure 28 is using the LM2662/LM2663 as a precision voltage divider. Since the off-voltage across each switch equals $V_{IN}/2$, the input voltage can be raised to +11 V.

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Typical Applications (continued)

9.2.3.2 Detailed Design Procedure

As discussed in the *Simple Negative Voltage Converter* section, the output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. The output voltage drop is the load current times the output resistance, and the power efficiency is

$$\eta = \frac{P_{out}}{P_{in}} = \frac{I_L^2 R_L}{I_L^2 R_L + I_L^2 R_{out} + I_Q (V+)} \quad (6)$$

Where $I_Q(V+)$ is the quiescent power loss of the IC device, and $I_L^2 R_{OUT}$ is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs.

Low ESR capacitors are recommended for both capacitors to maximize efficiency, reduce the output voltage drop and voltage ripple. For convenience, C_1 and C_2 are usually chosen to be the same.

The output resistance varies with the oscillator frequency and the capacitors. In Figure 26, the output resistance vs. oscillator frequency curves are drawn for four difference capacitor values. At very low frequency range, capacitance plays the most important role in determining the output resistance. Once the frequency is increased to some point (such as 100 kHz for the 47-µF capacitors), the output resistance is dominated by the ON resistance of the internal switches and the ESRs of the external capacitors. A low value, smaller size capacitor usually has a higher ESR compared with a bigger size capacitor of the same type. Ceramic capacitors can be chosen for their lower ESR. As shown in Figure 26, in higher frequency range, the output resistance using the 10-µF ceramic capacitors is close to these using higher value tantalum capacitors.

9.2.3.3 Application Curves

See *Application Curves* section.

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10 Power Supply Recommendations

The LM2662/LM2663 is designed to operate from as an inverter over an input voltage supply range between 1.5 V and 5.5 V when the LV pin is grounded. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the LM2662/LM2663 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

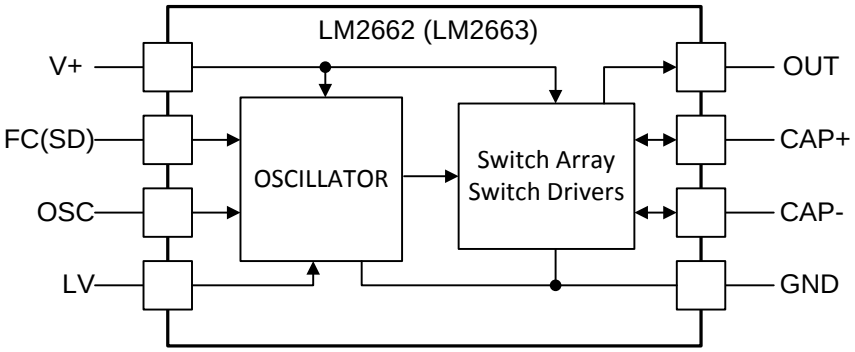
11 Layout

11.1 Layout Guidelines

The high switching frequency and large switching currents of the LM2662/LM2663 make the choice of layout important. The following steps should be used as a reference to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range

- Place C_{IN} on the top layer (same layer as the LM2662/2663) and as close to the device as possible. Connecting the input capacitor through short, wide traces to both the V+ and GND pins reduces the inductive voltage spikes that occur during switching which can corrupt the V+ line.
- Place C_{OUT} on the top layer (same layer as the LM2662/2663) and as close as possible to the OUT and GND pin. The returns for both C_{IN} and C_{OUT} should come together at one point, as close to the GND pin as possible. Connecting C_{OUT} through short, wide traces reduce the series inductance on the OUT and GND pins that can corrupt the V_{OUT} and GND lines and cause excessive noise in the device and surrounding circuitry.
- Place C_1 on the top layer (same layer as the LM2662/2663) and as close to the device as possible. Connect the flying capacitor through short, wide traces to both the CAP+ and CAP– pins.

11.2 Layout Example



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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Links

Table 3 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM2662	Click here	Click here	Click here	Click here	Click here
LM2663	Click here	Click here	Click here	Click here	Click here

12.3 Trademarks

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM2662M	Active	Production	SOIC (D) | 8	95 | TUBE	-	Call TI	Call TI	-40 to 85	LM26 62M
LM2662M.A	Active	Production	SOIC (D) | 8	95 | TUBE	-	Call TI	Call TI	-40 to 85	LM26 62M
LM2662M.B	Active	Production	SOIC (D) | 8	95 | TUBE	-	Call TI	Call TI	-40 to 85	LM26 62M
LM2662M/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM26 62M
LM2662M/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM26 62M
LM2662M/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM26 62M
LM2662MX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM26 62M
LM2662MX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM26 62M
LM2662MX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM26 62M
LM2663M	Active	Production	SOIC (D) | 8	95 | TUBE	No	SNPB	Level-1-235C-UNLIM	-40 to 85	LM26 63M
LM2663M.A	Active	Production	SOIC (D) | 8	95 | TUBE	No	SNPB	Level-1-235C-UNLIM	-40 to 85	LM26 63M
LM2663M.B	Active	Production	SOIC (D) | 8	95 | TUBE	No	SNPB	Level-1-235C-UNLIM	-40 to 85	LM26 63M
LM2663M/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM26 63M
LM2663M/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM26 63M
LM2663M/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM26 63M
LM2663MX	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	No	SNPB	Level-1-235C-UNLIM	-40 to 85	LM26 63M

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM2663MX.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	No	SNPB	Level-1-235C-UNLIM	-40 to 85	LM26 63M
LM2663MX.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	No	SNPB	Level-1-235C-UNLIM	-40 to 85	LM26 63M
LM2663MX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM26 63M
LM2663MX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM26 63M
LM2663MX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM26 63M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

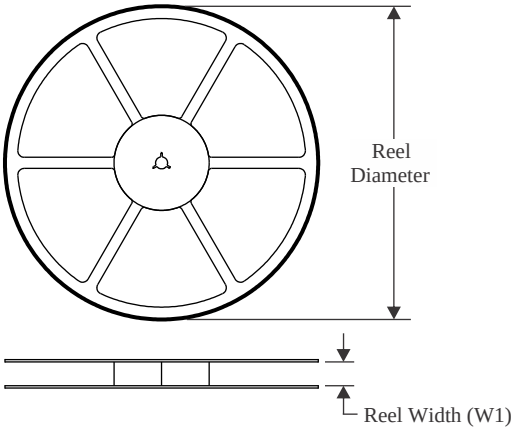
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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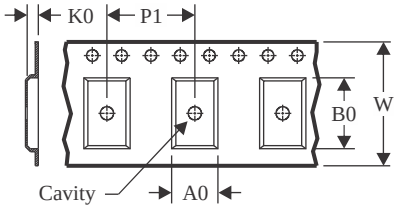
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

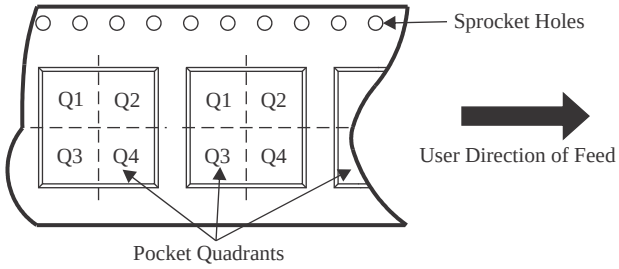


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

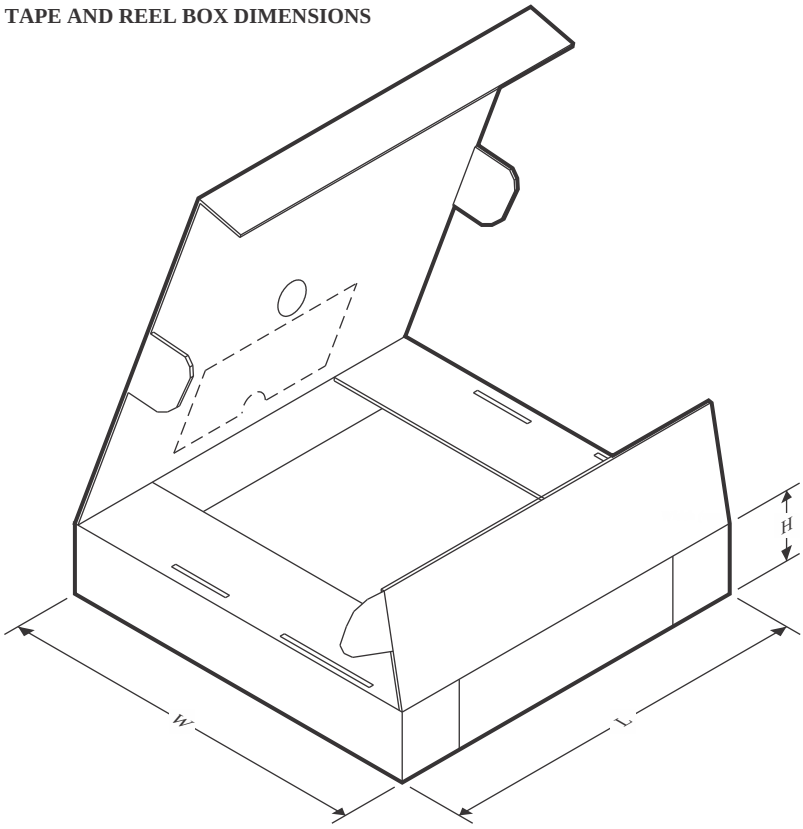
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2662MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2663MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

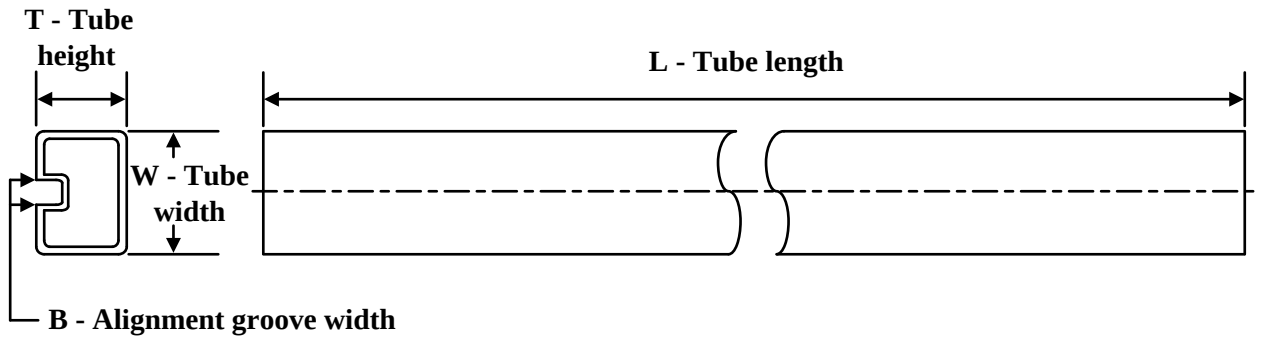
TAPE AND REEL BOX DIMENSIONS



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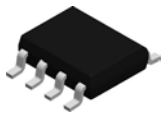
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2662MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM2663MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM2662M	D	SOIC	8	95	495	8	4064	3.05
LM2662M.A	D	SOIC	8	95	495	8	4064	3.05
LM2662M.B	D	SOIC	8	95	495	8	4064	3.05
LM2662M/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM2662M/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LM2662M/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LM2663M	D	SOIC	8	95	495	8	4064	3.05
LM2663M	D	SOIC	8	95	495	8	4064	3.05
LM2663M.A	D	SOIC	8	95	495	8	4064	3.05
LM2663M.A	D	SOIC	8	95	495	8	4064	3.05
LM2663M.B	D	SOIC	8	95	495	8	4064	3.05
LM2663M.B	D	SOIC	8	95	495	8	4064	3.05
LM2663M/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM2663M/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LM2663M/NOPB.B	D	SOIC	8	95	495	8	4064	3.05

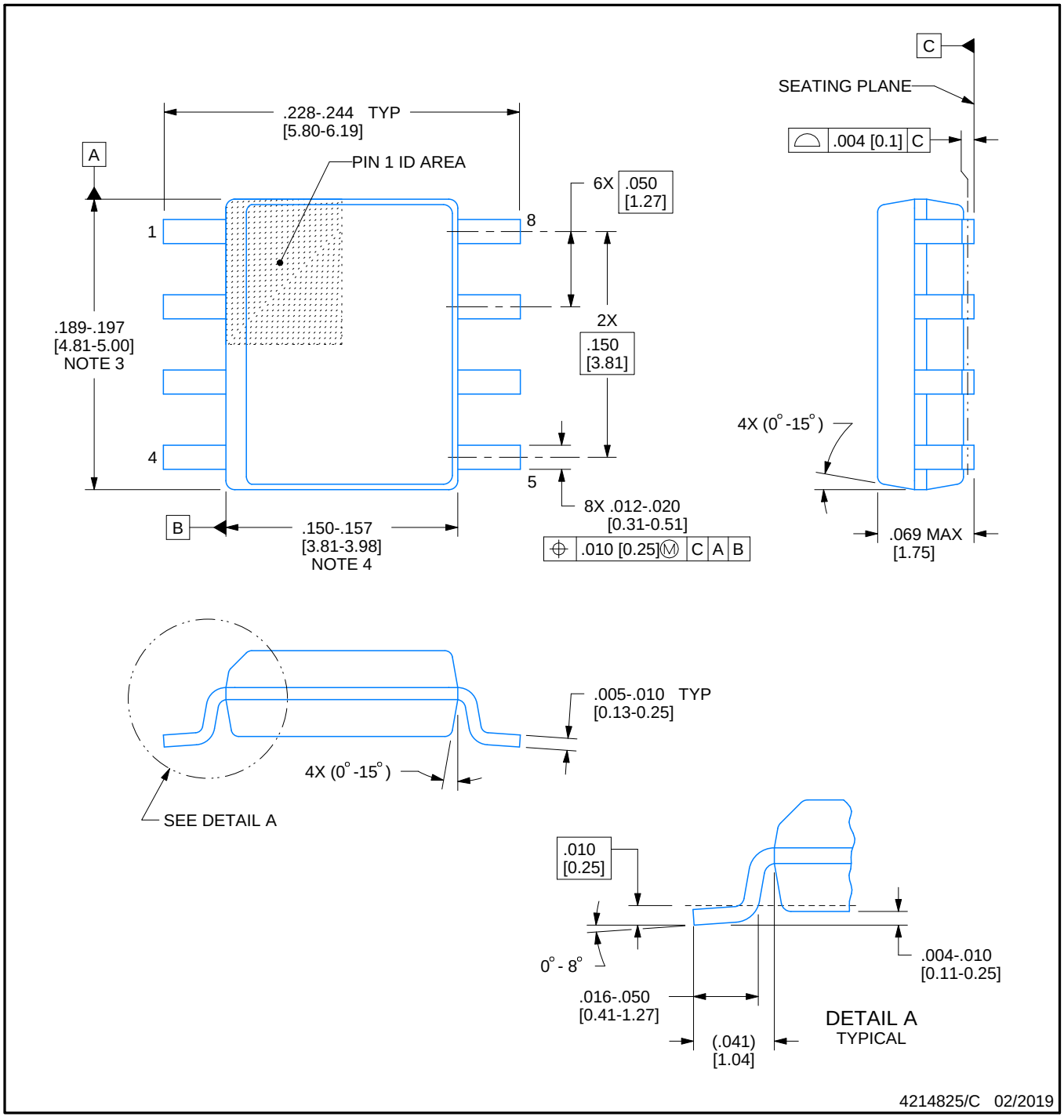


PACKAGE OUTLINE

D0008A

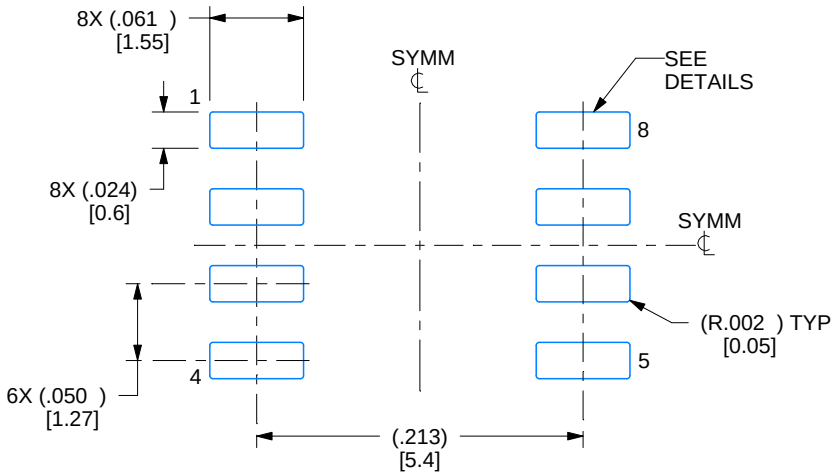
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

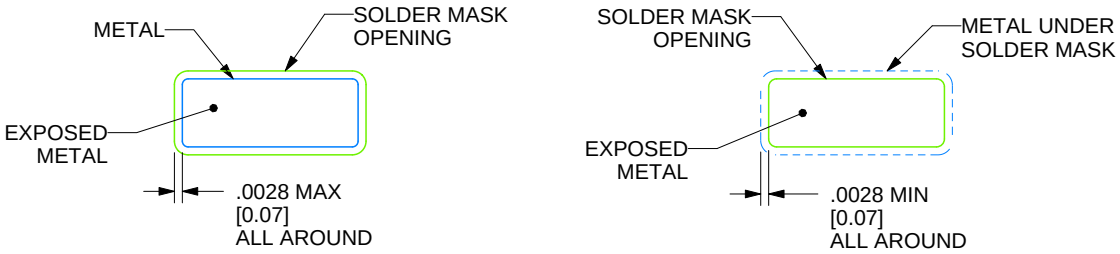


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

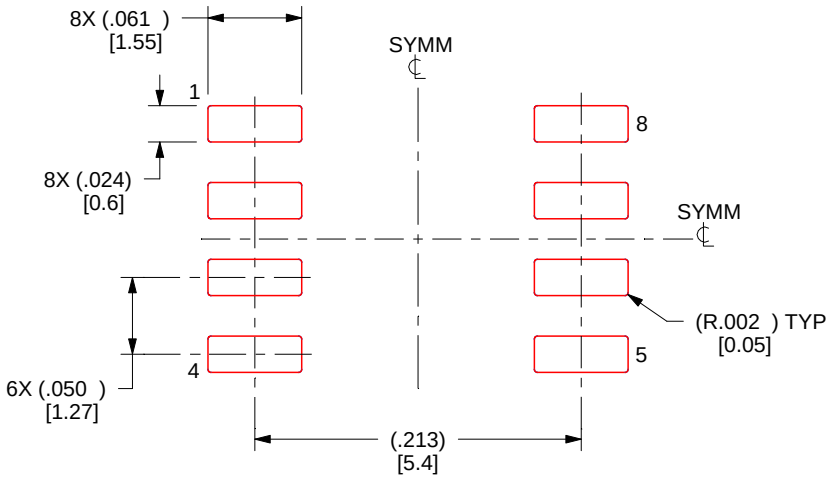
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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