

LM3648 具有 1.5A 高侧电流源的同步升压 LED 闪光灯驱动器

1 特性

- 1.5A LED 电流源可编程性
- 精确的可编程 LED 电流范围为 1.954mA 至 1.5A
- 优化了低电池电压条件下的闪存 LED 电流（输入电压闪存监控器 (IVFM)）
- 在火炬模式 (@ 100mA) 和闪存模式 (@ 1A 至 1.5A) 下效率超过 85%
- 支持阴极接地 LED 操作，改进了热管理
- 小型解决方案尺寸: < 16mm²
- 硬件选通使能 (STROBE)
- 射频功率放大器脉冲事件的同步输入 (TX)
- 硬件火炬使能 (TORCH/TEMP)
- 远程 NTC 监控 (TORCH/TEMP)
- 400kHz I²C 兼容接口
 - LM3648 (I²C 地址 = 0x63)

2 应用

可拍照手机白色 LED 闪光灯

3 说明

LM3648 是一款 LED 闪光灯驱动器，其采用小型解决方案尺寸，并且具备更强的适应能力。LM3648 采用 2MHz 或 4MHz 固定频率的同步升压转换器为 1.5A LED 恒流源供电。自适应调节方法确保电流源保持可调节状态，并且最大限度地提高效率。

LM3648 的功能通过 I²C 兼容接口进行控制。其功能包括：硬件闪光灯和硬件手电筒引脚（STROBE 和 TORCH/TEMP）、TX 中断以及 NTC 热敏电阻监视器。该器件在闪光灯模式下可提供 64 种电流，在摄像模式（手电筒）下可提供 128 种电流。

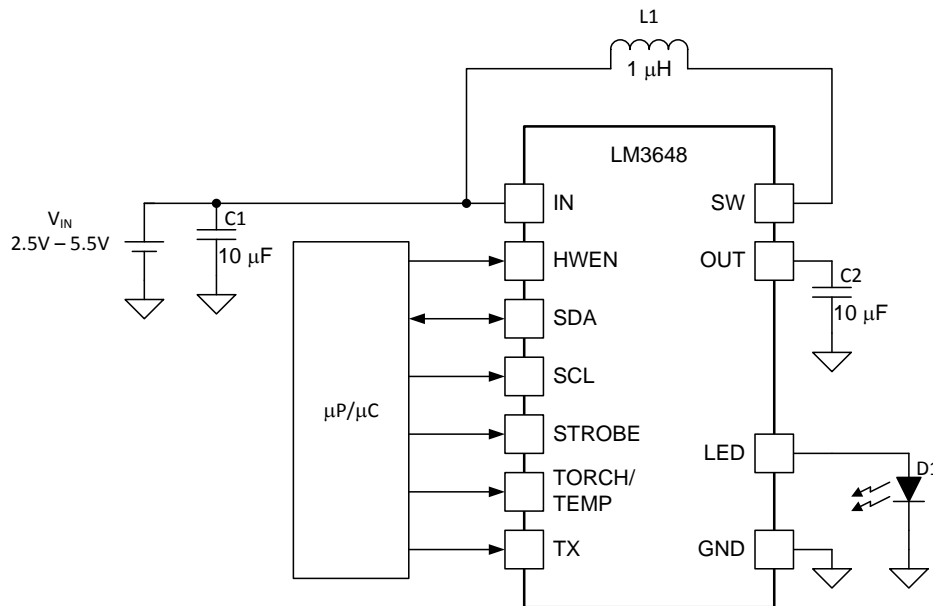
而且还提供有 2MHz 或 4MHz 开关频率选项、过压保护 (OVP) 功能以及可调限流功能，允许使用微型、超薄电感器和 (10μF) 陶瓷电容。该器件的工作环境温度范围为 -40°C 至 85°C。

器件信息⁽¹⁾

| 器件型号 | 封装 | 封装尺寸（最大值） |
|--------|---------------------------------|-----------------|
| LM3648 | 芯片级球状引脚 栅格阵列 (DSBGA) (12) | 1.69mm x 1.31mm |

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



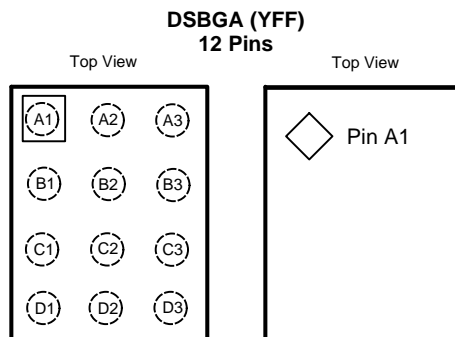
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4 修订历史记录

| 日期 | 修订版本 | 注释 |
|-------------|------|-------|
| 2014 年 10 月 | * | 最初发布。 |

5 Pin Configuration and Functions



Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|--------|------------|---------------------|---|
| NUMBER | NAME | | |
| A1 | GND | G | Ground |
| A2 | IN | P | Input voltage connection. Connect IN to the input supply and bypass to GND with a 10-μF or larger ceramic capacitor. |
| A3 | SDA | I/O | Serial data input/output in the I ² C Mode on LM3648. |
| B1 | SW | P | Drain Connection for Internal NMOS and Synchronous PMOS Switches. |
| B2 | STROBE | I | Active high hardware flash enable. Drive STROBE high to turn on Flash pulse. Internal pulldown resistor of 300 kΩ between STROBE and GND. |
| B3 | SCL | I | Serial clock input for LM3648. |
| C1 | OUT | P | Step-up DC/DC CONVERTER Output. Connect a 10-μF ceramic capacitor between this terminal and GND. |
| C2 | HWEN | I | Active high enable pin. High = Standby, Low = Shutdown/Reset. Internal pulldown resistor of 300 kΩ between HWEN and GND. |
| C3 | TORCH/TEMP | I/P | Torch terminal input or threshold detector for NTC temperature sensing and current scale back. |
| D1 | LED | P | High-side current source output for flash LED. Connect pin D1 to D3 externally. |
| D2 | TX | I | Configurable dual polarity power amplifier synchronization input. Internal pulldown resistor of 300 kΩ between TX and GND. |
| D3 | LED | P | High-side current source output for flash LED. Connect pin D1 to D3 externally. |

(1) A: Analog Pin, G: Ground Pin, P: Power Pin, I: Digital Input Pin

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

| | MIN | MAX | UNIT |
|---|--|-----|------|
| IN, SW, OUT, LED | −0.3 | 6 | V |
| SDA, SCL, TX, TORCH/TEMP, HWEN, STROBE | −0.3 to the lesser of (V _{IN} +0.3) w/ 6 V max | | |
| Continuous power dissipation ⁽³⁾ | Internally limited | | |
| Junction temperature (T _{J-MAX}) | 150 | | °C |
| Maximum lead temperature (soldering) | See ⁽⁴⁾ | | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the potential at the GND terminal.
- (3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 135°C (typ.). Thermal shutdown is ensured by design.
- (4) For detailed soldering specifications and information, please refer to Texas Instruments Application Note 1112: *DSBGA Wafer Level Chip Scale Package* (SNVA009).

6.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|--------------------|---------------------------|--|-------|------|------|
| T _{stg} | Storage temperature range | | −65 | 150 | °C |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | −2500 | 2500 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | −1500 | 1500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

| | MIN | MAX | UNIT |
|--|-----|-----|------|
| V _{IN} | 2.5 | 5.5 | V |
| Junction temperature (T _J) | -40 | 125 | °C |
| Ambient temperature (T _A) ⁽³⁾ | -40 | 85 | |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the potential at the GND terminal.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX-OP} = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application (R_{θJA}), as given by the following equation: T_{A-MAX} = T_{J-MAX-OP} - (R_{θJA} × P_{D-MAX}).

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | LM3648 | UNIT |
|-------------------------------|--|-------------|------|
| | | DSBGA (YFF) | |
| | | 12 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 90.2 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 0.5 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 40.0 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 3.0 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 39.2 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

Typical limits tested at $T_A = 25^\circ\text{C}$. Minimum and maximum limits apply over the full operating ambient temperature range ($-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$). Unless otherwise specified, $V_{IN} = 3.6\text{ V}$, $\text{HWEN} = V_{IN}$.⁽¹⁾⁽²⁾

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|--|--|-------|------|-----------------|------|------|
| CURRENT SOURCE SPECIFICATIONS | | | | | | | |
| I _{LED} | Current source accuracy | V _{OUT} = 4 V, flash code = 0x3F = 1.5 A flash | | -7% | 1.5 | 7% | A |
| | | V _{OUT} = 4 V, torch code = 0x3F = 178.6 mA torch | | -10% | 178.6 | 10% | mA |
| V _{HR} | LED current source regulation voltage | I _{LED} = 1.5 A | Flash | 290 | | mV | |
| | | I _{LED} = 178.6 mA | Torch | 158 | | | |
| V _{OVP} | | ON threshold | | 4.86 | 5 | 5.1 | V |
| | | OFF threshold | | 4.75 | 4.88 | 4.99 | |
| STEP-UP DC/DC CONVERTER SPECIFICATIONS | | | | | | | |
| R _{PMOS} | PMOS switch on-resistance | | | 86 | | mΩ | |
| R _{NMOS} | NMOS switch on-resistance | | | 65 | | | |
| I _{CL} | Switch current limit | Reg 0x07, bit[0] = 0 | | -12% | 1.9 | 12% | A |
| | | Reg 0x07, bit[0] = 1 | | -12% | 2.8 | 12% | |
| V _{UVLO} | Undervoltage lockout threshold | Falling V _{IN} | | -2% | 2.5 | 2% | V |
| V _{TRIP} | NTC comparator trip threshold | Reg 0x09, bits[3:1] = '100' | | -5% | 0.6 | 5% | V |
| I _{NTC} | NTC current | | | -6% | 50 | 6% | μA |
| V _{IVFM} | Input voltage flash monitor trip threshold | Reg 0x02, bits[5:3] = '000' | | -3% | 2.9 | 3% | V |
| I _Q | Quiescent supply current | Device not switching pass mode | | 0.3 | | 0.75 | mA |
| I _{SD} | Shutdown supply current | Device disabled, HWEN = 0 V 2.5 V ≤ V _{IN} ≤ 5.5 V | | 0.1 | | 4 | μA |
| I _{SB} | Standby supply current | Device disabled, HWEN = 1.8 V 2.5 V ≤ V _{IN} ≤ 5.5 V | | 2.5 | | 10 | μA |
| HWEN, TORCH/TEMP, STROBE, TX VOLTAGE SPECIFICATIONS | | | | | | | |
| V _{IL} | Input logic low | 2.5 V ≤ V _{IN} ≤ 5.5 V | | 0 | 0.4 | | V |
| V _{IH} | Input logic high | | | 1.2 | V _{IN} | | |
| I ² C-COMPATIBLE INTERFACE SPECIFICATIONS (SCL, SDA) | | | | | | | |
| V _{IL} | Input logic low | 2.5 V ≤ V _{IN} ≤ 4.2 V | | 0 | 0.4 | | V |
| V _{IH} | Input logic high | | | 1.2 | V _{IN} | | |
| V _{OL} | Output logic low | I _{LOAD} = 3 mA | | | | 400 | mV |

(1) All voltages are with respect to the potential at the GND pin.

(2) Minimum (Min) and Maximum (Max) limits are specified by design, test, or statistical analysis. Typical (typ.) numbers are not verified, but do represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: $V_{IN} = 3.6\text{ V}$ and $T_A = 25^\circ\text{C}$.

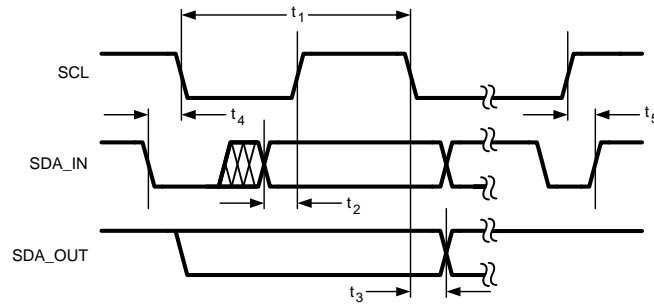
6.6 Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|-------|--|-----|-----|-----|------|
| t_1 | SCL clock period | 2.4 | | | μs |
| t_2 | Data in set-up time to SCL high | 100 | | | ns |
| t_3 | Data out stable After SCL low | 0 | | | |
| t_4 | SDA low set-up time to SCL low (start) | 100 | | | |
| t_5 | SDA high hold time after SCL high (stop) | 100 | | | |

6.7 Switching Characteristics

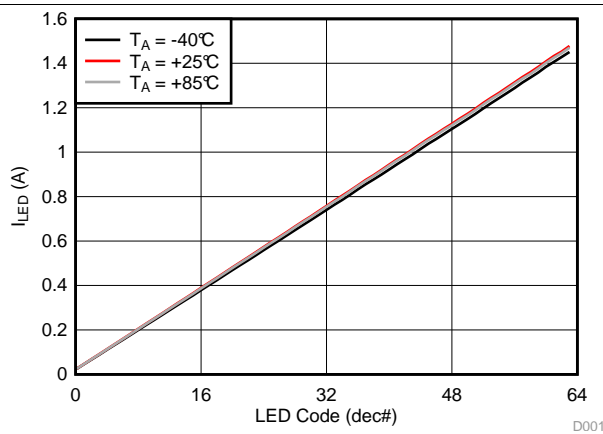
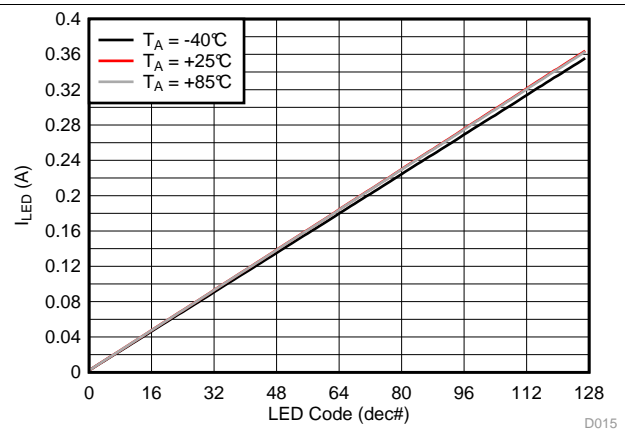
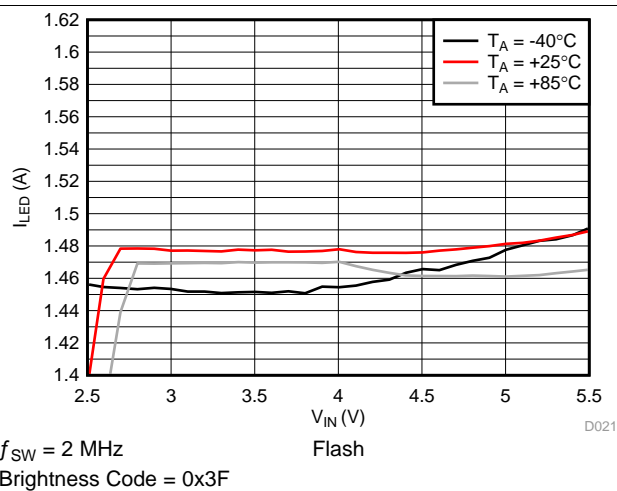
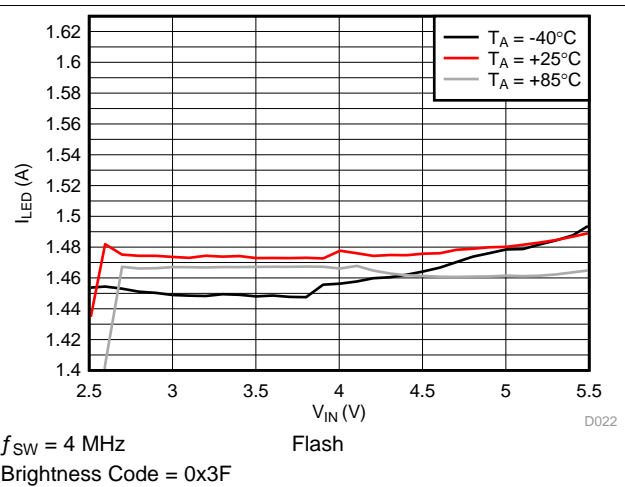
over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---------------------|--|-----|-----|-----|------|
| f_{SW} | Switching frequency | $2.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ | -6% | 4 | 6% | MHz |


Figure 1. I²C-Compatible Interface Specifications

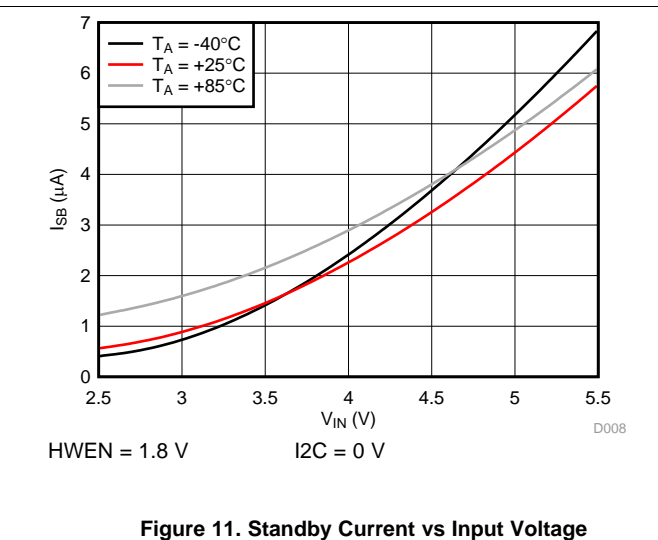
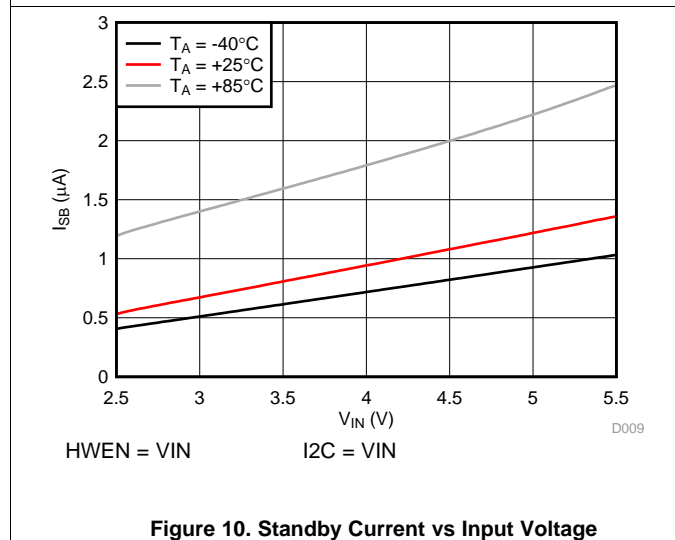
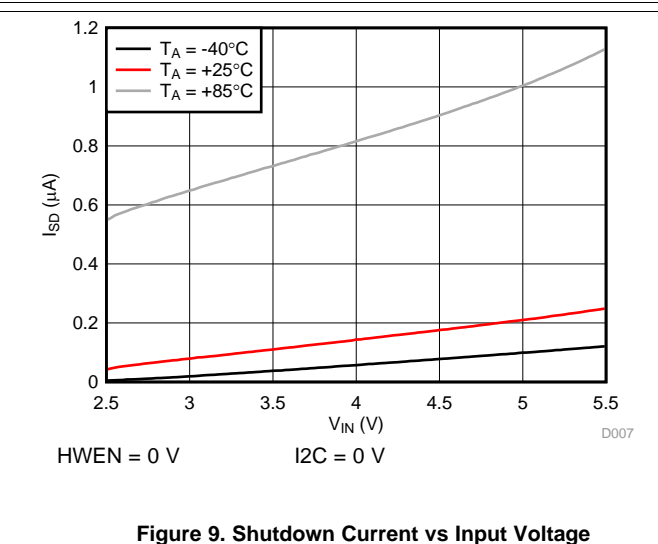
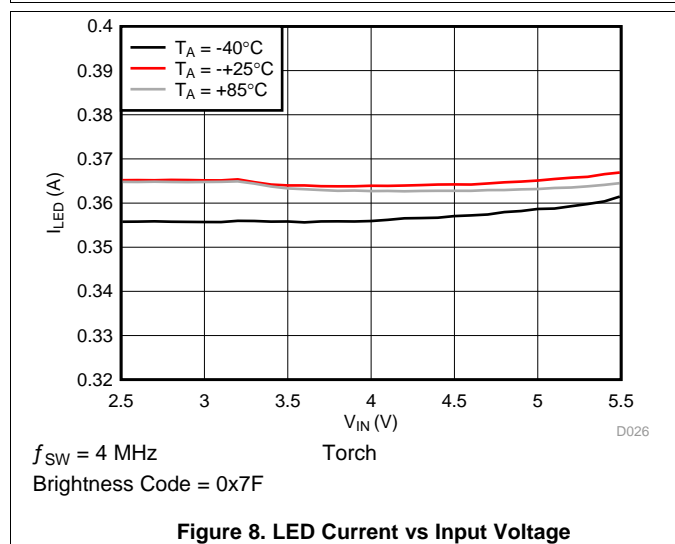
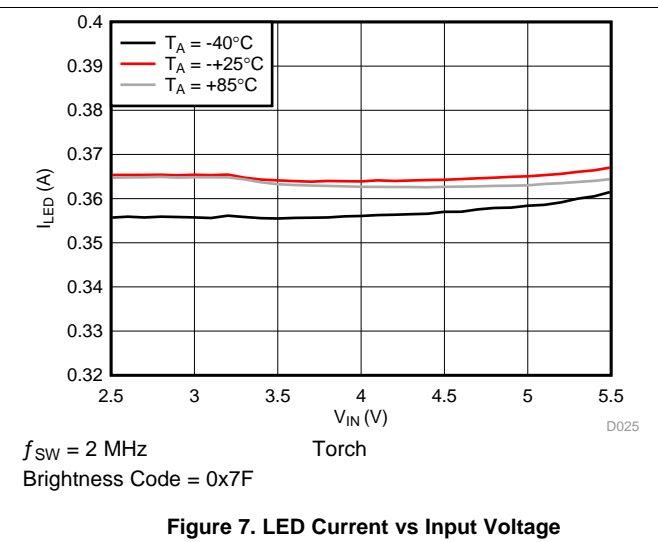
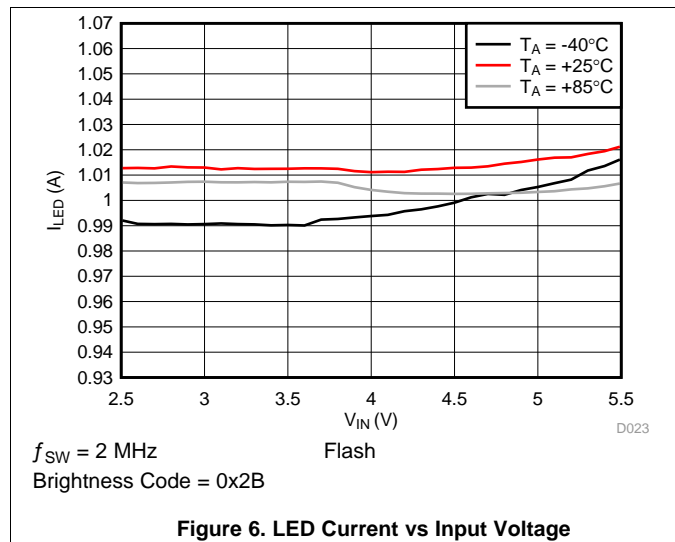
6.8 Typical Characteristics

Ambient temperature is 25°C, input voltage is 3.6 V, HWEN = V_{IN}, C_{IN} = C_{OUT} = 2 × 10 μF and L = 1 μH, unless otherwise noted.


Figure 2. LED Flash Current vs Brightness Code

Figure 3. LED Torch Current vs Brightness Code

Figure 4. LED Current vs Input Voltage

Figure 5. LED Current vs Input Voltage

Typical Characteristics (continued)

Ambient temperature is 25°C, input voltage is 3.6 V, $HWEN = V_{IN}$, $C_{IN} = C_{OUT} = 2 \times 10 \mu F$ and $L = 1 \mu H$, unless otherwise noted.



Typical Characteristics (continued)

Ambient temperature is 25°C, input voltage is 3.6 V, $HWEN = V_{IN}$, $C_{IN} = C_{OUT} = 2 \times 10 \mu F$ and $L = 1 \mu H$, unless otherwise noted.

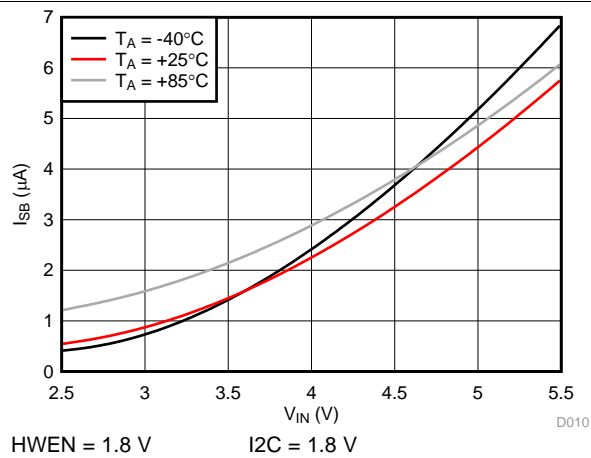


Figure 12. Standby Current vs Input Voltage

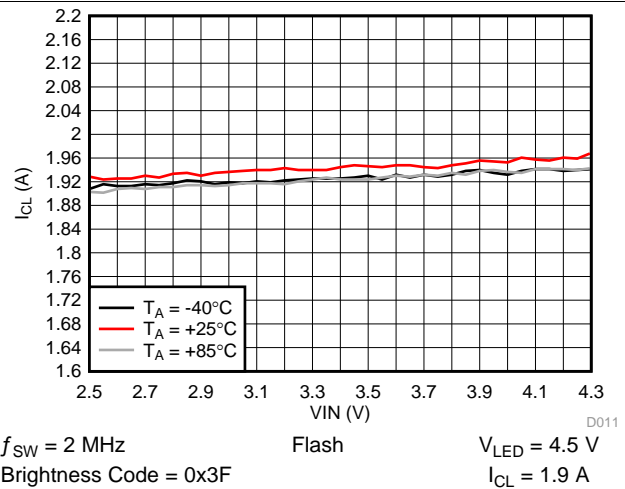


Figure 13. Inductor Current Limit vs Input Voltage

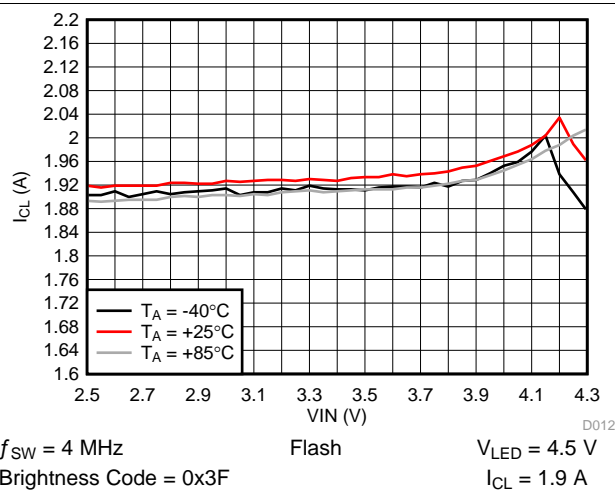


Figure 14. Inductor Current Limit vs Input Voltage

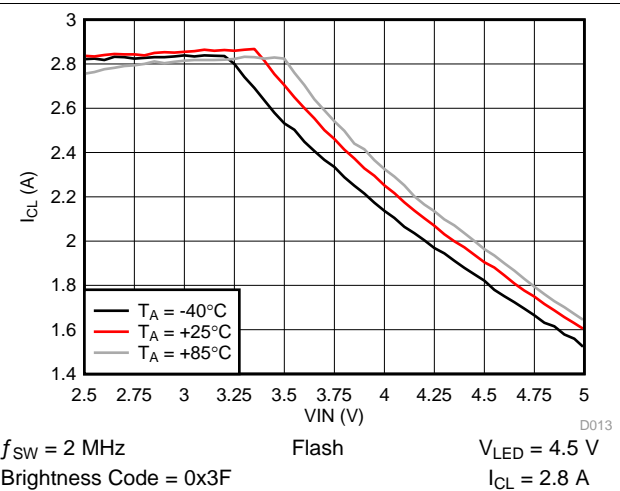


Figure 15. Inductor Current Limit vs Input Voltage

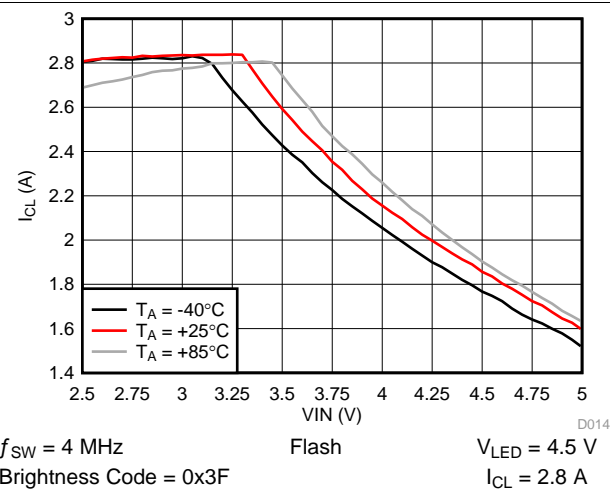


Figure 16. Inductor Current Limit vs Input Voltage

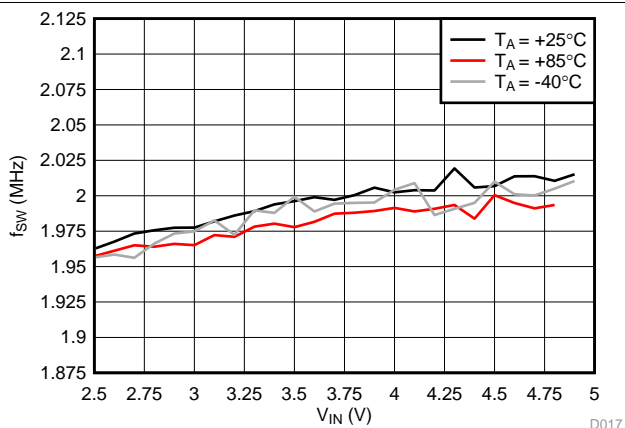


Figure 17. 2-MHz Switching Frequency vs Input Voltage

Typical Characteristics (continued)

Ambient temperature is 25°C, input voltage is 3.6 V, $HWEN = V_{IN}$, $C_{IN} = C_{OUT} = 2 \times 10 \mu F$ and $L = 1 \mu H$, unless otherwise noted.

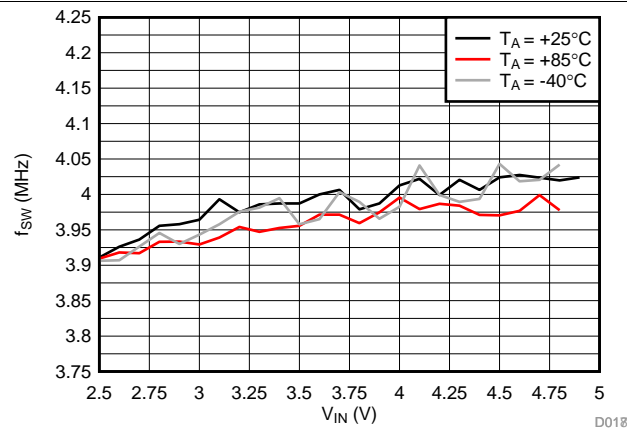


Figure 18. 4-MHz Switching Frequency vs Input Voltage

7 Detailed Description

7.1 Overview

The LM3648 is a high-power white LED flash driver capable of delivering up to 1.5 A to the LED. The device incorporates a 2-MHz or 4-MHz constant frequency-synchronous current-mode PWM boost converter and a high-side current source to regulate the LED current over the 2.5-V to 5.5-V input voltage range.

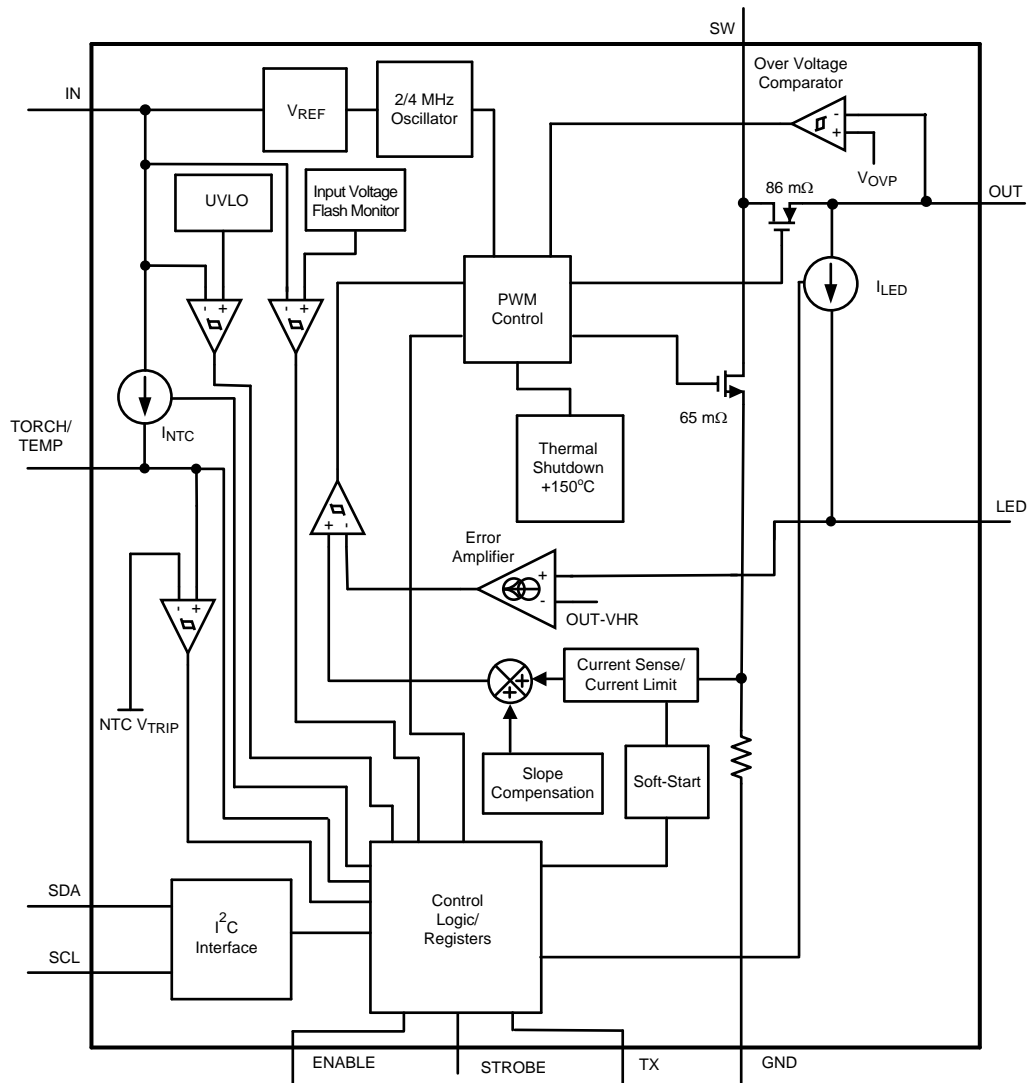
The LM3648 PWM DC/DC boost converter switches and boosts the output to maintain at least V_{HR} across the current source. This minimum headroom voltage ensures that the current source remains in regulation. If the input voltage is above the LED voltage + current source headroom voltage the device does not switch, but turns the PFET on continuously (Pass mode). In Pass mode the difference between $(V_{IN} - I_{LED} \times R_{PMOS})$ and the voltage across the LED is dropped across the current source.

The LM3648 has three logic inputs including a hardware Flash Enable (STROBE), a hardware Torch Enable (TORCH/TEMP, TORCH = default), and a Flash Interrupt input (TX) designed to interrupt the flash pulse during high battery-current conditions. These logic inputs have internal 300-k Ω (typ.) pulldown resistors to GND.

Additional features of the LM3648 include an internal comparator for LED thermal sensing via an external NTC thermistor and an input voltage monitor that can reduce the Flash current during low V_{IN} conditions. It also has a Hardware Enable (HWEN) pin that can be used to reset the state of the device and the registers by pulling the HWEN pin to ground.

Control is done via an I²C-compatible interface. This includes adjustment of the Flash and Torch current levels, changing the Flash Timeout Duration, and changing the switch current limit. Additionally, there are flag and status bits that indicate flash current time-out, LED overtemperature condition, LED failure (open/short), device thermal shutdown, TX interrupt, and V_{IN} undervoltage conditions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Flash Mode

In Flash Mode, the LED current source (LED) provides 64 target current levels from 21.8 mA to 1500 mA. Once the Flash sequence is activated the current source (LED) ramps up to the programmed Flash current by stepping through all current steps until the programmed current is reached. The headroom in the current source can be regulated to provide 21.8 mA to 1.5 A.

When the device is enabled in Flash Mode through the Enable Register, all mode bits in the Enable Register are cleared after a flash time-out event.

Feature Description (continued)

7.3.2 Torch Mode

In Torch mode, the LED current source (LED) provide 128 target current levels from 1.954 mA to 358 mA. The Torch current is adjusted via the LED Torch Brightness Register. Torch mode is activated by the Enable Register (setting M1, M0 to '10'), or by pulling the TORCH/TEMP pin HIGH when the pin is enabled (Enable Register) and set to Torch Mode. Once the TORCH sequence is activated the active current source (LED) ramps up to the programmed Torch current by stepping through all current steps until the programmed current is reached. The rate at which the current ramps is determined by the value chosen in the Timing Register.

Torch Mode is not affected by Flash Timeout or by a TX Interrupt event.

7.3.3 IR Mode

In IR Mode, the target LED current is equal to the value stored in the LED Flash Brightness Registers. When IR mode is enabled (setting M1, M0 to '01'), the boost converter turns on and sets the output equal to the input (pass-mode). At this point, toggling the STROBE pin enables and disables the LED current source (if enabled). The STROBE pin can only be set to be Level sensitive, meaning all timing of the IR pulse is externally controlled. In IR Mode, the current source does not ramp the LED output to the target. The current transitions immediately from off to on and then on to off.

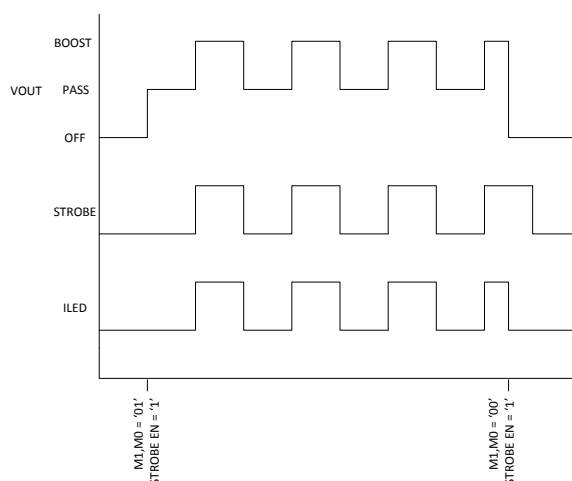


Figure 19. IR Mode with Boost

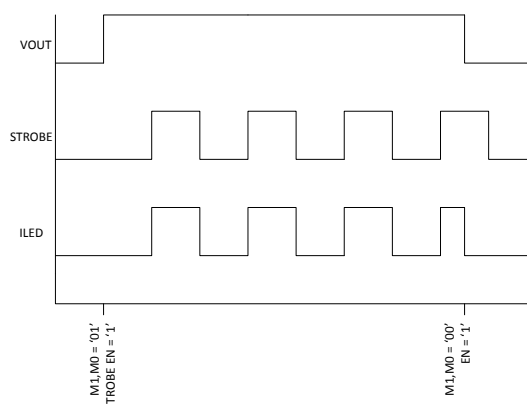


Figure 20. IR Mode Pass Only

Feature Description (continued)

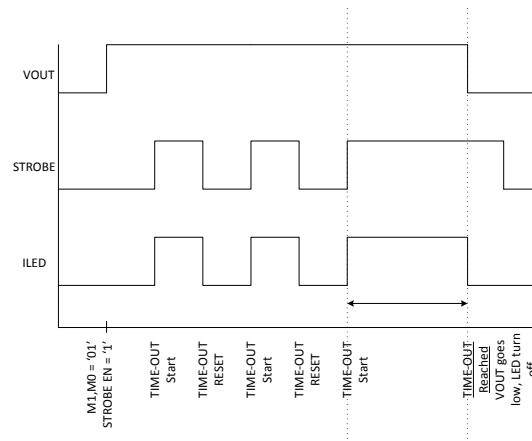


Figure 21. IR Mode Timeout

7.4 Device Functioning Modes

7.4.1 Start-Up (Enabling The Device)

Turnon of the LM3648 Torch and Flash modes can be done through the Enable Register. On start-up, when V_{OUT} is less than V_{IN} the internal synchronous PFET turns on as a current source and delivers 200 mA (typ.) to the output capacitor. During this time the current source (LED) is off. When the voltage across the output capacitor reaches 2.2 V (typ.), the current source turns on. At turnon the current source steps through each FLASH or TORCH level until the target LED current is reached. This gives the device a controlled turnon and limits inrush current from the V_{IN} supply.

7.4.2 Pass Mode

The LM3648 starts up in Pass Mode and stays there until Boost Mode is needed to maintain regulation. If the voltage difference between V_{OUT} and V_{LED} falls below V_{HR} , the device switches to Boost Mode. In Pass Mode the boost converter does not switch, and the synchronous PFET turns fully on bringing V_{OUT} up to $V_{IN} - I_{LED} \times R_{PMOS}$. In Pass Mode the inductor current is not limited by the peak current limit.

7.4.3 Power Amplifier Synchronization (TX)

The TX pin is a Power Amplifier Synchronization input. This is designed to reduce the flash LED current and thus limit the battery current during high battery current conditions such as PA transmit events. When the LM3648 is engaged in a Flash event, and the TX pin is pulled high, the LED current is forced into Torch Mode at the programmed Torch current setting. If the TX pin is then pulled low before the Flash pulse terminates, the LED current returns to the previous Flash current level. At the end of the Flash time-out, whether the TX pin is high or low, the LED current turns off.

7.4.4 Input Voltage Flash Monitor (IVFM)

The LM3648 has the ability to adjust the flash current based upon the voltage level present at the IN pin utilizing the Input Voltage Flash Monitor (IVFM). The adjustable threshold IVFM-D ranges from 2.9 V to 3.6 V in 100-mV steps, with three different usage modes (Stop and Hold, Adjust Down Only, Adjust Up and Down). The Flags2 Register has the IVFM flag bit set when the input voltage crosses the IVFM-D value. Additionally, the IVFM-D threshold sets the input voltage boundary that forces the LM3648 to either stop ramping the flash current during start-up (Stop and Hold Mode) or to start decreasing the LED current during the flash (Down Adjust Only and Up and Down Adjust). In Adjust Up and Down mode, the IVFM-D value plus the hysteresis voltage threshold set the input voltage boundary that forces the LM3648 to start ramping the flash current back up towards the target.

Device Functioning Modes (continued)

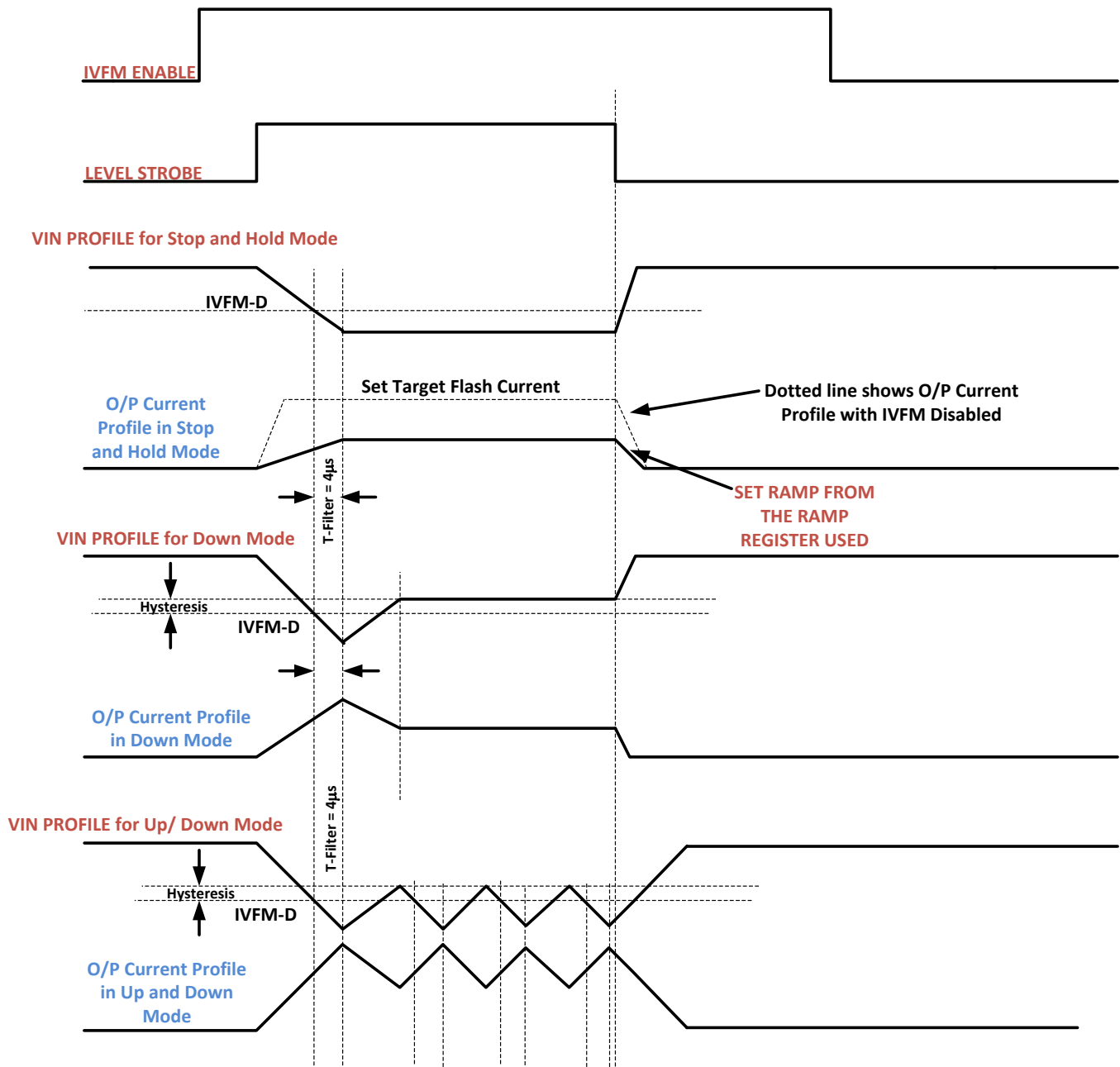


Figure 22. IVFM Modes

Device Functioning Modes (continued)

7.4.5 Fault/Protections

7.4.5.1 Fault Operation

If the LM3648 enters a fault condition, the device sets the appropriate flag in the Flags1 and Flags2 Registers (0x0A and 0x0B), and places the device into standby by clearing the Mode Bits ([1],[0]) in the Enable Register. The LM3648 remains in standby until an I²C read of the Flags1 and Flags2 Registers are completed. Upon clearing the flags/faults, the device can be restarted (Flash, Torch, IR, etc.). If the fault is still present, the LM3648 re-enters the fault state and enters standby again.

7.4.5.2 Flash Time-Out

The Flash Time-Out period sets the amount of time that the Flash Current is being sourced from the current source (LED). The LM3648 has 16 timeout levels ranging from 10 ms to 400 ms (see [Timing Configuration Register \(0x08\)](#) for more detail).

7.4.5.3 Overvoltage Protection (OVP)

The output voltage is limited to typically 5 V (see V_{OVP} spec in the [Electrical Characteristics](#)). In situations such as an open LED, the LM3648 raises the output voltage in order to keep the LED current at its target value. When V_{OUT} reaches 5 V (typ.), the overvoltage comparator trips and turns off the internal NFET. When V_{OUT} falls below the “ V_{OVP} Off Threshold”, the LM3648 begins switching again. The mode bits are cleared, and the OVP flag is set, when an OVP condition is present for three rising OVP edges. This prevents momentary OVP events from forcing the device to shut down.

7.4.5.4 Current Limit

The LM3648 features two selectable inductor current limits that are programmable through the I²C-compatible interface. When the inductor current limit is reached, the LM3648 terminates the charging phase of the switching cycle. Switching resumes at the start of the next switching period. If the overcurrent condition persists, the device operates continuously in current limit.

Since the current limit is sensed in the NMOS switch, there is no mechanism to limit the current when the device operates in Pass Mode (current does not flow through the NMOS in pass mode). In Boost mode or Pass mode if V_{OUT} falls below 2.3 V, the device stops switching, and the PFET operates as a current source limiting the current to 200 mA. This prevents damage to the LM3648 and excessive current draw from the battery during output short-circuit conditions. The mode bits are not cleared upon a Current Limit event, but a flag is set.

7.4.5.5 NTC Thermistor Input (Torch/Temp)

The TORCH/TEMP pin, when set to TEMP mode, serves as a threshold detector and bias source for negative temperature coefficient (NTC) thermistors. When the voltage at TEMP goes below the programmed threshold, the LM3648 is placed into standby mode. The NTC threshold voltage is adjustable from 200 mV to 900 mV in 100-mV steps. The NTC bias current is set to 50 μ A. The NTC detection circuitry can be enabled or disabled via the Enable Register. If enabled, the NTC block turns on and off during the start and stop of a Flash/Torch event.

Additionally, the NTC input looks for an open NTC connection and a shorted NTC connection. If the NTC input falls below 100 mV, the NTC short flag is set, and the device is disabled. If the NTC input rises above 2.3 V, the NTC Open flag is set, and the device is disabled. These fault detections can be individually disabled/enabled via the NTC Open Fault Enable bit and the NTC Short Fault Enable bit.

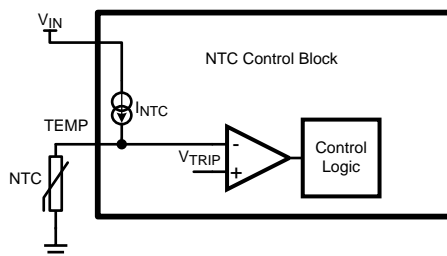


Figure 23. Temp Detection Diagram

Device Functioning Modes (continued)

7.4.5.6 Undervoltage Lockout (UVLO)

The LM3648 has an internal comparator that monitors the voltage at IN and forces the LM3648 into standby if the input voltage drops to 2.5 V. If the UVLO monitor threshold is tripped, the UVLO flag bit is set in the Flags1 Register (0x0A). If the input voltage rises above 2.5 V, the LM3648 is not available for operation until there is an I²C read of the Flags1 Register (0x0A). Upon a read, the Flags1 register is cleared, and normal operation can resume if the input voltage is greater than 2.5 V.

7.4.5.7 Thermal Shutdown (TSD)

When the LM3648 die temperature reaches 150°C, the thermal shutdown detection circuit trips, forcing the LM3648 into standby and writing a '1' to the corresponding bit of the Flags1 Register (0x0A) (Thermal Shutdown bit). The LM3648 is only allowed to restart after the Flags1 Register (0x0A) is read, clearing the fault flag. Upon restart, if the die temperature is still above 150°C, the LM3648 resets the Fault flag and re-enters standby.

7.4.5.8 LED and/or VOUT Short Fault

The LED Fault flags read back a '1' if the device is active in Flash or Torch mode and the LED output experiences a short condition. The Output Short Fault flag reads back a '1' if the device is active in Flash or Torch mode and the boost output experiences a short condition. An LED short condition is determined if the voltage at LED goes below 500 mV (typ.) while the device is in Torch or Flash mode. There is a deglitch time of 256 μ s before the LED Short flag is valid, and a deglitch time of 2.048 ms before the VOUT Short flag is valid. The LED Short Faults can be reset to '0' by removing power to the LM3648, setting HWEN to '0', setting the SW RESET bit to a '1', or by reading back the Flags1 Register (0x0A on LM3648). The mode bits are cleared upon an LED and/or V_{OUT} short fault.

7.5 Programming

7.5.1 Control Truth Table

| MODE1 | MODE0 | STROBE EN | TORCH EN | STROBE PIN | TORCH PIN | ACTION |
|-------|-------|-----------|----------|------------|-----------|------------------|
| 0 | 0 | 0 | 0 | X | X | Standby |
| 0 | 0 | 0 | 1 | X | pos edge | Ext Torch |
| 0 | 0 | 1 | 0 | pos edge | X | Ext Flash |
| 0 | 0 | 1 | 1 | 0 | pos edge | Standalone Torch |
| 0 | 0 | 1 | 1 | pos edge | 0 | Standalone Flash |
| 0 | 0 | 1 | 1 | pos edge | pos edge | Standalone Flash |
| 1 | 0 | X | X | X | X | Int Torch |
| 1 | 1 | X | X | X | X | Int Flash |
| 0 | 1 | 0 | X | X | X | IRLED Standby |
| 0 | 1 | 1 | X | 0 | X | IRLED Standby |
| 0 | 1 | 1 | X | pos edge | X | IRLED enabled |

7.5.2 I²C-Compatible Interface

7.5.2.1 Data Validity

The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when SCL is LOW.

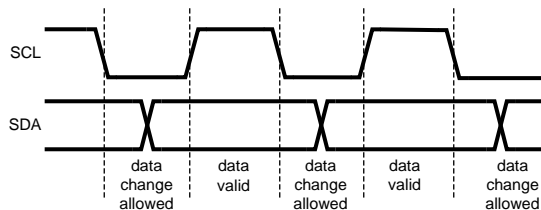


Figure 24. Data Validity Data

A pullup resistor between the controller's VIO line and SDA must be greater than $[(VIO - V_{OL}) / 3mA]$ to meet the V_{OL} requirement on SDA. Using a larger pullup resistor results in lower switching current with slower edges, while using a smaller pullup results in higher switching currents with faster edges.

7.5.2.2 Start and Stop Conditions

START and STOP conditions classify the beginning and the end of the I²C session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP conditions. The I²C bus is considered busy after a START condition and free after a STOP condition. During data transmission, the I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

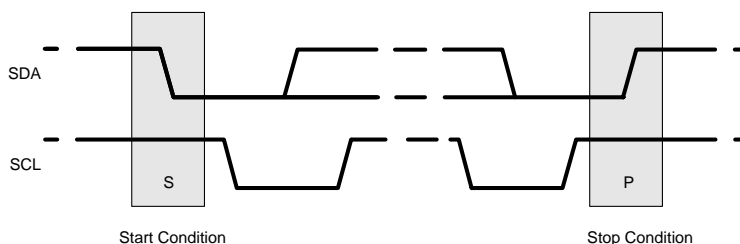


Figure 25. Start and Stop Conditions

7.5.2.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LM3648 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LM3648 generates an acknowledge after each byte is received. There is no acknowledge created after data is read from the device.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM3648 7-bit address is 0x63. For the eighth bit, a '0' indicates a WRITE and a '1' indicates a READ. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register.

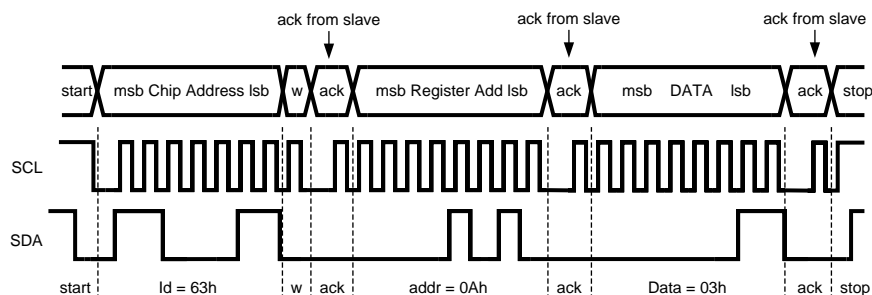


Figure 26. Write Cycle W = Write (SDA = "0") R = Read (SDA = "1") Ack = Acknowledge (SDA Pulled Down by Either Master or Slave) ID = Chip Address, 63h for LM3648

7.5.2.4 I²C-Compatible Chip Address

The device address for the LM3648 is 1100011 (0x63). After the START condition, the I²C-compatible master sends the 7-bit address followed by an eighth read or write bit (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data is written. The third byte contains the data for the selected register.

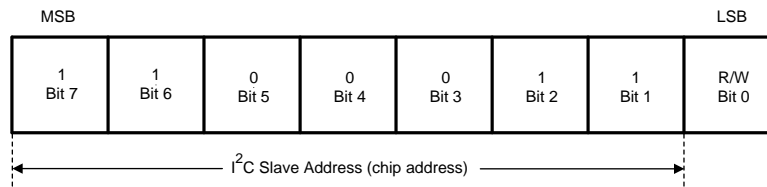


Figure 27. I²C-Compatible Chip Address

7.6 Register Descriptions

| REGISTER NAME | INTERNAL HEX ADDRESS | POWER ON/RESET VALUE |
|-------------------------------|----------------------|----------------------|
| | | LM3648 |
| Enable Register | 0x01 | 0x80 |
| IVFM Register | 0x02 | 0x01 |
| LED Flash Brightness Register | 0x03 | 0xBF |
| LED Torch Brightness Register | 0x05 | 0xBF |
| Boost Configuration Register | 0x07 | 0x09 |
| Timing Configuration Register | 0x08 | 0x1A |
| TEMP Register | 0x09 | 0x08 |
| Flags1 Register | 0x0A | 0x00 |
| Flags2 Register | 0x0B | 0x00 |
| Device ID Register | 0x0C | 0x00 |
| Last Flash Register | 0x0D | 0x00 |

7.6.1 Enable Register (0x01)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|-------|---|-------|
| TX Pin Enable 0 = Disabled 1 = Enabled (Default) | Strobe Type 0 = Level Triggered 1 = Edge Triggered | Strobe Enable 0 = Disabled (Default) 1 = Enabled | TORCH/TEMP Pin Enable 0 = Disabled (Default) 1 = Enabled | Mode Bits: M1, M0 '00' = Standby (Default) '01' = IR Drive '10' = Torch '11' = Flash | | LED Enable 00 = OFF (Default) 11 = ON 01 and 10 are not valid settings | |

NOTE

Edge Strobe Mode is not valid in IR MODE. Switching between Level and Edge Strobe Types while the device is enabled is not recommended.

In Edge or Level Strobe Mode, it is recommended that the trigger pulse width be set greater than 1 ms to ensure proper turn-on of the device.

7.6.2 IVFM Register (0x02)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|---|--|-------|-------|--|--|-------|
| RFU | UVLO Circuitry (Default) 0 = Disabled (Default) 1 = Enabled | IVFM Levels 000 = 2.9 V (Default) 001 = 3 V 010 = 3.1 V 011 = 3.2 V 100 = 3.3 V 101 = 3.4 V 110 = 3.5 V 111 = 3.6 V | | | IVFM Hysteresis 0 = 0 mV (Default) 1 = 50 mV | IVFM Selection 00 = Disabled 01 = Stop and Hold Mode (Default) 10 = Down Mode 11 = Up and Down Mode | |

NOTE

IVFM Mode Bits are static once the LM3648 is enabled in Torch, Flash or IR modes. If the IVFM mode needs to be updated, disable the device and then change the mode bits to the desired state.

7.6.3 LED Flash Brightness Register (0x03)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|-------|--|-------|-------|-------|-------|-------|
| MUST BE SET TO '10' FOR PROPER OPERATION | | LED Flash Brightness Level $I_{FLASH} \text{ (mA)} \approx (\text{Brightness Code} \times 23.45 \text{ mA}) + 21.8 \text{ mA}$ 000000 = 21.8 mA 011111 = 748.75 mA (Default) 111111 = 1.5 A | | | | | |

7.6.4 LED Torch Brightness Register (0x05)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--|-------|--|-------|-------|-------|-------|-------|
| MUST BE SET TO '1' FOR PROPER OPERATION | | LED Torch Brightness Levels $I_{TORCH} \text{ (mA)} \approx (\text{Brightness Code} \times 2.8 \text{ mA}) + 1.954 \text{ mA}$ 0000000 = 1.954 mA 0111111 = 178.35 mA (Default) 1111111 = 357.6mA | | | | | |

7.6.5 Boost Configuration Register (0x07)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|-------|-------|-------|--|---|---|--|
| Software Reset Bit 0 = Not Reset (Default) 1 = Reset | RFU | RFU | RFU | LED Pin Short Fault Detect 0 = Disabled (Default) 1 = Enabled (Default) | Boost Mode 0 = Normal (Default) 1 = Pass Mode Only | Boost Frequency Select 0 = 2 MHz (Default) 1 = 4 MHz | Boost Current Limit Setting 0 = 1.9 A 1 = 2.8 A (Default) |

7.6.6 Timing Configuration Register (0x08)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|--|-------|-------|---|-------|-------|-------|
| RFU | Torch Current Ramp Time 000 = No Ramp 001 = 1 ms (Default) 010 = 32 ms 011 = 64 ms 100 = 128 ms 101 = 256 ms 110 = 512 ms 111 = 1024 ms | | | Flash Time-Out Duration 0000 = 10 ms 0001 = 20 ms 0010 = 30 ms 0011 = 40 ms 0100 = 50 ms 0101 = 60 ms 0110 = 70 ms 0111 = 80 ms 1000 = 90 ms 1001 = 100 ms 1010 = 150 ms (Default) 1011 = 200 ms 1100 = 250 ms 1101 = 300 ms 1110 = 350 ms 1111 = 400 ms | | | |

7.6.7 TEMP Register (0x09)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|---|--|---|--|-------|--|-------|
| RFU | TORCH Polarity 0 = Active High (Default) (Pulldown Resistor Enabled) 1 = Active Low (Pulldown Resistor Disabled) | NTC Open Fault Enable 0 = Disabled (Default) 1 = Enable | NTC Short Fault Enable 0 = Disabled (Default) 1 = Enable | TEMP Detect Voltage Threshold 000 = 0.2 V 001 = 0.3 V 010 = 0.4 V 011 = 0.5 V 100 = 0.6 V (Default) 101 = 0.7 V 110 = 0.8 V 111 = 0.9 V | | TORCH/TEMP Function Select 0 = TORCH (Default) 1 = TEMP | |

NOTE

The Torch Polarity bit is static once the LM3648 is enabled in Torch, Flash, or IR modes. If the Torch Polarity bit needs to be updated, disable the device and then change the Torch Polarity bit to the desired state.

7.6.8 Flags1 Register (0x0A)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------------------------|------------------|------------------|--------------------|------------------------------|------------|---------------------|
| TX Flag | V _{OUT} Short Fault | VLED Short Fault | VLED Short Fault | Current Limit Flag | Thermal Shutdown (TSD) Fault | UVLO Fault | Flash Time-Out Flag |

7.6.9 Flags2 Register (0x0B)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-----------------|----------------|----------------|-----------|-----------------|
| RFU | RFU | RFU | NTC Short Fault | NTC Open Fault | IVFM Trip Flag | OVP Fault | TEMP Trip Fault |

7.6.10 Device ID Register (0x0C)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-----------------|-------|-------|----------------------------|-------|-------|
| RFU | RFU | Device ID '011' | | | Silicon Revision Bit '010' | | |

7.6.11 Last Flash Register (0x0D)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|--|-------|-------|-------|-------|-------|-------|
| RFU | The value stored is always the last current value the IVFM detection block set. $I_{LED} = I_{FLASH-TARGET} \times ((Code + 1) / 128)$ | | | | | | |

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM3648 can drive a flash LED at currents up to 1.5 A. The 2-MHz/4-MHz DC/DC boost regulator allows for the use of small value discrete external components.

8.2 Typical Application

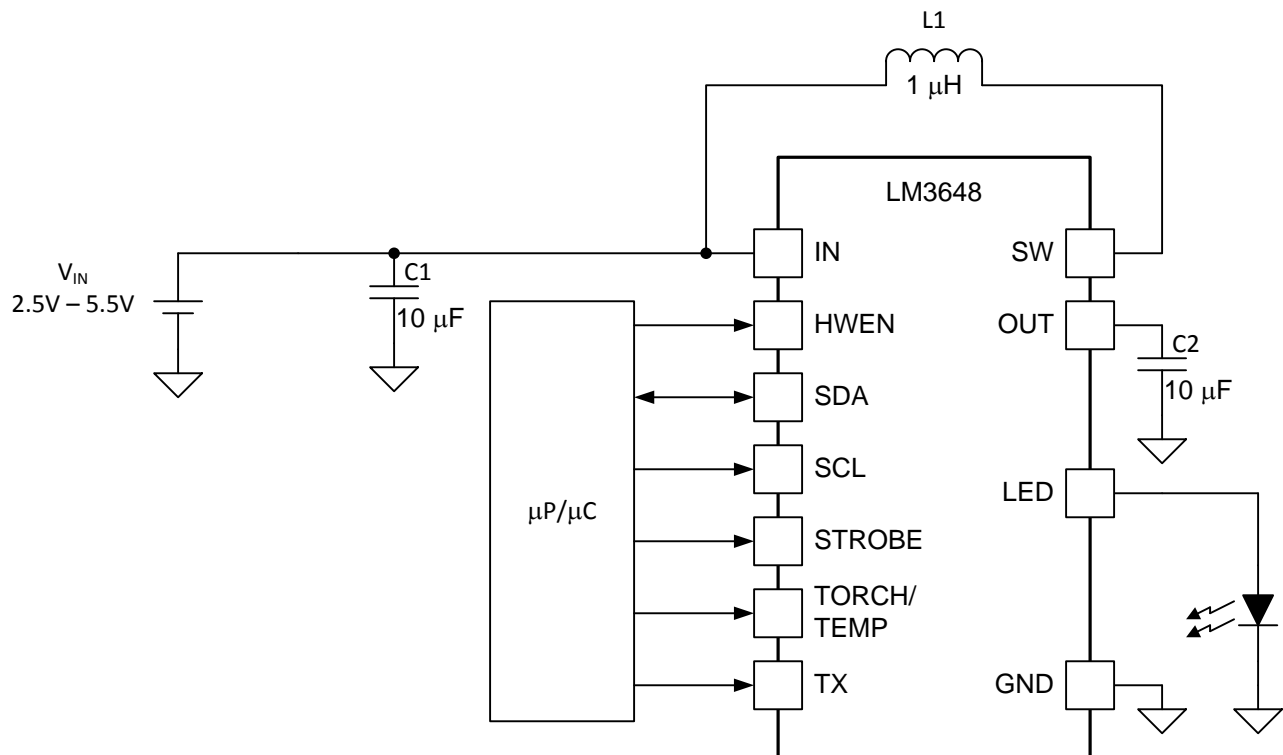


Figure 28. LM3648 Typical Application

8.2.1 Design Requirements

Example requirements based on default register values:

| DESIGN PARAMETER | EXAMPLE VALUE |
|---------------------------|---------------------------|
| Input Voltage Range | 2.5 V to 5.5 V |
| Brightness Control | I ² C Register |
| LED Configuration | 1 Flash LED |
| Boost Switching Frequency | 2 MHz (4 MHz selectable) |
| Flash Brightness | 1.5-A Max Current |

8.2.2 Detailed Design Procedure

8.2.2.1 Output Capacitor Selection

The LM3648 is designed to operate with a 10-μF ceramic output capacitor. When the boost converter is running, the output capacitor supplies the load current during the boost converter on-time. When the NMOS switch turns off, the inductor energy is discharged through the internal PMOS switch, supplying power to the load and restoring charge to the output capacitor. This causes a sag in the output voltage during the on-time and a rise in the output voltage during the off-time. The output capacitor is therefore chosen to limit the output ripple to an acceptable level depending on load current and input/output voltage differentials and also to ensure the converter remains stable.

Larger capacitors such as a 22-μF or capacitors in parallel can be used if lower output voltage ripple is desired. To estimate the output voltage ripple considering the ripple due to capacitor discharge (ΔV_Q) and the ripple due to the capacitors ESR (ΔV_{ESR}) use the following equations:

For continuous conduction mode, the output voltage ripple due to the capacitor discharge is:

$$\Delta V_Q = \frac{I_{LED} \times (V_{OUT} - V_{IN})}{f_{SW} \times V_{OUT} \times C_{OUT}} \quad (1)$$

The output voltage ripple due to the output capacitors ESR is found by:

$$\Delta V_{ESR} = R_{ESR} \times \left(\frac{I_{LED} \times V_{OUT}}{V_{IN}} + \Delta I_L \right)$$

where
$$\Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \quad (2)$$

In ceramic capacitors the ESR is very low so the assumption is that 80% of the output voltage ripple is due to capacitor discharge and 20% from ESR. [Table 1](#) lists different manufacturers for various output capacitors and their case sizes suitable for use with the LM3648.

8.2.2.2 Input Capacitor Selection

Choosing the correct size and type of input capacitor helps minimize the voltage ripple caused by the switching of the LM3648 boost converter and reduce noise on the boost converter's input pin that can feed through and disrupt internal analog signals. In the typical application circuit a 10-μF ceramic input capacitor works well. It is important to place the input capacitor as close as possible to the LM3648 input (IN) pin. This reduces the series resistance and inductance that can inject noise into the device due to the input switching currents. [Table 1](#) lists various input capacitors recommended for use with the LM3648.

Table 1. Recommended Input/Output Capacitors (X5R/X7R Dielectric)

| MANUFACTURER | PART NUMBER | VALUE | CASE SIZE | VOLTAGE RATING |
|-----------------|-------------------|-------|-----------------------------------|----------------|
| TDK Corporation | C1608JB0J106M | 10 μF | 0603 (1.6 mm × 0.8 mm × 0.8 mm) | 6.3 V |
| TDK Corporation | C2012JB1A106M | 10 μF | 0805 (2.0 mm × 1.25 mm × 1.25 mm) | 10 V |
| Murata | GRM188R60J106M | 10 μF | 0603 (1.6 mm × 0.8 mm × 0.8 mm) | 6.3 V |
| Murata | GRM21BR61A106KE19 | 10 μF | 0805 (2.0 mm × 1.25 mm × 1.25 mm) | 10 V |

8.2.2.3 Inductor Selection

The LM3648 is designed to use a 0.47-μH or 1-μH inductor. [Table 2](#) lists various inductors and their manufacturers that work well with the LM3648. When the device is boosting ($V_{OUT} > V_{IN}$) the inductor is typically the largest area of efficiency loss in the circuit. Therefore, choosing an inductor with the lowest possible series resistance is important. Additionally, the saturation rating of the inductor should be greater than the maximum operating peak current of the LM3648. This prevents excess efficiency loss that can occur with inductors that operate in saturation. For proper inductor operation and circuit performance, ensure that the inductor saturation and the peak current limit setting of the LM3648 are greater than I_{PEAK} in the following calculation:

$$I_{PEAK} = \frac{I_{LOAD}}{\eta} \times \frac{V_{OUT}}{V_{IN}} + \Delta I_L \quad \text{where} \quad \Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

where

- $f_{SW} = 2$ or 4 MHz

(3)

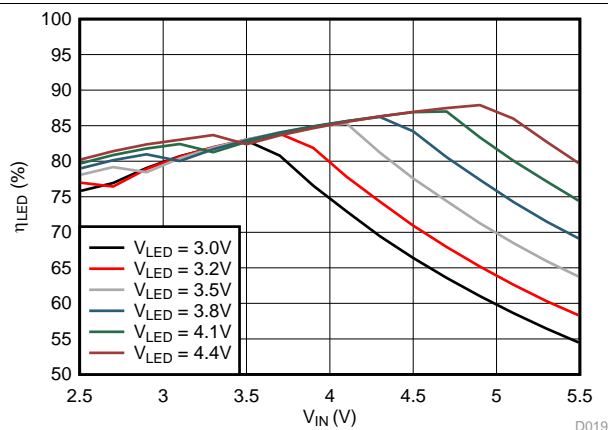
Efficiency details can be found in the [Application Curves](#).

Table 2. Recommended Inductors

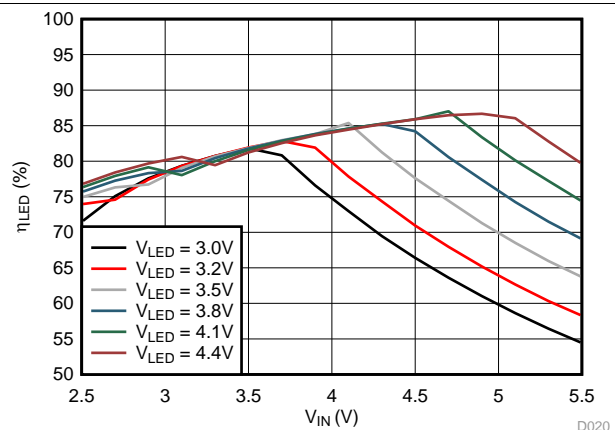
| MANUFACTURER | L | PART NUMBER | DIMENSIONS (LxWxH) | I _{SAT} | R _{DC} |
|--------------|---------|------------------|--------------------------|------------------|-----------------|
| TOKO | 0.47 µH | DFE201610P-R470M | 2.0 mm x 1.6 mm x 1.0 mm | 4.1 A | 32 mΩ |
| TOKO | 1 µH | DFE201610P-1R0M | 2.0 mm x 1.6 mm x 1.0 mm | 3.7 A | 58 mΩ |

8.2.3 Application Curves

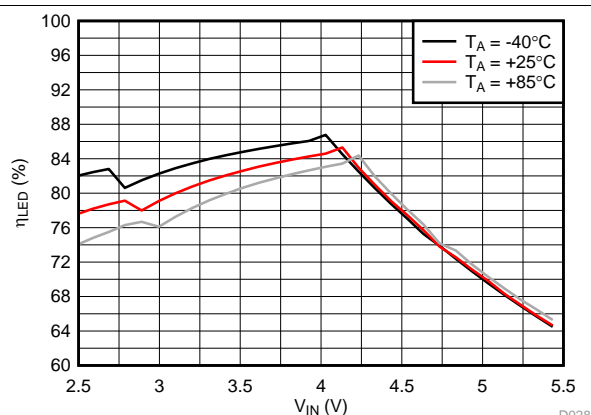
Ambient temperature is 25°C, input voltage is 3.6 V, HWEN = V_{IN}, C_{IN} = 2 × 10 µF, C_{OUT} = 2 × 10 µF and L = 1 µH, unless otherwise noted.



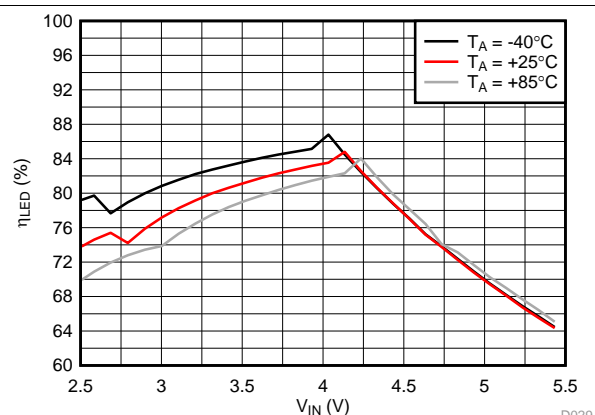
$f_{SW} = 2$ MHz
Brightness Code = 0x3F

Figure 29. 2-MHz LED Efficiency vs Input Voltage


$f_{SW} = 4$ MHz
Brightness Code = 0x3F

Figure 30. 4-MHz LED Efficiency vs Input Voltage


$f_{SW} = 2$ MHz
Brightness Code = 0x3F

Figure 31. LED Efficiency vs Input Voltage


$f_{SW} = 4$ MHz
Brightness Code = 0x3F

Figure 32. LED Efficiency vs Input Voltage

Ambient temperature is 25°C, input voltage is 3.6 V, $H_{WEN} = V_{IN}$, $C_{IN} = 2 \times 10 \mu F$, $C_{OUT} = 2 \times 10 \mu F$ and $L = 1 \mu H$, unless otherwise noted.

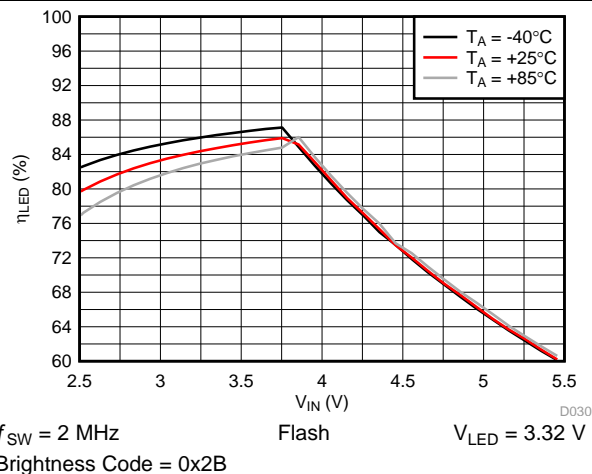


Figure 33. LED Efficiency vs Input Voltage

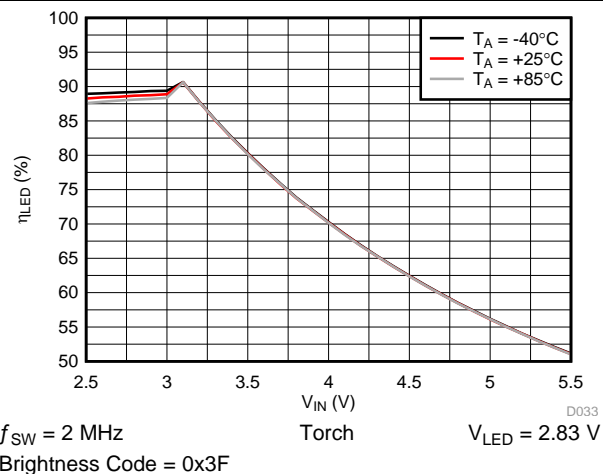


Figure 34. LED Efficiency vs Input Voltage

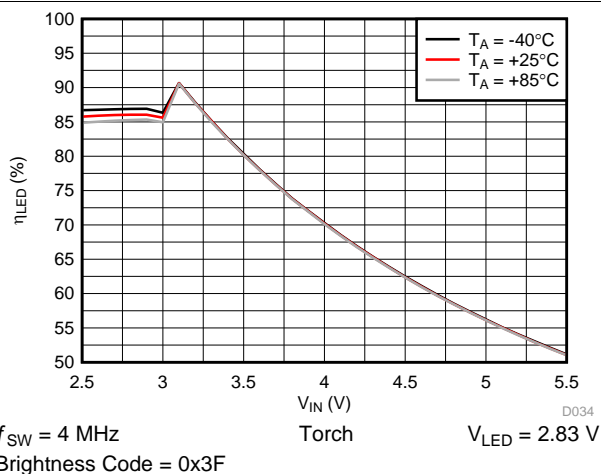


Figure 35. LED Efficiency vs Input Voltage

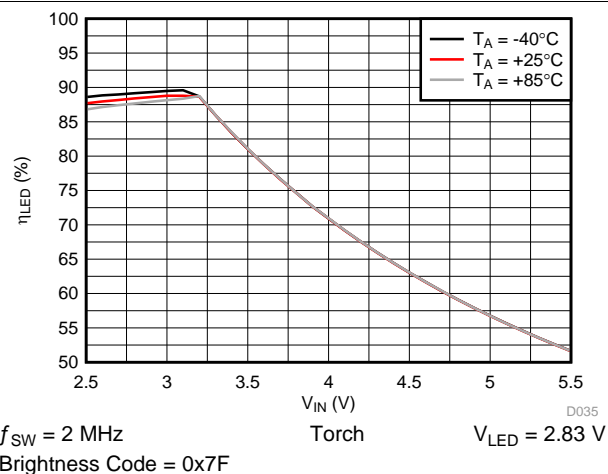


Figure 36. LED Efficiency vs Input Voltage

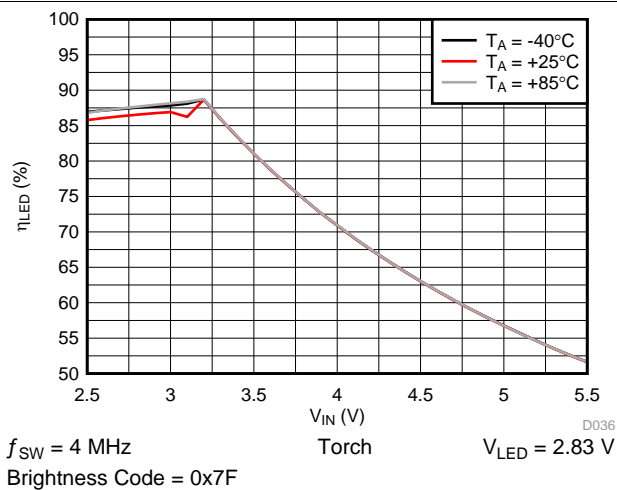


Figure 37. LED Efficiency vs Input Voltage

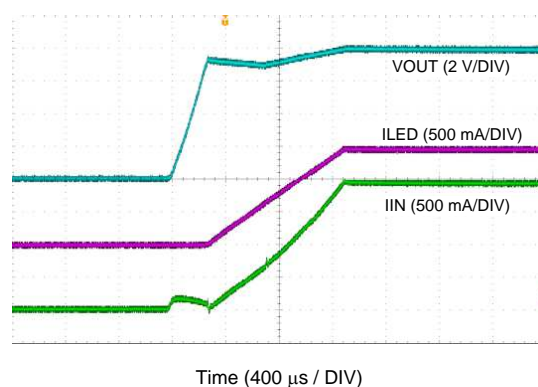


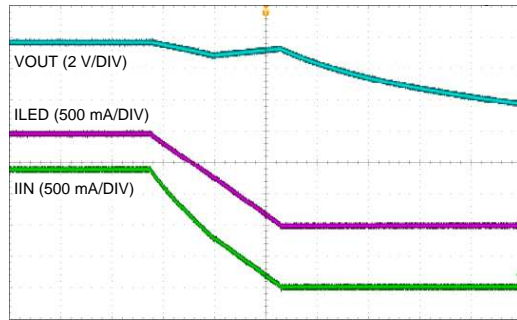
Figure 38. Start-Up

LM3648

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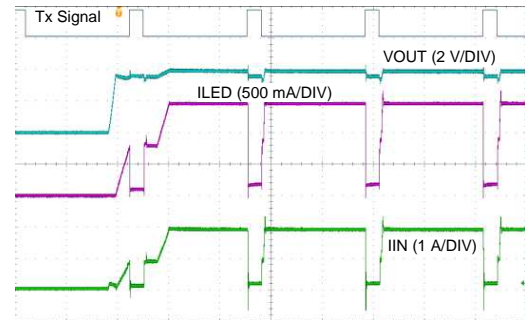
Ambient temperature is 25°C, input voltage is 3.6 V, HWEN = V_{IN} , $C_{IN} = 2 \times 10 \mu F$, $C_{OUT} = 2 \times 10 \mu F$ and $L = 1 \mu H$, unless otherwise noted.



Time (400 μs / DIV)

$f_{SW} = 2 \text{ MHz}$
Brightness Code = 0x7F
 $V_{LED} = 3.18 \text{ V}$

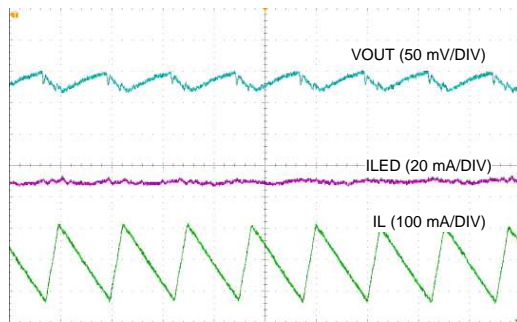
Figure 39. Ramp Down



Time (2 ms / DIV)

$f_{SW} = 2 \text{ MHz}$
Brightness Code = 0x7F
 $V_{LED} = 3.18 \text{ V}$

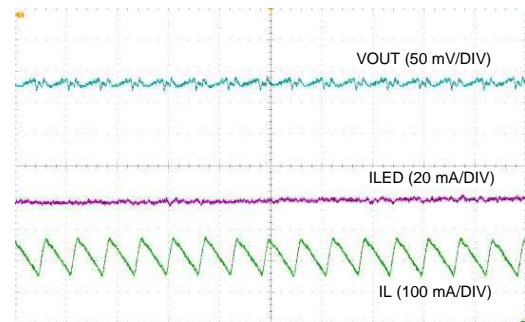
Figure 40. TX Interrupt



Time (400 ns / DIV)

$f_{SW} = 2 \text{ MHz}$
Brightness Code = 0x7F
 $V_{LED} = 3.18 \text{ V}$

Figure 41. Ripple @ 2 MHz



Time (400 ns / DIV)

$f_{SW} = 4 \text{ MHz}$
Brightness Code = 0x7F
 $V_{LED} = 3.18 \text{ V}$

Figure 42. Ripple @ 4 MHz

9 Power Supply Recommendations

The LM3648 is designed to operate from an input voltage supply range between 2.5 V and 5.5 V. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the LM3648 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

The high switching frequency and large switching currents of the LM3648 make the choice of layout important. The following steps should be used as a reference to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range.

1. Place C_{IN} on the top layer (same layer as the LM3648) and as close to the device as possible. The input capacitor conducts the driver currents during the low-side MOSFET turnon and turnoff and can detect current spikes over 1 A in amplitude. Connecting the input capacitor through short, wide traces to both the IN and GND pins reduces the inductive voltage spikes that occur during switching which can corrupt the V_{IN} line.
2. Place C_{OUT} on the top layer (same layer as the LM3648) and as close as possible to the OUT and GND pins. The returns for both C_{IN} and C_{OUT} should come together at one point, as close to the GND pin as possible. Connecting C_{OUT} through short, wide traces reduce the series inductance on the OUT and GND pins that can corrupt the V_{OUT} and GND lines and cause excessive noise in the device and surrounding circuitry.
3. Connect the inductor on the top layer close to the SW pin. There should be a low-impedance connection from the inductor to SW due to the large DC inductor current, and at the same time the area occupied by the SW node should be small so as to reduce the capacitive coupling of the high dV/dT present at SW that can couple into nearby traces.
4. Avoid routing logic traces near the SW node so as to avoid any capacitively coupled voltages from SW onto any high-impedance logic lines such as TORCH/TEMP, STROBE, HWEN, SDA, and SCL. A good approach is to insert an inner layer GND plane underneath the SW node and between any nearby routed traces. This creates a shield from the electric field generated at SW.
5. Terminate the Flash LED cathode directly to the GND pin of the LM3648. If possible, route the LED return with a dedicated path so as to keep the high amplitude LED current out of the GND plane. For a Flash LED that is routed relatively far away from the LM3648, a good approach is to sandwich the forward and return current paths over the top of each other on two layers. This helps reduce the inductance of the LED current path.

10.2 Layout Example

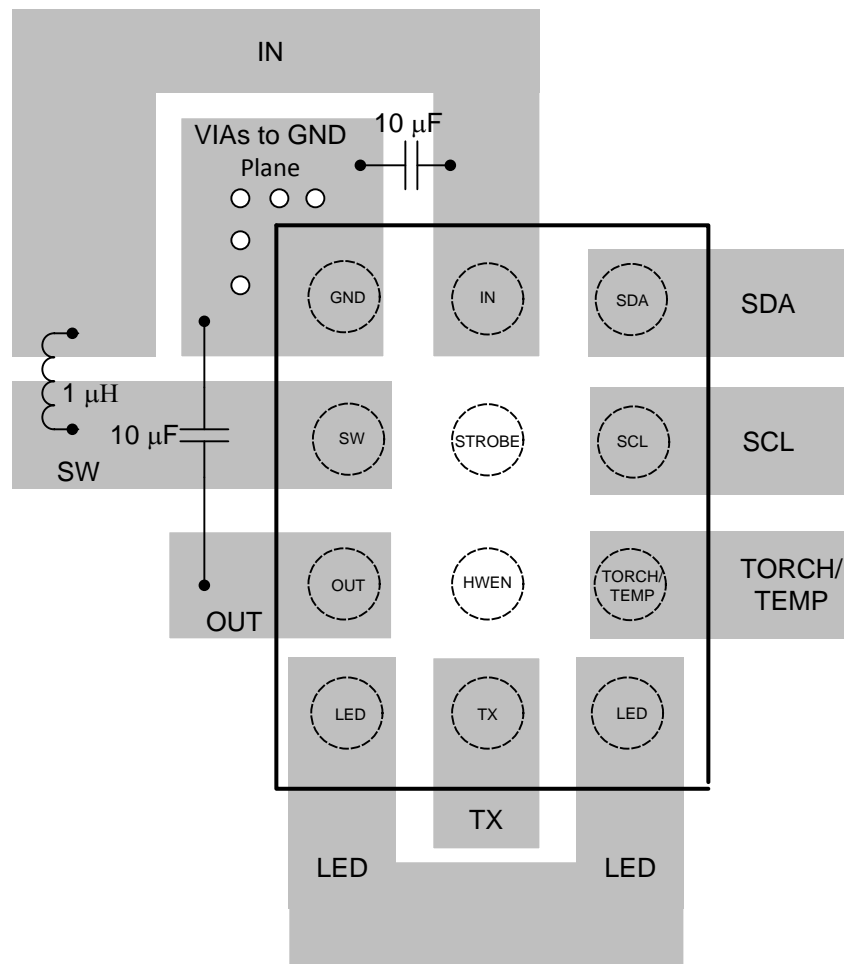


Figure 43. LM3648 Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

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11.2 文档支持

11.2.1 相关文档

相关文档如下：

德州仪器 (TI) 应用手册 1112: 《DSBGA 晶圆级芯片规模封装》（文献编号: [SNVA009](#)）。

11.3 商标

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ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| LM3648TTYFFR | Active | Production | DSBGA (YFF) 12 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 3648TT |
| LM3648TTYFFR.A | Active | Production | DSBGA (YFF) 12 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 3648TT |
| LM3648YFFR | Active | Production | DSBGA (YFF) 12 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 3648 |
| LM3648YFFR.A | Active | Production | DSBGA (YFF) 12 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 3648 |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

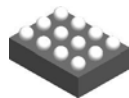
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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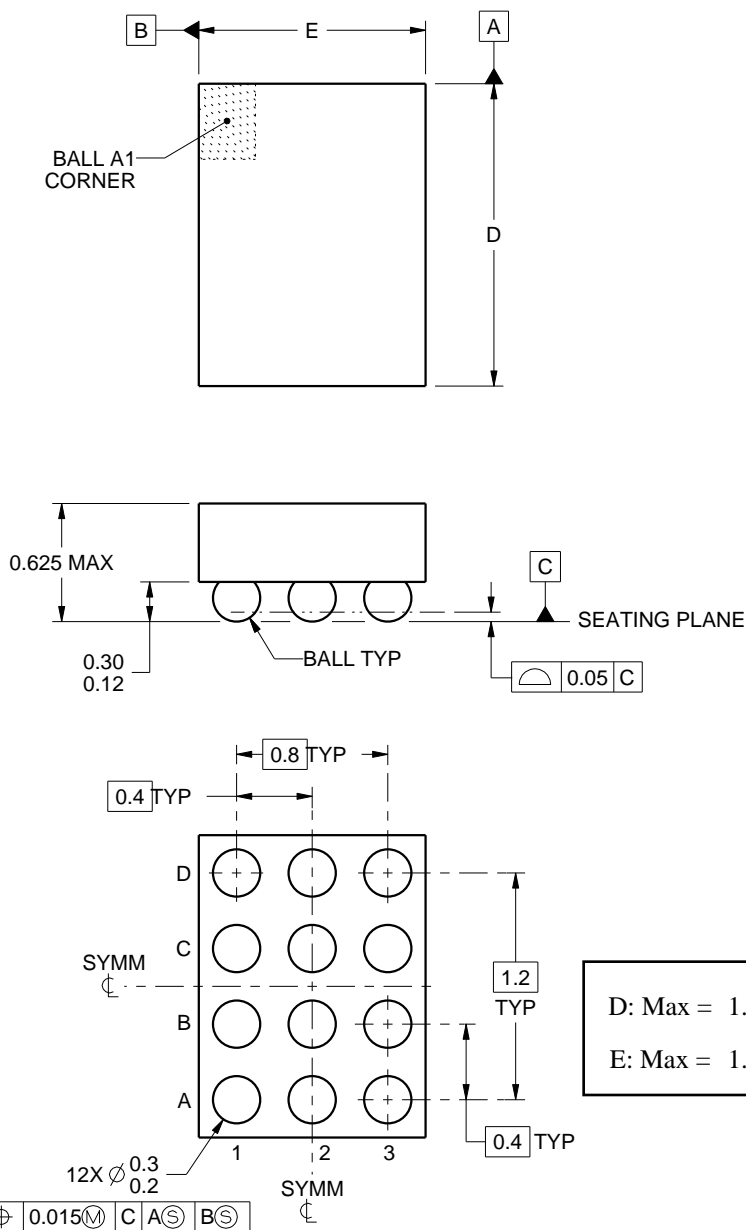
YFF0012



PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



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NOTES:

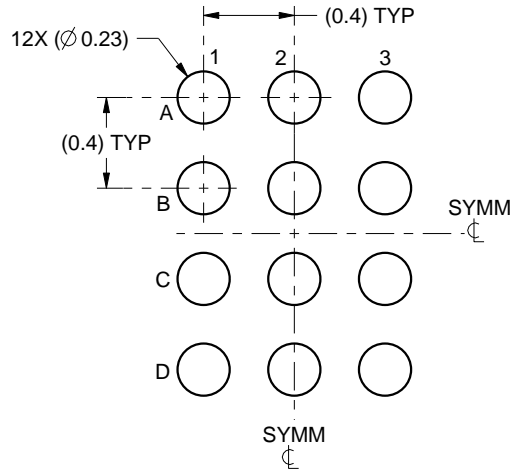
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

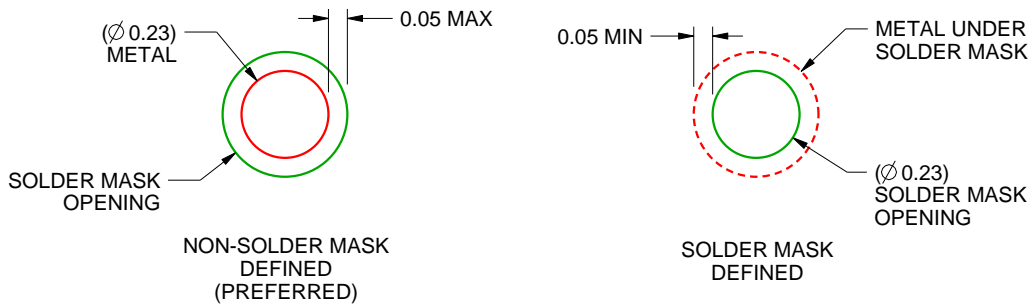
YFF0012

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

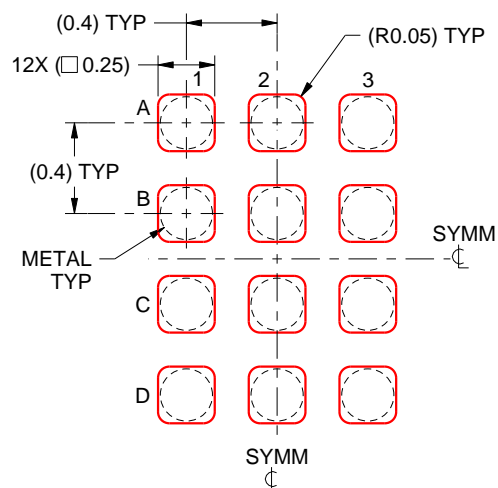
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFF0012

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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