LM4808 Boomer® Audio Power Amplifier Series
Low Voltage High Power Audio Power Amplifier

Check for Samples: LM4808

FEATURES

- **WSON, VSSOP, and SOIC Surface Mount Packaging**
- **Switch On/Off Click Suppression**
- **Excellent Power Supply Ripple Rejection**
- **Unity-Gain Stable**
- **Minimum External Components**

APPLICATIONS

- **Headphone Amplifier**
- **Personal Computers**
- **Portable Electronic Devices**

KEY SPECIFICATIONS

- **THD+N at 1kHz at 105mW Continuous Average Output Power Into 16Ω 0.1 % (typ)**
- **THD+N at 1kHz at 70mW Continuous Average Output Power Into 32Ω 0.1 % (typ)**
- **Output Power at 0.1% THD+N at 1kHz Into 32Ω 70 mW (typ)**

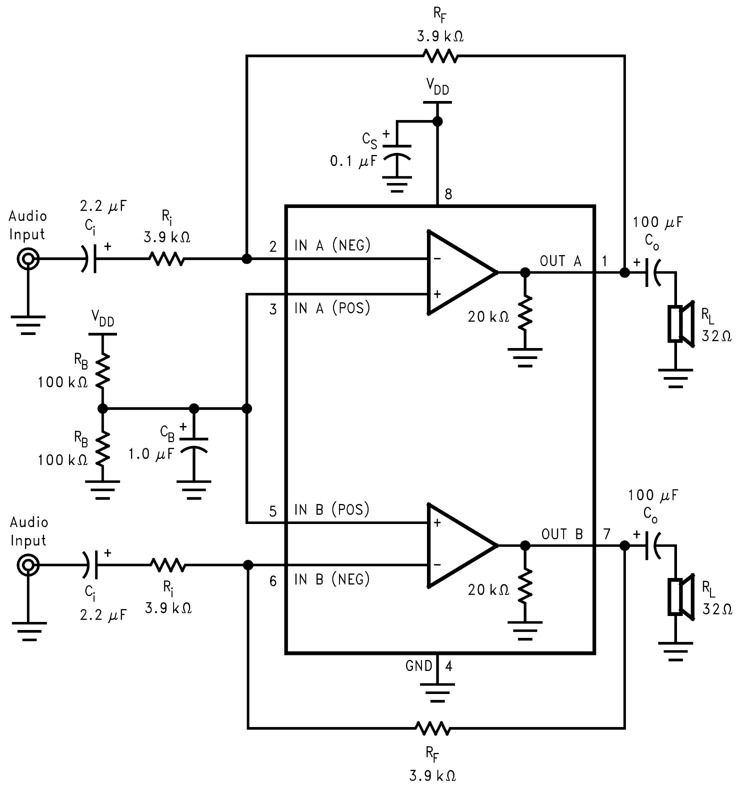
DESCRIPTION

The LM4808 is a dual audio power amplifier capable of delivering 105mW per channel of continuous average power into a 16Ω load with 0.1% (THD+N) from a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components using surface mount packaging. Since the LM4808 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

The unity-gain stable LM4808 can be configured by external gain-setting resistors.

Typical Application



*Refer to the APPLICATION INFORMATION section for information concerning proper selection of the input and output coupling capacitors.

Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram

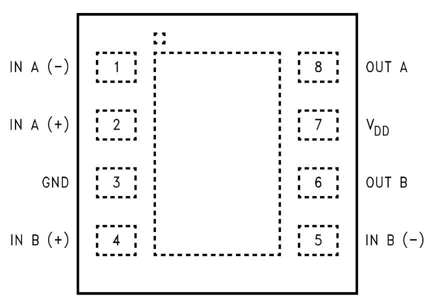


Figure 2. Top View
WSON Package
See Package Number NGL0008B

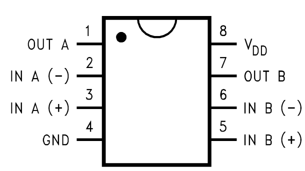


Figure 3. Top View
SOIC & VSSOP Package
See Package Number D0008A, DGK0008A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS [1][2]

Supply Voltage			6.0V
Storage Temperature			−65°C to +150°C
Input Voltage			−0.3V to V_{DD} + 0.3V
Power Dissipation [3]			Internally limited
ESD Susceptibility [4]			3500V
ESD Susceptibility [5]			250V
Junction Temperature			150°C
Soldering Information [6]	Small Outline Package	Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C
Thermal Resistance		θ_{JC} (VSSOP)	56°C/W
		θ_{JA} (VSSOP)	210°C/W
		θ_{JC} (SOIC)	35°C/W
		θ_{JA} (SOIC)	170°C/W
		θ_{JC} (WSON)	15°C/W
		θ_{JA} (WSON)	117°C/W [7]
		θ_{JA} (WSON)	150°C/W [8]

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$. For the LM4808, T_{JMAX} = 150°C, and the typical junction-to-ambient thermal resistance, when board mounted, is 210°C/W for package DGK0008A and 170°C/W for package D0008A.
(4) Human body model, 100 pF discharged through a 1.5 kΩ resistor.
(5) Machine Model, 220 pF–240 pF discharged through all pins.
(6) See http://www.ti.com for other methods of soldering surface mount devices.
(7) The given θ_{JA} is for an LM4808 packaged in an NGL0008B with the Exposed-DAP soldered to a printed circuit board copper pad with an area equivalent to that of the Exposed-DAP itself.
(8) The given θ_{JA} is for an LM4808 packaged in an NGL0008B with the Exposed-DAP not soldered to any printed circuit board copper.

OPERATING RATINGS

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤ T_A ≤ 85°C
Supply Voltage		2.0V ≤ V_{DD} ≤ 5.5V

ELECTRICAL CHARACTERISTICS [1] [2]

The following specifications apply for V_{DD} = 5V unless otherwise specified, limits apply to T_A = 25°C.

Symbol	Parameter	Conditions	LM4808		Units (Limits)
			Typ [3]	Limit [4]	
V_{DD}	Supply Voltage			2.0	V (min)
				5.5	V (max)
I_{DD}	Supply Current	V_{IN} = 0V, I_O = 0A	1.2	3.0	mA (max)

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Tested limits are specified to AOQL (Average Outgoing Quality Level). Datasheet min/max specification limits are specified by design, test, or statistical analysis.

ELECTRICAL CHARACTERISTICS (1) (2) (continued)

The following specifications apply for V_{DD} = 5V unless otherwise specified, limits apply to T_A = 25°C.

Symbol	Parameter	Conditions	LM4808 Typ (3)	LM4808 Limit (4)	Units (Limits)
P_{tot}	Total Power Dissipation	V_{IN} = 0V, I_O = 0A	6	16.5	mW (max)
V_{OS}	Input Offset Voltage	V_{IN} = 0V	10	50	mV (max)
Ibias	Input Bias Current		10		pA
V_{CM}	Common Mode Voltage		0		V
			4.3		V
G_V	Open-Loop Voltage Gain	R_L = 5kΩ	67		dB
Io	Max Output Current	THD+N < 0.1 %	70		mA
R_O	Output Resistance		0.1		Ω
V_O	Output Swing	R_L = 32Ω, 0.1% THD+N, Min	.3		V
		R_L = 32Ω, 0.1% THD+N, Max	4.7		
PSRR	Power Supply Rejection Ratio	Cb = 1.0µF, Vripple = 100mV_{PP}, f = 100Hz	89		dB
Crosstalk	Channel Separation	R_L = 32Ω	75		dB
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz			
		R_L = 16Ω, V_O =3.5V_{PP} (at 0 dB)	0.05		%
			66		dB
		R_L = 32Ω, V_O =3.5V_{PP} (at 0 dB)	0.05		%
			66		dB
SNR	Signal-to-Noise Ratio	V_O = 3.5V_{pp} (at 0 dB)	105		dB
f_G	Unity Gain Frequency	Open Loop, R_L = 5kΩ	5.5		MHz
P_o	Output Power	THD+N = 0.1%, f = 1 kHz			
		R_L = 16Ω	105		mW
		R_L = 32Ω	70	60	mW
		THD+N = 10%, f = 1 kHz			
		R_L = 16Ω	150		mW
		R_L = 32Ω	90		mW
C_I	Input Capacitance		3		pF
C_L	Load Capacitance			200	pF
SR	Slew Rate	Unity Gain Inverting	3		V/µs

ELECTRICAL CHARACTERISTICS (1) (2)

The following specifications apply for V_{DD} = 3.3V unless otherwise specified, limits apply to T_A = 25°C.

Symbol	Parameter	Conditions	Conditions Typ (3)	Conditions Limit (4)	Units (Limits)
I_{DD}	Supply Current	V_{IN} = 0V, I_O = 0A	1.0		mA (max)
V_{OS}	Input Offset Voltage	V_{IN} = 0V	7		mV (max)

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Tested limits are specified to AOQL (Average Outgoing Quality Level). Datasheet min/max specification limits are specified by design, test, or statistical analysis.

ELECTRICAL CHARACTERISTICS [1] [2] (continued)

The following specifications apply for V_{DD} = 3.3V unless otherwise specified, limits apply to T_A = 25°C.

Symbol	Parameter	Conditions	Conditions		Units (Limits)
			Typ [3]	Limit [4]	
P_o	Output Power	THD+N = 0.1%, f = 1 kHz			
		R_L = 16Ω	40		mW
		R_L = 32Ω	28		mW
		THD+N = 10%, f = 1 kHz			
		R_L = 16Ω	56		mW
		R_L = 32Ω	38		mW

ELECTRICAL CHARACTERISTICS [1] [2]

The following specifications apply for V_{DD} = 2.6V unless otherwise specified, limits apply to T_A = 25°C.

Symbol	Parameter	Conditions	Conditions		Units (Limits)
			Typ [3]	Limit [4]	
I_{DD}	Supply Current	V_{IN} = 0V, I_O = 0A	0.9		mA (max)
V_{OS}	Input Offset Voltage	V_{IN} = 0V	5		mV (max)
P_o	Output Power	THD+N = 0.1%, f = 1 kHz			
		R_L = 16Ω	20		mW
		R_L = 32Ω	16		mW
		THD+N = 10%, f = 1 kHz			
		R_L = 16Ω	31		mW
		R_L = 32Ω	22		mW

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Tested limits are specified to AOQL (Average Outgoing Quality Level). Datasheet min/max specification limits are specified by design, test, or statistical analysis.

EXTERNAL COMPONENTS DESCRIPTION

(Figure 1)

Components	Functional Description
1. R_i	The inverting input resistance, along with R_f, set the closed-loop gain. R_i, along with C_i, form a high pass filter with $f_c = 1/(2\pi R_i C_i)$.
2. C_i	The input coupling capacitor blocks DC voltage at the amplifier's input terminals. C_i, along with R_i, create a highpass filter with $f_C = 1/(2\pi R_i C_i)$. Refer to the section, SELECTING PROPER EXTERNAL COMPONENTS, for an explanation of determining the value of C_i.
3. R_f	The feedback resistance, along with R_i, set closed-loop gain.
4. C_S	This is the supply bypass capacitor. It provides power supply filtering. Refer to the APPLICATION INFORMATION section for proper placement and selection of the supply bypass capacitor.
5. C_B	This is the half-supply bypass pin capacitor. It provides half-supply filtering. Refer to the section, SELECTING PROPER EXTERNAL COMPONENTS, for information concerning proper placement and selection of C_B.
6. C_O	This is the output coupling capacitor. It blocks the DC voltage at the amplifier's output and forms a high pass filter with R_L at $f_O = 1/(2\pi R_L C_O)$
7. R_B	This is the resistor which forms a voltage divider that provides 1/2 V_{DD} to the non-inverting input of the amplifier.

TYPICAL PERFORMANCE CHARACTERISTICS

THD+N vs Frequency

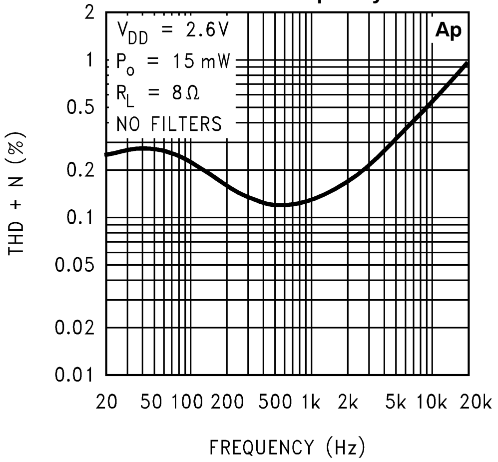


Figure 4.

THD+N vs Frequency

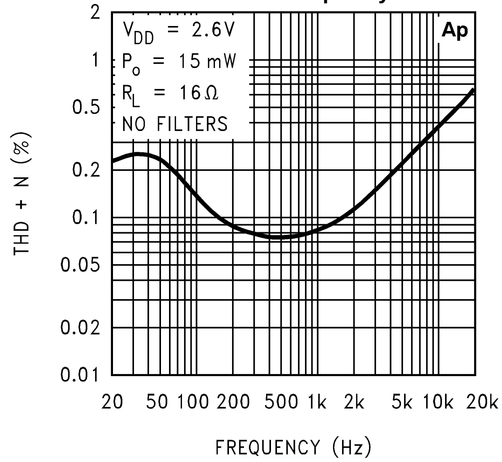


Figure 5.

THD+N vs Frequency

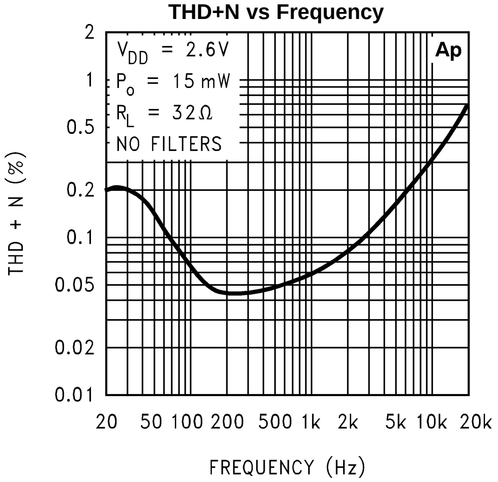


Figure 6.

THD+N vs Frequency

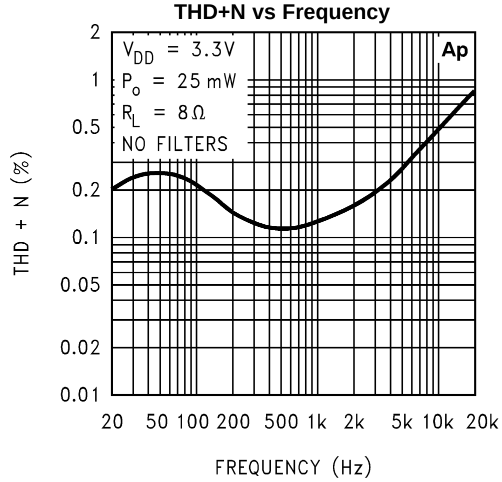


Figure 7.

THD+N vs Frequency

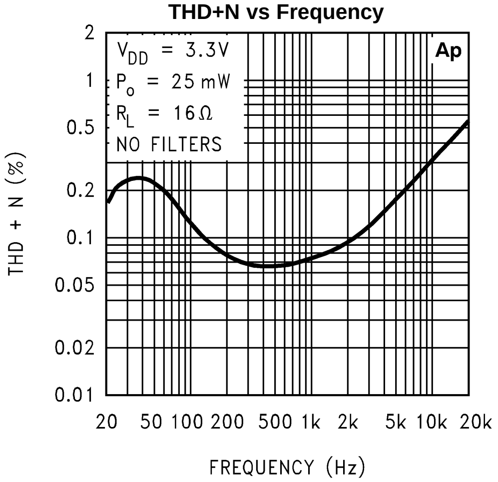


Figure 8.

THD+N vs Frequency

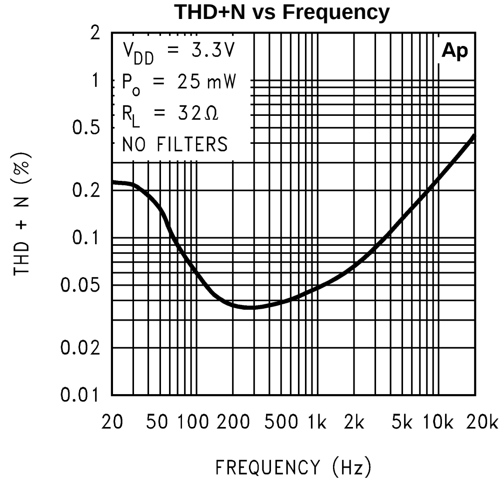


Figure 9.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

THD+N vs Frequency

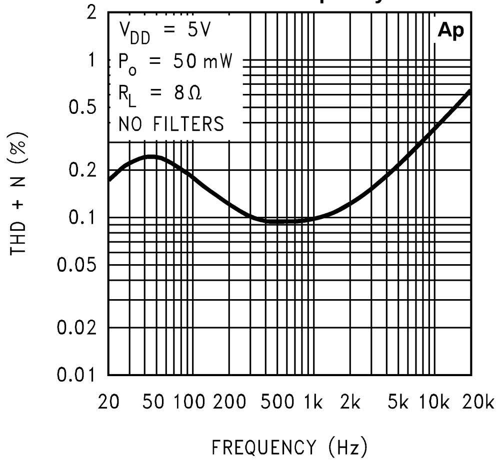


Figure 10.

THD+N vs Frequency

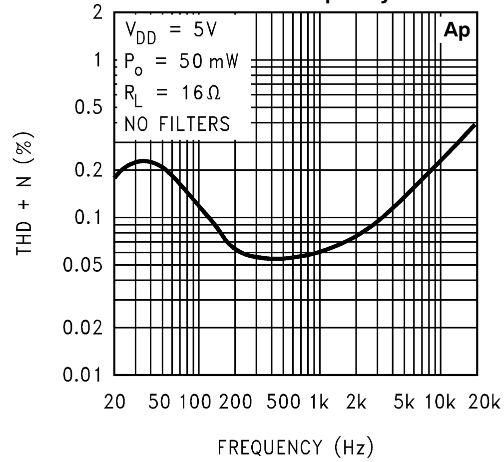


Figure 11.

THD+N vs Frequency

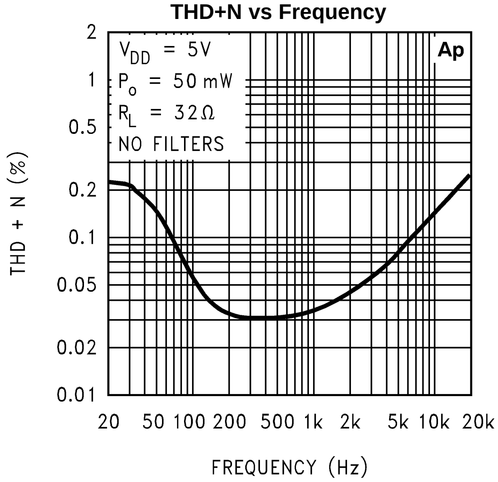


Figure 12.

THD+N vs Frequency

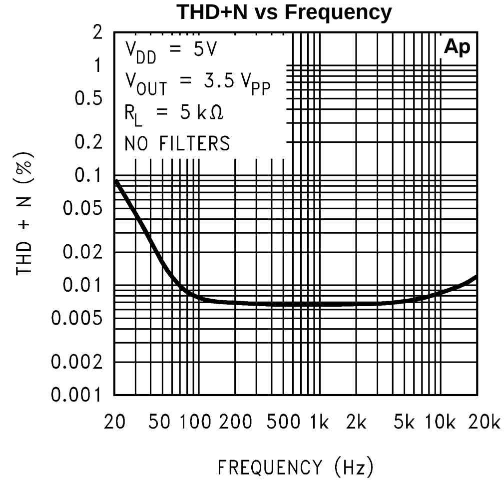


Figure 13.

THD+N vs Output Power

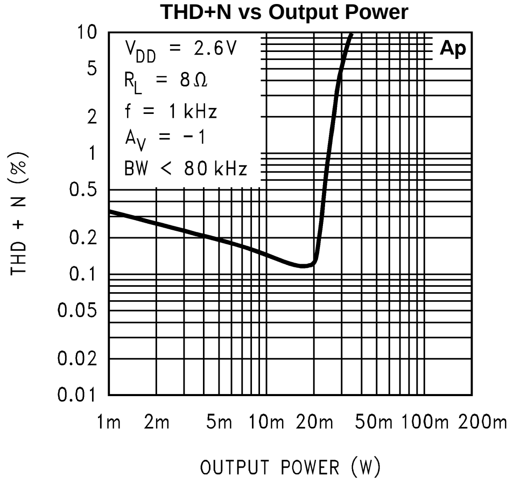


Figure 14.

THD+N vs Output Power

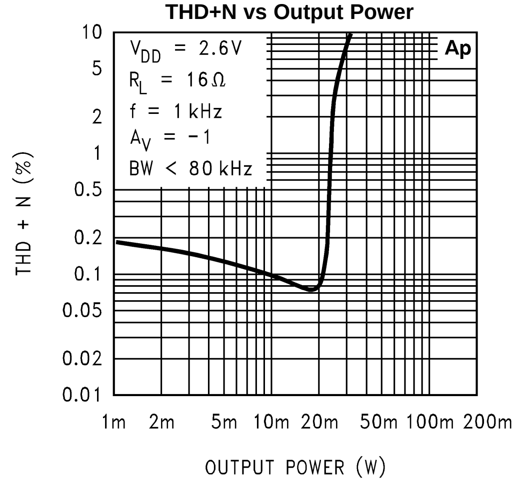


Figure 15.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

THD+N vs Output Power

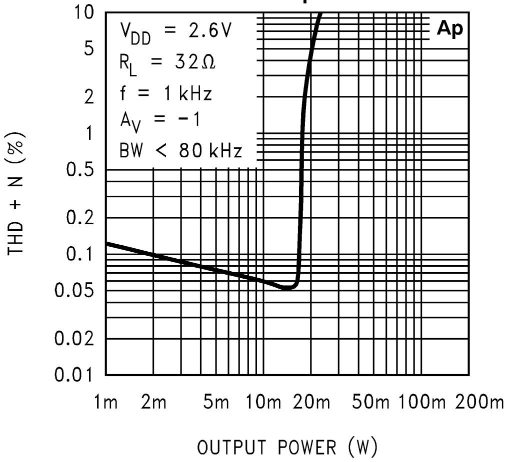


Figure 16.

THD+N vs Output Power

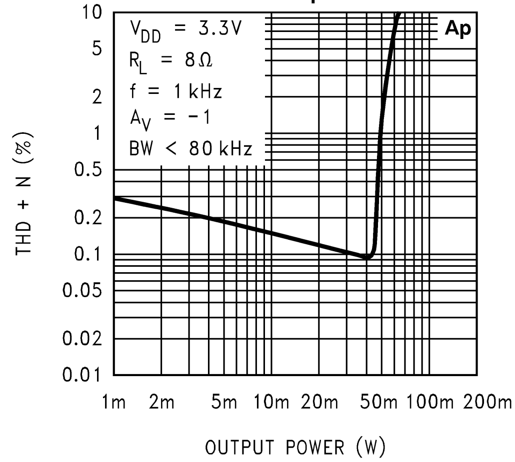


Figure 17.

THD+N vs Output Power

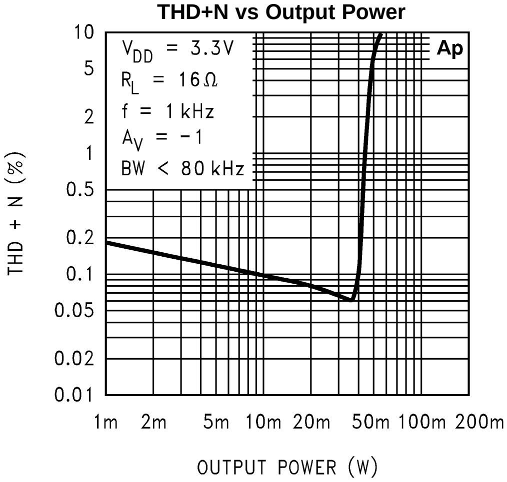


Figure 18.

THD+N vs Output Power

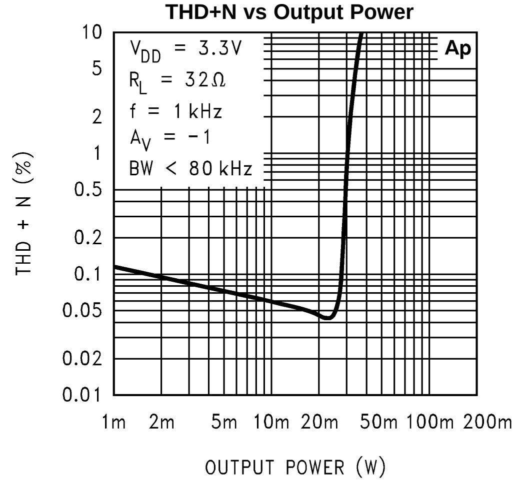


Figure 19.

THD+N vs Output Power

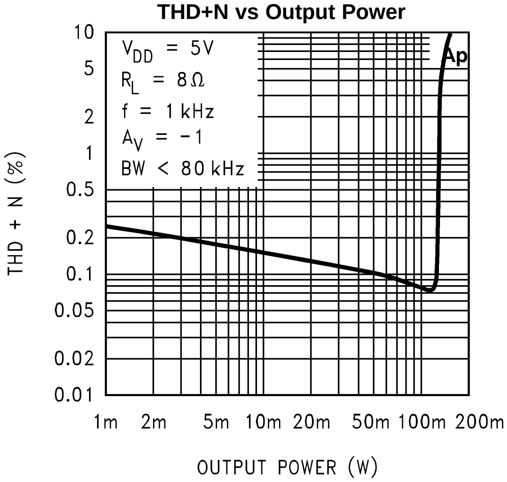


Figure 20.

THD+N vs Output Power

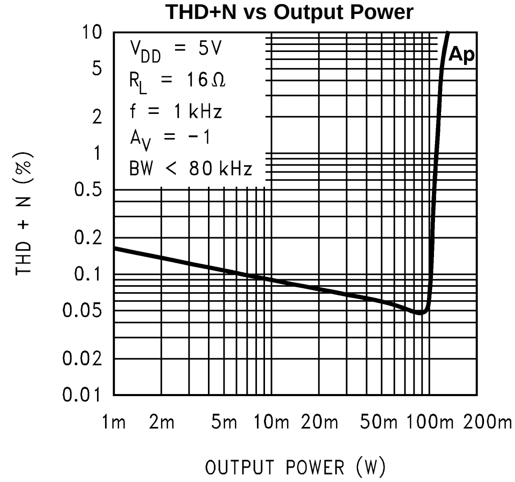


Figure 21.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

THD+N vs Output Power

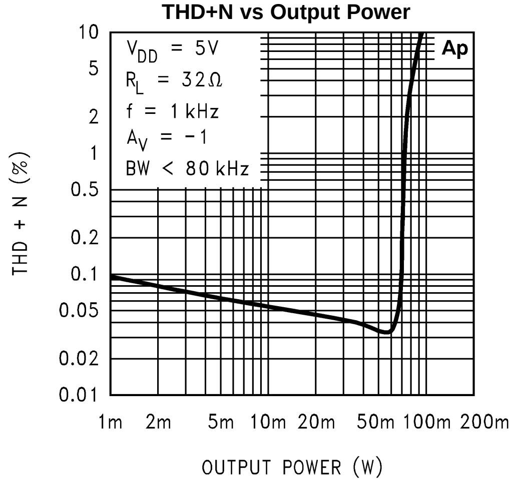


Figure 22.

Output Power vs Load Resistance

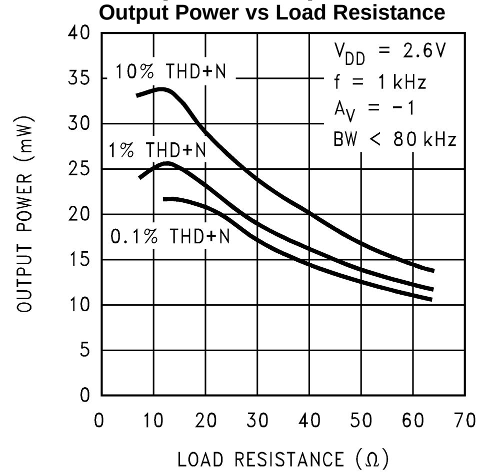


Figure 23.

Output Power vs Load Resistance

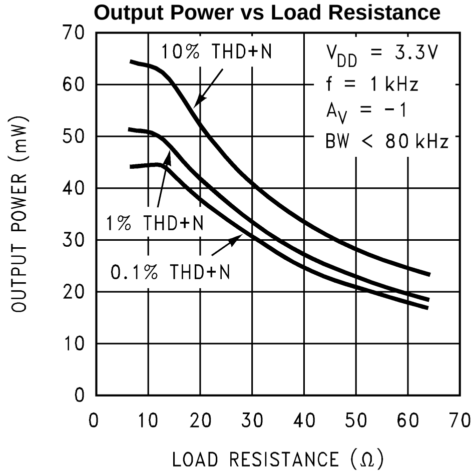


Figure 24.

Output Power vs Load Resistance

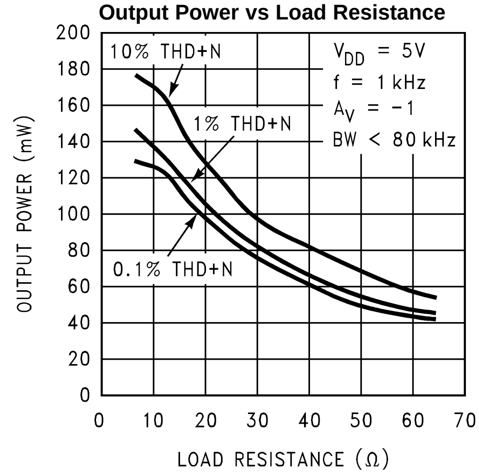


Figure 25.

Output Power vs Supply Voltage

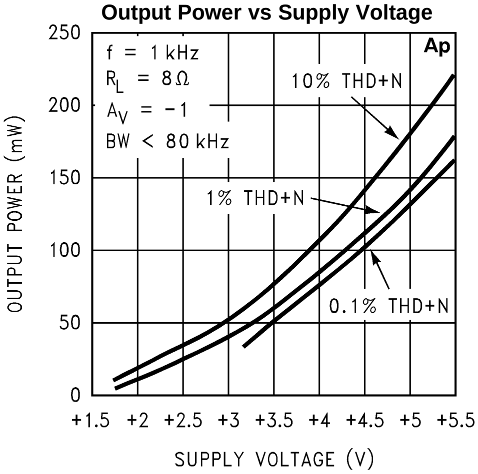


Figure 26.

Output Power vs Power Supply

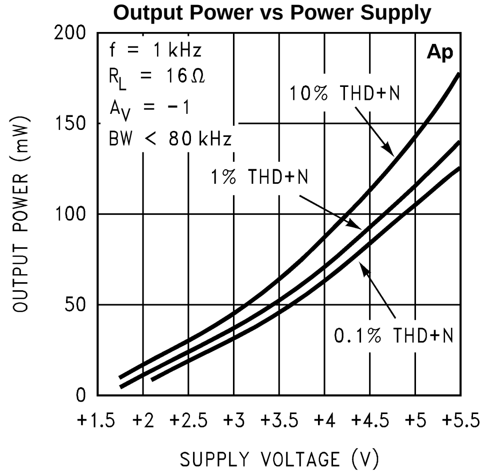


Figure 27.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Output Power vs Power Supply

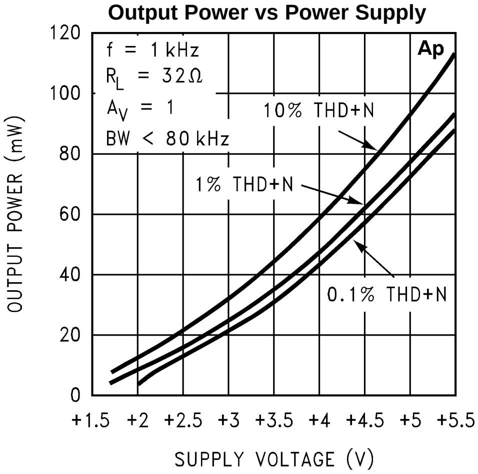


Figure 28.

Clipping Voltage vs Supply Voltage

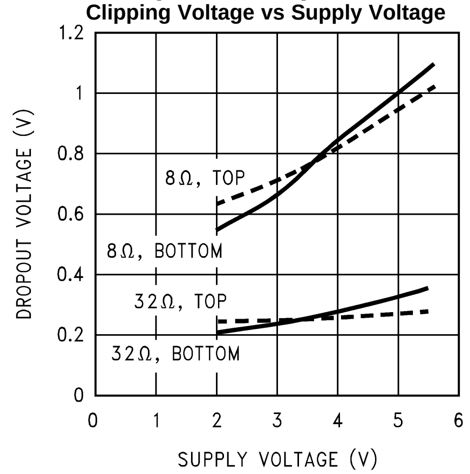


Figure 29.

Power Dissipation vs Output Power

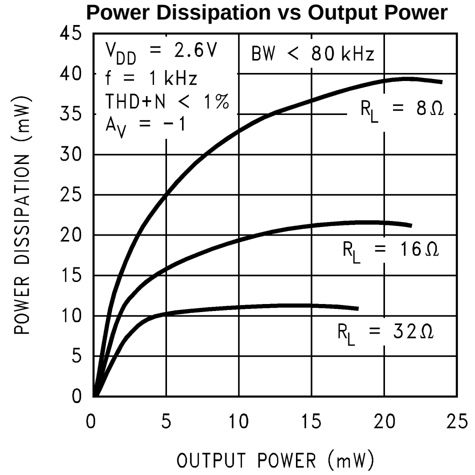


Figure 30.

Power Dissipation vs Output Power

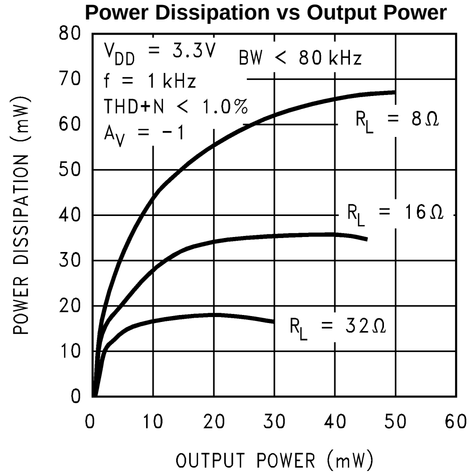


Figure 31.

Power Dissipation vs Output Power

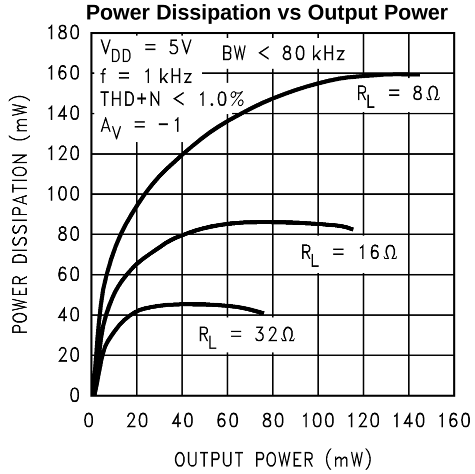


Figure 32.

Channel Separation

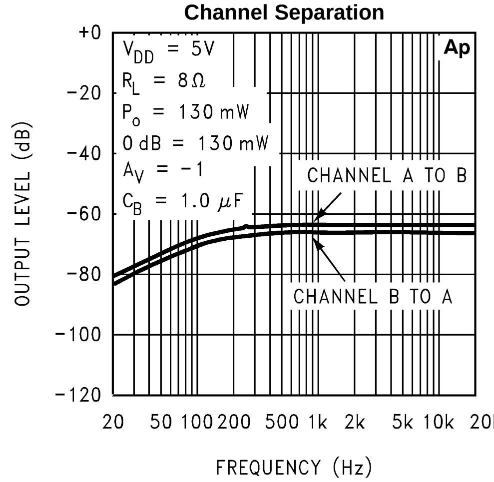


Figure 33.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Channel Separation

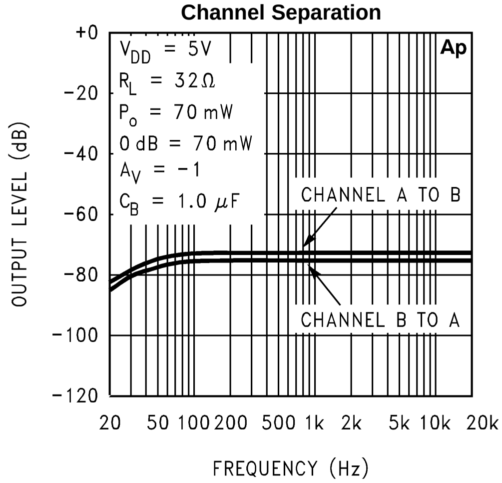


Figure 34.

Noise Floor

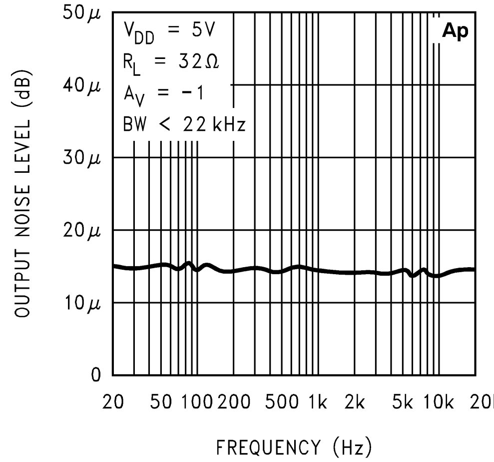


Figure 35.

Power Supply Rejection Ratio

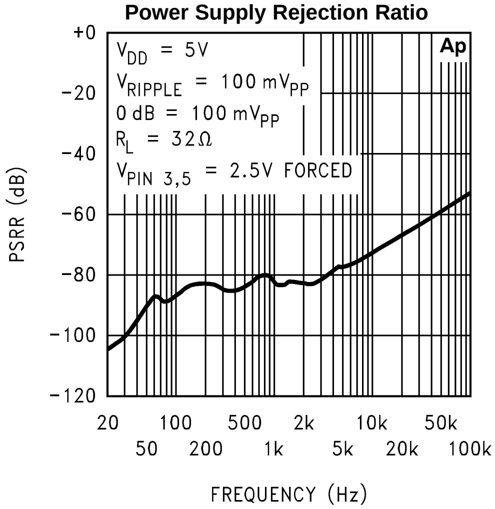


Figure 36.

Frequency Response

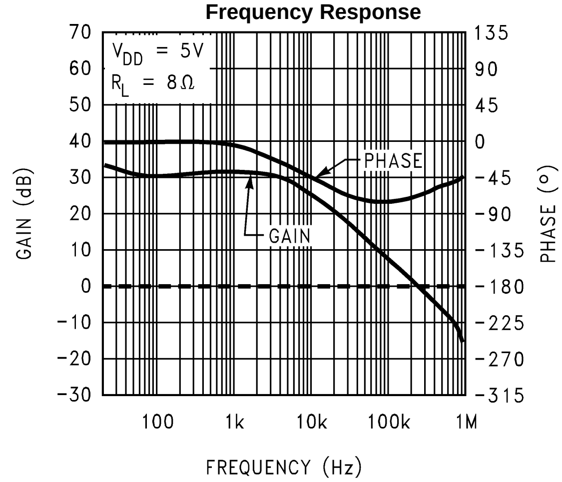


Figure 37.

Open Loop Frequency Response

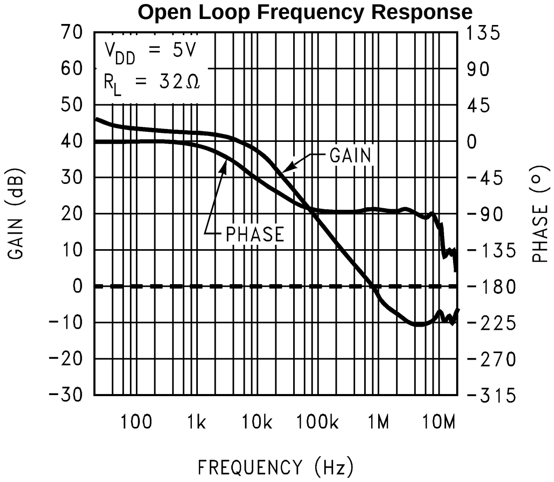


Figure 38.

Open Loop Frequency Response

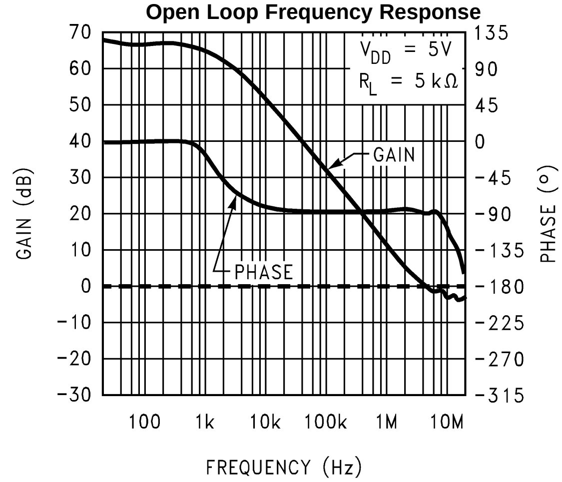


Figure 39.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Supply Current vs Supply Voltage

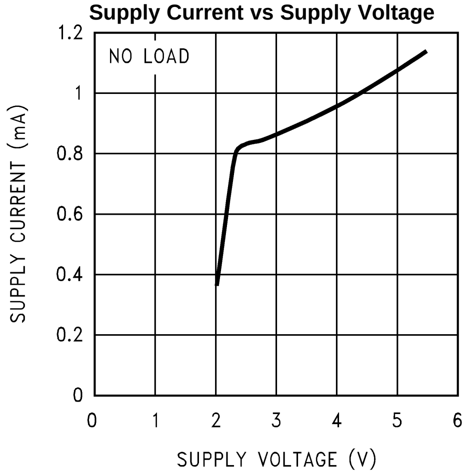


Figure 40.

Frequency Response vs Output Capacitor Size

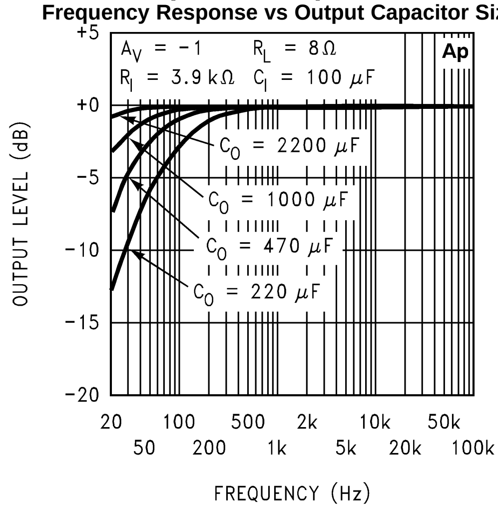


Figure 41.

Frequency Response vs Output Capacitor Size

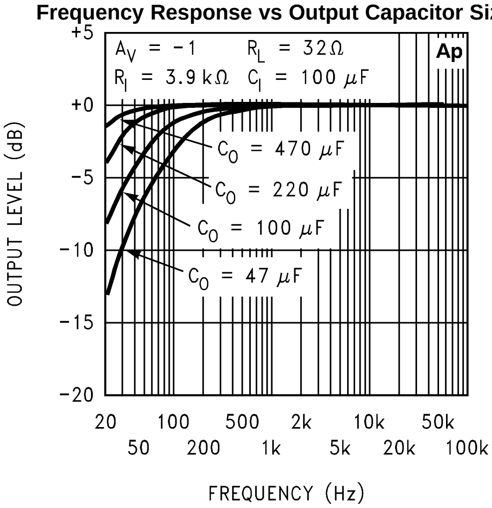


Figure 42.

Frequency Response vs Output Capacitor Size

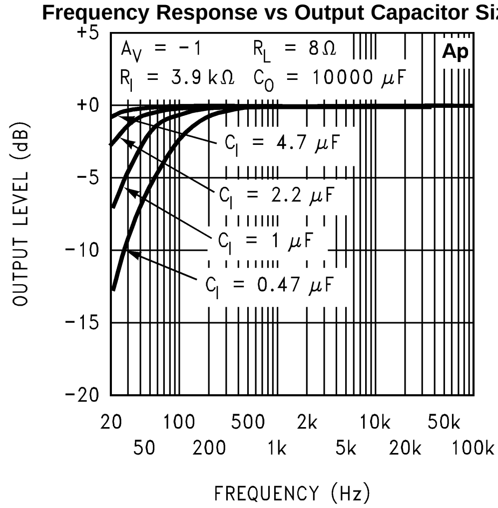


Figure 43.

Typical Application Frequency Response

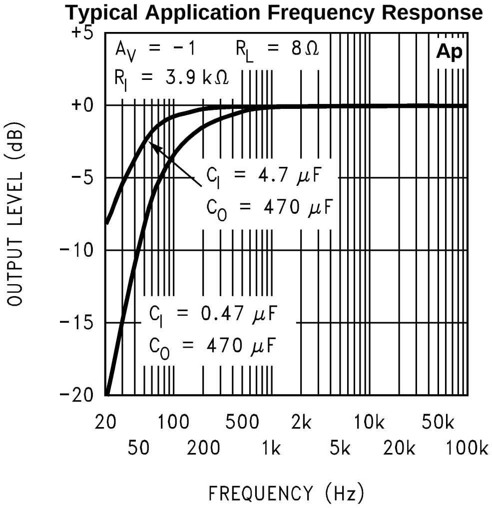


Figure 44.

Typical Application Frequency Response

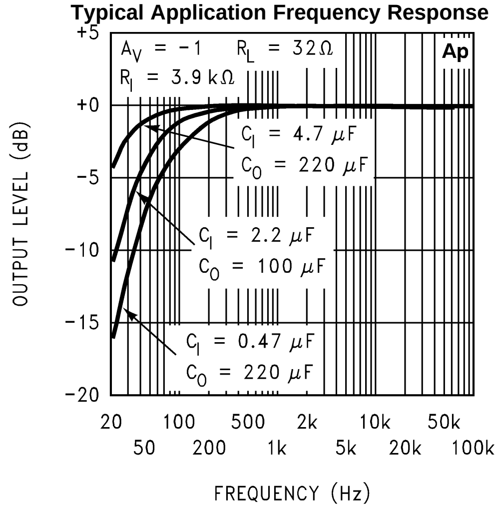


Figure 45.

APPLICATION INFORMATION

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATION

The LM4808's exposed-dap (die attach paddle) package (LD) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane, and surrounding air.

The LD package should have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad may be connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area.

However, since the LM4808 is designed for headphone applications, connecting a copper plane to the DAP's PCB copper pad is not required. The LM4808's Power Dissipation vs Output Power Curve in the TYPICAL PERFORMANCE CHARACTERISTICS shows that the maximum power dissipated is just 45mW per amplifier with a 5V power supply and a 32Ω load.

Further detailed and specific information concerning PCB layout, fabrication, and mounting an LD (WSON) package is available from Texas Instruments' Package Engineering Group under application note AN-1187 (literature number SNOA401).

POWER DISSIPATION

Power dissipation is a major concern when using any power amplifier and must be thoroughly understood to ensure a successful design. Equation 1 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \qquad (1)$$

Since the LM4808 has two operational amplifiers in one package, the maximum internal power dissipation point is twice that of the number which results from Equation 1. Even with the large internal power dissipation, the LM4808 does not require heat sinking over a large range of ambient temperature. From Equation 1, assuming a 5V power supply and a 32Ω load, the maximum power dissipation point is 40mW per amplifier. Thus the maximum package dissipation point is 80mW. The maximum power dissipation point obtained must not be greater than the power dissipation that results from Equation 2:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$$

where

- θ_{JA} = 210°C/W for package DGK0008A
- T_{JMAX} = 150°C for the LM4808 (2)

Depending on the ambient temperature, T_A, of the system surroundings, Equation 2 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 1 is greater than that of Equation 2, then either the supply voltage must be decreased, the load impedance increased or T_A reduced. For the typical application of a 5V power supply, with a 32Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 133.2°C provided that device operation is around the maximum power dissipation point. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature may be increased accordingly. Refer to the TYPICAL PERFORMANCE CHARACTERISTICS curves for power dissipation information for lower output powers.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 0.1µF supply bypass capacitor, C_S, connected between the LM4808's supply pins and ground. Keep the length of leads and traces that connect capacitors between the LM4808's power supply pin and ground as short as possible. Connecting a 1.0µF capacitor, C_B, between the IN A(+) / IN B(+) node and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases the amplifier's turn-on time. The selection of bypass capacitor values, especially C_B, depends on desired PSRR requirements, click and pop performance (as explained in the section, SELECTING PROPER EXTERNAL COMPONENTS), system cost, and size constraints.

SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the LM4808's performance requires properly selecting external components. Though the LM4808 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The LM4808 is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of $1V_{RMS}$ ($2.83V_{P-P}$). Please refer to the AUDIO POWER AMPLIFIER DESIGN section for more information on selecting the proper gain.

Input and Output Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input and output coupling capacitors (C_I and C_O in Figure 1). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using high value input and output capacitors.

Besides affecting system cost and size, C_i has an effect on the LM4808's click and pop performance. The magnitude of the pop is directly proportional to the input capacitor's size. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired −3dB frequency.

As shown in Figure 1, the input resistor, R_I and the input capacitor, C_I, produce a −3dB high pass filter cutoff frequency that is found using Equation 3. In addition, the output load R_L, and the output capacitor C_O, produce a -3db high pass filter cutoff frequency defined by Equation 4.

$$f_{I\text{-}3db}=1/2\pi R_I C_I \tag{3}$$

$$f_{O\text{-}3db}=1/2\pi R_L C_O \tag{4}$$

Also, careful consideration must be taken in selecting a certain type of capacitor to be used in the system. Different types of capacitors (tantalum, electrolytic, ceramic) have unique performance characteristics and may affect overall system performance.

Bypass Capacitor Value

Besides minimizing the input capacitor size, careful consideration should be paid to the value of the bypass capacitor, C_B. Since C_B determines how fast the LM4808 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4808's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing C_B equal to 1.0µF or larger, will minimize turn-on pops. As discussed above, choosing C_i no larger than necessary for the desired bandwidth helps minimize clicks and pops.

AUDIO POWER AMPLIFIER DESIGN

Design a Dual 70mW/32Ω Audio Amplifier

Given:

Power Output	70mW
Load Impedance	32Ω
Input Level	1Vrms (max)
Input Impedance	20kΩ
Bandwidth	100Hz–20kHz ± 0.50dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs Supply Voltage curve in the TYPICAL PERFORMANCE CHARACTERISTICS section. Another way, using Equation 5, is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Dropout Voltage vs Supply Voltage in the TYPICAL PERFORMANCE CHARACTERISTICS curves, must be added to the result obtained by Equation 5. For a single-ended application, the result is Equation 6.

$$V_{opeak} = \sqrt{(2R_L P_0)} \quad (5)$$

$$V_{DD} \geq (2V_{OPEAK} + (V_{ODTOP} + V_{ODBOT})) \quad (6)$$

The Output Power vs Supply Voltage graph for a 32Ω load indicates a minimum supply voltage of 4.8V. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the LM4808 to produce peak output power in excess of 70mW without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates maximum power dissipation as explained above in the POWER DISSIPATION section. Remember that the maximum power dissipation point from Equation 1 must be multiplied by two since there are two independent amplifiers inside the package. Once the power dissipation equations have been addressed, the required gain can be determined from Equation 7.

$$A_V \geq \sqrt{(P_0 R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (7)$$

Thus, a minimum gain of 1.497 allows the LM4808 to reach full output swing and maintain low noise and THD+N perfromance. For this example, let A_V=1.5.

The amplifiers overall gain is set using the input (R_i) and feedback (R_f) resistors. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation 8.

$$A_V = R_f/R_i \quad (8)$$

The value of R_f is 30kΩ.

The last step in this design is setting the amplifier's −3db frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at lease one−fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an

$$f_L = 100\text{Hz}/5 = 20\text{Hz} \quad (9)$$

and a

$$f_H = 20\text{kHz}^*5 = 100\text{kHz} \quad (10)$$

As stated in the EXTERNAL COMPONENTS DESCRIPTION section, both R_i in conjunction with C_i, and C_o with R_L, create first order highpass filters. Thus to obtain the desired low frequency response of 100Hz within ±0.5dB, both poles must be taken into consideration. The combination of two single order filters at the same frequency forms a second order response. This results in a signal which is down 0.34dB at five times away from the single order filter −3dB point. Thus, a frequency of 20Hz is used in the following equations to ensure that the response is better than 0.5dB down at 100Hz.

$C_i \geq 1 / (2\pi * 20\ \text{k}\Omega * 20\ \text{Hz}) = 0.397\mu\text{F}$; use 0.39µF.

$C_o \geq 1 / (2\pi * 32\Omega * 20\ \text{Hz}) = 249\mu\text{F}$; use 330µF.

The high frequency pole is determined by the product of the desired high frequency pole, f_H, and the closed-loop gain, A_V. With a closed-loop gain of 1.5 and f_H = 100kHz, the resulting GBWP = 150kHz which is much smaller than the LM4808's GBWP of 900kHz. This figure displays that if a designer has a need to design an amplifier with a higher gain, the LM4808 can still be used without running into bandwidth limitations.

Demonstration Board Layout

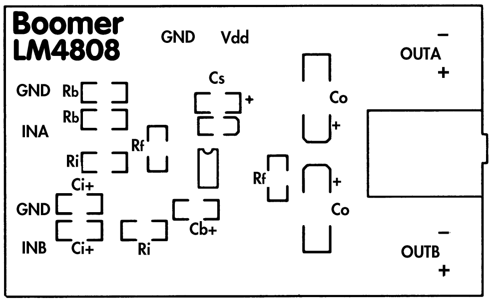


Figure 46. Recommended SO PC Board Layout: Top Silkscreen

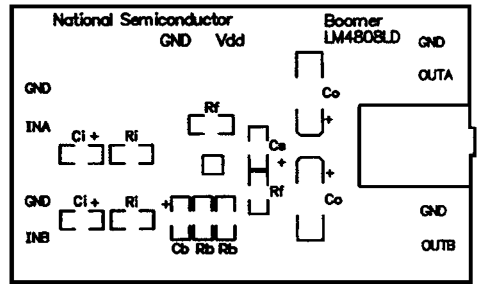


Figure 47. Recommended LD PC Board Layout: Top Silkscreen

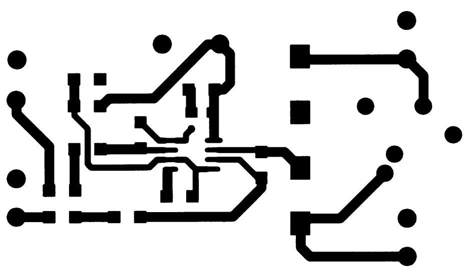


Figure 48. Recommended SOIC PC Board Layout: Top Layer

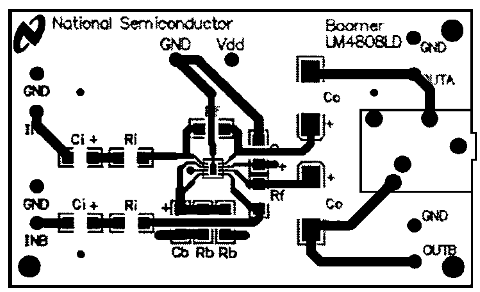


Figure 49. Recommended LD PC Board Layout: Top Layer

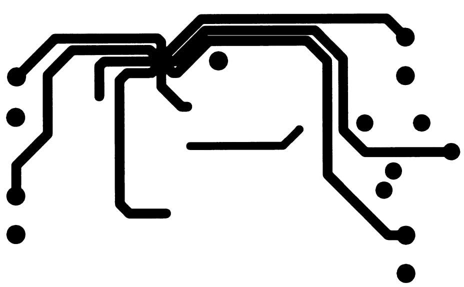


Figure 50. Recommended SOIC PC Board Layout: Bottom Layer

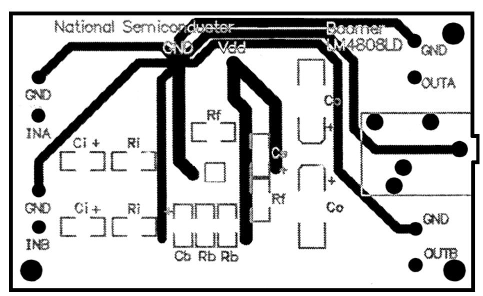


Figure 51. Recommended LD PC Board Layout: Bottom Layer

REVISION HISTORY

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM4808M/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM48 08M
LM4808M/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM48 08M
LM4808MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	G08
LM4808MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	G08
LM4808MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	G08
LM4808MMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	G08
LM4808MMX/NOPB.B	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
LM4808MX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM48 08M
LM4808MX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM48 08M
LM4808MX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

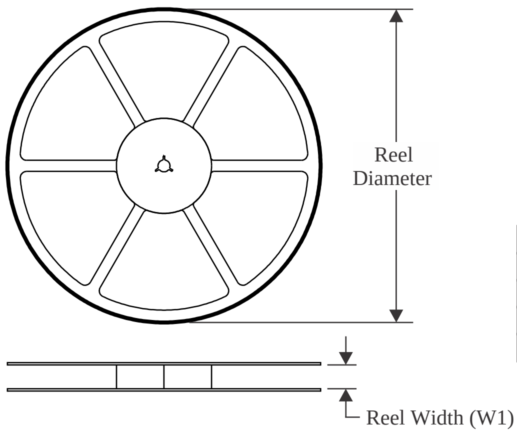
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

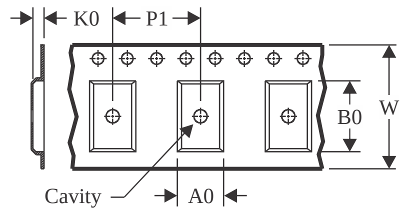
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

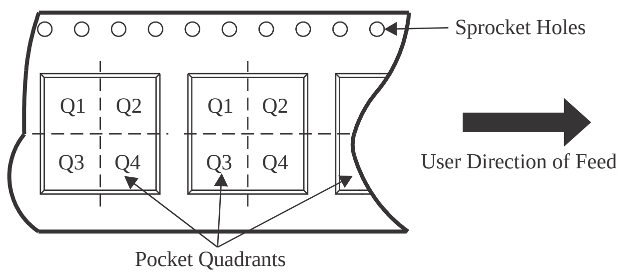


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

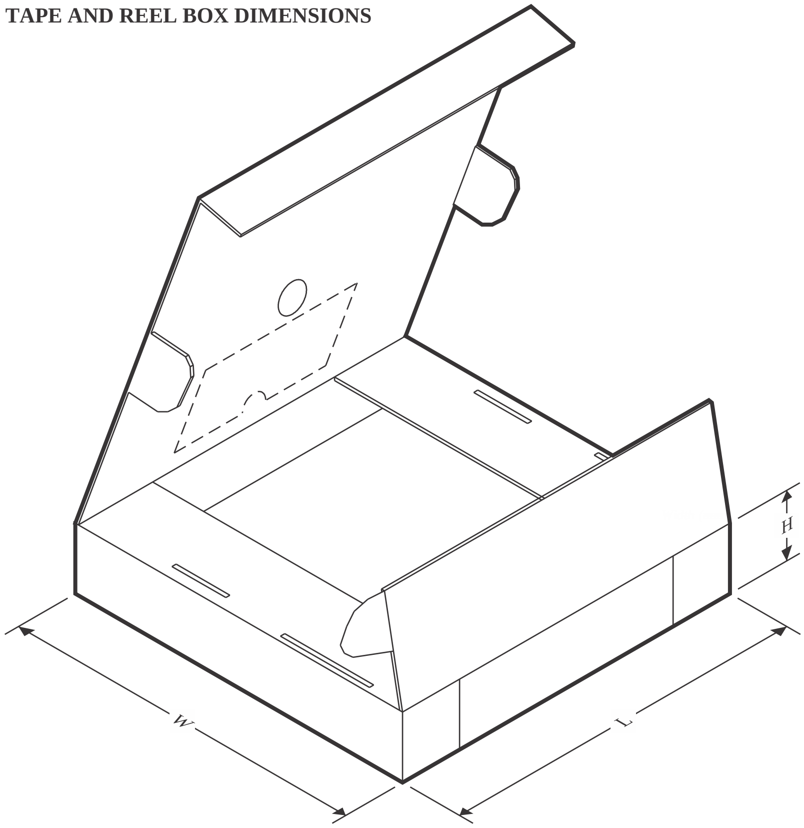
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4808MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4808MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4808MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

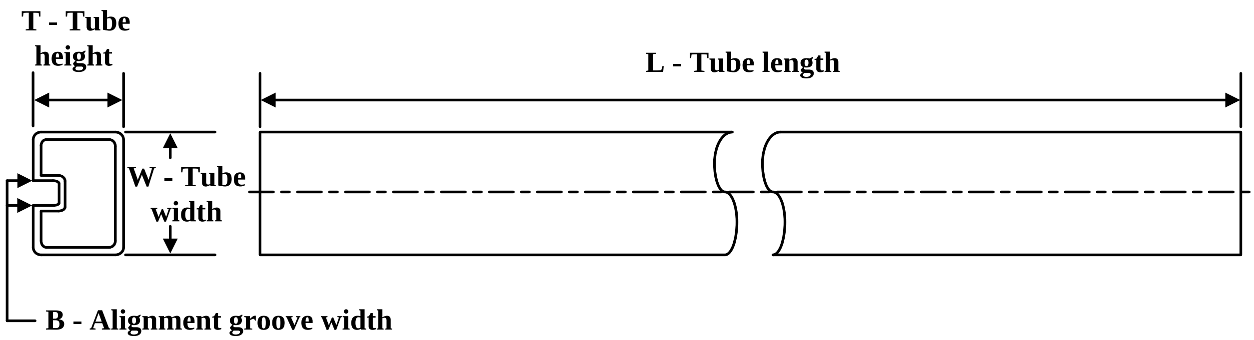
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

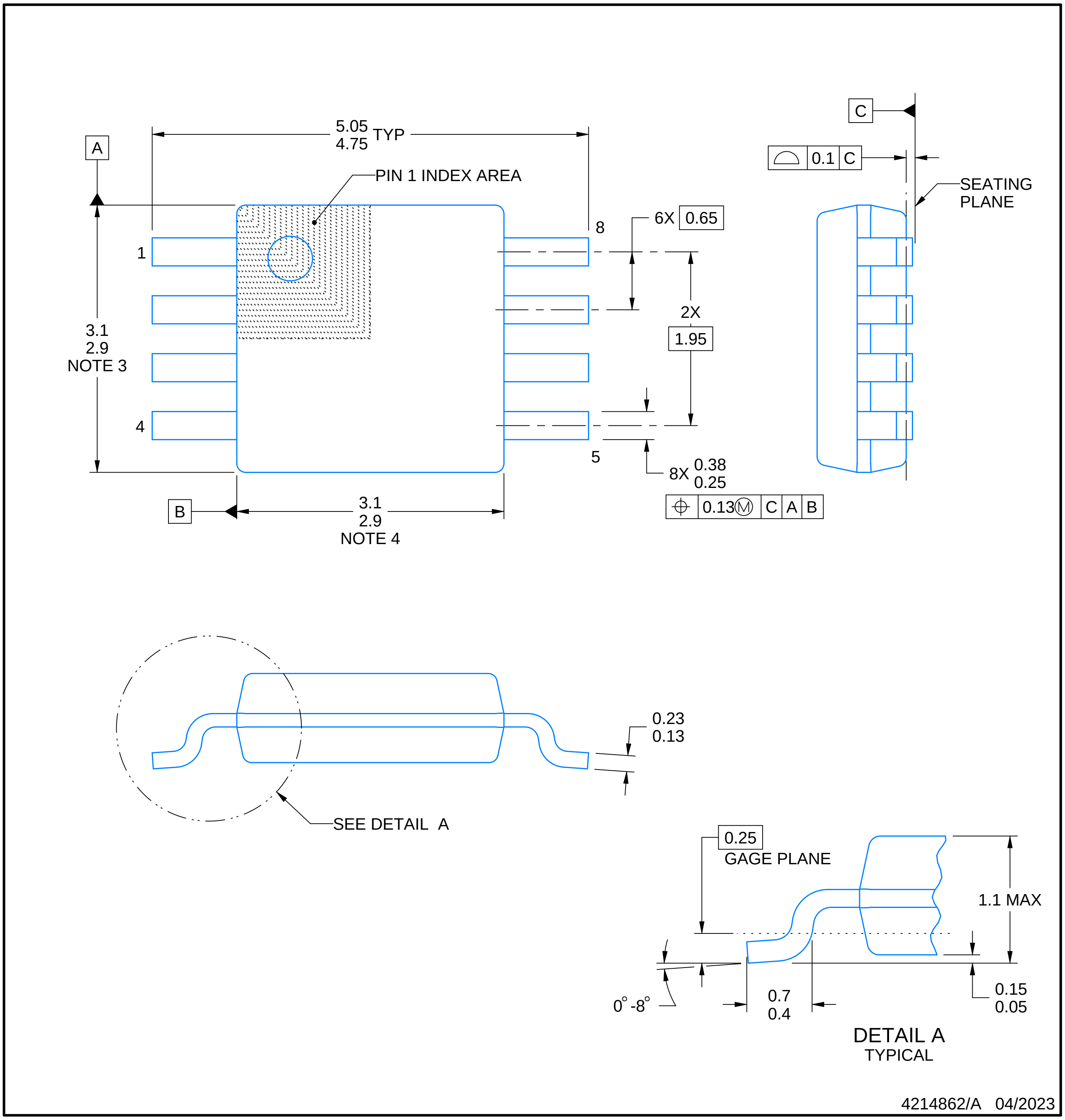
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4808MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM4808MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM4808MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

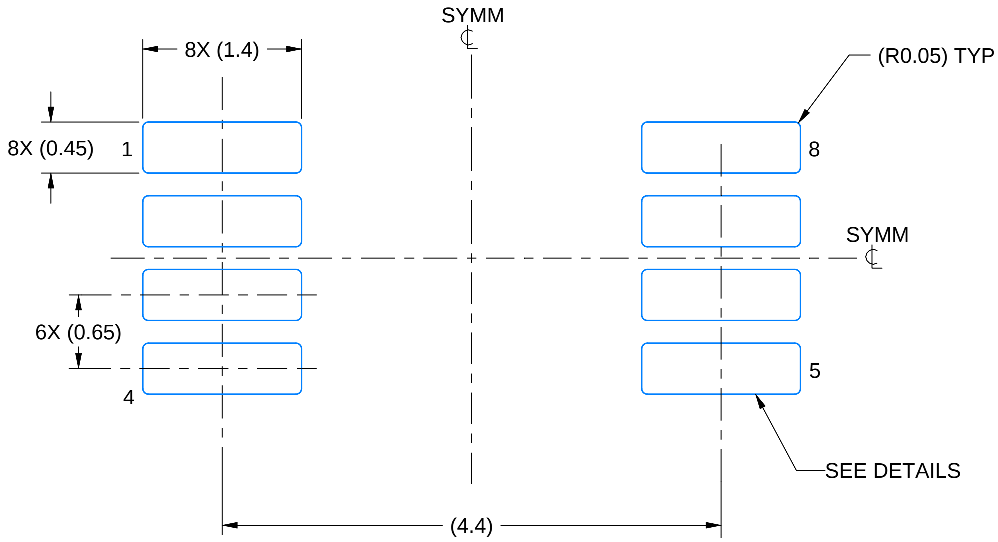
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM4808M/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM4808M/NOPB.A	D	SOIC	8	95	495	8	4064	3.05



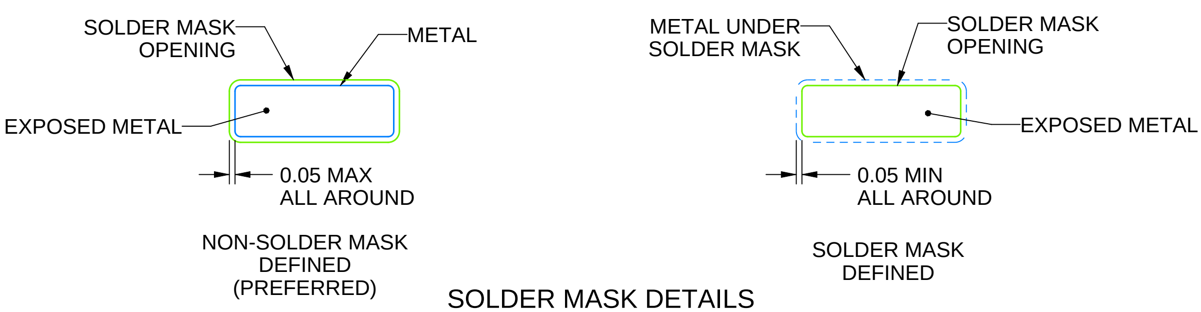
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

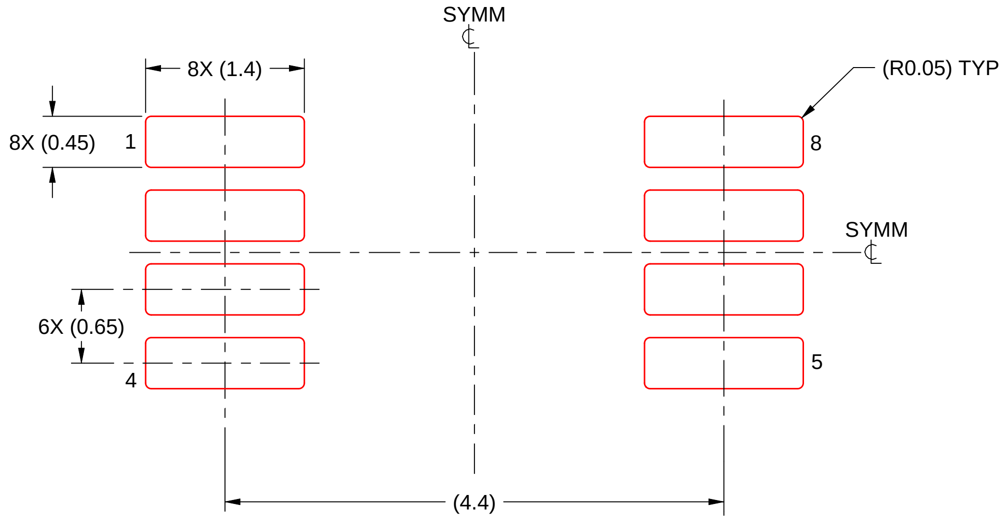


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

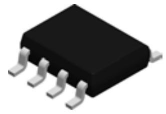


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

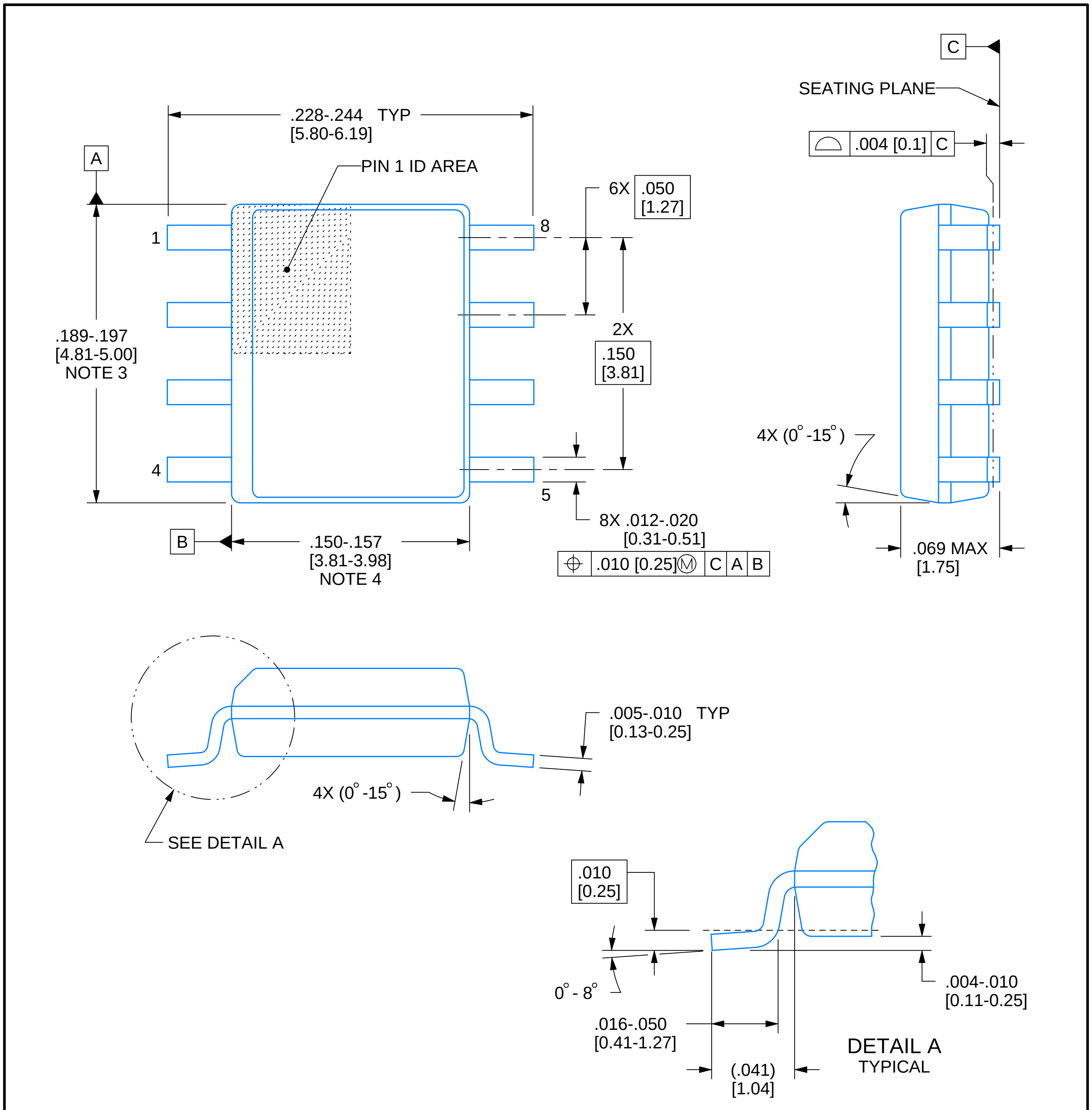


PACKAGE OUTLINE

D0008A

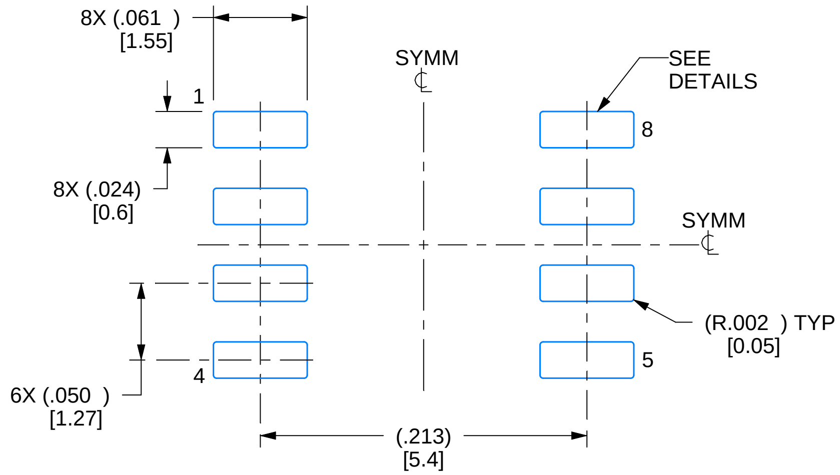
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

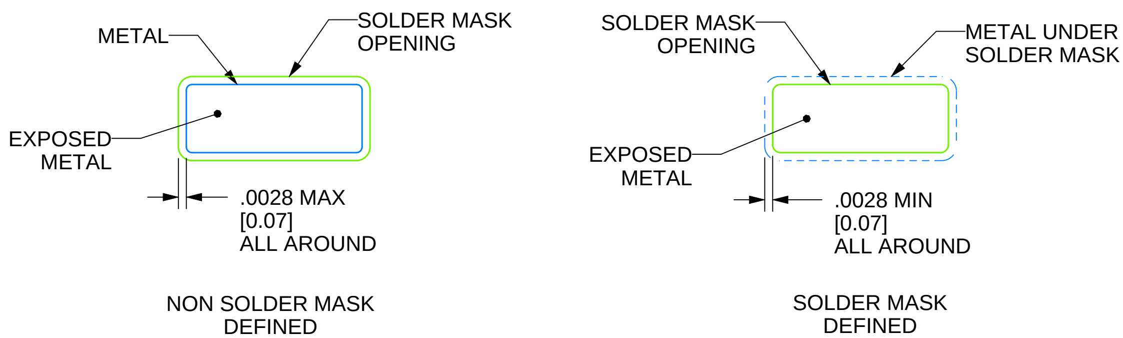


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

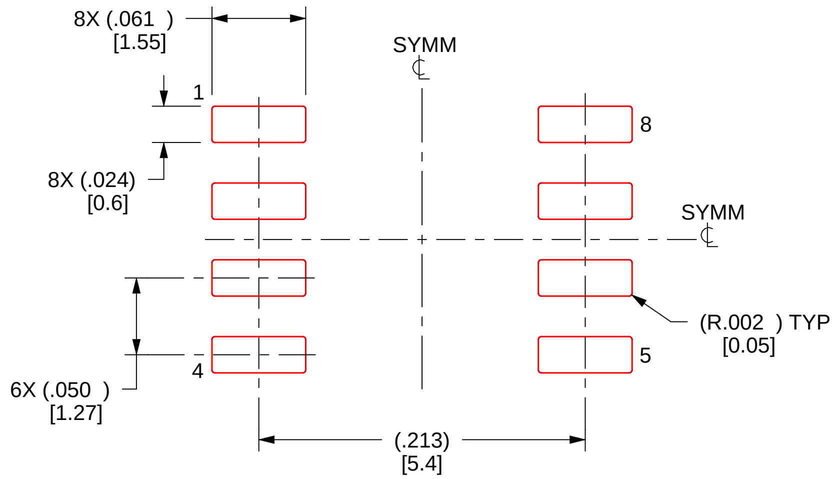


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER