LM4864 Boomer® Audio Power Amplifier Series 725mW Audio Power Amplifier with Shutdown Mode

Check for Samples: LM4864

FEATURES

- **VSSOP, SOIC, PDIP(1), and WSON Packaging**
- **No Output Coupling Capacitors, Bootstrap Capacitors, or Snubber Circuits are Necessary**
- **Thermal Shutdown Protection Circuitry**
- **Unity-Gain Stable**
- **External Gain Configuration Capability**

APPLICATIONS

- **Cellular phones**
- **Personal computers**
- **General purpose audio**

KEY SPECIFICATIONS

- **P_O at 1% THD+N with V_{DD} = 5V, 1kHz**
  - **LM4864LD, 4Ω load 625 mW (typ)**
  - **LM4864LD, 8Ω load 725 mW (typ)**
  - **LM4864M & LM4864N(1), 8Ω load 675 mW (typ)**
  - **LM4864MM, 8Ω load (2) 300 mW (typ)**
  - **LM4864, 16Ω load 550 mW (typ)**
  - **Shutdown current 0.7 µA (typ)**

(1) Not recommended for new designs. Contact TI Audio Marketing.

(2) The DGK0008BA package is thermally limited to 595 mW of power dissipation at room temperature. Referring to Figure 21 in Typical Performance Characteristics, the power dissipation limitation for the package occurs at 300 mW of output power. This package limitation is based on 25°C ambient temperature and θ_{JA} = 210°C. For higher output power possibilities refer to POWER DISSIPATION.

DESCRIPTION

The LM4864 is a bridged audio power amplifier capable of delivering 725mW of continuous average power into an 8Ω load with 1% THD+N from a 5V power supply.

Boomer® audio power amplifiers were designed specifically to provide high quality output power from a low supply voltage while requiring a minimal amount of external components. Since the LM4864 does not require output coupling capacitors, bootstrap capacitors or snubber networks, it is optimally suited for low-power portable applications.

The LM4864 features an externally controlled, low power consumption shutdown mode, and thermal shutdown protection.

The closed loop response of the unity-gain stable LM4864 can be configured by external gain-setting resistors. The device is available in multiple package types to suit various applications.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Boomer is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1999–2013, Texas Instruments Incorporated

Typical Application

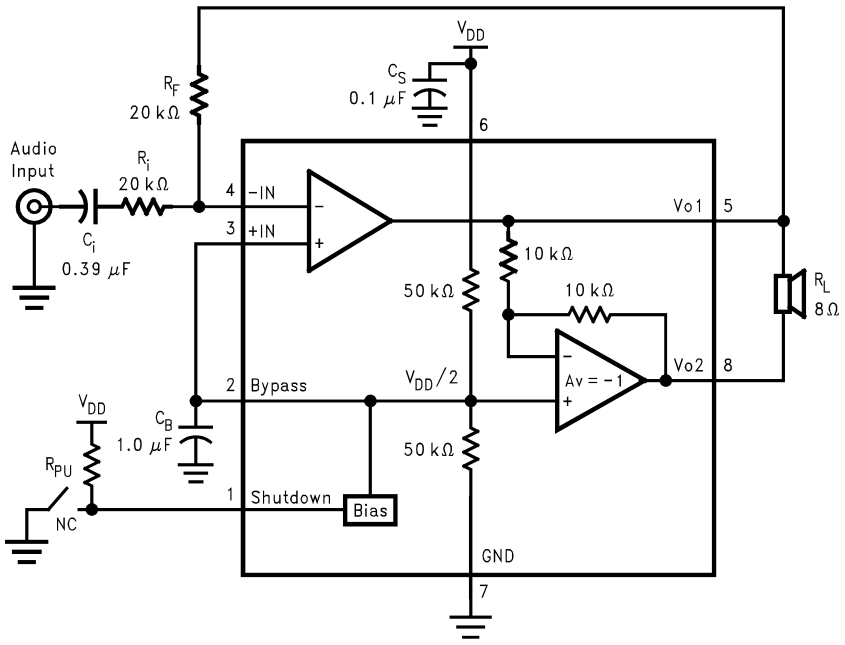


Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram

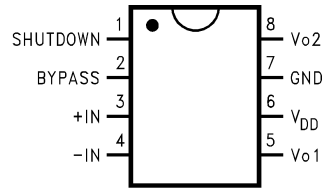


Figure 2. VSSOP, SOIC, and PDIP Package- Top View
See Package Number DGK0008A, D0008A or P0008E(3)

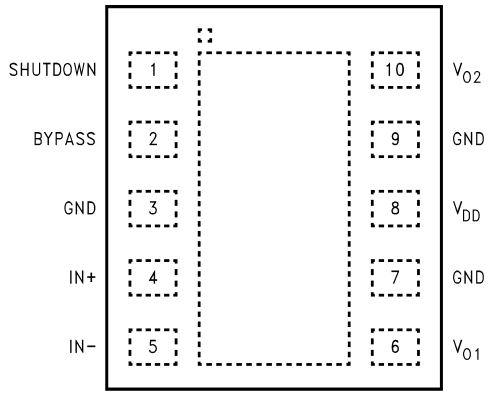


Figure 3. WSON Package- Top View
See Package Number NGY0010A

(3) Not recommended for new designs. Contact TI Audio Marketing.

Copyright © 1999–2013, Texas Instruments Incorporated

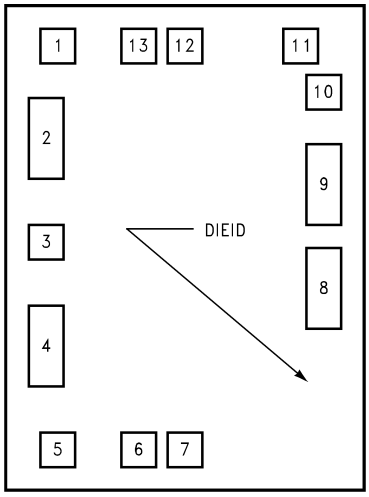


Figure 4. DIE LAYOUT (B-STEP)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage			6.0V
Storage Temperature			−65°C to +150°C
Input Voltage			−0.3V to V_{DD} + 0.3V
Power Dissipation (3)			Internally limited
ESD Susceptibility (4)			2000V
ESD Susceptibility (5)			200V
Junction Temperature			150°C
Soldering Information	Small Outline Package	Vapor Phase (60 sec.)	215°C
		Infrared (15 sec.)	220°C
Thermal Resistance	θ_{JC} (VSSOP)		56° C/W
	θ_{JA} (VSSOP)		210°C/W
	θ_{JC} (SOIC)		35°C/W
	θ_{JA} (SOIC)		170°C/W
	θ_{JC} (PDIP)*		37°C/W
	θ_{JA} (PDIP)*		107°C/W
	θ_{JA} (WSON) (6)		63°C/W
	θ_{JC} (WSON) (6)		12°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not specified for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM4864, T_{JMAX} = 150°C. The typical junction-to-ambient thermal resistance, when board mounted, is 230°C/W for package number DGK0008A, 170°C/W for package number D0008A and is 107°C/W for package number P0008E*.
(4) Human body model, 100pF discharged through a 1.5kΩ resistor.
(5) Machine Model, 220pF – 240pF discharged through all pins.
(6) The NGY0010A package has its exposed-DAP soldered to an exposed 1.2in^2 area of 1oz printed circuit board copper.

Copyright © 1999–2013, Texas Instruments Incorporated

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage		$2.7V \le V_{DD} \le 5.5V$

Electrical Characteristics V_{DD} = 5V (1) (2)

The following specifications apply for V_{DD} = 5V, for all available packages, unless otherwise specified. Limits apply for T_A = 25°C

Symbol	Parameter	Conditions	LM4864		Units (Limits)
			Typical (3)	Limit (4)(5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A (6)	3.6	6.0	mA (max)
I_{SD}	Shutdown Current	$V_{PIN1} = V_{DD}$	0.7	5	µA (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5	50	mV (max)
P_O	Output Power	THD = 1% (max); f = 1 kHz; R_L = 4Ω; LM4864LD (7)	625		mW (min)
		THD = 1% (max); f = 1 kHz; R_L = 8Ω; LM4864LD (7)	725		mW (min)
		THD = 1% (max); f = 1 kHz; R_L = 8Ω; LM4864MM (8)		300	mW (min)
		THD = 1% (max); f = 1 kHz; R_L = 8Ω; LM4864M and LM4864N*	675	300	mW (min)
		THD+N = 1%; f = 1 kHz; R_L = 16Ω;	550		mW
THD+N	Total Harmonic Distortion+Noise	P_O = 300 mWrms; A_{VD} = 2; R_L = 8Ω; 20 Hz ≤ f ≤ 20 kHz, BW < 80kHz	0.7		%
PSRR	Power Supply Rejection Ratio	V_{DD} = 4.9V–5.1V	50		dB

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not specified for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(6) The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.
(7) The NGY0010A package has its exposed-DAP soldered to an exposed $1.2in^2$ area of 1oz printed circuit board copper.
(8) The DGK0008BA package is thermally limited to 595 mW of power dissipation at room temperature. Referring to Figure 21 in Typical Performance Characteristics, the power dissipation limitation for the package occurs at 300 mW of output power. This package limitation is based on 25°C ambient temperature and θ_{JA} = 210°C. For higher output power possibilities refer to POWER DISSIPATION.

Copyright © 1999–2013, Texas Instruments Incorporated

Electrical Characteristics V_{DD} = 3V (1) (2)

The following specifications apply for V_{DD} = 3V, for all available packages, unless otherwise specified. Limits apply for T_A = 25°C

Symbol	Parameter	Conditions	LM4864		Units (Limits)
			Typical (3)	Limit (4)(5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A (6)	1.0	3.0	mA (max)
I_{SD}	Shutdown Current	$V_{PIN1} = V_{DD}$	0.3	2.0	µA (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5		mV
P_O	Output Power	THD = 1% (max); f = 1 kHz; R_L = 8Ω	200		mW
		THD = 1% (max); f = 1 kHz; R_L = 16Ω	175		mW
THD+N	Total Harmonic Distortion+Noise	P_O = 100 mWrms; A_{VD} = 2; R_L = 8Ω; 20 Hz ≤ f ≤ 20 kHz, BW < 80 kHz	1.5		%
PSRR	Power Supply Rejection Ratio	V_{DD} = 2.9V–3.1V	50		dB

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not specified for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(6) The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.

Copyright © 1999–2013, Texas Instruments Incorporated

External Components Description

(See Figure 1)

Components		Functional Description
1.	R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_F. This resistor also forms a high pass filter with C_i at $f_c = 1/(2\pi R_i C_I)$.
2.	C_i	Input coupling capacitor which blocks the DC voltage at the amplifier's input terminals. Also creates a highpass filter with R_i at $f_c = 1/(2\pi R_i C_i)$. Refer to PROPER SELECTION OF EXTERNAL COMPONENTS for an explanation of how to determine the value of C_i.
3.	R_F	Feedback resistance which sets the closed-loop gain in conjunction with R_i.
4.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to POWER SUPPLY BYPASSING section for information concerning proper placement and selection of the supply bypass capacitor.
5.	C_B	Bypass pin capacitor which provides half-supply filtering. Refer to PROPER SELECTION OF EXTERNAL COMPONENTS for information concerning proper placement and selection of C_B.

Copyright © 1999–2013, Texas Instruments Incorporated

Typical Performance Characteristics

THD+N vs Frequency

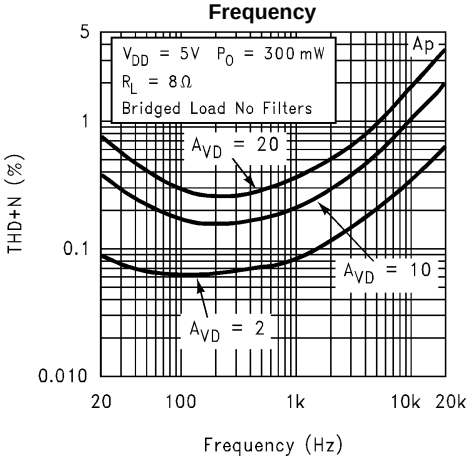


Figure 5.

THD+N vs Frequency

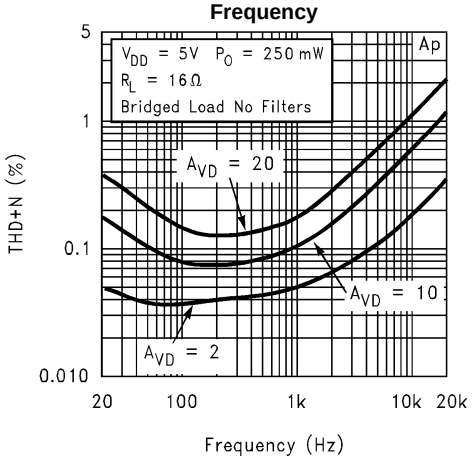


Figure 6.

THD+N vs Frequency

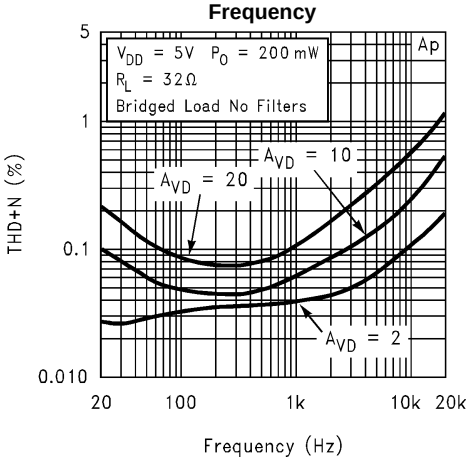


Figure 7.

THD+N vs Frequency

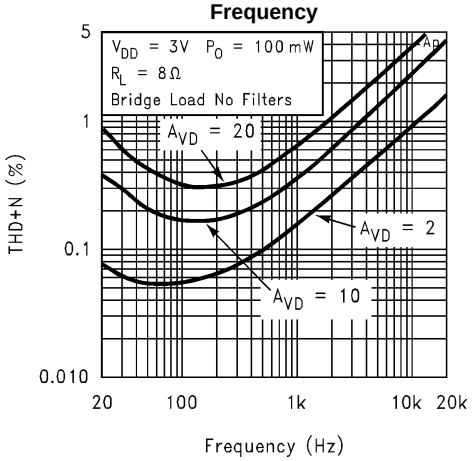


Figure 8.

THD+N vs Frequency

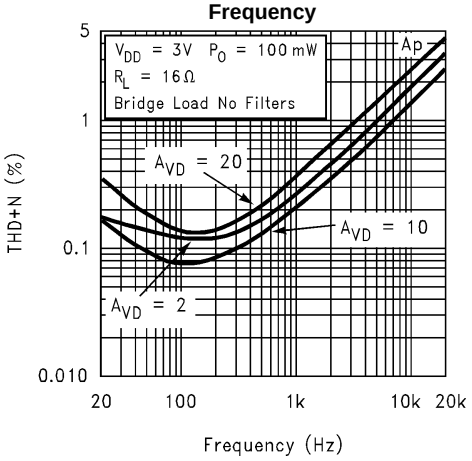


Figure 9.

THD+N vs Frequency

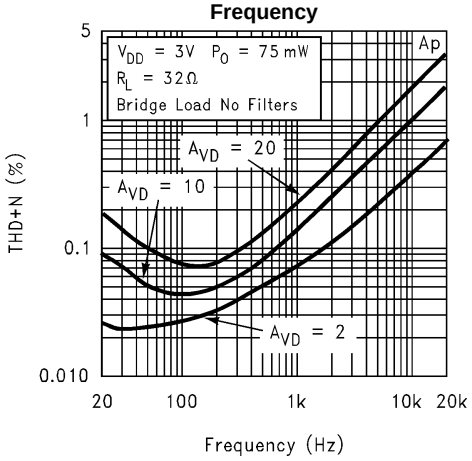


Figure 10.

Copyright © 1999–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

THD+N vs Output Power

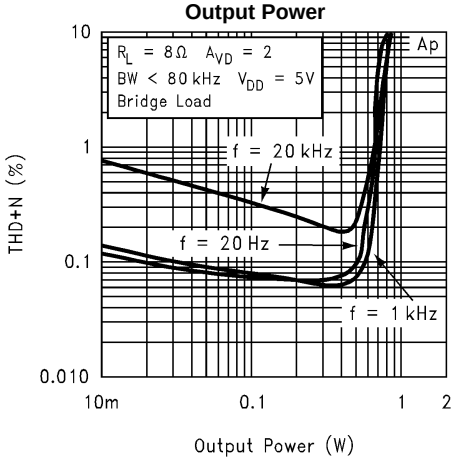


Figure 11.

THD+N vs Output Power

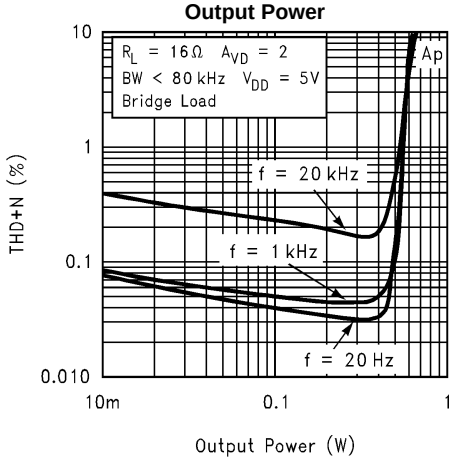


Figure 12.

THD+N vs Output Power

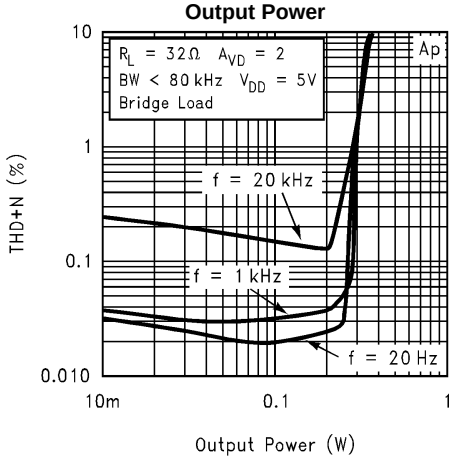


Figure 13.

THD+N vs Output Power

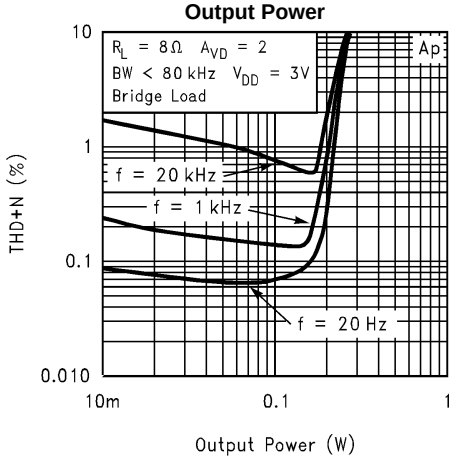


Figure 14.

THD+N vs Output Power

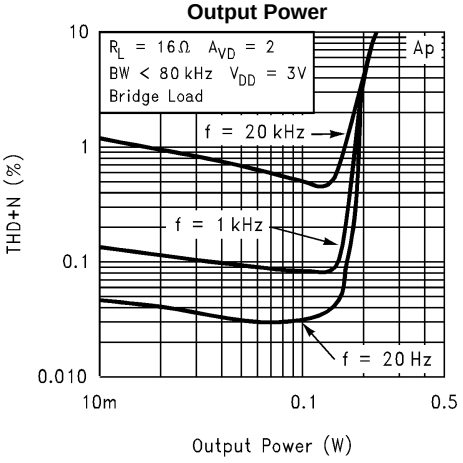


Figure 15.

THD+N vs Output Power

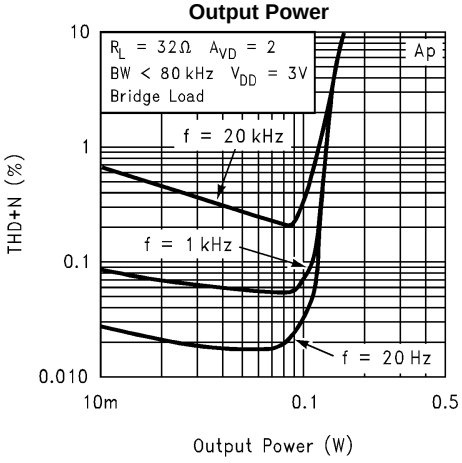


Figure 16.

Copyright © 1999–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

Output Power vs Supply Voltage

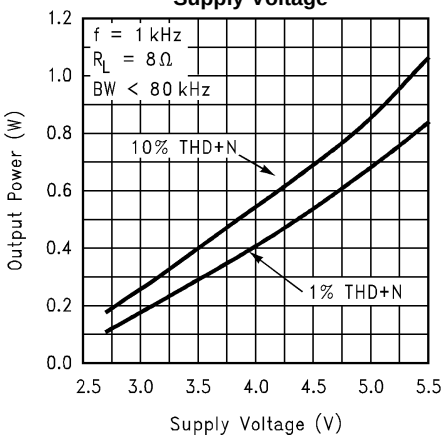


Figure 17.

Output Power vs Supply Voltage

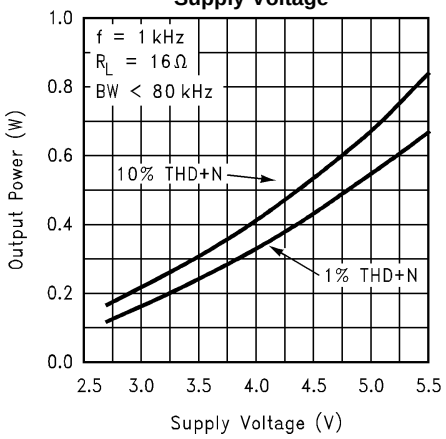


Figure 18.

Output Power vs Supply Voltage

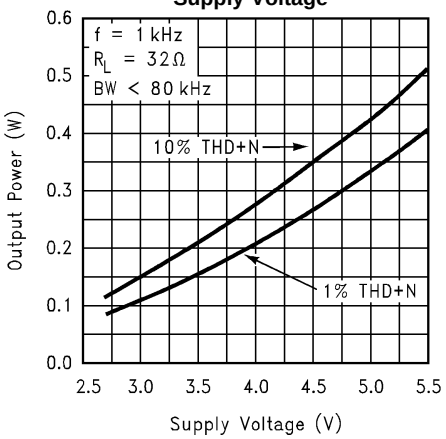


Figure 19.

Output Power vs Load Resistance

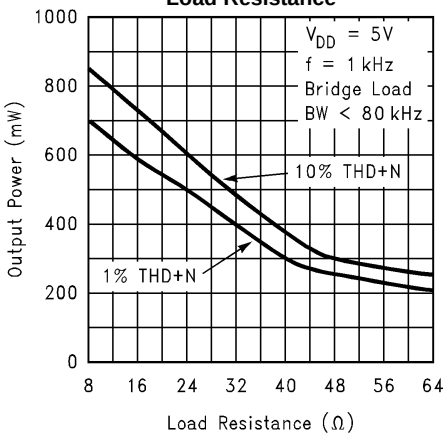


Figure 20.

Power Dissipation vs Output Power

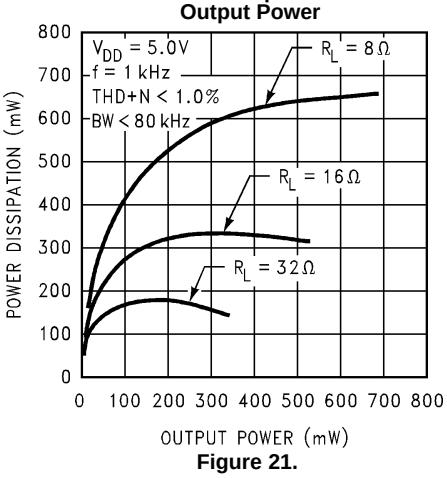


Figure 21.

Power Derating Curve

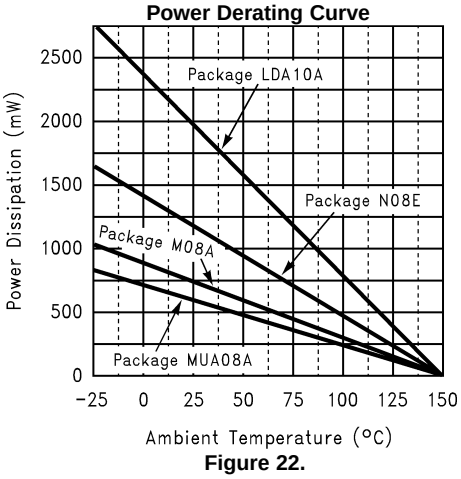


Figure 22.

Typical Performance Characteristics (continued)

Dropout Voltage vs Supply Voltage

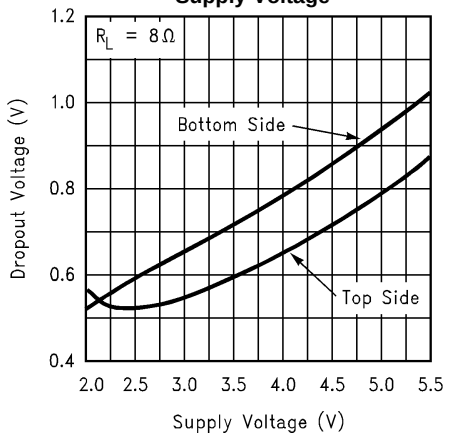


Figure 23.

Noise Floor

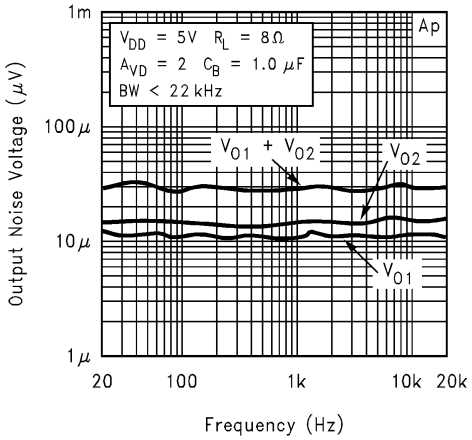


Figure 24.

Frequency Response vs Input Capacitor Size

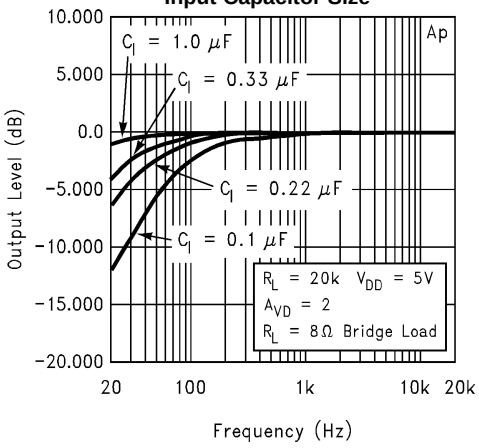


Figure 25.

Power Supply Rejection Ratio

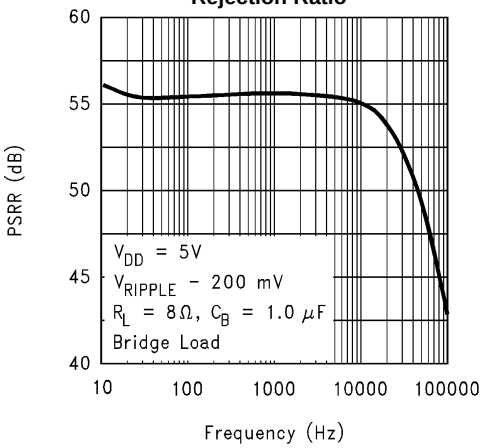


Figure 26.

Open Loop Frequency Response

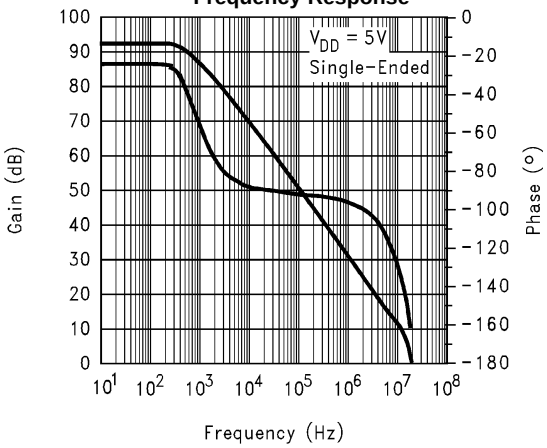


Figure 27.

Supply Current vs Supply Voltage

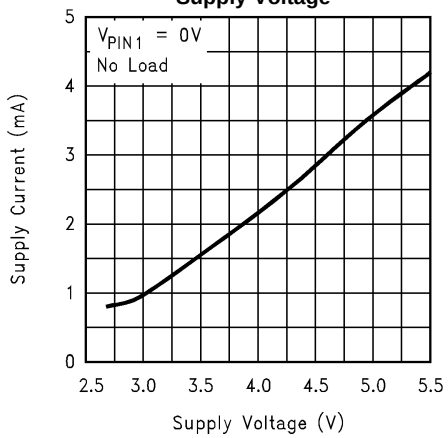


Figure 28.

Copyright © 1999–2013, Texas Instruments Incorporated

Typical Performance Characteristics for the LM4864LD (1)

THD+N vs Frequency

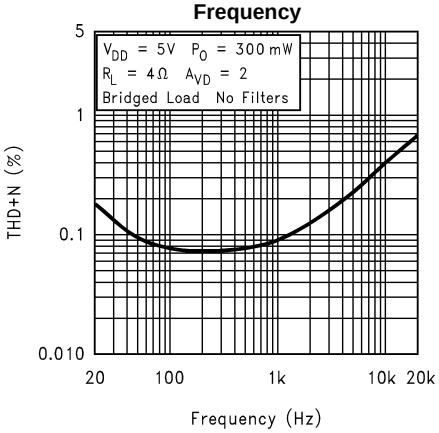


Figure 29.

THD+N vs Frequency

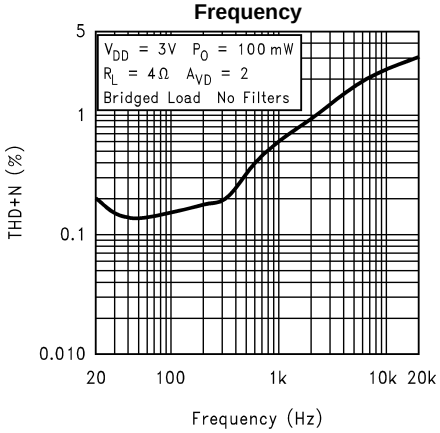


Figure 30.

THD+N vs Power Out

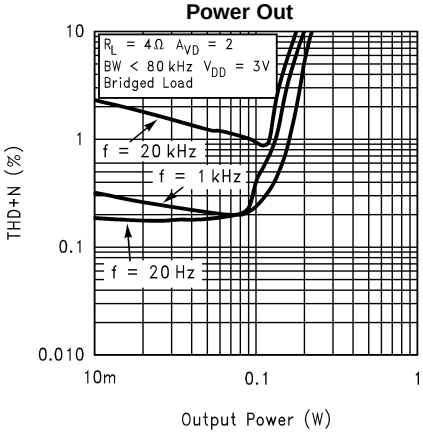


Figure 31.

THD+N vs Power Out

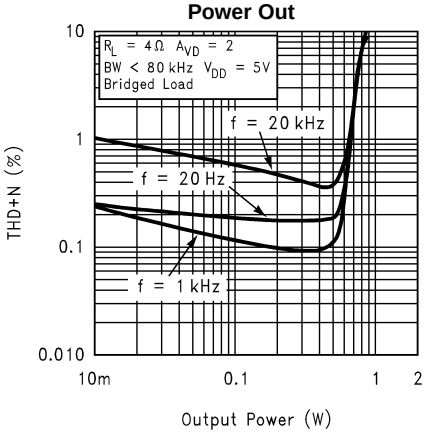


Figure 32.

Output Power vs Supply Voltage

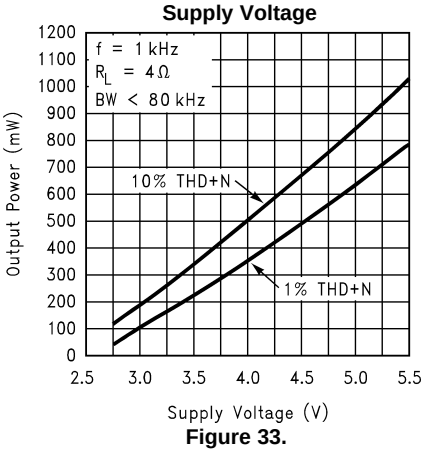


Figure 33.

Power Dissipation vs Output Power

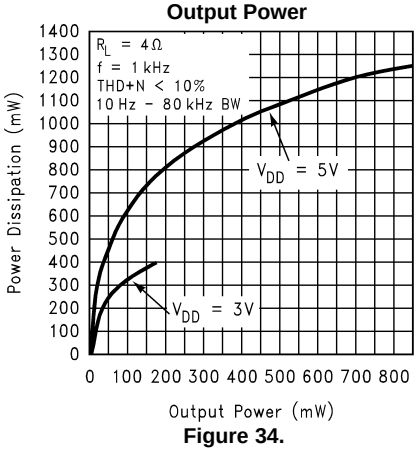


Figure 34.

(1) The NGY0010A package has its exposed-DAP soldered to an exposed 1.2in^2 area of 1oz printed circuit board copper.

APPLICATION INFORMATION

BRIDGE CONFIGURATION EXPLANATION

As shown in *Figure 1*, the LM4864 has two operational amplifiers internally, allowing for a few different amplifier configurations. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_F to R_i while the second amplifier's gain is fixed by the two internal 10kΩ resistors. *Figure 1* shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase 180°. Consequently, the differential gain for the IC is

$$A_{VD} = 2*(R_F/R_i) \quad (1)$$

By driving the load differentially through outputs V_{o1} and V_{o2}, an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of its load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to AUDIO POWER AMPLIFIER DESIGN section.

A bridge configuration, such as the one used in LM4864, also creates a second advantage over single-ended amplifiers. Since the differential outputs, V_{o1} and V_{o2}, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. If an output coupling capacitor is not used in a single-ended configuration, the half-supply bias across the load would result in both increased internal IC power dissipation as well as permanent loudspeaker damage.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. Equation 2 states the maximum power dissipation point for a bridge amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2/(2\pi^2 R_L) \quad \text{Single-Ended (1)} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation point for a bridge amplifier operating at the same conditions.

$$P_{DMAX} = 4(V_{DD})^2/(2\pi^2 R_L) \quad \text{Bridge Mode (2)} \quad (3)$$

Since the LM4864 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. Even with this substantial increase in power dissipation, the LM4864 does not require heatsinking. From Equation 2, assuming a 5V power supply and an 8Ω load, the maximum power dissipation point is 633 mW. The maximum power dissipation point obtained from Equation 3 must not be greater than the power dissipation that results from Equation 4:

$$P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA} \quad (3) \quad (4)$$

For package DGK0008A, θ_{JA} = 210°C/W, for package D00008A, θ_{JA} = 170°C/W, for package P0008E, θ_{JA} = 107°C/W, and for package NGY0010A, θ_{JA} = 63°C/W. T_{JMAX} = 150°C for the LM4864. Depending on the ambient temperature, T_A, of the system surroundings, Equation 4 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 3 is greater than that of Equation 4, then either the supply voltage must be decreased, the load impedance increased, the ambient temperature reduced, or the θ_{JA} reduced with heatsinking. In many cases larger traces near the output, V_{DD}, and GND pins can be used to lower the θ_{JA}. The larger areas of copper provide a form of heatsinking allowing a higher power dissipation. For the typical application of a 5V power supply, with an 8Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 44°C provided that device operation is around the maximum power dissipation point and assuming surface mount packaging. Internal power dissipation is a function of output power. If typical operation is not around the maximum power dissipation point, the ambient temperature can be increased. Refer to Typical Performance Characteristics for power dissipation information for lower output powers.

Copyright © 1999–2013, Texas Instruments Incorporated

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATION

The LM4864's exposed-dap (die attach paddle) package (NGY) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane, and surrounding air.

The NGY package should have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad may be connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area.

Further detailed and specific information concerning PCB layout, fabrication, and mounting an NGY (WSON) package is available from Texas Instruments's Package Engineering Group under application note AN1187.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. The effect of a larger half supply bypass capacitor is improved PSRR due to increased half-supply stability. Typical applications employ a 5V regulator with 10 µF and a 0.1 µF bypass capacitors which aid in supply stability, but do not eliminate the need for bypassing the supply nodes of the LM4864. The selection of bypass capacitors, especially C_B, is thus dependent upon desired PSRR requirements, click and pop performance as explained in PROPER SELECTION OF EXTERNAL COMPONENTS, system cost, and size constraints.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4864 contains a shutdown pin to externally turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when a logic high is placed on the shutdown pin. The trigger point between a logic low and logic high level is typically half supply. It is best to switch between ground and supply to provide maximum device performance. By switching the shutdown pin to V_{DD}, the LM4864 supply current draw will be minimized in idle mode. While the device will be disabled with shutdown pin voltages less than V_{DD}, the idle current may be greater than the typical value of 0.7 µA. In either case, the shutdown pin should be tied to a definite voltage to avoid unwanted state changes.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry which provides a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch in conjunction with an external pull-up resistor. When the switch is closed, the shutdown pin is connected to ground and enables the amplifier. If the switch is open, then the external pull-up resistor will disable the LM4864. This scheme ensures that the shutdown pin will not float, thus preventing unwanted state changes.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4864 is tolerant to a variety of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4864 is unity-gain stable, giving a designer maximum system flexibility. The LM4864 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1 Vrms are available from sources such as audio codecs. Please refer toAUDIO POWER AMPLIFIER DESIGN, for a more complete explanation of proper gain selection.

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in *Figure 1*. The input coupling capacitor, C_i, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

Selection of Input Capacitor Size

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150 Hz. In this case using a large input capacitor may not increase system performance.

Copyright © 1999–2013, Texas Instruments Incorporated

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, C_i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally ½ V_{DD}). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, C_B, is the most critical component to minimize turn-on pops since it determines how fast the LM4864 turns on. The slower the LM4864's outputs ramp to their quiescent DC voltage (nominally ½ V_{DD}), the smaller the turn-on pop. Choosing C_B equal to 1.0 µF along with a small value of C_i (in the range of 0.1 µF to 0.39 µF), should produce a clickless and popless shutdown function. While the device will function properly, (no oscillations or motorboating), with C_B equal to 0.1 µF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_B equal to 1.0 µF or larger is recommended in all but the most cost sensitive designs.

AUDIO POWER AMPLIFIER DESIGN

Design a 300 mW/8Ω Audio Amplifier

Given:	
Power Output	300 mWrms
Load Impedance	8Ω
Input Level	1 Vrms
Input Impedance	20 kΩ
Bandwidth	100 Hz–20 kHz ± 0.25 dB

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating fromFigure 18 and Figure 19 in Typical Performance Characteristics, the supply rail can be easily found. A second way to determine the minimum supply rail is to calculate the required V_{opeak} using Equation 5 and add the dropout voltage. Using this method, the minimum supply voltage would be (V_{opeak} + (2*V_{OD})), where V_{OD} is extrapolated from Figure 23 in Typical Performance Characteristics.

$$V_{opeak} = \sqrt{(2R_L P_O)} \tag{5}$$

Using Figure 17 for an 8Ω load, the minimum supply rail is 3.5V. But since 5V is a standard supply voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4864 to reproduce peaks in excess of 500 mW without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in POWER DISSIPATION.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 6.

$$A_{VD} \geq \sqrt{(P_O R_L)} / (V_{IN}) = V_{orms}/V_{inrms} \tag{6}$$

$$R_F/R_i = A_{VD}/2 \tag{7}$$

From Equation 6, the minimum A_{VD} is 1.55; use A_{VD} = 2.

Since the desired input impedance was 20 kΩ, and with a A_{VD} of 2, a ratio of 1:1 of R_F to R_i results in an allocation of R_i = R_F = 20 kΩ. The final design step is to address the bandwidth requirements which must be stated as a pair of −3 dB frequency points. Five times away from a pole gives 0.17 dB down from passband response which is better than the required ±0.25 dB specified.

$$f_L = 100 \text{ Hz}/5 = 20 \text{ Hz} \tag{8}$$

$$f_H = 20 \text{ kHz} \times 5 = 100 \text{ kHz} \tag{9}$$

As stated in External Components Description , R_i in conjunction with C_i create a highpass filter.

$$C_i \geq \frac{1}{2\pi R_i f_c} \tag{10}$$

$$C_i \geq 1/(2\pi * 20 \text{ k}\Omega * 20 \text{ Hz}) = 0.397 \text{ µF}; \quad \text{use } 0.39 \text{ µF} \tag{11}$$

Copyright © 1999–2013, Texas Instruments Incorporated

The high frequency pole is determined by the product of the desired high frequency pole, f_H, and the differential gain, A_{VD}. With a A_{VD} = 2 and f_H = 100 kHz, the resulting GBWP = 100 kHz which is much smaller than the LM4864 GBWP of 18 MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the LM4864 can still be used without running into bandwidth problems.

LM4864LD DEMO BOARD ARTWORK

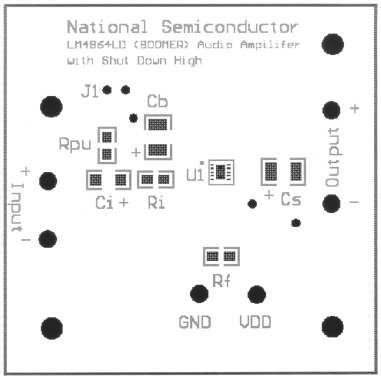


Figure 35. Silk Screen View of LM4864LD

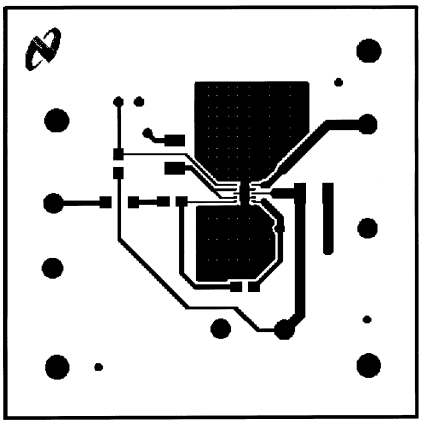


Figure 36. Top Layer of LM4864LD

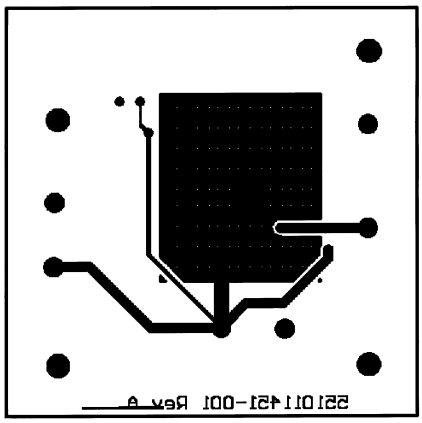


Figure 37. Bottom Layer of LM4864LD

LM4864 MDC MWC
725MW Audio Power Amplifier With Shutdown Mode

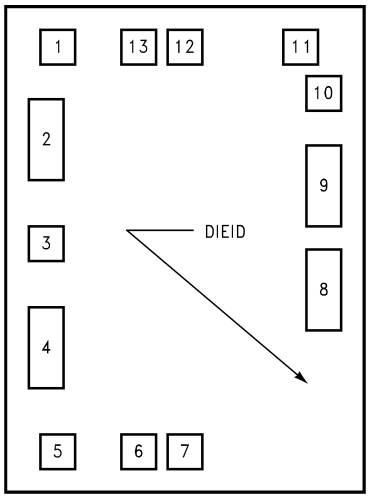


Figure 38. Die Layout (B - Step)

Table 1. DIE/WAFER CHARACTERISTICS

Fabrication Attributes		General Die Information	
Physical Die Identification	LM4862B	Bond Pad Opening Size (min)	86µm x 86µm
Die Step	B	Bond Pad Metalization	ALUMINUM
Physical Attributes		Passivation	NITRIDE
Wafer Diameter	150mm	Back Side Metal	Bare Back
Dise Size (Drawn)	1283µm x 952µm 51mils x 37mils	Back Side Connection	GND
Thickness	406µm Nominal		
Min Pitch	117µm Nominal		

Special Assembly Requirements:
Note: Actual die size is rounded to the nearest micron.

Die Bond Pad Coordinate Locations (B - Step)						
(Referenced to die center, coordinates in µm) NC = No Connection						
SIGNAL NAME	PAD# NUMBER	X/Y COORDINATES		PAD SIZE		
		X	Y	X		Y
BYPASS	1	-322	523	86	x	86
GND	2	-359	259	86	x	188
INPUT +	3	-359	5	86	x	86
GND	4	-359	-259	86	x	188
NC	5	-323	-523	86	x	86
INPUT -	6	-109	-523	86	x	86
VOUT 1	7	8	-523	86	x	86
VDD	8	358	-78	86	x	188
GND	9	358	141	86	x	188
NC	10	359	406	86	x	86
NC	11	323	523	86	x	86
VOUT 2	12	8	523	86	x	86
SHUTDOWN	13	-109	523	86	x	86

Copyright © 1999–2013, Texas Instruments Incorporated

REVISION HISTORY

Changes from Revision E (May 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	16

Copyright © 1999–2013, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM4864M/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM48 64M
LM4864M/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM48 64M
LM4864MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	Z64
LM4864MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	Z64
LM4864MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	Z64
LM4864MMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	Z64
LM4864MX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM48 64M
LM4864MX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM48 64M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

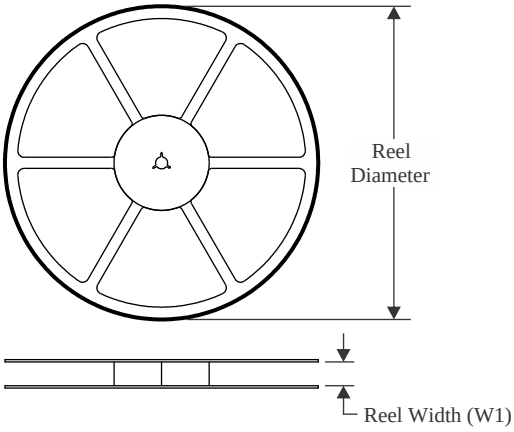
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

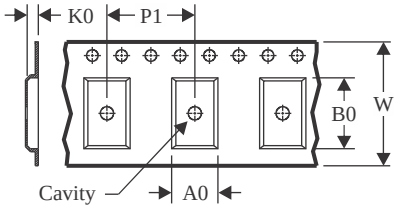
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

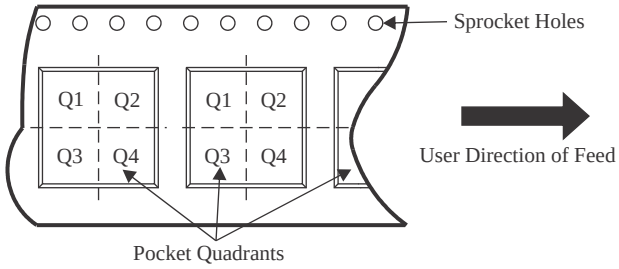


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

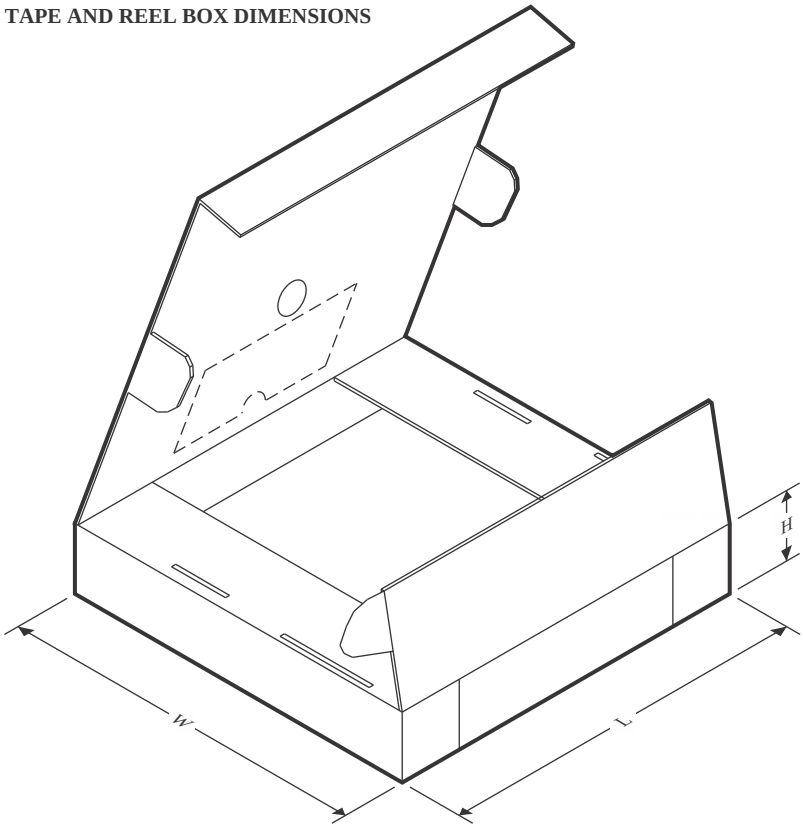
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4864MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4864MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4864MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

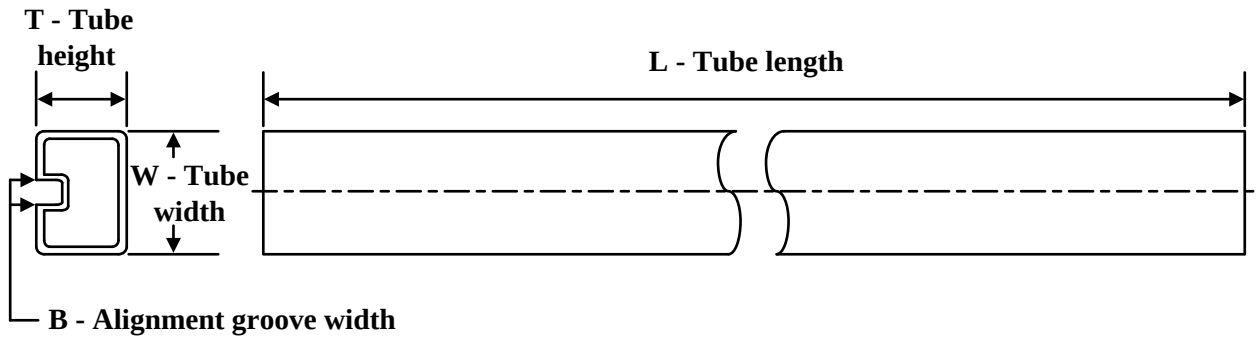
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

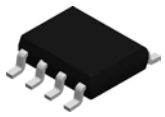
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4864MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM4864MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM4864MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM4864M/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM4864M/NOPB.A	D	SOIC	8	95	495	8	4064	3.05

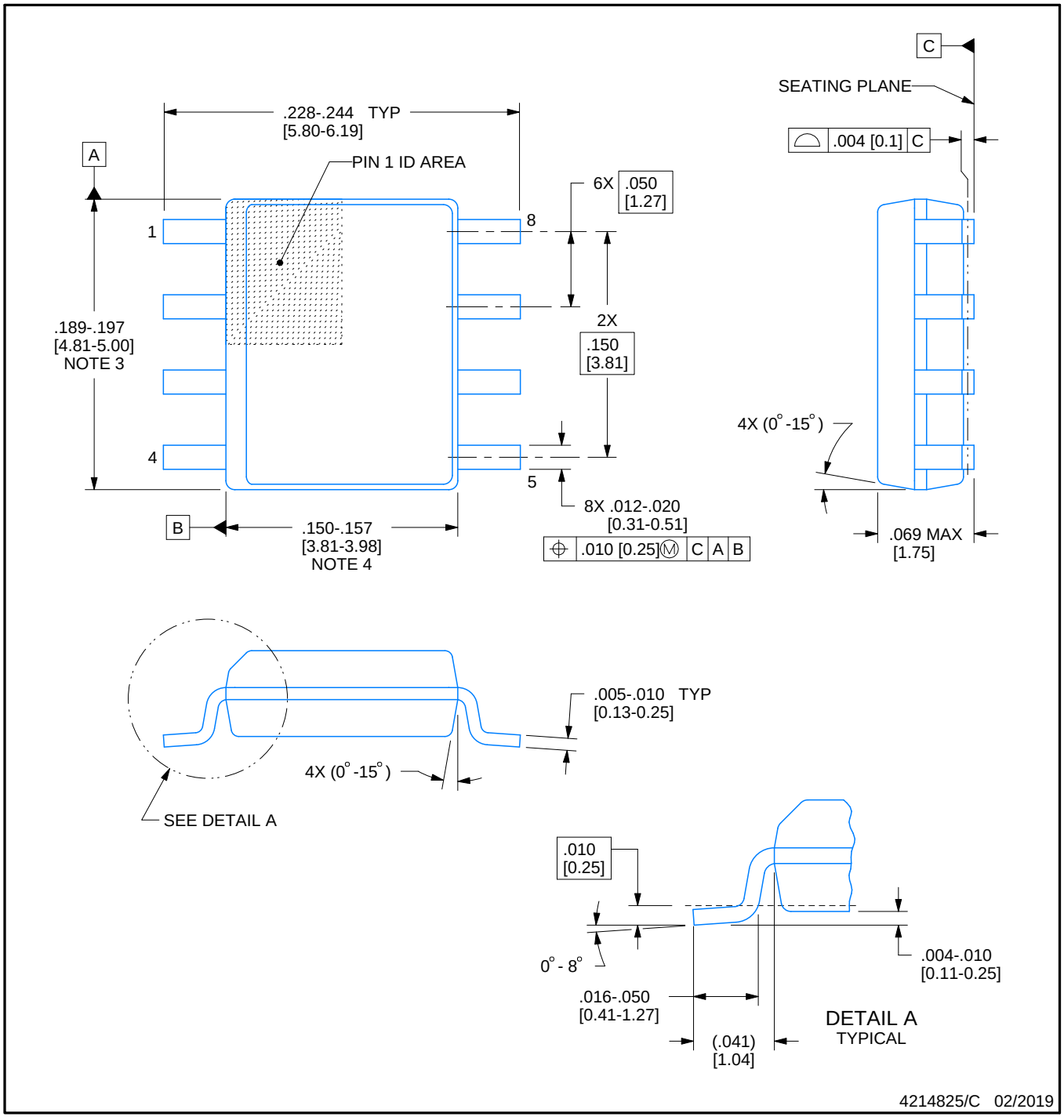


PACKAGE OUTLINE

D0008A

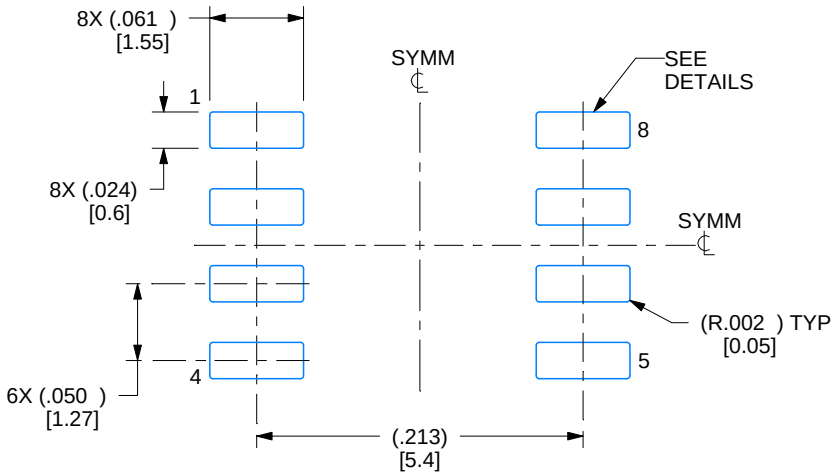
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

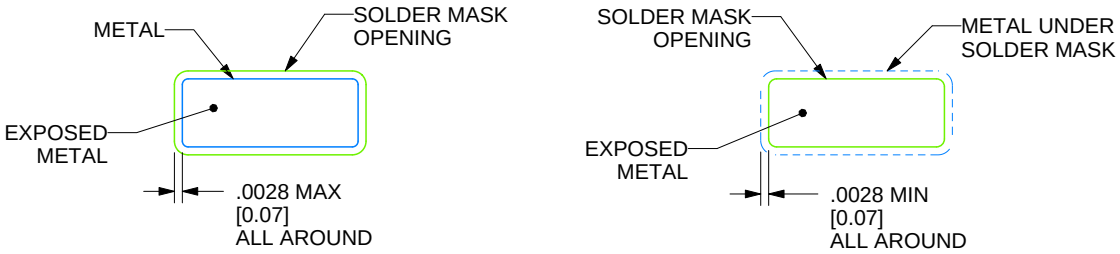


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

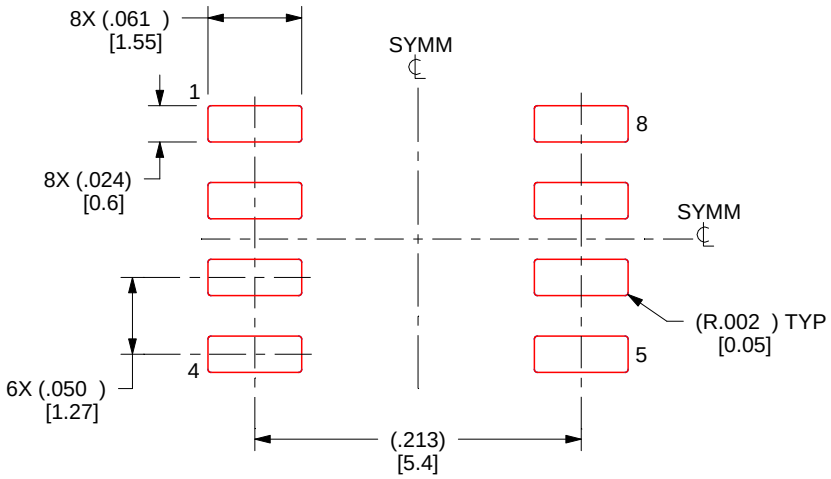
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

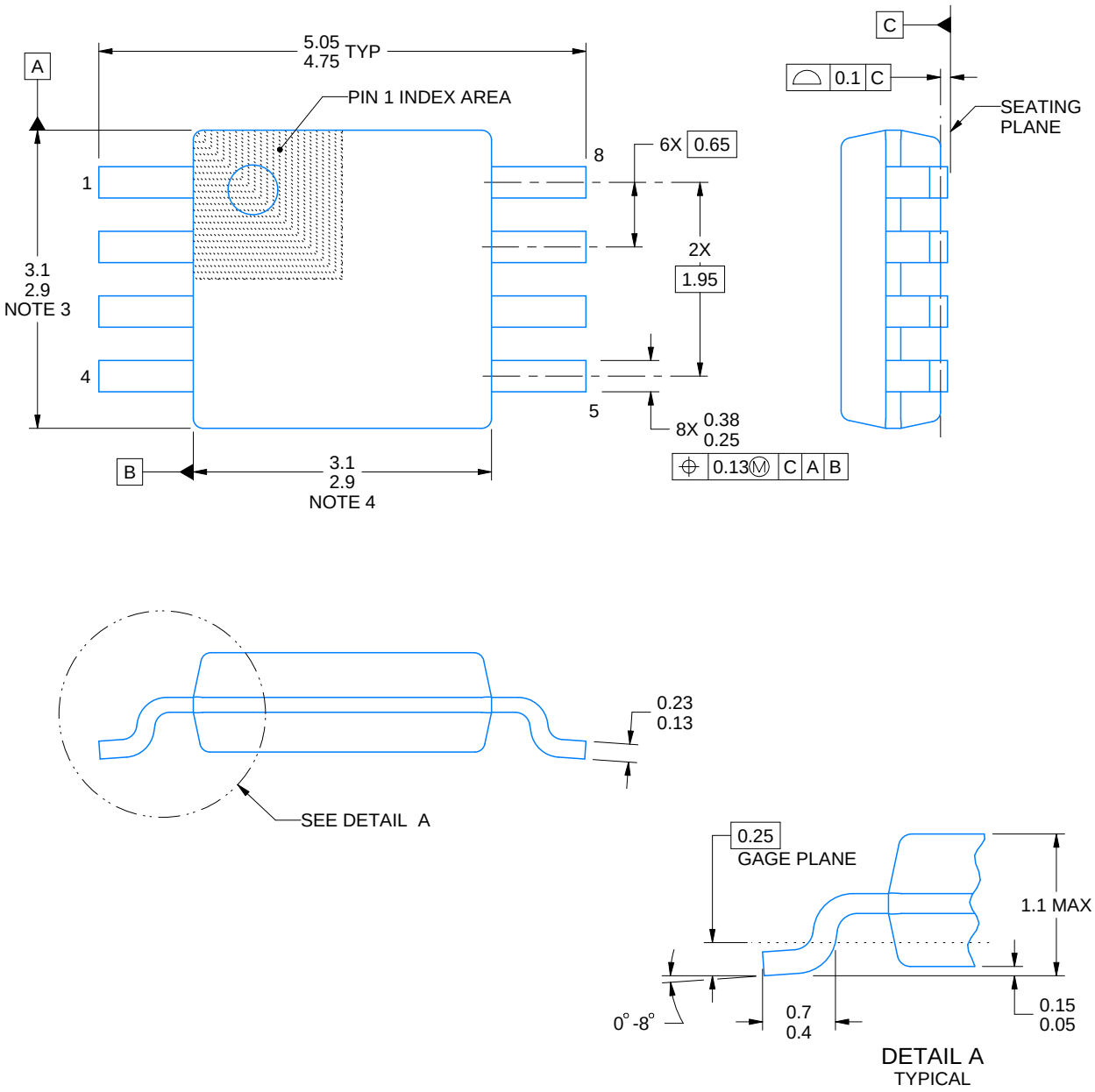
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

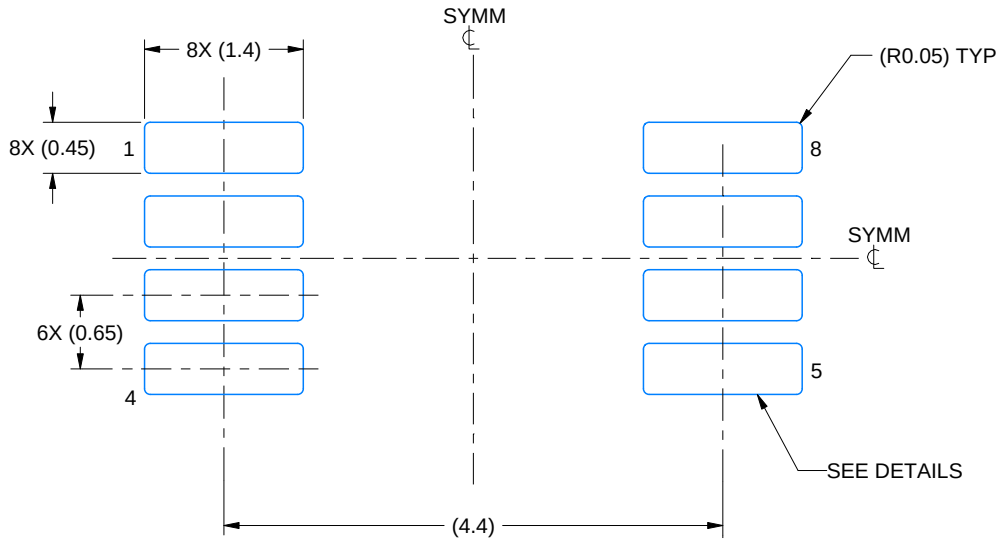
SMALL OUTLINE PACKAGE



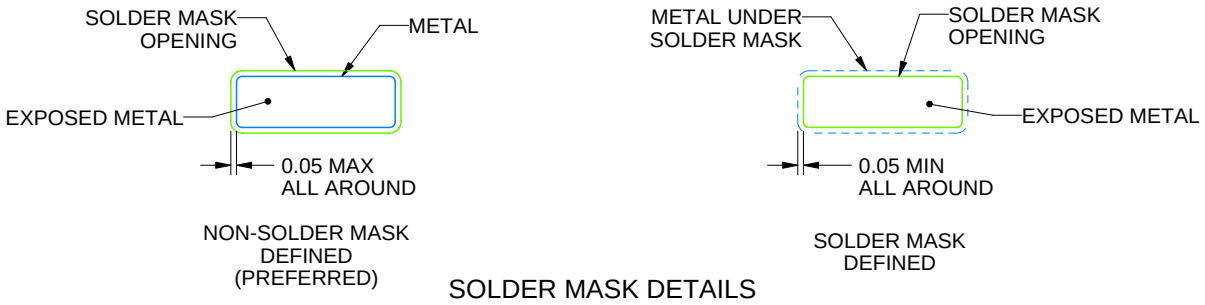
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

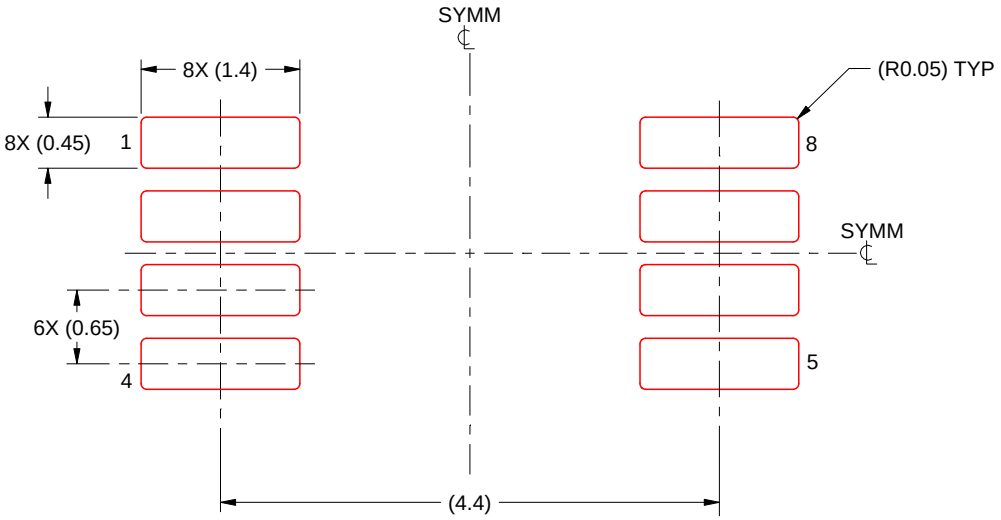


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025